Silicon Integrated Terahertz Light-Field Imaging Systems

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Dedicated to my wonderful family
for their love, support, and encouragement,
and to all my teachers
for their wisdom and inspiration.

Declaration

I, Ritesh Jain, herewith declare that I have produced this thesis without the prohibited assistance of third parties and without making use of aids other than those specified; notions taken over directly or indirectly from other sources have been identified as such. This work has not previously been presented in identical or similar form to any other German or foreign examination board.

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List of Abbreviations

Abbreviation	Meaning
THz	Terahertz
EM	Electromagnetic
sub-mm	Sub-millimeter
5G	Fifth-generation
mm-wave	Millimeter wave
THz-TDS	Terahertz time-domain spectroscopy
HEMT	High-electron mobility transistor
KID	Kinetic inductance detector
CW	Continuous-wave
MMIC	Microwave monolithic integrated circuit
QCL	Quantum cascade laser
CMOS	Complementary metal-oxide-semiconductor
RF	Radio-frequency
SiGe	Silicon-germanium
HBT	Heterojunction bipolar transistor
BiCMOS	Bipolar and CMOS
EU	European Union
SoC	System-on-a-chip
DFG	*Deutsche forschungsgemeinschaft* (German research foundation)
SPP	*Schwerpunktprogramm* (Priority program)
TX	Transmitter
RX	Receiver
2D	Two-dimensional
3D	Three-dimensional
CT	Computational tomography
ASIC	Application specific integrated circuit
IHCT	Institute for High-Frequency and Communication Technology, University of Wuppertal, Germany
MIMO	Multiple-input, multiple-output
FEOL	Front-end-of-line

BEOL	Back-end-of-line
IC	Integrated circuit
MPW	Multi-purpose wafer
RFIC	RF integrated circuit
DAC	Digital to analog convertor
ADC	Analog to digital convertor
USB	Universal serial bus
SPI	Serial peripheral interface
I2C	Inter integrated circuit
SNR	Signal-to-noise ratio
GaAs	Gallium Arsenide
InGaAs	Indium Gallium Arsenide
GaN	Gallium Nitride
MIM	Metal-insulator-metal
FD-SOI	Fully depleted silicon-on-insulator
FET	Field-effect transistor
IO	Input-output
VCO	Voltage controlled oscillator
PLL	Phase-locked loop
EIRP	Effective isotropic radiated power
PVT	Process, voltage, and temperature
NEP	Noise equivalent power
NETD	Noise equivalent temperature difference
RF-BW	RF bandwidth
BB-BW	Baseband bandwidth
PSD	Power spectral density
DR	Dynamic range
LNA	Low-noise amplifier
NF	Noise factor
IF	Intermediate frequency
LO	Local oscillator
BB	Baseband
RMS	Root-mean-square
SBD	Schottky barrier diode
fps	Frames per second
FoV	Field of view
HPBW	Half-power beam width
PCB	Printed circuit board
IR	Infrared
FPA	Focal plane array
AMC	Analog-multiplier chain

BRDF	Bidirectional reflectance distribution function
HDPE	High-density polyethylene
PCA	Principal component analysis
RMSE	Root-mean-square-error
CTI	Computational THz imaging
SPC	Single-pixel camera
CS	Compressive sensing
SLM	Spatial light modulator
FDM	Frequency division multiplexing
BIST	Built-in power test
DSP	Digital signal processor
PGA	Programmable gain amplifier
FADC	Flash ADC
FIFO	First-in first-out
XTAL	Crystal oscillator
VNAX	Vector network analyzer extender
PTFE	Polytetrafluoroethylene (Teflon)
PGA	Programmable gain amplifier
NMOS	N-type metal-oxide-semiconductor FET
PMOS	P-type metal-oxide-semiconductor FET
DFB	Distributed feedback
FIR	Finite-impulse response
UCA	User-controlled attenuation

Publications

Journal Publications

1. R. Zatta, D. Headland, E. Ashna, **R. Jain**, P. Hillger, J. Grzyb, and U. R. Pfeiffer, "Silicon lens optimization to create diffuse, uniform illumination from incoherent THz source arrays, " *J Infrared Milli Terahz Waves*, 2021 (Accepted for publication).

2. R. Zatta, **R. Jain**, J. Grzyb, and U. R. Pfeiffer, "Resolution limits of hyper-hemispherical silicon lens-integrated THz cameras employing geometrical multiframe super-resolution imaging, " *IEEE Trans. THz Sci. Technol.*, vol. 11, no. 3, pp. 277-286, May 2021.

3. **R. Jain**, P. Hillger, E. Ashna, J. Grzyb, and U. R. Pfeiffer, "A 64-pixel 0.42-THz source SoC with spatial modulation diversity for computational imaging", *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3281–3293, 2020.

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1. M. Schröter, U. Pfeiffer, and **R. Jain**, "7. Future of SiGe HBT technology and its applications," in *Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling and Circuit Applications,* Editors: N. Rinaldi, M. Schröter, River Publishers, Denmark, pp. 309-324, 2018, ISBN: 978-8793519619.

2. A. Mukherjee, W. Liang, M. Schröter, U. Pfeiffer, **R. Jain**, J. Grzyb, and P. Hillger, "6. Millimeter-wave circuits and applications," in *Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling and Circuit Applications,* Editors: N. Rinaldi, M. Schröter, River Publishers, Denmark, pp. 235-308, 2018, ISBN: 978-8793519619.

Contributions of Others

This work was conducted at the Institute for High-Frequency and Communication Technology (IHCT), University of Wuppertal in Wuppertal, Germany. The research group is led by Prof. Dr. rer. nat. Ullrich R. Pfeiffer. The contributions made by other group members to the circuits and measurements presented in this work are listed below. Any research not included in the list was conducted by myself.

- **Chapter 2:** Some initial data on the performance of THz sources and detectors was collected and summarized by Dr. Philipp Hillger.
- **Chapter 3:** The scanning-based light-field imaging experiments were conducted by Frank Landskron. The experiments on confocal reflection-mode imaging were a part of his M.Sc. thesis work.
- **Chapter 4:** The source pixel, including the in-pixel BIST, as well as the shared BIST readout, were designed by Dr. Philipp Hillger, who also did the chip layout. The in-pixel antenna was originally designed by Dr. Janusz Grzyb. The on-chip SPI and ADC were designed by Prof. Ullrich R. Pfeiffer, and the ADC characterization was done by Marcel Andree as part of his M.Sc. thesis. The circuit simulations were also set up by Dr. Philipp Hillger. The PCBs for source module packaging were designed by Wolfgang Förster. Eamal Ashna assisted with the characterization. He also performed the SPC imaging experiments as a part of his M.Sc. thesis. The data on the performance of state-of-the-art silicon integrated THz sources was compiled by Dr. Philipp Hillger.
- **Chapter 5:** The in-pixel antenna was designed by Dr. Janusz Grzyb. Prof. Ullrich R. Pfeiffer did initial simulations to conceptualize the in-pixel readout circuit. The shared pixel readout which includes the programmable gain amplifiers and the correlated-double sampling circuit, as well as the on-chip bias generators, were designed by Dr. Philipp Hillger. He also combined the pixel array, analog, and digital blocks with a top level chip routing. The on-chip ADC and SPI blocks were reused from the source-array design presented in Chapter 4. The ASIC was initially designed by Prof. Ullrich Pfeiffer. The camera wire bonding PCB and the control PCB were designed by Wolfgang Förster. The wideband RF characterization was conducted by Dr. Vishal Jagtap, while Eamal Ashna assisted with the digital characterization and the light-field imaging experiments.

- **Chapter 6:** The multi-chip camera array was assembled and tested by Eamal Ashna. He also set up the imaging demonstration.

Abstract

Terahertz (THz) radiation has many unique properties. Most importantly, these electromagnetic waves can "see-through" the dielectric materials without risking any ionization damage. Also, battery operated and compact THz components can be designed using the silicon process technology. All of these characteristics are very appealing for diverse industrial imaging applications.

However, the two-dimensional (2D) imaging does not provide enough information about an object specially in see-through imaging. Three-dimensional (3D) imaging is comparatively much better for such inspection and object identification. Unfortunately, the 3D THz imaging has required phase coherent systems so far. These are expensive, bulky, and power-consuming. Also, images can only be acquired with a slow, pixel-wise scanning. As of today, the practicality of coherent THz systems is very limited and there is no clear path to scaling up the image dynamic range or the pixel count.

This dissertation offers a paradigm shift, by bringing the light-field imaging to the THz radiation. The light-field technique allows 3D imaging by monitoring the position and direction of incoherent light rays, without needing any phase information. This method is now widely used for computational visible-light imaging. We look back at the fundamental ideas and evaluate them for THz imaging. From the system perspective, the THz light-field imaging is very interesting as it needs silicon integrated and lens-coupled incoherent THz pixel arrays, which are highly scalable in terms of frequency and pixel count over the single-chip and the multi-chip configurations. In this work, the THz light-field imaging is experimentally verified with a scanning-based imaging setup. Also, a multi-chip scaling approach is proposed to build economical and practical light-field systems for real-time, single shot 3D THz imaging. A silicon-integrated THz source-array and a THz camera are also designed and characterized. These systems-on-a-chip (SoCs) offer the digital interface and programmability that is necessary for multi-chip scaling. The 8×8 pixel 0.42 THz source-array SoC shows a record THz radiation power and integration density compared to the state-of-the-art. It also provides an exceptional illumination reconfigurability with spatial patterns and chopping frequency division multiplexing. The 32×32 pixel broadband THz camera SoC, specifically designed for all-silicon THz imaging systems, is also a fully digital system with the most compact form factor and the lowest power consumption. Building upon this SoC, a multi-chip THz light-field camera is also designed and demonstrated.

The light-field technique is a disruptive approach for THz imaging. The fundamental analysis, experiments, and hardware presented in this work now enable the fully-fledged, real-time THz light-field imaging systems. It is the first time that dedicated components have become available for silicon integrated THz light-field imaging, and they will serve as the crucial building blocks for the scientific community to conceptualize and test many new imaging setups and ideas.

Zusammenfassung

Terahertz (THz) Strahlung hat viele einzigartige Eigenschaften. Am wichtigsten ist, dass diese elektromagnetischen Wellen dielektrische Materialien "durchschauen" können, und in biologischen Systemen keine Ionisationschäden verursachen. Außerdem können batteriebetriebene und kompakte THz-Komponenten in Silizium-Prozesstechnologie entwickelt werden. All diese Eigenschaften sind sehr attraktiv für diverse industrielle Bildgebungsanwendungen.

Die zweidimensionale (2D) Bildgebung gibt jedoch nicht genügend Informationen über ein Objekt insbesondere bei der Durchsichtsbildgebung. Die dreidimensionale (3D) Bildgebung ist für diese Art der Inspektion und Objektidentifikation deutlich besser geeignet. Leider sind für die 3D-THz-Bildgebung bisher phasenkohärente Systeme erforderlich. Diese sind teuer, voluminös und verbrauchen viel Strom. Außerdem können Bilder nur mit langsamen Raster-Scans erfasst werden. Bis heute ist die Zweckmäßigkeit von kohärenten THz-Systemen sehr begrenzt und gibt keine klare Perspektive, den Bilddynamikbereich oder die Anzahl der Pixel zu erhöhen.

Diese Dissertation bietet einen Paradigmenwechsel, indem sie erstmals die Lichtfeld-Bildgebung mit THz-Wellen addressiert. Die Lichtfeldtechnik ermöglicht eine 3D-Abbildung durch Analyse der Position und Richtung inkohärenter Lichtstrahlen, ohne dass eine Phaseninformation benötigt wird. Diese Methode wird heute weitläuftig für die Computerbildgebung mit visuellem Licht verwendet. Aus der Systemperspektive ist die THz-Lichtfeld-Bildgebung sehr interessant, da sie siliziumintegrierte und linsengekoppelte inkohärente THz-Pixelarrays benötigt, die in Bezug auf Frequenz und Pixelanzahl über Ein-Chip- und Multi-Chip-Konfigurationen hoch skalierbar sind. In dieser Dissertation blicken wir zunächst auf die grundlegenden Ideen der Lichtfeld-Bildgebung zurück und stellen die Besondereheiten für deren Anwendung im THz-Bereich heraus. Daraufhin wird die THz-Lichtfeld-Bildgebung experimentell mit einem Scanning-basierten Bildgebungsaufbau verifiziert. Außerdem wird ein Multi-Chip-Skalierungsansatz vorgeschlagen, um wirtschaftliche und praktische Lichtfeldsysteme für die 3D-THz-Bildgebung in Echtzeit und mit nur einer einzigen Aufnahme zu ermöglichen. Ein siliziumintegriertes THz-Quellen-Array und eine THz-Kamera werden ebenfalls entwickelt und charakterisiert. Diese Systems-on-a-Chip (SoCs) bieten die digitale Schnittstelle und Programmierbarkeit, die für die

Multi-Chip-Skalierung erforderlich ist. Das 8×8 Pixel 0,42 THz Source-Array SoC weist im Vergleich zum Stand der Technik eine deutlich höhere THz-Stahlungsleistung und Integrationsdichte auf. Es bietet auch eine außergewöhnliche Beleuchtungs-Rekonfigurierbarkeit mit räumlichen Mustern und Chopping-Frequenzmultiplexing. Das breitbandinge 32×32 Pixel große THz-Kamera-SoC, das THz-Bildgebungssysteme entwickelt wurde die ausschließlich auf Siliziumkomponenten basieren, ist ebenfalls ein volldigitales System mit dem kompaktesten Formfaktor und dem geringsten Stromverbrauch. Aufbauend auf diesem SoC wird auch eine Multi-Chip-THz-Lichtfeldkamera entwickelt und demonstriert.

Die Lichtfeldtechnik ist ein disruptiver Ansatz für die THz-Bildgebung. Die grundlegende Analyse, die Experimente und die Hardware, die in dieser Arbeit vorgestellt wurden, ermöglichen nun vollwertige THz-Lichtfeld-Bildgebungssysteme in Echtzeit. Es ist das erste Mal, dass dedizierte Komponenten für die siliziumintegrierte THz-Lichtfeld-Bildgebung erforscht werden. Sie werden als entscheidende Bausteine für die wissenschaftliche Gemeinschaft dienen, um viele neue Bildgebungsanwendungen und Ideen zu konzipieren und zu testen.

Chapter 1

Introduction

Terahertz (THz) is the electromagnetic (EM) radiation roughly defined as having a frequency between $100\,\mathrm{GHz}$ and $10\,\mathrm{THz}$, which translates into a free-space wavelength λ_o ranging from $3\,\mathrm{mm}$ (at $100\,\mathrm{GHz}$) to $30\,\mu\mathrm{m}$ (at $10\,\mathrm{THz}$). This also includes the *submillimeter wave* (sub-mm)[1] band for frequencies between $300\,\mathrm{GHz}$ and $3\,\mathrm{THz}$ (λ_o from $1\,\mathrm{mm}$ to $10\,\mu\mathrm{m}$) [1]. From the quantum viewpoint, THz photons have very low energies ($6.6 \times 10^{-22}\,\mathrm{J}$ or $4\,\mathrm{meV}$ at $1\,\mathrm{THz}$). The THz waves have a range of practical applications in communications, imaging, and sensing. As an air interface, THz waves offer large fractional bandwidth, which is inevitably required to push the wireless data transfer rates beyond the fifth-generation (5G) communications [2]. For imaging and sensing, THz waves offer disruptive capabilities due to the unique wave-matter interaction and a favorable combination of radiation energy and wavelength, as discussed later.

This dissertation focuses on THz imaging and sensing, and presents the fundamental methodology of light-fields for THz radiation. Arguably, this framework can also be adopted for the THz beams serving as communication links, although such discussions are beyond the current scope. The next sections present a brief overview of THz imaging and sensing to motivate the development of THz light-field imaging. Later, the central topic of this dissertation is introduced by posing the primary research questions and listing the key achievements that were made during the course of this work. An outline for the subsequent chapters is presented towards the end.

1.1 Terahertz Imaging and Sensing

1.1.1 Benefits

The THz waves offer several unique advantages for imaging and sensing applications. As compared to the lower frequency microwaves or millimeter-waves (mm-wave), THz offers a finer, sub-mm scale image resolution, which is practical for a range of applications that one

[1] The band classification is not well-defined. Some authors may call the whole $100\,\mathrm{GHz}$ – $10\,\mathrm{THz}$ band as the submillimeter wave band, or the $300\,\mathrm{GHz}$ – $3\,\mathrm{THz}$ band as the THz band.

might encounter in everyday life (some of these applications are discussed later). Micrometer scale image resolution is also possible by leveraging on the near-field characteristics of THz waves [3]. There is another practical advantage that comes with the small THz wavelength. The passive structures e.g. transmission lines, inductors, capacitors, and antennas – that are used to manipulate and radiate an EM wave in an electronic system – scale with the wavelength. At THz, the size of such elements is small enough that multiple of them can be combined within a single miniaturized substrate to form completely monolithic circuits[2]. When compared to the X-rays, THz waves again offer a multitude of advantages for see-through imaging. X-rays possess large energy photons which can cause ionization of bio-molecules such as the human genetic structures [4], and therefore X-ray doses have to be limited and shielded to prevent unintentional exposure. THz waves do not come with such side effects, and they can be operated freely. The only known biophysical impact of THz waves is the vibration related heating of human tissues at very large exposure dose [5], [6]. Also, THz waves offer the absorption-driven higher imaging contrast for dielectric materials such as plastics, as compared to the scattering related contrast mechanisms for X-rays [7], [8]. From the technological perspective, optical elements such as lenses are abundantly available in THz as materials continue to show a finite, non-unity permittivity. On the other hand, X-ray optics is limited to small grazing angles only because the frequency-dependent material permittivity approaches to unity [9]. Another important advantage of THz waves is the spectral resonance of molecular vibrational states that offer identification signatures for several gases [10]. For materials in denser (liquid and solid) states, THz waves exhibit broad, frequency-dependent absorption or reflection that can also be utilized for material identification [11]. The position of THz in the electromagnetic spectrum, along with the associated wavelength, photon energies, and wave-matter interaction mechanisms [7] are summarized in Fig. 1.1.

1.1.2 Applications

The benefits of THz waves as listed above have motivated researchers to explore a wide range of imaging applications. Several interesting use cases emerge from the following fundamental properties of THz radiation: (a) it is strongly absorbed by polar solvents such as water, (b) it is strongly reflected by high conductivity surfaces such as metals, and (c) it undergoes partial absorption and reflection from dielectrics, based on the material properties and probing frequency. The scientific community has characterized the transmission and reflection spectral response of several materials within the complete THz frequency band using THz time-domain spectroscopy (THz-TDS), which have been compiled into several online databases [12], [13]. THz waves have been used for security screening, package inspection, quality control, biomedical diagnosis, and art conservation. The security and industrial applications include the detection of explosives, weapons, and drugs [14], [15], personnel inspection [16], conveyor belt postal mail inspection system [17], food content inspection [18], quality control of plastic joints [19],

[2]The wavelength scales with the medium permittivity. The relative permittivity (ϵ_r) for silicon is 11.7, therefore the effective wavelength is $\lambda_o/\sqrt{11.7}$.

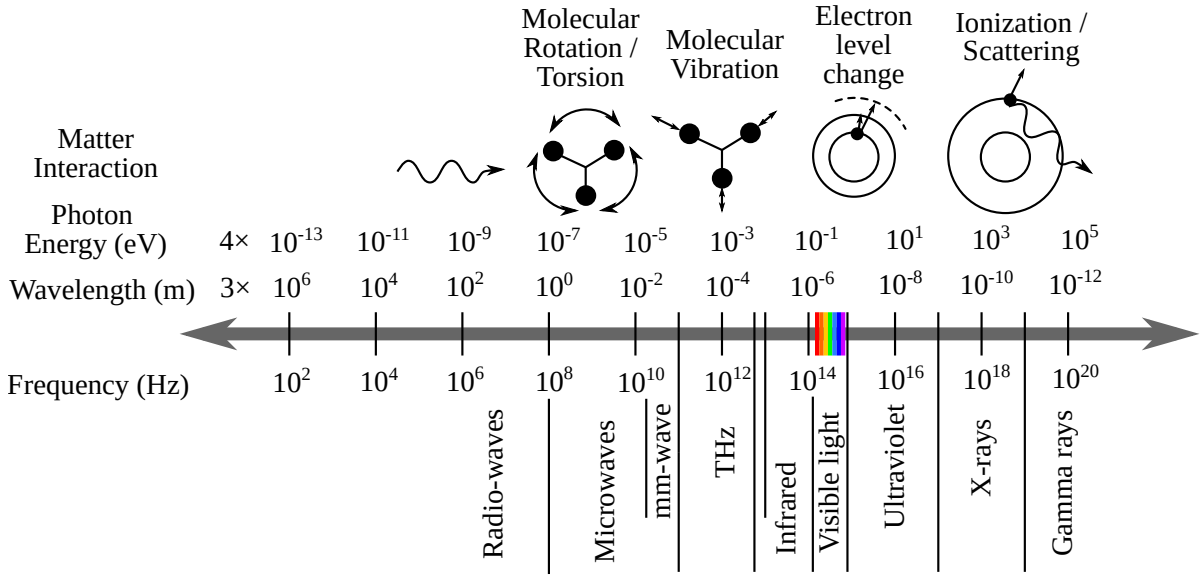


Figure 1.1: The electromagnetic spectrum and wave-matter interaction mechanisms.

and counterfeit detection [20]. Biomedical applications are also aplenty, and some notable examples include inspection of the tooth cavity [21], imaging for cancerous tissues [22], and diagnosis of diabetes with the imaging of water retention in the human foot [23]. There have also been significant attempts to use THz radiation for revealing hidden details of fragile and priceless art works, including medieval and renaissance paintings [24], ancient ceramics [25], and manuscripts [26]. Note that several of these demonstrations have used wideband THz spectroscopy signatures. However, the instrumentation can be simplified by limiting to those discrete or narrowband frequency components that provide the largest imaging contrast.

1.1.3 Instrumentation

So far, a rosy picture of THz imaging and sensing has been outlined, focusing on the benefits and applications. In reality, the potential of THz imaging and sensing has been held back by two fundamental technological limitations. First, as per the Plank's law, the natural ambient THz radiation is very weak [1]. Therefore, our surroundings, when seen in the THz spectrum with state-of-the-art room temperature THz sensors, simply appears dark. In order to make imaging possible, THz radiation needs to be generated with artificial sources. This is termed as *active imaging* as compared to *passive imaging* [27] where the natural blackbody or thermal emission from an object is recorded. The latter, although not impossible in THz [28], requires cryogenically cooled high-electron mobility transistors (HEMT), kinetic inductance detectors (KID), superconducting junctions, or microbolometers [29], which mostly find applications in large radio-telescope observatories for high-sensitivity detection [30]. This is related to the second technological limitation at THz, that both electronic and photonic components nearly exhaust their performance in this frequency range. Notably, the lower and higher frequency regions around THz are dominated by electronic and photonic systems respectively. The transition nature of the THz region manifests as a technological gap (sometimes called

the *terahertz gap* [31]) as the THz instrumentation design is extremely challenging. From the electronics perspective, THz frequencies are large enough that charge carriers in electronic transistors do not efficiently follow the fast phase changes due to transit time limitation. Photonic technologies are based on photoelectric emission of charge carriers, and THz photons have energies in the range of few milli-electronvolts. While these energy levels are easily dominated by thermal phonons at the room-temperature, even at lower temperatures it is extremely challenging to find a material with such a low band gap for photoemission.

These fundamental technological limitations have forced the scientific community to explore a variety of creative innovations to build THz sources and detectors with different technologies. Most common instruments today are based on laser-based pulsed and continuous-wave (CW) THz generation and detection systems, and III-V semiconductor-based microwave monolithic integrated circuits (MMICs) coupled to hollow metal waveguide blocks. Although both systems provide wideband and low phase noise operation, they are often heavy, complex, and power-consuming; despite amounting to a single transmitter and / or receiver. Laser-based systems in particular have an ultra-wide bandwidth ($\sim$1 THz) but they require individual bulky components (laser generators, fiber couplers, cryogenic cooler etc.). Interested readers may refer to [32] and [33], [34] for more details on THz photonic and MMIC technologies respectively. Band gap engineering with cascaded semiconductor junctions, in the form of quantum cascade lasers (QCLs) for THz emission, are also in active development [35]. Detailed reviews of different THz source and detector technologies have been provided in [36] and [29] respectively. While such systems remain very important measurement tools in laboratories – they are not the best suited for adoption into practical imaging applications unless they incorporate complex system integration in compact form factors with low-power consuming components, and exhibit economies of scale (lower production cost per unit with increase in production volume) and reliability as expected from the consumer, industrial, and government marketed end-products.

The modern information age has been created by the silicon process technology, which refers to the standard CMOS or CMOS based fabrication technology used to manufacture large scale integrated circuits. Such processes offer numerous advantages, including low electrical dc power consumption, compact size, high integration density, mixed-signal monolithic integration (combining analog, RF, and digital blocks on a single silicon chip), reliable operation, and high-yield production. Research into silicon integrated THz components has been ongoing for more than a decade, with the promise of a new era for THz imaging. Here, the implementation challenges have been exacerbated by the slow transistor speeds and large conductive and dielectric losses of underlying materials at THz. Note that these parameters do not improve with conventional Moore scaling, which is instead targeted towards improving the integration density for very large scale digital circuits. Silicon-Germanium hetero-junction bipolar transistors (SiGe HBTs) with bipolar and CMOS (BiCMOS) integration have become the dominant technology for THz circuits. With the improvements supported by the European Union (EU) funded projects DOTFIVE [37] and DotSeven [38], the unity current-gain cutoff frequency f_{T} and the unity power-gain cutoff frequency f_{MAX} of SiGe HBTs have reached $505\,\mathrm{GHz}$ and $720\,\mathrm{GHz}$

respectively [39]. For the foreseeable future, silicon-integrated THz systems are expected to be limited below 1 THz operation frequency [40]. Silicon integrated monolithic THz circuits form the essential part for this dissertation, and the state-of-the-art is further discussed in Chapter 2. More importantly, the role of silicon technologies in complex THz system design is increasingly being noticed [3], [41], and several innovative system-on-a-chip (SoC) designs for uniquely capable THz imaging and sensing systems have been demonstrated in the recent years [42]–[47]. The readers are introduced to two such SoCs in Chapters 4 and 5. The German research foundation (*Deutsche Forschungsgemeinschaft*, DFG) has also recently funded the interdisciplinary priority program (*Schwerpunktprogramm*, SPP) 'Integrated THz systems enabling novel functionality – INTEREST' (SPP 2314) to combine different technologies and approaches into working THz systems. Such developments ensure that THz systems would continue to improve and extend into novel application areas in the coming future. However, silicon technology would continue to play a crucial role due to its inherent advantages.

1.1.4 Approaches

This section briefly describes the existing THz imaging approaches. An understanding of the current methods is crucial in order to appreciate the THz light-field imaging advancements demonstrated in this dissertation. Note that the overview presented here is limited to active far-field THz imaging as it is the most relevant modality for the subsequent discussions.

The goal of active THz imaging is to record the interaction of THz waves with a target (also called an imaging object). Such target is spread to a finite extent in space, e.g. a space occupied by a cardboard packaging box. An image can be obtained by recording THz response across different points located on an imaginary grid at the object. This can be done in one of the following two ways. In scanning based imaging, a focused THz beam between a single THz source (or transmitter TX) and detector (or receiver RX) pair is moved around the object mechanically, capturing point-wise response in a serial fashion. In single-shot imaging, multiple THz TX/RX pairs distributed in space capture the response across multiple points in parallel. Both techniques can operate in either transmission or reflection-mode, and both can also be combined in a single setup for a large object area. Clearly, scanning suffers from a slower imaging speed prohibiting real-time (video rate) imaging. Single-shot imaging is always more desirable. However, simply using a number of independent TX/RX pairs in parallel isn't economically or technically feasible. Each TX/RX pair may require power-supplies, external RF signals, or other off-the-shelf components which prove bulky and costly to scale. A more efficient technique is to integrate multiple TX/RX units onto a single substrate with multiplexed biasing, signal sourcing, and readout. Such integrated components are termed as *arrays*. Unfortunately, array integration means sacrificing the complexity of TX/RX elements for minimizing chip area, power consumption, and array variability. The array integration therefore favors simpler TX/RX components. The distinction between silicon integrated THz TX/RX elements and arrays is further explored in Chapter 2.

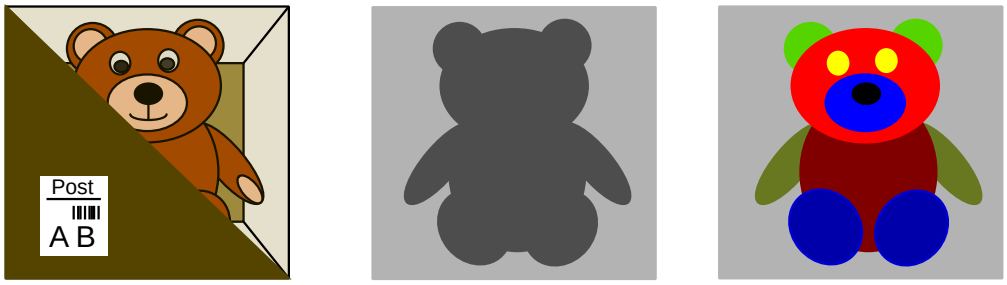


Figure 1.2: (Illustrative) Imaging in 2D versus 3D for object identification. Different colors in 3D image indicate different height or structural profiles which are not resolved in 2D.

The image itself can either be two-dimensional (2D) or three-dimensional (3D) as per the employed technique. The latter contains depth or range information along with the 2D spatial object response. Drawing out the experience of human vision perception, anyone who has ever played with hand shadow animals knows that 2D projections of 3D objects are largely ambiguous. This issue especially impacts see-through imaging where a surface might be concealing multiple object layers along the depth axis. This is the reason why trained personnel are required alongside X-ray baggage scanners (which produce 2D images) at airport security checkpoints to scrutinize the displayed images and point out any contraband, and the object identification still remains susceptible to the human errors. Any target can be better identified in 3D imaging [48]. Fig. 1.2 illustrates this difference with a conceptual sketch.

Imaging in 3D requires recording larger information content from the imaging process. 2D images can be created with simple radiometry by measuring the transmitted or reflected THz power from an object. However, 3D imaging requires encoding of the depth information in additional *diversity* at the response. This diversity can be temporal, in the form of time delay or wave phase, typically used in radar [49] and holographic imaging [50]. It can also be incorporated in the form of angular object projection, as in THz computational tomography (CT) [51] and photogrammetry [25]. A narrow depth-of-focus can also be used to image the object at different depth planes [52]. However, none of these diversities conform to the simple integration of THz TX/RX arrays. All the above-mentioned cases require a high component complexity that necessitates mechanical scanning either with a single TX/RX or with multiple TX/RX pairs. These issues are further elaborated in Chapter 2.

Note that see-through imaging is also in research for lower frequencies, such as seeing through walls or corners with Wi-Fi [53], [54] and mm-wave 3D imaging radars (including automotive radars) [55], [56]. However, at lower frequencies, the beam radiation has a lower directivity (higher diffraction), and therefore a coherent approach is used for 3D image generation and scanning. For example, the airport full body scanners fall into this category: R&S®QPS201 is a modern commercial E-band scanner (frequencies f = 70–80 GHz) with $2\,\mathrm{m} \times 1\,\mathrm{m}$ aperture that weighs more than $400\,\mathrm{kg}$ and consumes $2.4\,\mathrm{kW}$ of electric power to operate around 6000 phase-locked transmit/receive pairs [57]. This huge, bulky system provides an imaging

resolution of $1.9\,\mathrm{mm}$ – yet systems like these remain highly specific and non-accessible to most other applications. As discussed later, coherent components suffer from major scalability and image quality issues, and we seek a more portable and power efficient see-through imaging solution at THz frequencies with silicon integration.

1.2 This Dissertation

The preceding discussions were aimed towards equipping the readers with necessary preliminary knowledge about THz imaging and sensing. The brief review clearly points towards the need of a 3D THz imaging technique that is compatible with THz TX and RX arrays for real-time imaging. In this context, this section formally introduces the subject matter of this dissertation.

1.2.1 Primary research questions

The investigations in this dissertation start with the following central research question:

Central Research Question
How can one enable 3D THz imaging with silicon integrated THz arrays?

Light-field imaging is proposed as the answer to the above problem. In this technique, the light flowing into and out of the object is considered as a vector field composed of ray bundles, which are quantified in terms of the energy density along a specified direction and position in the 3D space. If the positions and directions of individual light rays are known, back-propagation can be applied to reconstruct a 3D volume source of the field disturbance [58]. This fundamental idea is further elaborated in Chapter 3. Notably, the light-field method requires *spatio-directional* sources and detectors, i.e. components which can synthesize and sample the light along multiple angles across different spatial locations. Modern advances in visible light-field imaging have leveraged on the excellent incoherent spatio-directional light that is available in plentiful both naturally (from the sun) and artificially (from lighting lamps), and on the large format image sensors with millions of pixels that are accessible cheaply. Unfortunately, both of these ingredients are missing for THz radiation. The challenges for THz light-field imaging are summarized as the following:

1. Strong isotropic, incoherent THz sources (THz sun or THz lamp) do not exist so far. It is not possible to do computational light-field imaging in the absence of appropriate illumination.
2. Due to the inherently large THz wavelength as compared to the visible light, THz imaging pixels are around $10\times$ larger than visible light pixels. Therefore, THz arrays do not reach the demanding pixel count for good spatial resolution and wide field of view required for light-field imaging.

3. There is no established scientific knowledge on the formulation, interpretation, generation, capture, and manipulation of THz light-fields. This is an unexplored scientific domain waiting for discovery from the first principles.

Note that the above listed challenges are only partially true now, as the research conducted in this dissertation has discovered potential answers as listed under Section 1.2.2. Efforts have been focused to answer the following derived research questions, which also form the research objectives.

Derived Research Questions
1. What kind of first principle knowledge or know-how can be imparted to the formalization, interpretation, generation, capture, and manipulation of THz light-fields, in order to guide the future development for THz light-field imaging systems?
2. How to implement THz light-field imaging hardware (both sources and cameras) with silicon integrated THz arrays?
3. How to impart scalability, programmability, and reconfigurability to such hardware for extending the pixel count, aperture size, computational complexity, and diversity of the imaging system?
4. How can we extract 3D information and synthetic apertures out of such THz light-fields?

1.2.2 Key achievements

The following key achievements were obtained from the research reported in this dissertation:

1. Based on a review of state-of-the-art literature, and interdisciplinary investigations into visible light computational photography, the concept of THz light-field imaging was proposed for the first time. A proposal for investigating 'Light-field methods for terahertz imaging – T-Field' was granted funding by DFG under the individual research grant program. A multi-chip integration approach was envisaged to design spatio-directional and scalable light-field arrays at THz.

2. The first experiments for THz light-field imaging were successfully carried out with single camera scanning. The formative idea and these initial results were communicated in a well-accepted peer-reviewed scientific journal [59].

3. A novel THz source array SoC was developed that integrates 64 free-running source pixels to radiate more than $10\,\mathrm{mW}$ of maximum power at $0.42\,\mathrm{THz}$ [46]. The SoC integrates a digital application specific integrated circuit (ASIC) for spatial and modulation diversity for computational imaging, as well as in-situ monitoring and calibration of the relative radiated power from different pixels. The SoC shows a record integration complexity,

radiation power, pixel count, and reconfigurability among the silicon integrated THz sources to date. In particular, the pixel count and radiated power are improved by factors of $4\times$ and $10\times$ respectively with about $3\times$ larger total chip area as compared to the 0.53 THz source array developed previously [60] at IHCT. These developments were funded under the DFG SPP 1798 'Compressed Sensing in Information Processing – CoSIP', Phase 1, under the project 'Terahertz illumination concepts for reciprocal compressive imaging in silicon technologies – LumiCS' specifically targeting compressive imaging applications. A DFG individual research grant for project 'Silicon integrated smart terahertz source arrays for reciprocal imaging – SI-STAR' continues to fund the follow-on developments at the time of writing this manuscript.

4. A 1k-pixel broadband THz camera SoC in a low-cost 130 nm CMOS technology was also developed [47]. The camera SoC integrates the full rolling-shutter digital readout with programmable gain and bias settings, in part due to a novel differential transimpedance based THz detector readout scheme that was invented during the course of this research. The optimum camera performance is tuned for $0.4\,\mathrm{THz}$ to $0.7\,\mathrm{THz}$ frequency band, while maintaining a compact chip area, in order to match the source SoC and other emerging silicon-integrated THz sources. The integration complexity targets multi-chip light-field arrays, and a prototype for the same has also been demonstrated.

5. Building upon this research, subsequent development of THz light-field imaging systems has been funded under the European Research Council advanced research grant for year 2020 as 'Direct temporal synthesis of terahertz light fields enabling novel computational imaging – DIRECTS'. Here, the invention of THz multiple input, multiple output (MIMO) light-fields has been proposed to exponentially improve the THz imaging pixel count to millions of pixels. Such resolution is expected to provide a breakthrough capability for THz imaging systems for a rapid industrial adoption.

1.2.3 Outline

This dissertation is divided into seven chapters. The content in these chapters has been organized as the following:

Chapter 1: Introduction, i.e. this chapter, introduces THz imaging and sensing, draws out the research motivation, poses the primary research questions, and lists the key achievements and chapter outline.

Chapter 2: Silicon integrated THz systems presents insights on different state-of-the-art silicon integrated component and system design approaches for THz imaging and sensing, debating upon their applicability for 3D THz imaging and light-field technique.

Chapter 3: Light-field imaging provides the basic formulation for light-fields. The formalization approaches of ray diagrams and two-plane parameterization are discussed with emphasis on THz radiation properties, to form a crucial mental model for the reader.

Scanning based THz light-field imaging is also presented. These results validate several key premises and applications.

Chapter 4: THz source array SoC details the design approach and characterization results for the 64-pixel 0.42 THz source array SoC for computational THz imaging. Reciprocal imaging with both spatial and modulation encoded apertures is demonstrated.

Chapter 5: THz camera SoC reports on the design and detailed characterization of 1k-pixel broadband CMOS THz camera.

Chapter 6: Multi-chip THz light-field camera discusses the demonstration of 3×3 multi-chip THz light-field camera array system consisting of individual lens-coupled camera SoCs with lens-scale packaging and shared control interface.

Chapter 7: Conclusions and outlook presents the end conclusions and future outlook for THz light-field imaging systems.

1.3 Chapter Summary

This chapter has presented an overview of THz imaging and sensing, listing out the benefits of THz waves over lower frequency microwaves or higher frequency X-rays for see-through imaging. A brief review of some THz imaging applications and THz instrumentation options has also been stated. Silicon integrated THz components provide a very practical platform for implementing THz systems due to the offered economies of scale, mixed signal integration complexity, compact form factors, and low dc power consumption. While the technology is continuously improving in terms of transistor speed, it is the novel system integration that promises the largest value addition at THz frequencies.

From the review of existing THz imaging approaches, the need for real-time 3D THz imaging has been underlined. Light-field imaging can be used for the same, along with silicon integrated THz source and detector arrays for compact, low-power consuming, scalable THz systems. The chapter lists out primary research questions that must be answered in such an undertaking. Following this, the key contributions and innovations originating from this research have been listed. The organization and structure of this dissertation has also been briefly outlined.

Chapter 2

Silicon integrated THz systems

In this chapter, we look briefly at the advantages and challenges offered by commercial silicon process technologies. This shall be followed by a discussion on design and performance of state-of-the-art silicon integrated sources and detectors. The design approach selected for THz light-field imaging systems is also presented.

2.1 Introduction to silicon process technology

Silicon technology primarily includes the commercial CMOS and BiCMOS fabrication processes consisting of active devices i.e. transistors, and passive devices, including diodes and resistors. Transistors, diodes, and some form of resistors are fabricated by selectively doping the silicon substrate and patterning electrical contacts over it. This portion is called the front-end-of-line (FEOL). This is followed by a number of metal layers (commonly aluminum or copper), one atop the other and separated by interlayer dielectric (typically silicon dioxide), which can be patterned either to form vias for electrical contacts, or to design EM passives including inductors, capacitors, transmission lines, and antennas. The metal stack is called back-end-of-line (BEOL). Different processes are commonly differentiated by minimum geometrical feature size and may consist different FEOL devices and BEOL stack. The transistor speed is benchmarked by f_T/f_{MAX} cutoff frequencies. The BEOL is capped with a passivation layer (silicon nitride or silicon oxide) which can be selectively excluded, for example, at biasing and signal pads for making electrical contacts externally, through fine-pitch probes for on-wafer breakout characterization, or through wire bonding, or bump bonding for packaging purpose. The technology allows monolithic combination of different elements in form of an integrated circuit (IC) or silicon chip.

The pricing model of silicon ICs follows the economies of scale. The primary cost is associated with the fabrication of photomasks. These are designed with a specialized electron beam etching process, and are used to pattern different structures on a silicon wafer for selective doping and etching. A complete process can use multiple photomasks. However, once a set of photomasks

is created, it can be used to produce an infinite number of identical IC units (dies). Therefore, the initial fixed cost is large as it is associated with the process complexity (number of masks) and the chip area (size of each mask). However, with an increase in the number of dies produced, the cost per die asymptotically reaches to zero. The common photomask size is 6 inches $\times$ 6 inches. For smaller designs at prototyping volumes, the foundries (fabrication companies) offer multipurpose wafer (MPW) service where multiple ICs (mostly different designs) are combined within a single photomask, and the individual dies are sawed and separated later. In Europe, vendors like CMP and Europractice offer aggregate MPW services from different foundries and technologies. MOSIS provides similar services primarily in the United States.

The ICs are classified as analog, RF, digital, or mixed-signal as per their operation. RFICs typically consist a few transistors, and a larger portion of the chip area is occupied by distributed passive EM structures. They require full custom design including finite element simulation of the EM passives. Analog ICs often consist a larger number of transistors with lumped passives, and custom design is also valued here. Digital ICs may consist of millions of transistors, and the design follows an automated process where the behavioral level description of the circuit (specified in a hardware description language such as Verilog) is translated to the IC layout using automated processes with some custom intervention from the designer. The mixed signal ICs consist some combination of the digital, analog, and RF blocks. Several electronic design and automation tools, from vendors such as Cadence, Synopsys, Ansoft, Mentor Graphics etc. are used across the whole design process.

The above stated whirlwind introduction to the silicon integrated circuits is by no means comprehensive. Only selected concepts and terms have been introduced specifically for the readers from a non IC design background, as these details are necessary to understand the key ideas presented throughout this dissertation.

2.1.1 Advantages and limitations

The following features of silicon technology are beneficial for THz IC design:

1. **Integration complexity:** Silicon technology allows mixed signal integration. This can be used to create THz ICs with RF blocks (oscillators, mixers, amplifiers, detectors) and associated passives (inductors, capacitors, transmission lines, baluns, hybrids, transformers, filters, antennas); analog baseband signal conditioning (amplification, integration, sampling, multiplexing) and biasing; with digital control using digital to analog convertors (DACs); and digital signal readout using analog to digital convertors (ADCs). A programmable digital logic can be configured using standard computer interfaces such as universal serial bus (USB), serial peripheral interface (SPI), and inter-integrated circuit (I2C) etc.

   Note that the distributed THz EM structures can be completely integrated on chip as the wavelengths in silicon are in the order of $100\,\mu\mathrm{m}$. Such systems show compact form factors (due to monolithic integration), simplified operation and interfacing. The dc power

consumption is also low as the silicon technology, especially CMOS, is generally power efficient.

2. **Low cost:** As discussed, silicon ICs approach a marginal cost per unit in mass production due to the economies of scale. The mature processes have die yields higher than 90%.

3. **Reliability and reproducibility:** Silicon technology in general has gone through years of maturity (although new processes periodically emerge to push the performance and integration limits). Several design techniques, specially for analog and digital ICs, are well understood. Specific mechanisms are already in place to improve the operation reliability and to minimize variability.

4. **Ecosystem and availability:** The foundry services, design tools, packaging services, and interfacing technologies are widely available. The ICs themselves integrate well with modern computers, and often both the RFICs and computing processors can be combined on the same substrate (silicon or other common carrier).

However, THz IC design also suffers from several major challenges due to the following limitations of the silicon technology:

1. **Slow transistor speed:** As noted above, the fastest SiGe HBT transistors available today are still limited to $f_{\mathrm{MAX}} < 1\,\mathrm{THz}$. For an RF power amplification stage, the accepted operation limit is up to $f_{\mathrm{MAX}}/2$. Therefore, it is expected that silicon THz sources would remain dominant below $1\,\mathrm{THz}$ in the near future. Increasingly higher operation frequencies also result into lower power conversion efficiencies and low signal-to-noise ratio (SNR) due to the gain roll-off [3].

2. **Transmission line losses:** For silicon integrated transmission lines, both the conductivity loss and the dielectric loss increase with frequency. The former is due to a reduced skin depth in proportion to the square root of frequency. The latter is the result of an increased dielectric loss tangent proportional to the frequency [61]. These losses are further exacerbated at scaled (small feature sized) technologies because of more restrictive design rules. For non-shielded lines and other passive structures such as antennas, higher conductivity silicon substrates at smaller technology nodes also lead to larger losses.

3. **Low power handling capacity:** The silicon process technology, specially the one used in high frequency applications, inherently has a low RF power handling capacity due to the low breakdown voltages (associated with lower band gap junctions and thin oxides) as compared to III-V MMIC technologies such as GaAs/InGaAs and GaN [62]. To increase the power, large and/or multiple transistors are used at the cost of increased parasitics.

4. **RF interfacing:** With increase in frequency, it becomes exceedingly difficult to feed and extract the signals out of silicon ICs, as the interfaces require small dimensions (for low losses) and tight tolerances. Therefore, combining III-V and silicon technologies at an RF interface, or feeding RF signal output to low loss metal waveguides, are non-trivial

tasks. As we shall see later, in several architectures a lower frequency RF signal is fed and up-converted on-chip. Distributing the RF signal to multiple chips synchronously is also difficult due to tight phase tolerance (change in signal phase per unit length) and large signal losses.

2.1.2 Technologies used

The $0.13\,\mu\mathrm{m}$ SG13C SiGe:C CMOS and SG13G2 SiGe:C BiCMOS twinned technologies from IHP Microelectronics GmbH are used for the SoCs presented in this dissertation. They consist of 7 metal layers, including five thin metal layers (M1 – M5) and two thick metal layers (TM1, TM2) at the top to implement low loss passives. The technologies also features optional high permittivity dielectric (silicon nitride) between layers M5 and TM1 for high density metal-insulator-metal (MIM) capacitors. The SG13C process is lower cost and offers only CMOS transistors, while the SG13G2 process offers additional high-speed SiGe HBTs ($f_\mathrm{T}/f_\mathrm{MAX}$ of 300/500 GHz) for millimeter-wave (mm-wave) and THz circuits [63]. The next generation of this technology, with HBTs reaching $f_\mathrm{T}/f_\mathrm{MAX}$ of 505/720 GHz, is in active development [39]. Note that all transistors must be operated within a specified voltage and current density (specified as breakdown limits) for a reliable operation. The SG13C CMOS transistors allow an optimum VDD of $1.2\,\mathrm{V}$ and the SG13G2 HBTs allow a base-emitter voltage up to $1.7\,\mathrm{V}$. Thick channel oxide FETs for $3.3\,\mathrm{V}$ input-output (IO) are also facilitated.

2.2 Design approaches

To circumvent the aforementioned limitations of silicon integration, THz IC design utilizes some common techniques and architectures. From the component perspective, architectures for THz signal generation and reception are the most interesting.

2.2.1 THz signal generation

2.2.1.1 Performance metrics

The important metrics for THz signal generation are the output frequency, signal power, conversion efficiency, and the spectral purity. The selection of an output frequency depends on the application, and several applications such as frequency modulated continuous wave radar require a broadband, tunable output signal frequency as specified by the tuning range of the voltage controlled oscillator (VCO). Silicon integrated pulsed THz sources for wideband THz radiation are also in research [64]. For imaging and sensing, the frequency dependent reflection or absorption behavior can be used for spectroscopy. Some THz sources, such as the comb generator in [65] and multicolor imaging source in [66] can simultaneously generate a set of discrete frequencies for THz spectroscopy. The imaging SNR depends on the radiated signal power. Note that beyond f_MAX the signal power typically rolls-off in proportion to f^{-3}orf^{-4} (where f is the output frequency) of THz radiators [3]. The output power is usually in the

order of microwatts to milliwatts, and is often specified in decibel-milliwatts (dBm) scale. The efficiency relates to the dc-to-RF power conversion factor and is typically below 1% for silicon integrated THz signal generators [46]. For free-space radiators, the antenna gain also play a role in effectively extracting and directing the radiation beams.

Spectral purity refers to the quality of the THz signal with respect to a pure sinusoidal tone at the desired frequency. Here, the first parameter of interest is the phase noise, which is indicative of the noise related time jitter in the signal. A larger phase noise implies a smaller phase coherence. In coherent systems where the phase is a necessary information, minimization of phase noise is of paramount importance. The phase noise is measured in decibel scale relative to the carrier (dBc) where carrier refers to the principal sinusoidal tone, at a specified offset frequency ($100\,\text{Hz}$ – $10\,\text{MHz}$) from the carrier. The phase noise rolls off with increase in the offset frequency [67]. The other important parameter is the level of harmonic spurs, which quantifies the extent of undesired harmonics (integer frequency multiples of a signal) at the generator output [68].

2.2.1.2 Design approaches

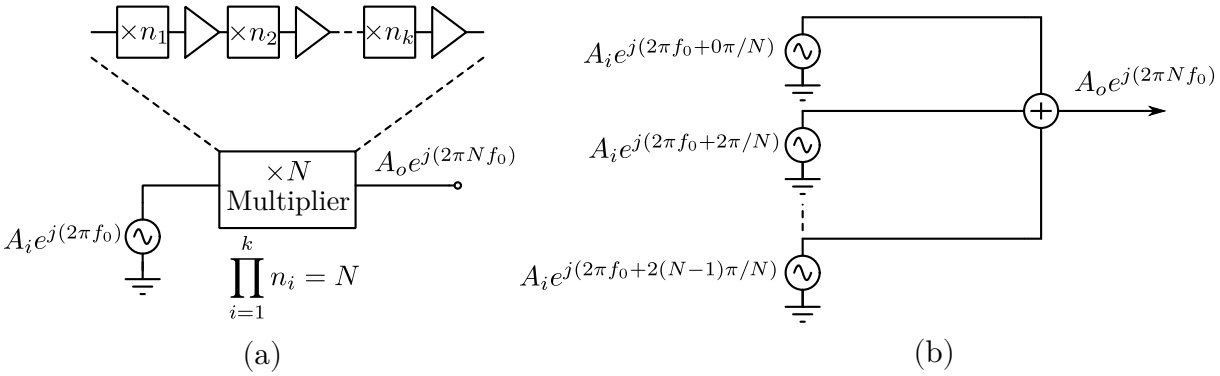


Figure 2.1: THz signal generation with (a) multiplier based source, and (b) N-push source.

Silicon integrated THz sources generate signals with frequencies beyond transistor f_{MAX}. There are two primary ways to do this – (1) frequency multiplication, and (2) harmonic oscillators. In the first approach, shown in Fig. 2.1(a), a fundamental frequency signal, mostly supplied externally, is multiplied in frequency using cascaded frequency multiplier blocks. The overall frequency multiplication factor is often in double digits, such as $\times 45$ multiplier chain for $820\,\text{GHz}$ signal generation in [69], $\times 16$ multiplier chain for $240\,\text{GHz}$ source in [70], $\times 30$ multiplier chain $607.5\,\text{GHz}$ source in [71], and varactor based passive $\times 10$ multiplier chain for $1.4\,\text{THz}$ source in [72]. Larger multiplication factors are often accompanied by larger phase noise and spurs [73]. However, depending on the external fundamental signal source, THz frequency multipliers may show a better phase noise and bandwidth than harmonic THz oscillators.

Harmonic oscillators, as the name implies, consist of on-chip highly non-linear VCOs generating a fundamental signal and several higher order harmonics. These harmonics are extracted either using on-chip filtering based on impedance matching [74], [75], or by facilitating on-chip constructive interference of the desired harmonic along with destructive interference for others

using distributed structures [76] or N-push approach [77], [78]. The N-push technique is shown in Fig. 2.1(b). Here, the non-sinusoidal outputs from N number of highly non-linear fundamental oscillators with progressive phase shifts are combined at a common node to extract the N^{th} harmonic in-phase, while the lower harmonics are cancelled out. Most common implementations exist for $\times 2$ or $\times 3$ harmonic extraction, and are termed as *push-push* [79] and *triple push* [60] oscillators respectively. The extracted harmonic can be further multiplied on-chip using single stage frequency doublers [80] or triplers [81]. The output signal can also be divided and fed back to a phase-locked loop (PLL) for output frequency stability and low phase noise [82]. Overall, harmonic oscillators are more efficient in terms of dc power consumption and chip area as compared to the frequency multiplier sources [83].

2.2.1.3 Array integration

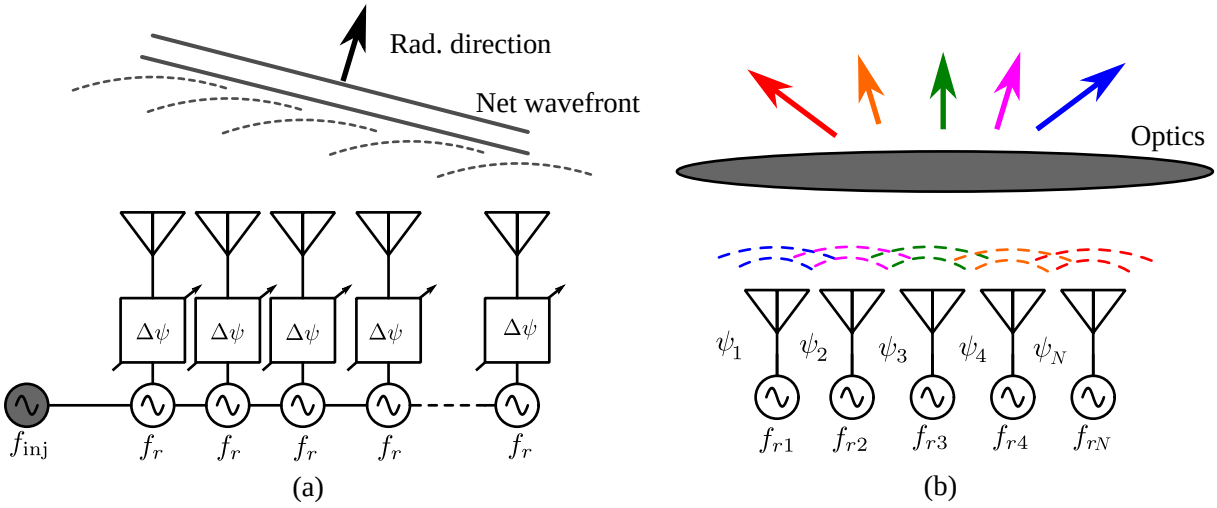


Figure 2.2: (a) Coherent phased-array locked at external signal f_{inj} and radiating at f_r with phase shifters before the antennas, (b) unlocked source array with N-elements radiating at slightly different frequencies $[f_{r1}, f_{rN}]$ and random phases $[\psi_1, \psi_N]$ with optical beam switching.

Another design issue relates to the development of THz source arrays for increasing the radiated power. Due to their compact size and small dc power consumption, harmonic oscillators are best suited for this task. Limited scalability has also been demonstrated for frequency multiplier sources, such as four parallel multiplier chains sharing a common input in [66], [69], and 2×4 amplifier-quadrupler array in [84].

For harmonic oscillators, the power can be combined in either coherent or incoherent manner. In coherent arrays, the signals generated from different elements are correlated or locked in phase, which improves the output phase noise by $10 \log N$, and output effective isotropic radiated power (EIRP) by $10 \log N^2$ in dB scale for N elements in the array [85]. The mutual phase locking can be provided with distributed coupling structures between the oscillators [83], [86], [87], individual tuning of proximity elements without dedicated coupling [88], injection locking to a reference source at lower frequency supplied on-chip [76], [89] or externally with wired [90], [91] or wireless [92] coupling, and hybrid approaches [93], [94]. Coherent arrays generate a

single radiation beam with combined power. For moving this beam electronically, e.g. to scan a scene, the signal phase at each individual element must be tuned. Such arrays are termed as phased-arrays. THz implementations include distributed phase shifting [94]–[96] or individual element biasing [97] for mutually coupled elements, and injection signal phase tuning [76], [91] or RF vector modulation [90] for externally locked elements. Fig. 2.2(a) illustrates a THz phased-array radiating at frequency f_r with all elements injection locked to an external signal frequency f_{inj} and individually tunable $\Delta\psi$ phase shifts before each antenna for beam steering.

For incoherent power combining, each element must be free-running, i.e. the signals generated from individual elements must be unlocked or uncorrelated in phase. Incoherent arrays generate multiple beams with can either be overlapped or separate in space and direction. For combined radiation from N unlocked elements, the phase noise in dB is $10\log N$ higher than the phase noise of an individual element. In practice, the center radiation frequencies of different oscillators are also randomized (within a small range) due to process, voltage, and temperature (PVT) variations, which further randomizes the overall radiation phase. The directivity and EIRP of each individual element can be increased using a silicon lens which can also distribute the output beams across multiple directions (see Sec. 2.2.3). In this case, a scene can be scanned with beam switching instead of beam steering. Note that unlike the coherent beam steering where power from all elements is combined into a single beam, each switched beam carries the power radiated from a single component. Fig. 2.2(a) shows an incoherent THz source array for N elements radiating random frequencies $[f_{r1}, f_{rN}]$ and random phases $[\psi_1, \psi_N]$, along with some external optics for beam separation and angular diversity. Two incoherent THz source arrays, one with 4×4 pixels radiating maximum $0\,\text{dBm}$ power at $0.53\,\text{THz}$ [60], and another with 8×8 pixels radiating maximum $10.3\,\text{dBm}$ power at $0.42\,\text{THz}$ [46], have been reported in the literature. Both have been designed at IHCT. Detailed design for the latter is also reported in Chapter 4.

2.2.1.4 Discussions

Fig. 2.3 plots the frequency versus output power for some state-of-the-art THz radiation sources discussed earlier. Note that for frequency tunable sources, only the center design point with maximum output power has been considered. The following insights emerge from this graph. First, nearly all sources have frequencies below $0.7\,\text{THz}$ with only [69], [72], [86] showing higher frequencies. More designs have been reported in CMOS as compared to SiGe HBTs. These CMOS processes are 65nm or better technologies. The output power for single oscillator degrades with increase in the radiation frequency. Array scaling is widely adopted to improve the radiated power. The highest total radiated power is reported by our own work from [46] which also occupies the largest area of $12.6\,\text{mm}^2$ among all the sources. Note that this power includes around $4\,\text{dB}$ of thermal throttling because of all the oscillators running simultaneously [46].

As compared to their incoherent counterparts, coherent arrays provide power combining and a low phase noise. The signal phase can be used for 3D imaging. While the radiation power can

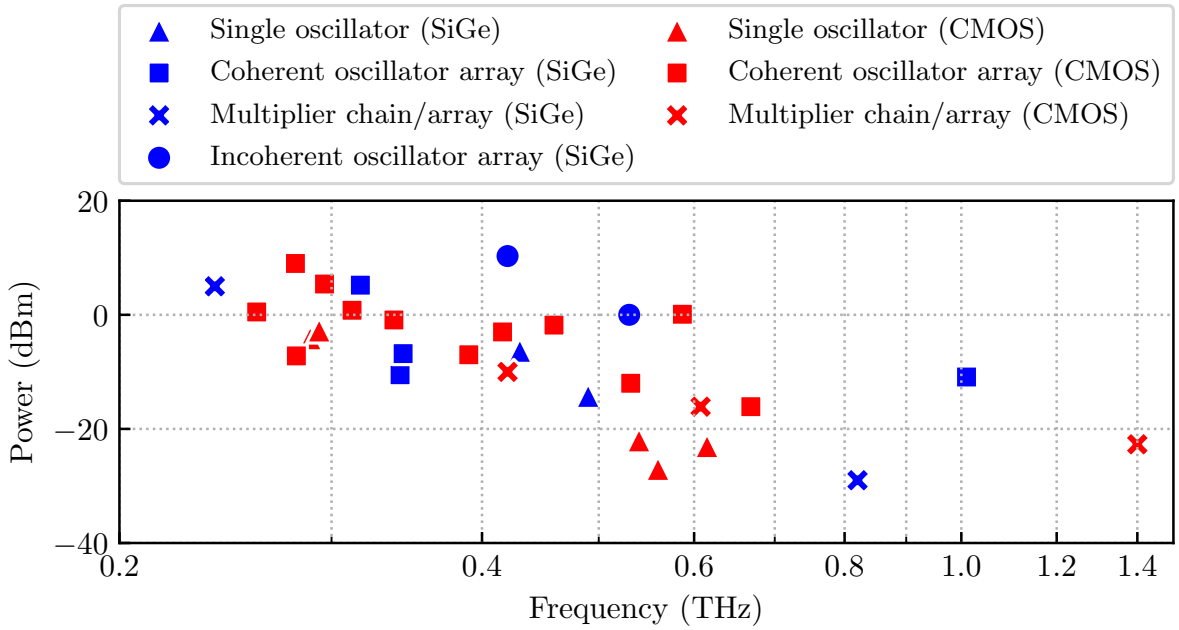


Figure 2.3: Radiation frequency versus power for state-of-the-art silicon integrated THz sources.

be further scaled with multi-chip scaling (see Sec. 2.3), only incoherent arrays are capable of this feat. Any coherent arrays would quickly face issues related to the generation and distribution of phase locking signal in a multi-chip structure. While the mutually coupled source arrays are at least on-chip scalable, they also have a small locking range (from $f_0/20$ to $f_0/10$ where f_0 is the fundamental locking frequency [94]). Thus, for large arrays, PVT variation can destroy the mutual synchronization resulting into phase noise degradation. All the elements in a mutually coupled coherent array must also operate together for phase locking, and the illumination reconfigurability is restricted to the non-trivial beam steering. Incoherent arrays, on the other hand, do not face such limitations. They allow extensive on-chip and multi-chip scaling. Thermal throttling and dc bias routing are the biggest issues here for such scalability, but these can be managed since individual elements can also be operated by selectively turning off most or some part of the array. As reported in [46] and also in Chapter 4, this allows interesting THz computational imaging techniques. Another important advantage of incoherent source arrays is the mitigation of image speckles [98]. These are formed due to unintended interference between EM waves that are scattered and reflected from an object. In the best case, they result in image ambiguities, while in the worst case, large constructive or destructive interferences can destroy the useful image dynamic range. Clearly, the coherence length is larger for coherent source arrays, and this causes higher or more image speckles. This is not an issue for incoherent array based illumination since the radiated power is divided into multiple beams with uncorrelated phases.

2.2.2 THz signal reception

2.2.2.1 Performance metrics

For THz receivers, the most important performance metric is sensitivity which implies the minimum power detectable by a receiver. This in turn is related to the undesired output noise of a receiver which can drown the desired response signal if the former is relatively higher. For RF, the sensitivity is defined in terms of noise equivalent power (NEP) for active receivers or noise equivalent temperature difference (NETD) for passive radiometers. The NEP value can be converted into NETD and vice-versa [99]. The discussions here will be limited to NEP since this is a more relevant metric for the active imaging systems. The second important parameter relates to the front-end RF input bandwidth (RF-BW) and the baseband response signal bandwidth (BB-BW). The former is important for wideband radiometers [99] and spectroscopy [66], while additionally, the latter is important for noise and speed trade-off at the receiver output response signal. Assuming that the output noise power spectral density (PSD) is $\mathbf{S}_n(f)$ (where f is the frequency) and BB-BW is f_{BB}, the integrated output noise $\mathbf{S}_{n,int.}$ of the receiver is:

$$\mathbf{S}_{n,int.} = \int_{-\infty}^{\infty} \mathbf{S}_n(f)df \approx \int_{0}^{f_{BB}} \mathbf{S}_n(f)df \tag{2.1}$$

since $\mathbf{S}_n(f) \approx 0$ for $f > f_{BB}$ and $f < 0$ (assuming a low-pass output). Along with this, if f_{BB} is the 3dB bandwidth, e.g. related to a first-order RC time constant τ_{BB}, the integration time τ_{int} required to read 99% of final signal value is:

$$\tau_{int} \approx 5\tau_{BB} = 5/f_{BB} \tag{2.2}$$

Thus a larger BB-BW results in a faster readout at the cost of a larger integrated noise. A low output noise PSD is therefore crucial for fast, high sensitivity receivers.

The other important performance metrics are the dynamic range (DR), which is the ratio of maximum to minimum detectable power within the linear range of operation at a receiver; and its dc power consumption. When abundant source power is available, a high DR is desired over a high sensitivity. For low light environments, a low NEP (or high sensitivity) is preferred. One receiver design challenge is to manage both, i.e. a low NEP and a high DR, for all lighting conditions. Lastly, a low dc power consumption is always an advantage.

2.2.2.2 Design approaches

Silicon integrated THz receivers have either heterodyne or direct architecture. The block diagram for a heterodyne THz receiver is shown in Fig. 2.4(a). The dashed lines indicate the front-end low-noise amplifier (LNA), which is intended to boost the signal without adding much additional noise. This is characterized by the noise factor (NF), which is the ratio of the SNR at input to the SNR at output of an amplifier or a frequency conversion block. Note that NF is always ≥ 1 and a smaller value indicates a better noise performance. Room-temperature

THz LNAs are difficult to design in silicon because of the available small power gain [40].

In heterodyne THz receivers, the incoming RF signal is down converted to an intermediate frequency (IF) signal by using a local oscillator (LO) and a down conversion mixer. For an RF signal $A_{RF}\cos(2\pi f_{RF}t+\psi)$ and an LO signal $A_{LO}\cos(2\pi f_{LO}t)$, the general down conversion process to an IF signal S_{IF} can be described as:

$$\begin{aligned} S_{IF}(t) &= A_{RF}\cos(2\pi f_{RF}t+\psi)\cdot A_{LO}\cos(2\pi f_{LO}t) \\ &= \underbrace{\frac{A_{RF}A_{LO}}{2}\cos(2\pi t(f_{RF}-f_{LO})+\psi)}_{\text{Downconverted IF}} + \frac{A_{RF}A_{LO}}{2}\cos(2\pi t(f_{RF}+f_{LO})+\psi) \end{aligned} \tag{2.3}$$

where ψ represents the additional RF phase. The down converted IF frequency f_{IF} is $|f_{RF}-f_{LO}|$. The up converted signal with frequency $f_{RF}+f_{LO}$ is filtered out. It can be noticed that the LO signal boosts the IF signal power. The LO frequency can either be equal or different from the RF frequency. In the former case, the LO frequency can also be derived from the RF signal. This is termed as homodyne or zero-IF down conversion. In the later case, the LO frequency can be higher (upper-side injection) or lower (lower-side injection) than the RF, but this is a more important consideration in communication receivers with specific band and image rejection requirements. For imaging receivers, the IF signal is down converted to a baseband response signal using a direct power detector, which generates an electric voltage or current signal proportional to the IF signal power. Amplifiers may be placed after the mixer and the direct detector. Assuming that the detector signal is a voltage output V_o with voltage noise spectral density v_n, the voltage responsivity R_V and NEP of the receiver can be defined as:

$$R_V = \frac{V_o}{P_{in,THz}} = CG_{RX}\cdot R_{V,IF} \qquad [\mathrm{V\,W^{-1}}] \tag{2.4}$$

$$\mathrm{NEP} = \frac{v_n}{R_V} \qquad [\mathrm{W}/\sqrt{\mathrm{Hz}}] \tag{2.5}$$

where CG_{RX} is the conversion gain of the receiver front-end (LNA and mixer combined), and $R_{V,IF}$ is the voltage responsivity of direct detector at IF frequency. The units are mentioned in square brackets. In the above equations (2.4) and (2.5) the RF-BW and BB-BW are assumed to be unity. When BB-BW is not unity, the noise power can be summed over this bandwidth to arrive at an integrated NEP. Along with sensing the THz signal power, quadrature heterodyne receivers can also recover the signal phase [70].

Heterodyne receiver architecture improves the sensitivity by LO boosting of the IF signal power, with minimal noise addition, before feeding it to the detector. In this way the detector output noise doesn't degrade the SNR practically. However, such circuits consume large chip area and large dc power because of the required components (LO and the mixer). A power detector can also be used directly for THz sensing. This is shown in Fig. 2.4(b). Such direct detector uses the device non-linearity to rectify the incoming THz signal into an electric voltage or current. A front-end LNA also benefits the sensitivity here, but it again leads to a larger chip area, larger

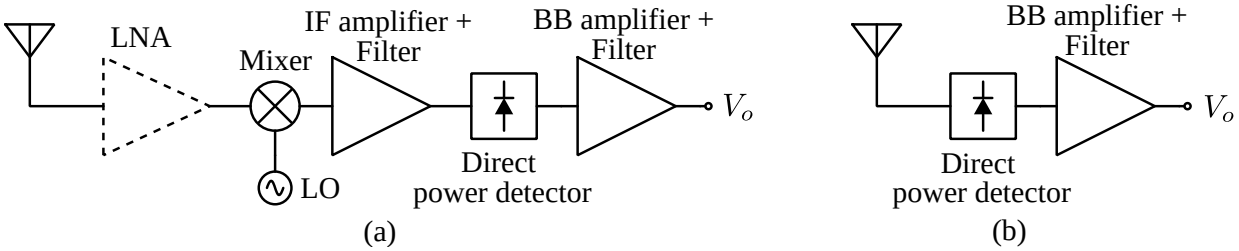


Figure 2.4: Antenna-coupled THz sensor topologies for (a) heterodyne, and (b) direct detector.

power consumption, and a narrowband performance. For power detectors without any LNA, the NEP is higher by up to six orders of magnitude as compared to heterodyne receivers (Fig. 2.5). The phase information is also lost. However, the chip area and the power consumption are much smaller. For antenna-coupled THz power detectors, the majority of chip area is occupied by an integrated antenna, which is scaled in proportion to the THz signal wavelength [100]. In silicon technology, CMOS FETs [101], [102], SiGe HBTs [103], [104], schottky barrier diodes (SBDs) [105], and even substrate well diodes [106], have been used for direct THz detection. The best sensitivities and bandwidth have been achieved from SiGe HBT detectors [104]. However, they also consume dc power in the forward active region of operation [104]. CMOS transistors, with cut-off frequencies much smaller than THz frequencies, can also detect THz radiation. The detection principle is based on distributed resistive mixing [107]. They offer a near-zero power consumption in cold-channel configuration and a lower-cost fabrication as compared to the HBTs. The empirical evidence also suggests that CMOS detectors scale better to higher frequencies [102] as compared to SiGe HBTs [104] while the latter allow for a wideband impedance match between the antenna and detector due to a lower impedance level at the detector input [3]. The responsivity and the NEP can be measured directly for such detectors, as per the equations (2.4) and (2.5).

2.2.2.3 Array integration

A single pixel THz receiver cannot be used for single-shot imaging[1]. Array integration is desirable to parallelize the received signal into multiple pixels. A heterodyne receiver array can use locked or unlocked LO for each pixel. In the former case, the phase information can be recovered and the receiving phased-arrays can also be implemented exactly like the source counterparts [108]. In the latter case, phase information is lost yet the sensitivity advantage of heterodyne detectors remain. As already discussed in the previous case, heterodyne detectors consume large chip area and dc power. Therefore, such arrays cannot have a large pixel count in practice due to the thermal, variability, and cost bottlenecks (see Sec. 2.3 for further explanation).

Direct detectors, on the other hand, consume very small chip area and a near zero dc power. Therefore, thousands of direct detector pixels can be implemented on a single chip. With the same approach, world's first CMOS integrated 1k-pixel 0.7–1.1 THz camera was demonstrated by IHCT in 2012 [109]. No heterodyne arrays can potentially match such integration density.

[1]One exception is reciprocal imaging or compressed sensing, which is discussed in Chapter 4

An important consideration here is to readout multiple pixels with a shared scheme, but this requires row-column multiplexing and a small readout period (or a large readout bandwidth) per pixel for real-time image frames. For example, using a rolling shutter with 1k-pixel THz camera, imaging at 25 frames per second (fps) allows maximum $40\,\mu s$ integration time per pixel, corresponding to a readout bandwidth of $125\,kHz$ as per Eq. (2.2). Since the direct detectors have a large NEP, the design of a low noise readout circuit becomes crucial to preserve the camera sensitivity.

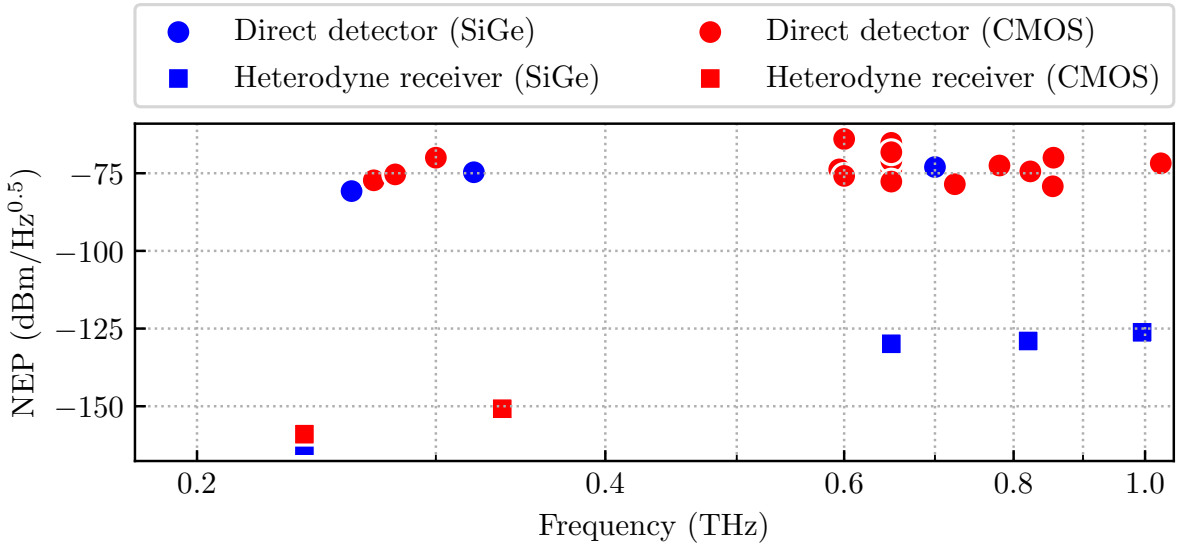


Figure 2.5: Frequency versus sensitivity for state-of-the-art antenna-coupled silicon integrated THz receivers at their best operation points. Note that the bandwidth for direct detectors can be a significantly large fraction of the reported frequency band, which has not been indicated.

2.2.2.4 Discussions

A detailed comparison between all different silicon integrated THz receivers is difficult to present in a single graph due to the differences in reporting of their RF-BW and BB-BW. Fig. 2.5 presents the NEP versus best operation frequency for some state-of-the-art antenna-coupled silicon integrated THz receivers in both CMOS and SiGe technologies. For this comparison, the NF of heterodyne receivers has been converted to an equivalent NEP [3]. Note that heterodyne receivers have around 60 to $80\,dB$ (six to eight orders of magnitude) better sensitivity than direct detectors. Heterodyne receivers beyond $0.3\,THz$ are rare, and the discrete data points reported at $0.65\,THz$, $0.82\,THz$, and $0.99\,THz$ originate form the same multicolor THz imaging chipset developed at IHCT [66]. Heterodyne detectors are also narrowband, large, and power hungry. For example, a harmonic oscillator based heterodyne receiver pixel in 40nm CMOS in [110], operating at $335\,GHz$ with an equivalent NEP of $-150\,dBm/\sqrt{Hz}$ consumes $53.1\,mW$ power and $0.26\,mm^2$ chip area. The direct detectors might appear as missing in the 0.3–$0.6\,THz$ band, yet this is not the case in practice. As reported earlier, direct detectors can be ultra-wideband. For example, IHCT has demonstrated NEP as low as $40\,pW/\sqrt{Hz}$ ($-74\,dBm/\sqrt{Hz}$) in the continuous

band from $220\,\mathrm{GHz}$–$1\,\mathrm{THz}$ for a $0.0225\,\mathrm{mm}^2$ large SiGe HBT detector pixel [111], and in the continuous band from 0.7–$1\,\mathrm{THz}$ for a $0.01\,\mathrm{mm}^2$ large CMOS detector pixel [102]. Both detectors consume near zero dc power. Due to the small chip area, high pixel integration density, small power consumption, large bandwidth, and mixed signal integration in a low-cost technology, a CMOS-direct-detector-based fully digital THz camera has been designed in this work. The digital NEP and operation frequencies of such THz cameras from the literature will be compared in Chapter 5.

2.2.3 Lens-coupled arrays

The antenna-coupled source and detector arrays can hugely benefit from attaching a high-resistivity hyper-hemispherical silicon lens. In the preferred configuration, the antennas radiate from the backside (towards the substrate) of the chip. The chip is centered and glued from the backside to the plane of silicon lens as shown in Fig. 2.6(a). The extension length of this lens is selected such that the pixel-array is located at the focal point of an approximate ellipse formed by the hyper-hemispherical lens [112]. In ray optics, such elliptical focus allows a collimated beam with infinite directivity [113]. From the EM perspective, the radiation from the source antenna is coupled to the lens and is radiated outwards for transmission, or the radiation incident on the lens is coupled to the detector antenna for reception. The far-field directivity depends on the ratio of the lens extension length X to the lens radius R (Fig. 2.6). In [112], an extension-to-radius ratio of 0.38 – 0.39 was reported to provide the largest directivity for a double-slot antenna. The directivity also drops for the off-axis pixels, i.e. pixels that are farther away from the antenna center [114]. In reality, these values may vary based on the frequency and the type of antenna used, and an exact and precise design requires full-wave EM simulations.

Assuming that the lens-antenna is well-designed, the silicon lens approach provides the following benefits as compared to the other antennas and lenses:

1. **High gain:** The hyper-hemispherical lens acts as a semi-infinite substrate. The energy from the antenna is directed more towards the higher permittivity silicon as compared to the air, leading to a higher gain. There are no coupling losses because both chip substrate and lens are of made of silicon. The lens to air coupling loss ($\sim 30\,\%$) can also be mitigated with a $\lambda/4$ anti-reflection coating [112]. However, such coating is futile whenever a broadband antenna behavior is desired.

2. **Low substrate losses:** The EM energy from the antenna to the lens is directed at a normal angle to the lens curvature. Thus, the structure does not support surface-waves [112]. This prevents the formation of any energy trapping substrate modes, thus minimizing the substrate losses.

3. **Small pixel cross-coupling:** Because of the absence of substrate modes, the mutual cross-coupling between different pixels is also smaller than $-30\,\mathrm{dB}$ [100]. Therefore, such a lens allows the integration very dense pixel arrays.

4. **Small chip area:** One significant advantage of the silicon lens is that it allows smaller on-chip antennas. For front-side radiating antennas such as patches [115], the antenna size is related to the permittivity of free-space. When the antennas radiate from the chip backside into a silicon lens acting as a semi-infinite substrate, the antenna size becomes a function of the silicon permittivity [116]. Due to this, the linear dimension and the area of an antenna can be reduced by up to $3\times$ and $10\times$ respectively as compared to the patches. Combined with a large pixel packing density, the saving in chip area more than compensates for any additional cost of the lens.

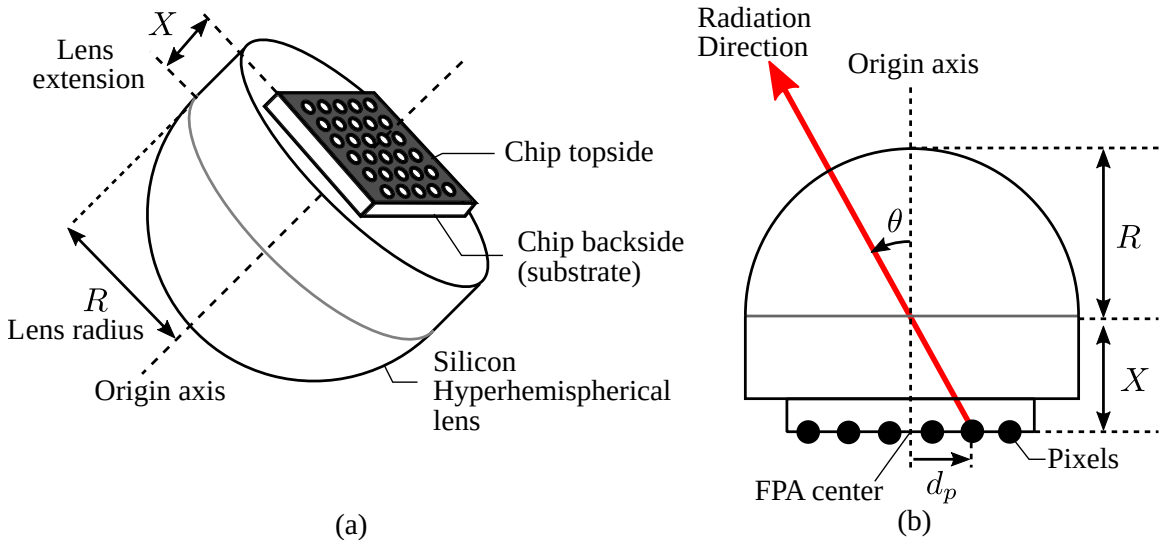


Figure 2.6: (a) Lens-coupled array assembly and (b) pixel to angle mapping.

In addition to the above stated benefits, the close-to-elliptical focus of the lens also allows for pixel to angle mapping [59]. This implies that the spatial location of a pixel on an array corresponds directly to the transmitting or the receiving beam angle, assuming a collimated beam for the latter. The mapping is deterministic, and it can be predicted to the first order with a pinhole image formation model. This is shown in Fig. 2.6(b). Here, the 2D beam angle (θ, ϕ) can be calculated as:

$$\theta = \tan^{-1} \frac{d_p}{X} \quad \text{and} \quad \phi = \tan^{-1} \frac{d_q}{X} \tag{2.6}$$

where d_p and d_q indicate the respective distances of the row and column of a pixel with index (p, q) from the FPA center (aligned to the lens center). Here, the FPA is assumed to consist of $P \times Q$ pixels, with $p \in [1, P]$ and $q \in [1, Q]$. The elliptical lens extension length is denoted by X which includes the chip thickness (typically $150\,\mu\text{m}$ [100]). Note that some interpolation is necessary for the $(\theta, \phi) \mapsto (d_p, d_q)$ mapping to conform to the discrete pixel locations at the FPA. A zero-order scheme interpolates (d_p, d_q) to the nearest pixel. For a rectangular array, the overall field of view (FoV) resembles a rectangular pyramid, and the maximum FoV angle along the

array diagonal can be calculated as:

$$\text{FoV} = 2 \cdot \tan^{-1} \frac{(d_P + d_Q)^{0.5}}{X} \tag{2.7}$$

where (d_P, d_Q) is the distance of the corner (i.e. pixel (P, Q)) from the lens FPA center. The ideal maximum directivity D_0 for the central pixel can be calculated from the lens aperture area A_e as [117]:

$$D_0 = \frac{4\pi A_e}{\lambda_0^2} \tag{2.8}$$

where $A_e = \pi R^2$ is the effective lens aperture for radius R. The directivity rolls down for off-axis pixels, which is a complex function related to the field definitions at the lens surface and a reduction of the effective lens cross-section normal to the radiation direction of the pixel [114]. The directivity in turn can be used to calculate approximate half-power beam width (HPBW) of the beam with standard formulas [117].

This imaging model was used in [59] for the first demonstration of THz light-field imaging with a CMOS THz camera [109], which is discussed in Chapter 3. There, a lens with radius $R = 7.5\,\text{mm}$ and extension length $X = 2.83\,\text{mm}$ was used. For a $2.56 \times 2.56\,\text{mm}^2$ camera chip with $80\,\mu\text{m}$ pixel pitch [109], this results in a net diagonal FoV of $65.2°$ ($\pm\, 32.6°$) and D_0 varying between 40.2 and $44.2\,\text{dBi}$ for the 650 – $1028\,\text{GHz}$ frequency band. The model was further verified with light-field mapping based spectral analysis of a grating coupled THz source reported as in [118].

2.3 Multi-chip scaling

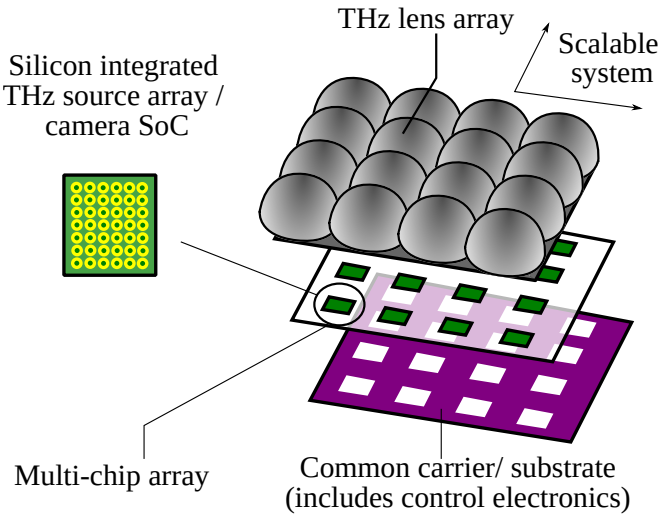


Figure 2.7: The proposed multi-chip scaling approach.

The previous discussions establish that highly integrated unlocked source arrays and incoherent cameras fabricated in silicon technology allow the pixel-count scalability that is required for 2D single-shot active THz imagers. Such arrays, when coupled with a silicon lens, also allow

a pixel to angle mapping, i.e. the pixels readily provide a directional diversity. As we shall see in Chapter 3, light-field imaging needs a spatio-directional diversity. Directly adopting the technique now popular in visible light cameras [119], one can assemble a lens-array atop a very large monolithic pixel array. However, because of large THz pixels (compared to the visible light), this approach presents the following problems:

- More transistors on a single chip result in a larger heat generation, leading to a thermal throttling of the radiated power in sources, a large noise in cameras, thermal drifts in the circuit operating points, and the breakdown related chip failures.
- A larger chip area leads to a higher chip fabrication cost which increases linearly with the pixel count. The fabrication capabilities also limit the number of pixels that can be integrated on a single chip, necessitating complex wafer level die stitching with fabrication area and cost overheads.
- A larger chip area directly correlates to a larger pixel performance variation, due to the statistical distribution of the impurities and the dopant concentration, the change in dc bias points due to the routed metal resistance, and the large temperature gradients that may develop over the chip area. It becomes increasingly difficult to calibrate and accommodate this variability in an imaging system.

Therefore, an extensive scaling of the pixel count over a single chip is not practically feasible. To avoid all these issues, a multi-chip scaling approach is proposed. This is illustrated in Fig. 2.7(a). The SoC can be a small pixel count array with a lower thermal envelope, manageable variability, and an economical fabrication cost. Multiple SoCs are combined on a common carrier or substrate to scale up the pixel count. Each SoC also has its own lens to provide a spatio-directional diversity over the multi-chip array.

Note that multi-chip scaling is only possible with unlocked source arrays and incoherent cameras which do not need any external RF interfacing, since distributing a phase synchronized RF signal becomes exponentially difficult with increasing number of chips. For the same reason, SoCs must have a low pixel count. Digital interfaces are preferred for their robustness, reconfigurability, and multiplexing. Since an SoC has a smaller number of pixels, it can be designed for an optimum performance over the thermal, power, and cost budgets. On-chip digital logic can be added to provide smart features such as in-situ calibration and modulation diversity [46]. Particular design requirements for source array and camera SoCs are discussed separately in Chapters 4 and 5 respectively.

The technology to fabricate THz lens arrays is also not available yet. Full array manufacturing has been demonstrated with stacking of ion-etched silicon wafers [120], [121], but such lenses are restricted in their thickness and require a high directivity from the on-chip antenna to avoid a spillover loss. This can be specially challenging for compact pixel footprints. In the multi-chip camera system presented in Chapter 6, the lens attached SoC packages are assembled side-by-side over a printed circuit board (PCB) with header pin based alignment.

2.4 Summary

In this chapter, we have looked at the silicon process technology, reviewing some benefits and challenges pertaining to the THz IC design. The SG13C/SG13G2 technologies used to design the SoCs in this work have also been briefly introduced. Silicon technology offers a large integration complexity, low marginal unit cost for high-volume production, and reliable operation specially for mixed-signal ICs. However, the challenges related to slow transistor speed, low power handling capacity, transmission line losses, and external RF interfacing must be dealt with ingenious system design approaches. A review has also been presented for the design techniques and expected performance from state-of-the-art THz sources and detectors. Based on this analysis, it has been argued that the incoherent THz source arrays and incoherent THz cameras offer the best path forward for pixel count scalability required in light-field imagers. Attaching these arrays at the elliptical focus of a silicon hyper-hemispherical lens readily provides the directional diversity with a pixel to angle mapping. The lens also reduces pixel coupling, size, and chip area, together while improving the antenna radiation efficiency. Building upon these aspects, a multi-chip scaling has been introduced for incorporating spatio-directional diversity as a practical and cost-efficient approach to design THz light-field imaging systems.

Chapter 3

Light-field imaging

In this chapter, we describe the concept and formulation of the light-fields. These ideas have been described for visible light [58], [119] or even millimeter wave and lower frequency coherent RF waves [122] in the existing literature. Our discussions are biased towards incoherent THz light as per the subject matter of this dissertation. The relevant differences between the visible and THz radiation are pointed in Table 3.1. A series of imaging experiments that were conducted for scanning based THz light-field imaging are also discussed.

3.1 General introduction

The light-field is a ray-tracing based technique. Here, the light flowing into and out of the object is considered as a vector field composed of ray bundles, which are quantified in terms of the energy density propagating along a specified direction and position in the 3D space. If the position and flow direction of individual light rays are known, either back-propagation (from the sensor) or forward propagation (from the source) can be applied to reconstruct a 3D volume source of the field disturbance [58], [123]. The light-field method works with incoherent radiation, but it requires spatio-directional sources and detectors, i.e. components which can synthesize and sample the light along multiple angles across different spatial locations. Isotropic, incoherent sources are excellent at generating spatio-directional light-fields that can be readily sampled by a camera. Light-field techniques have become really popular for visible light imaging due to the ubiquitous availability of such sources and inexpensive cameras [124].

3.1.1 The fundamental concept

The fundamental idea behind light-field imaging is illustrated in Fig. 3.1(a). This diagram corresponds to a simplified representation commonly used to illustrate the ideas on the paper flatland [125]. A spatio-directional light-field is shown between two planes, one classified as the source plane and other classified as the sensor plane based on the direction of energy flow. In reality, such representation may encompass one subspace of a full light-field system which

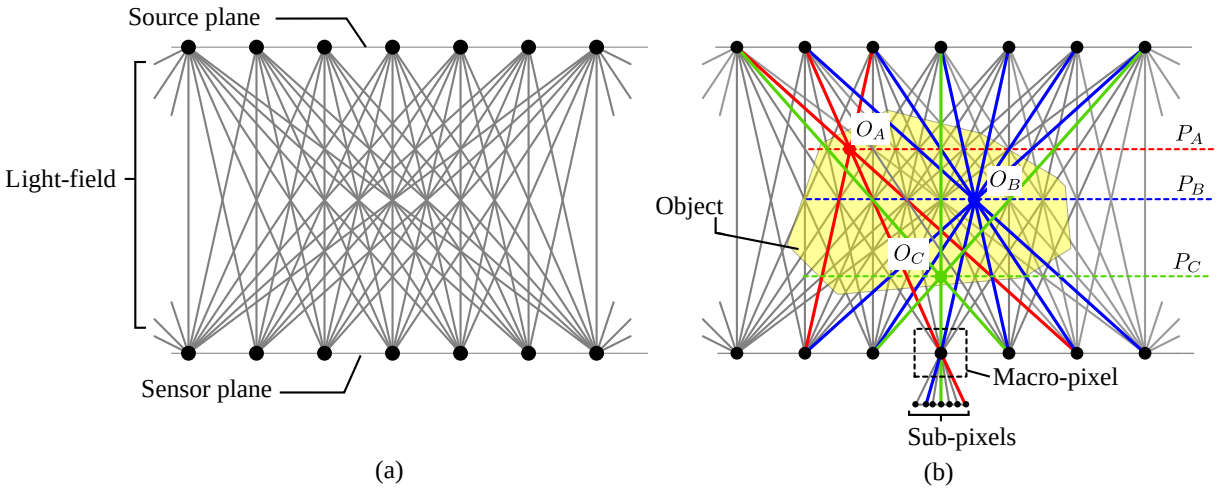


Figure 3.1: (a) Spatio-directional light-field between a source and sensor plane, (b) focusing onto different points / planes along the object depth by integrating light rays highlighted with same colors. The sub-pixel and macro-pixel arrangement at one sensing point is also shown.

might also consist of other components such as lenses and mirrors. It is assumed that the sources and sensors are isotropic, i.e. they radiate and capture energy respectively along all directions. Assuming that there are no wave effects (diffraction and interference), the straight lines joining the sources and the sensors form the light-rays. Next, Fig. 3.1(b) shows an object placed within the light-field. The exact nature of this object is immaterial for the current discussions and here it is assumed to be fully transparent. In reality, an object is partially transmissive and partially reflective thus perturbing the light-field.

If all the spatio-directional light-rays are sampled at the sensor plane, ray-tracing and integration of light intensity along different sets of rays in post-processing can allow focusing on different parts of the object (including its depth axis). This is shown in Fig. 3.1(b) with three sets of rays highlighted in red, blue, and green colors to focus on points O_A, O_B, and O_C inside the object respectively. The concept can be extended to multiple sets of rays to acquire three 2D images corresponding to the planes P_A, P_B, and P_C forming cross-sections along the object depth, leading to a 3D reconstruction.

How do we sample the light-field? If each point on the sensor plane is a single pixel, all the light rays captured within this pixel are integrated in intensity, and the spatio-directional information is irrevocably lost. Instead, multiple sub-pixels are required at each sensor position (macro-pixel) to sample the incident light along different directions [126], [127] as shown in Fig. 3.1(b). This macro-pixel is the key building block for any light-field imaging system. The object sampling density corresponds to the discretization of the light-field, which is associated with the spatial and angular arrangement of the sub-pixels and the macro-pixels.

3.1.2 Applications in other EM frequencies

Light-field imaging has been very popular for the visible light due to the ubiquitous availability of the incoherent and diffused sources (sunlight / lamps), cameras (analog and digital), and optical lenses. Comprehensive reviews of the history and techniques for visible light-field imaging can be found in [58], [124], [125]. The first experiments were based on scanning a scene by moving a single camera, for applications such as modelling of a 3D illumination source [128], virtual imaging illustration [129], digital archiving of renaissance art sculptures [130], and the interactive city panoramas [131]. Later systems also utilized camera arrays, including an 8×8 array [132] and a 6×8 array [133] of video cameras without explicit synchronization, a 100 video cameras array with explicit synchronization scheme [134], and others [135]. More compact light-field camera designs have also been demonstrated, consisting of a 2D array of micro-lenslets arranged over a digital camera sensor [125]. This technology is now commercialized for 3D imaging and computational aperture synthesis in photography [136], [137]. A similar camera has also been used for single-shot 3D microscopy [138]. Some of these advancements have led to the multi-camera setups available widely in modern day smartphones [139], [140]. The "Shack-Hartmann sensors" used for wavefront sensing in adaptive optics are based on a similar light-field principle [141]. The light-field technology is also being pursued for mixed reality displays [142]–[144].

Light-fields have also been used for infrared (IR) and X-ray radiation. A passive IR camera for 3D imaging, using the natural thermal emission from imaging targets, was demonstrated in [145]. In [146], light-field approach was used for computational aperture synthesis to remove the fixed pattern noise from an IR camera. The light-field technique is also being explored for low-dose volumetric X-ray imaging [147], [148]. However, since the optical lenses do not work for X-rays (refractive index ~ 1), these light-field approaches build a few (mostly two) perspective views of a scene, e.g. by splitting the incident X-ray beam along two different angles.

3.1.3 Challenges at THz frequencies

There are many similarities between the visible light and the incoherent THz light-field systems. Both require spatio-directional sensors and diffused illumination. The plenoptic function for both (see Sec. 3.2) is real valued and the intensity drops by $1/r^2$ for a distance r away from a point source for a spherical wavefront in the far-field. However, there are also significant differences between THz and visible light, as outlined in Table 3.1, thus presenting unique challenges for THz light-field systems.

First, the wavelength at THz is around three orders of magnitude larger than the visible light. This comes at the cost of a larger scale wave diffraction, resulting into larger beam waist and beam divergence angles. The ray based light-field formulation does not account for such behavior. Also, high intensity isotropic incoherent THz sources do not exist so far. It is not possible to do computational light-field imaging in the absence of appropriate illumination. The same is also true for THz sensors. Another particularly important challenge at THz is the

	Visible light	THz radiation
Wavelength	100s of nm	100s of $\mu\mathrm{m}$
Source		
Strong natural sources	Yes	No
Artificial sources	Yes	Yes
Type	Area emitters / diffused	Antenna emitters / directive
Power	High	Low
Carrier frequency	100s of THz	~ 1 THz
Receiver		
Sensors	Area-based	Antenna-based
Sensitivity	High	Low
Number of sensors	Few millions	Few hundreds
Lens arrays	Yes	No

Table 3.1: Comparison between visible light and THz radiation for light-field imaging

low integration density, as only a few hundreds of THz sensors can be integrated within a focal-plane array (FPA) as compared to the visible light sensors with millions of pixels. This directly limits the light-field density and the achievable image resolution. The lens-arrays [119] that are required to capture the spatio-directional light-field in compact cameras are also not available at THz frequencies.

3.2 Light-field formulation

The light-field formulation discussed here assumes a distribution of light in the form of rays. A ray is an abstract concept which describes the flow of a radiation intensity or radiance along a specific location and direction in space. Most commonly, the light-field is described as a multidimensional function, called the plenoptic function [123]. It can be stated with all possible dependent variables as:

$$\text{Plenoptic function} := L(x, y, z, \theta, \phi, t, f) \tag{3.1}$$

where L quantifies the radiant intensity for an EM wave at frequency f at a point (x, y, z) in the 3D space, flowing along a direction with elevation θ and azimuth ϕ, at a time instant t. For coherent radiation, L measures the complex wave amplitude instead of the intensity [122]. In addition, the wave polarization can also be quantified if required.

3.2.1 4D plenoptic function

For incoherent diffused radiation, polarization and precise frequency specifications are irrelevant. A steady state case is assumed for the time-independent or static light-fields. For dynamic (video) light-fields, the different frames can also be treated independently as quasi steady states. Additionally, only a few planes along the propagation axis z modify the direction of light rays, which include components such as lenses, mirrors, as well as the imaging objects. Apart from these, the propagation axis z can also be ignored without any loss in information. This results

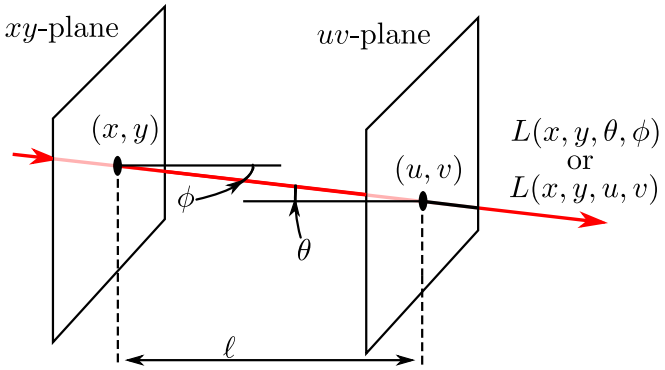


Figure 3.2: A light ray in space (highlighted in red) with 4D angular and two-plane parameterized plenoptic function. Planes xy and uv are parallel to each other.

into a reduced 4D parameterization of the light-field that is common in the literature [149]. For two parallel planes separated by a distance ℓ along axis z, the angles can be replaced with a two plane parameterization as shown in Fig. 3.2.

$$\text{4D plenoptic function} := \underbrace{L(x, y, \theta, \phi)}_{\text{Angular parameterization}} \equiv \underbrace{L(x, y, u, v)}_{\text{Two-plane parameterization}} \tag{3.2}$$

Here, xy and uv are the two parallel planes. The two formulations are interchangeable as per the spherical to cartesian coordinate transformation in the following manner [150]:

$$\begin{aligned} x - u &= \ell \cot\theta \cos\phi \\ y - v &= \ell \cot\theta \sin\phi \\ \sin\theta &= \frac{\ell}{\sqrt{(x-u)^2 + (y-v)^2 + \ell^2}} \\ \tan\phi &= \frac{y-v}{x-u} \end{aligned} \tag{3.3}$$

For example, for a point source at location (x_0, y_0) transmitting a total power P_T from an antenna with directivity $D_T(\theta, \phi)$ at the boresight perpendicular to the xy-plane, the 4D plenoptic function quantized to a location (u_0, v_0) at the sensor plane located at a far-field distance ℓ_0 can be written as:

$$L(x_0, y_0, u_0, v_0) = \frac{P_T}{4\pi r^2} D_T(\theta_0, \phi_0) \tag{3.4}$$

where $r = \sqrt{(x-u)^2 + (y-v)^2 + \ell_0^2}$ is the length of straight line joining the source and sensor points, and $D_T(\theta_0, \phi_0)$ is the directivity of source antenna along this line for the angles (θ_0, ϕ_0) as per Eq. (3.3). For an antenna-coupled receiver at location (u_0, v_0) with a directivity $D_R(\theta', \phi')$ and a boresight perpendicular to the uv-plane, the received power P_R can be calculated as per the Friis transmission equation [151]:

$$P_R = L(x_0, y_0, u_0, v_0) \frac{\lambda^2}{4\pi} D_R(\theta_0', \phi_0') = P_T \Big(\frac{\lambda}{4\pi r}\Big)^2 D_T(\theta_0, \phi_0) D_R(\theta_0', \phi_0') \tag{3.5}$$

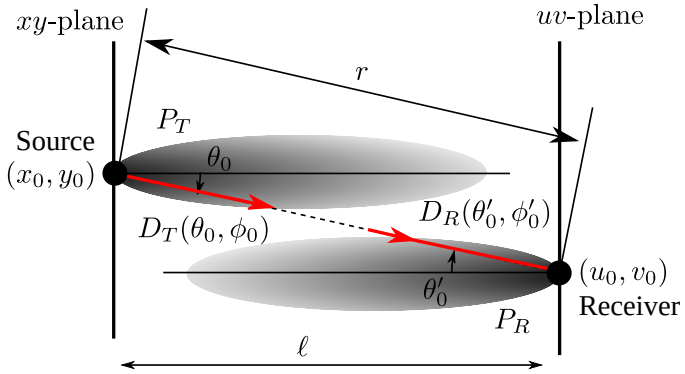


Figure 3.3: Light-field formulation for single point source and receiver with directivities D_T and D_R respectively. Transmitted power P_T and received power P_R are related as per Eq. (3.5).

Here, $(\lambda^2/4\pi)D_R(\theta_0', \phi_0')$ is the effective aperture of the receiver looking into the direction of source. Also note that for the parallel xy and uv planes, the angles are $\theta = -\theta'$ and $\phi = -\phi'$ including the sign convention. This formulation, as depicted in Fig. 3.3, explains how the light-field plenoptic function relates to the energy transfer formulation used for mm-waves and THz.

Equations (3.2) to (3.5) represent the fundamental math that can be used to investigate any light-field system operating in the far-field. For THz, additional modifications are required, such as quasi-optics [152] to account for the near-field diffraction, and scattering models [153] to quantify the interaction of light-field with an object. Several research studies have discussed the similarities of light-fields to other abstract level wave theories, and have proposed extension of computation enabled light-fields to include other wave effects. In [122] the authors compared light-field and MIMO coherent 3D imaging approaches for mm-wave and lower frequency RF composed of very few antenna elements and low directivity beams. In [154], the authors discussed the similarities between the light-field and the "Wigner distribution function" from optics that takes account of the wave phase. In [155], the authors extended the light-fields to "Augmented light-fields" by postulating positive and negative radiance to account for the wave interference. Another extension of light-fields towards "Quasi light-fields" for coherent radiation has been proposed in [156].

3.2.2 Rayspace simplification

The esoteric 4D formulation just discussed is primarily intended for computational algorithms. In light-field literature, a more simplified form is commonly used to develop a high-level intuition about an imaging setup [125]. A 2D spatio-directional slice of the plenoptic function, for example in (x, θ), is easier to sketch on the paper, while also conveying sufficient information along an axial symmetry. This is termed as the "rayspace diagram", where the radiation and the sampling space available from the source and the sensor respectively can be highlighted along the spatial and angular coordinates. The rayspace diagrams for an isotropic source and a Gaussian beam [152] are shown in Fig. 3.4 and 3.5 respectively. For the Gaussian beam, the

rayspace diagram in the diffraction dominated confocal region (within the Rayleigh range) cannot be plotted because of the complex physical behavior [157]. This is also true for the near-field of an antenna. The far-field rayspace diagram for a silicon-lens coupled THz camera is illustrated in Fig. 3.6. This is also valid in general for any lens coupled pixel array. Fig. 3.6 also shows the rayspace transformation introduced by a collimating lens commonly used at THz for 2D imaging [109]. The sampling density and resolution are limited by the diffraction constrained finite beam width and divergence, and the power integrating spatio-directional aperture of each beam is seen as a box in the rayspace.

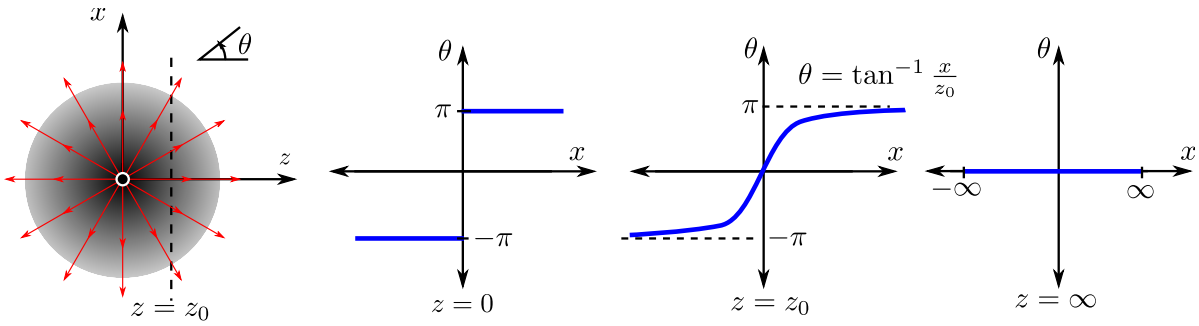


Figure 3.4: Rayspace diagrams for an isotropic source (rays shown in red) at different propagation distances along z, ultimately transforming into a plane wave rayspace at $z = \infty$.

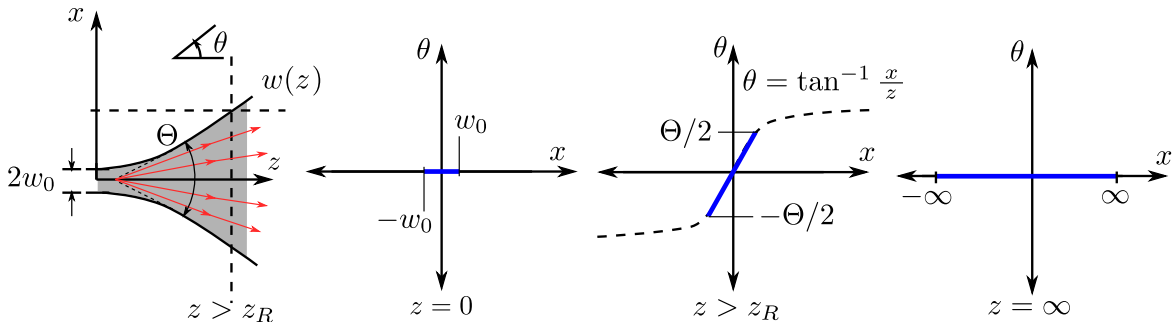


Figure 3.5: Rayspace diagram for a Gaussian beam with waist size w_0, total angular spread Θ, and beam edge $w(z)$ at different propagation distance along z. The physical behavior between of the beam between origin waist ($z = 0$) and Rayleigh range z_R is much more complex [157].

How does the rayspace of a 3D imaging system look like? The rayspace for a THz CT imaging setup from [51] is analyzed in Fig. 3.7. Here, the object is stepped along the x and θ axes relative to the focal point for acquiring one 3D cross-section. The corresponding rayspace consists a set of points spread around multiple θ for single x and vice-versa. This spatio-directional rayspace sampling is necessary whenever 3D imaging is required. A higher sampling density along x and θ axes point to a finer spatial and angular resolution respectively [125]. However, the resolution is ultimately restricted by the diffraction limited width and depth of the focal spot.

Based on this observation, the rayspace diagrams for 3D THz light-field imaging systems comprising either a multi-chip camera array or a multi-chip source array (Sec. 2.3) are conceptualized in Fig. 3.8(a) and (b) respectively. The first case is similar to visible light 3D

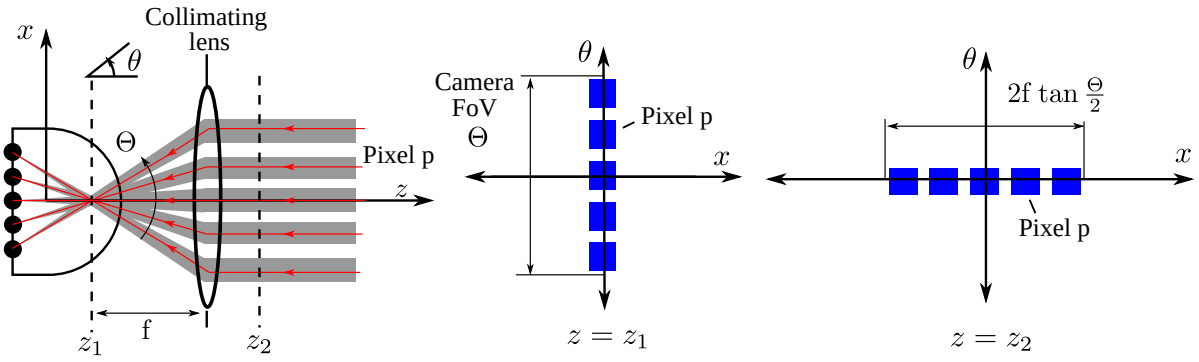


Figure 3.6: Rayspace illustration for a silicon lens coupled camera at the focus plane (z_1) and at the object plane (z_2) after an external collimating lens of focal length f. Blue boxes indicate the spatio-directional power integrating apertures of individual pixels with non-overlapped FoVs.

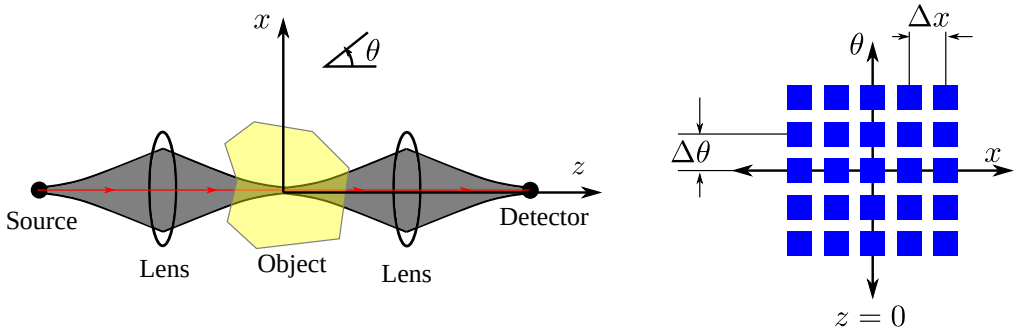


Figure 3.7: Rayspace sampling in a CT imaging system [51]. At focus $z = 0$, the object is incrementally stepped by Δx and $\Delta\theta$ in x and θ respectively to create a 3D image slice. Size of each diffraction limited rayspace integral (blue box) relates to the width and depth of beam focus.

cameras [125]. When diffused radiation is available, the pixels in a multi camera array can resolve it into the spatio-directional rayspace. The second case is equivalent to the compressive light-field sensing system [158]. Here, a single detector with a large angular (or isotropic) and large spatial aperture can be used. The illumination itself is divided into spatial and angular domains, and these components are encoded into a basis that can be identified at the detector output. For compressive sensing, this basis is in the form of coded apertures [158]. This technique is also familiar from 3D cinema, where two angular perspectives of a scene are encoded into orthogonal polarizations (basis) that are separated at each human eye by using polarizing 3D glasses. As reported in Chapter 4, the source array SoC also allows direct encoding of spatio-directional beams in a temporal or a Fourier basis [46]. Unfortunately, neither a diffused illumination source nor a large isotropic single detector is available for THz radiation. Therefore, the imaging systems that are demonstrated later are limited by currently realizable counterparts to the source array and camera SoCs. In Chapter 7, a THz light-field MIMO imaging system is proposed as an outlook that can utilize both multi-chip source array and multi-chip camera array in a unified imaging system for general 3D imaging.

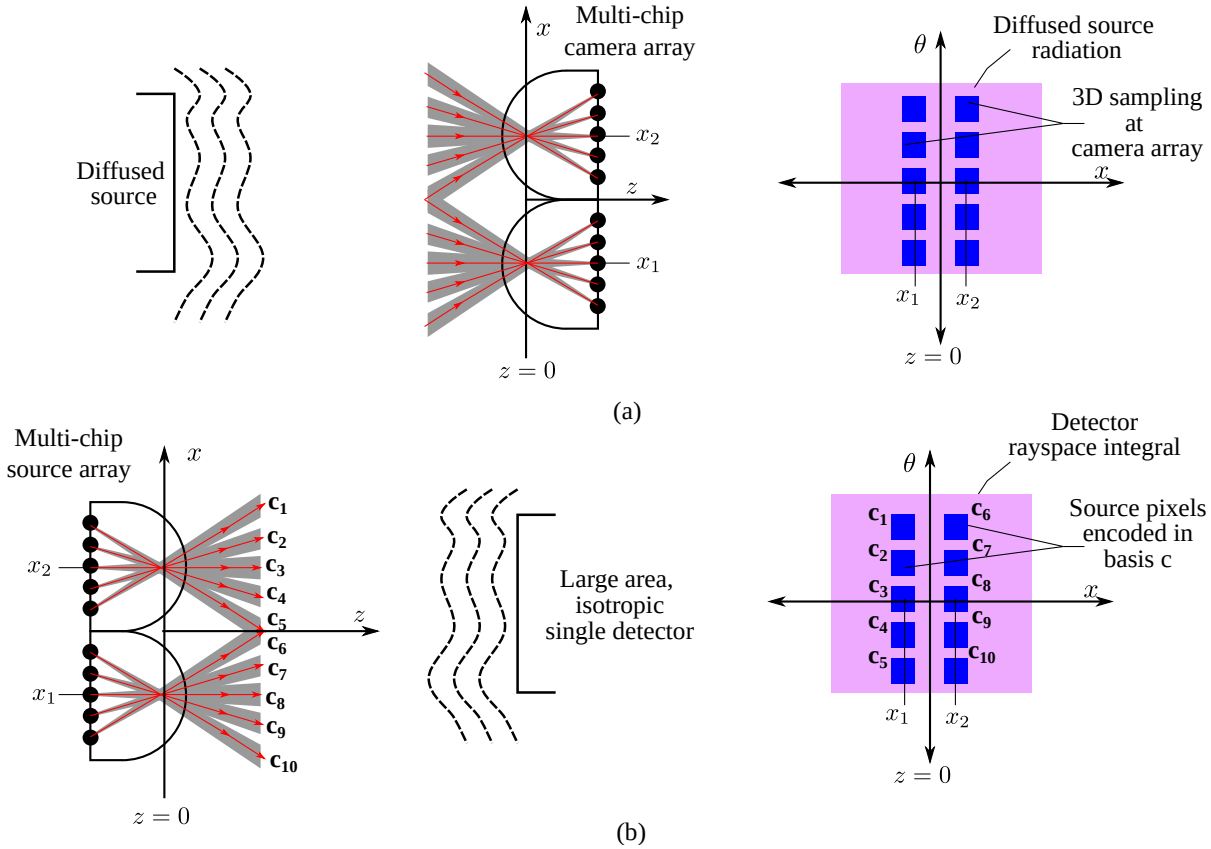


Figure 3.8: Rayspace for 3D THz light-field imaging with (a) multi-chip camera array and a diffused source, (b) multi-chip source array and a single large area, isotropic detector. Here, the source pixels are encoded in a basis **c** that is resolvable at the detector output.

3.3 Scanning based THz light-field imaging

This section presents the light-field imaging experiments that were conducted with the existing 1k-pixel camera module [109]. These experiments were aimed at the verification of the THz light-field imaging concepts and to understand the fundamental capabilities and challenges of the same. Some of these results have been published in [59], [159].

The terminology that shall be used throughout this section is illustrated in Fig. 3.9. The camera FPA consists of $P \times Q$ total pixels where P is the number of pixel rows and Q is the number of pixel columns, with uniform pixel pitch δ. For the 1k-pixel camera module in [109], $P = Q = 32$ and $\delta = 80\,\mu\text{m}$. The pixel index is (p, q) where p is the row index in range $[1, P]$ and q is the column index in range $[1, Q]$. The camera is used to capture images at $M \times N$ positions arranged in a uniformly spaced square grid with step size Δ. The positions can refer either to the camera scanning with a stationary object and source (Fig. 3.10), or to the object scanning with a stationary source and camera (Fig. 3.17). The position index is labeled as (m, n) with m and n in range $[1, M]$ and $[1, N]$ respectively. Comparing to the two-plane parameterization from Fig. 3.2, the position indices may be visualized as discrete points at the uv-plane. The recorded signal value V (in volts) of a camera pixel (p, q) at position (m, n) is referred as $V(m, n : p, q)$. The full raw

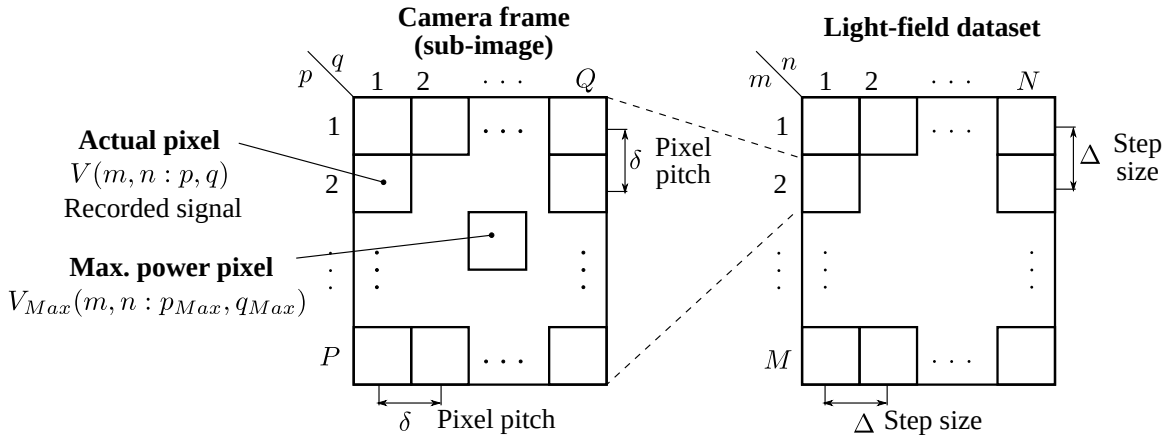


Figure 3.9: Addressing and indexing terminology for the light-field dataset.

image consisting of $M \times N \times P \times Q$ pixels is called the light-field dataset, wherein the individual $P \times Q$ pixels camera images are referred to as the *sub-images*. For several algorithms described later, the pixel with the highest signal at each sub-image is also relevant. These pixels, termed as *maximum power pixels*, are denoted as $V_{Max}(m, n : p_{Max}, q_{Max})$ referring to the largest recorded signal value of V_{Max} and the corresponding pixel index (p_{Max}, q_{Max}) for a sub-image at position (m, n).

3.3.1 Transmission-mode imaging

The goal of these measurements was to capture and render the radiation from a point THz source in transmission mode using light-field based ray-tracing [59]. Ideal ray-tracing was used while disregarding any diffraction and near-field effects. The measurement scheme is illustrated in Fig. 3.10(a). The camera scan plane was located at a distance d away from the source approximately perpendicular to the source boresight. No external optical component were used. Fig. 3.10(b) shows the corresponding rayspace diagram for the image formation. Note that for a planar scan, the FoV limitation still applies and only the source radiation with divergence under $46°$ (equal to the camera FoV [109]) in both E-plane and H-plane can be measured this way. At the scan plane, the camera was stepped along a uniform square grid to capture sub-images. The terminology shown in Fig. 3.9 applies.

From the raw light-field dataset, the point source illumination was recovered using two separate algorithms – (A) light-field mapping, and (B) maximum power pixel.

(A) Light-field mapping – This algorithm is designed from the ideal geometrical ray-tracing. For each camera position (m, n), a pixel with index (p, q) is selected as per the geometric light-field mapping.

Let us assume that the center of scan plane is aligned to the source boresight, and consider only the row axis at both the scan plane and the camera FPA as shown in Fig. 3.10. The distance of the m^{th} scan position from the scan plane center is $u = \Delta[m - (M + 1)/2]$. At this point, the straight ray joining the source to the camera is sampled at an angle θ, by a pixel p at the camera

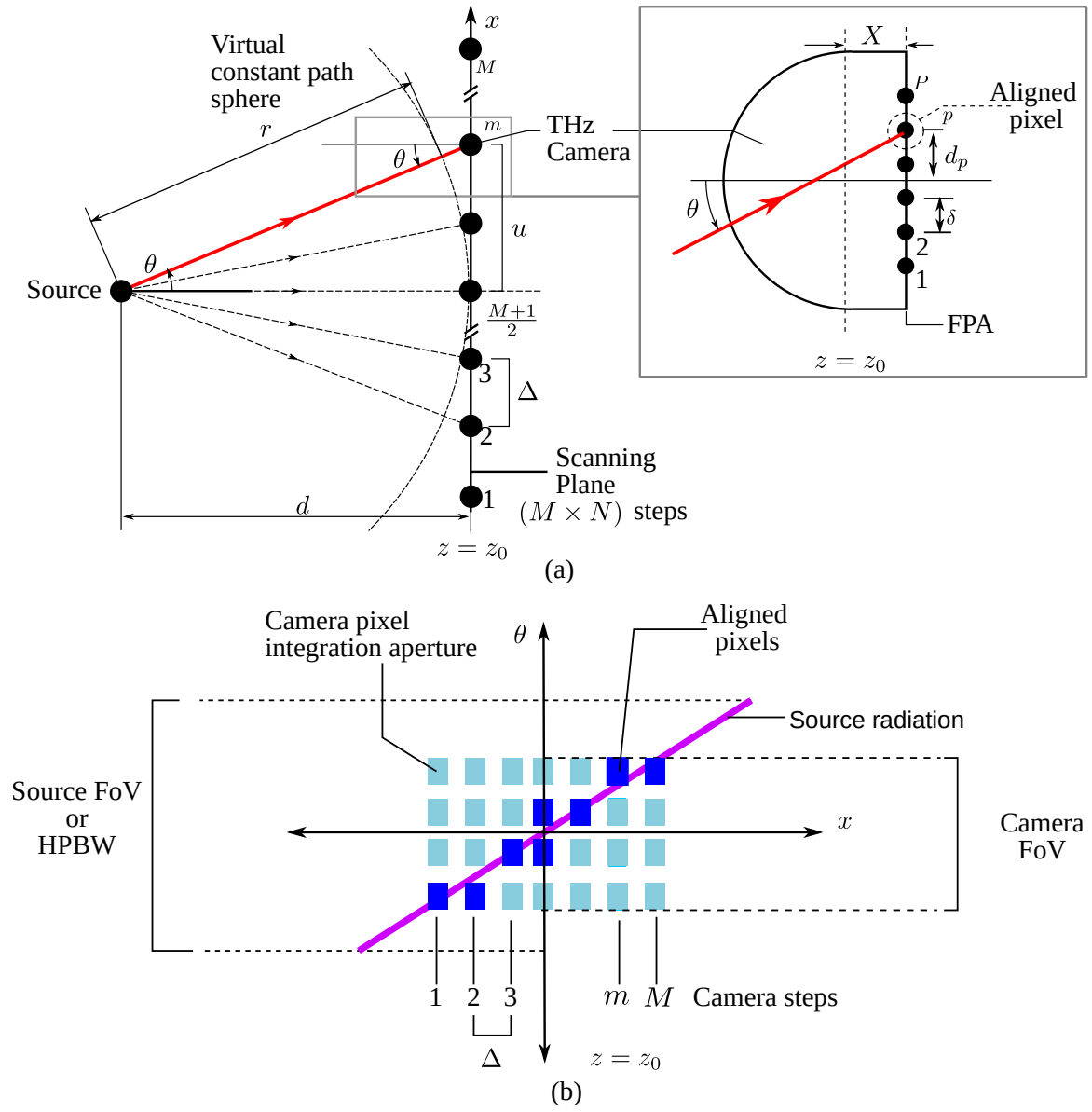


Figure 3.10: (a) Scanning based and transmission mode THz light-field imaging scheme. Terminology from Fig. 3.9 applies. (b) Corresponding rayspace diagram at the scan plane.

FPA, as per the model discussed in Sec. 2.2.3, Eq. (2.6). The distance of this pixel from the FPA center (co-aligned to the lens center) is $d_p = \delta[p - (P+1)/2]$. In other words, this pixel p at scan position m is the one which is oriented towards the source. The goal is to find a mapping $p = f(m)$ to select this pixel p from the sub-image captured at position m. This can be done by equating the tangent of angle θ at the camera scan plane and at the FPA, i.e. by solving for $u/d = d_p/X$ where X is the lens extension thickness ($2.83\,\mathrm{mm}$ for the camera used [59]). The

same analysis also applies for the column axis, yielding the following mapping functions:

$$p = \frac{1}{2}\Big[(2m - M - 1)\frac{\Delta}{\delta} + (P + 1)\Big] \tag{3.6}$$

$$q = \frac{1}{2}\Big[(2n - N - 1)\frac{\Delta}{\delta} + (Q + 1)\Big] \tag{3.7}$$

Note that since (p, q) must be integers, some interpolation scheme has to be applied. This can, for example, take into account the Gaussian FoV profile of the camera pixels. Here, a zero order interpolation scheme is used, i.e. the values are rounded off to the nearest integer. Simulations from [59] suggest that even with zero-order interpolation, the mapped pixel (p, q) samples a $-3\,\mathrm{dB}$ or better fraction of the ray power. Also, the mapping scheme is valid in the far-field where the incident radiation approximates a plane wave at the camera aperture. In the near-field, physical diffraction complicates the mapping scheme, and it has not been accounted in our first-order analysis.

As the camera moves farther away from the scan plane center, the distance between camera and source increases, resulting in a higher path loss. The signal $V(m, n : p, q)$ measured at the mapped pixel can be corrected for this variation as following:

$$\widetilde{V}(m, n : p, q) = \frac{V(m, n : p, q)}{d^2} \cdot \Big[(m - \frac{M+1}{2}\Delta)^2 + (n - \frac{N+1}{2}\Delta)^2 + d^2\Big] \tag{3.8}$$

where $\widetilde{V}(m, n : p, q)$ is the corrected signal. The above expression relies on the r^{-2} proportionality of source power in free-space as per the Friis transmission equation.

(B) Maximum power pixel – Since the radiation power is available from a single point source, the camera pixel best aligned to the source should sample the maximum power in the sub-image. Therefore, instead of a geometric mapping based pixel selection, the pixel with the largest signal V_{Max} can be picked from each sub-image along with its index (p_{Max}, q_{Max}) for each camera position (m, n). This signal must also be corrected as per Eq. (3.8). This technique is much simpler, and it can be used to verify if the ray mapping from Eq. (3.6) and (3.7) correctly predicts the brightest pixel.

Two imaging experiments were conducted in the transmission mode as described next.

3.3.1.1 Radiation pattern characterization of a THz source

In this experiment, the radiation pattern of a CW THz source was extracted with light-field scanning. Classically, such characterization has been done by moving a single detector along a sphere centered at the fixed source, or by moving the source along its pivotal point using a two-axis rotational stage with a fixed detector at the boresight [117]. In both techniques, the pattern quality depends on the precise alignment of the source center. The light-field based planar scan does not require such precision as any alignment errors can be corrected during the computational post-processing.

In the particular experiment shown here, the radiation pattern of a $0.53\,\mathrm{THz}$ 4×4 pixel source with $0\,\mathrm{dBm}$ ($1\,\mathrm{mW}$) of power [60] was characterized. The reference pattern power profile from [60] was also available for comparison. The distance d was chosen to be $20\,\mathrm{cm}$. It is notably smaller than the source antenna far-field distance of approximately $80\,\mathrm{cm}$, but it was necessary to limit the free-space propagation losses in view of the low camera sensitivity at 0.53 THz [109]. The camera was mounted on a Universal robots UR5 6-axis robotic arm, and it was stepped in $M \times N = 41 \times 41$ positions on a square grid with step size Δ of $4\,\mathrm{mm}$ ($\pm 0.1\,\mathrm{mm}$ accuracy), covering a scan area of $16 \times 16\,\mathrm{cm}^2$. Images were read out at the video-rate (25–30 fps), and 1024 frames were averaged at each position to reduce noise by a factor of 32 [160]. This corresponds to an integration time of approximately $40\,\mathrm{s}$ for each camera position. The fixed pattern noise of the camera [160] was also calibrated periodically before each horizontal line scan. The overall image time was $17\,\mathrm{h}$. Note that the scanning parameters were determined based on the basic knowledge of the source radiation characteristics (total FoV and directivity of each source pixel) to acquire a reasonable pattern quality within a practical measurement time. In particular, the fan-out angle of the source beams ($\pm 15°$), and the spatial extent of each source pixel at the scan plane ($\approx 3.5\,\mathrm{cm}$) were used to set up the scan plane dimensions and the step size respectively. In the absence of such information, these parameters can be optimized iteratively over multiple scans. A multi-chip camera array along with more sensitive detector pixels can expedite such measurement significantly. More details about the measurement setup are available in [59].

The logarithmic scaled raw light-field image dataset (normalized to the largest pixel value) that was acquired is shown in Fig. 3.11(a). The dataset consists of 1.72 million pixels. It can be noticed that a single beam marked within a circle is sampled across multiple sub-images in the light-field dataset. One sub-image in Fig. 3.11(b) shows the distribution of sampled power along multiple pixels. This can be attributed to the near-field distance between the camera and the source module which results in a non-planar wavefront at each scan position. The original pattern measured in [60] is also shown in Fig. 3.11(c).
From the raw dataset, the pattern was rendered using both – the light-field mapping and the maximum power pixel algorithms. The results are shown in Fig. 3.12. Here, the patterns are plotted in decibel color scale normalized to their maximum values. For THz imaging, the signal can be multiple orders of magnitude larger than the noise, so a logarithmic scale offers better visualization of the dynamic range. The following differences were observed for the two algorithms. First, the maximum power pixel technique exhibits a worse SNR as compared to the light-field mapping. This is simply because in the absence of a signal, the pixel with the largest background noise is selected. Second, two highlighted source beams are not well resolved in the light-field mapping. This can be attributed to the inter-pixel inhomogeneities, thermal drifts, developing near-field wavefront, and switching power non-uniformity [161] of these source elements, that may disturb the radiation propagation in a way that does not conform to the light-field mapping direction. In comparison, these beams are visible during maximum power pixel selection as it does not follow specific direction mapping. The highlighted E-plane and H-plane cross-sections of the rendered patterns are compared to the classical pattern

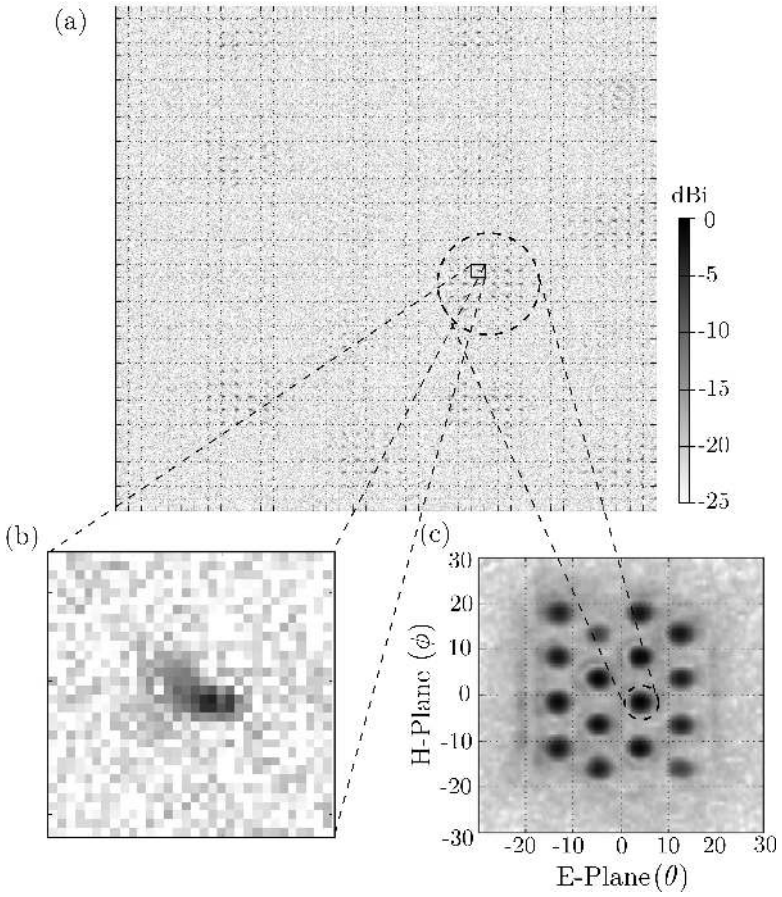


Figure 3.11: (a) Normalized light-field dataset with 41×41 sub-images. The dashed circle marks sub-images sampling a single source beam. (b) A close-in view of one sub-image. (c) Classical source beam radiation pattern of the source module measured in [60]. From [59] © 2016 IEEE.

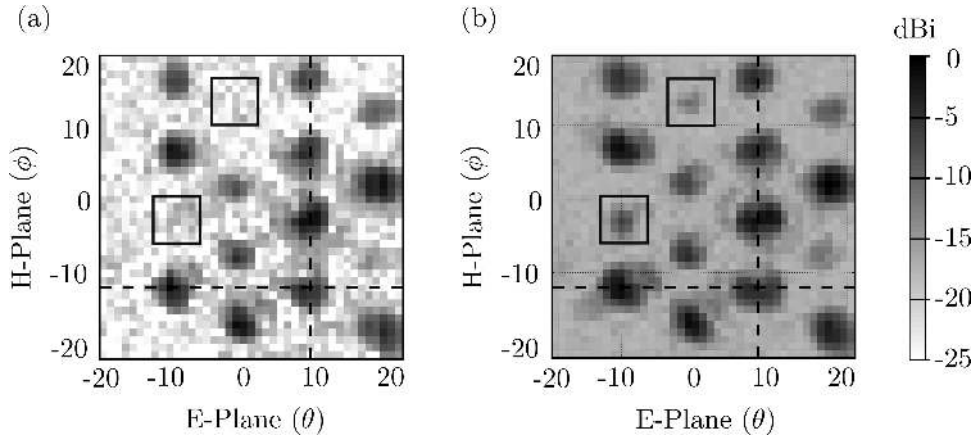


Figure 3.12: The source radiation pattern rendered using (a) light-field mapping, and (b) maximum power pixel selection. Squares mark the source beams that did not render in light-field mapping. See Fig. 3.13 for highlighted E-plane and H-plane profiles. From [59] © 2016 IEEE.

power profiles from [60] in Fig. 3.13. Note that the cross-sections are manually centered to compensate for any tilts. The pixels selected by the light-field mapping sample close to maximum power. Both techniques show a reasonable quantitative estimation of the pattern power profile.

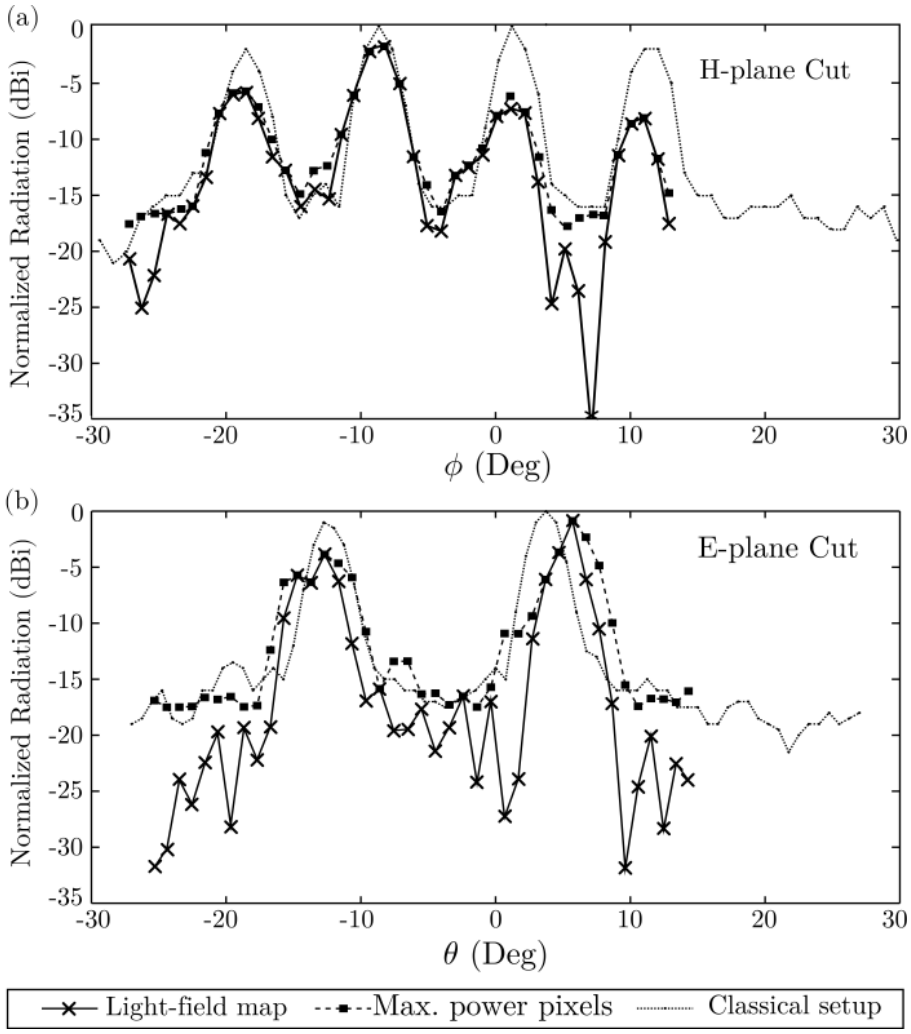


Figure 3.13: Comparison of radiation pattern profiles along the E-plane and the H-plane cuts from Fig. 3.12 rendered using different methods. From [59] © 2016 IEEE.

Differences from the classical setup measurement can be attributed to the near-field effects and the switching power non-uniformity of the source [161].

3.3.1.2 Lens-less transmission mode imaging

In a classical transmission mode imaging setup, the diverging beam from a single point source is collimated using a lens, an object is placed within this collimated beam, and the transmitted beam is refocused to the camera with another lens [109]. The optical train results in attenuation of THz power. Also, when more complex illumination schemes are required, the design of this optical train quickly becomes challenging. In this experiment, the light-field technique was used to create a transmission mode image from the diverging beam of a point source without using any external optics.

Here, a commercial 0.65 THz CW THz source from Virginia Diodes Inc. was used. The source consists of waveguide based ×48 analog-multiplier chain (AMC) and WR-1.5 diagonal horn

antenna (directivity $\sim 25\,\mathrm{dBi}$). The output power of $1.2\,\mathrm{mW}$ was radiated in a single beam. Due to a higher directivity and larger power of the source, as well as a higher camera sensitivity at $0.65\,\mathrm{THz}$, the camera scan plane was located at a farther distance d of $50\,\mathrm{cm}$. The object – a metallic stencil composed of two $3\,\mathrm{cm} \times 2\,\mathrm{cm}$ large rectangular holes separated by a distance of $1.5\,\mathrm{cm}$ – was placed along a plane parallel to the scan plane at an intermediate distance of $40\,\mathrm{cm}$ from the source [59]. The HPBW of $11°$ at the source results in a $9.6 \times 9.6\,\mathrm{cm}^2$ spatial extent of illumination at the scan plane. The camera was scanned along 61×61 points on a rectangular grid with $2\,\mathrm{mm}$ step size, to cover an area of $12 \times 12\,\mathrm{cm}^2$. A 100 frame averaging corresponding to $4\,\mathrm{s}$ integration time at each point was used for an overall imaging time of around $220\,\mathrm{min}$.

From the raw light-field data (not shown here), images were processed using both light-field mapping and maximum power pixel selection. The visual image of the object, as well as rendered THz transmission mode images from both approaches, are compared in Fig. 3.14. The images are shown in linear color scale to contrast the highly saturated signal and noise components, and the image dimensions have been scaled down to reflect the object plane dimensions. Both light-field mapping and maximum power pixel selection produce similar images except for one interesting difference. The latter method shows one scattering related artifact at the corner of one hole of the metal stencil. From visual inspection of the object, it was verified that this corner had developed broken edges due to some unintentional mishandling of the object. The power scattering in random directions is not visible in the light-field rendered image due to its direction specificity. Therefore, light-field mapping can be used to filter out such scattering related artifacts which otherwise pose a major issue for THz imaging [98]. The image and physical dimensions also match. The image cross-sections are shown in Fig. 3.15 to point out the edge profiles and scattered power levels.

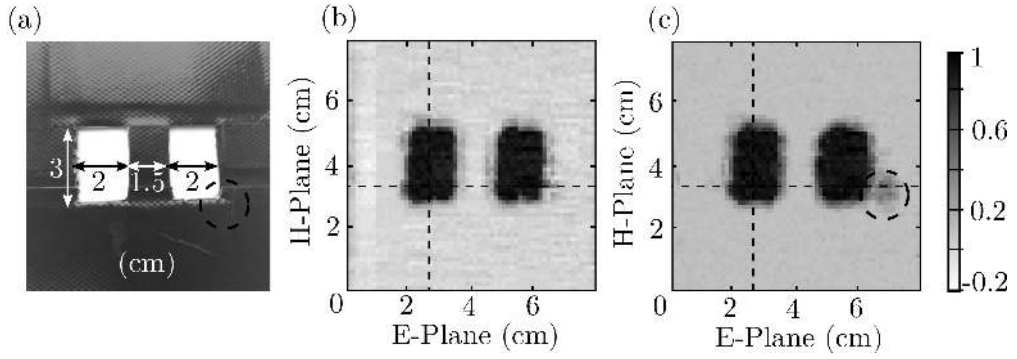


Figure 3.14: (a) Photograph of the metal stencil, (b) normalized light-field rendered image, and (c) normalized maximum power pixel rendered image. Scattering artifact as marked by a circle, and profile cross-sections for Fig. 3.15 are highlighted. From [59] © 2016 IEEE.

Both the above experiments were first-ever demonstration of THz light-field imaging. Despite the limited radiation from a single point source and the ideal geometrical formulation, THz light-field imaging was found to be experimentally feasible.

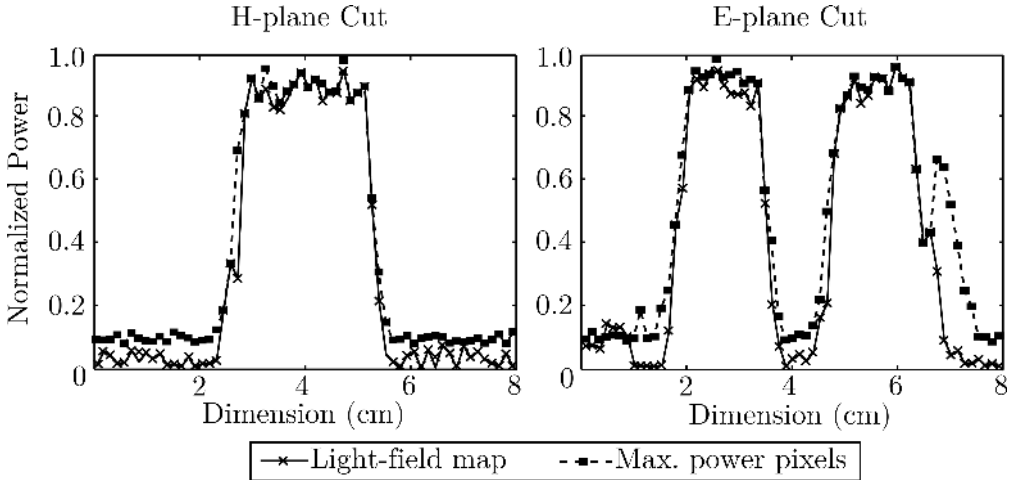


Figure 3.15: Profiles for cross-sections highlighted in Fig. 3.14. From [59] © 2016 IEEE.

3.3.2 Confocal reflection mode imaging

THz reflection mode imaging is particularly preferred for thick dielectric objects and metals that become opaque in the transmission mode, for example in standoff screening and detection [162]. Reflection from a surface is specified in terms of its bidirectional reflectance distribution function (BRDF) [163] which changes with the orientation, roughness, depth, and reflectivity of a surface. An important challenge in reflection imaging is to contrast these surface properties for target identification. Currently, radar systems with confocal optics and mechanical scanning are preferred for THz reflection mode imaging [49], [162]. Here, the term 'confocal' implies that both transmission and reflection optical trains share the same focus. Light from the source is focused at a point on the target, and the reflected light is collected at the receiver with another optical train. To create an image, the focal point is raster scanned relative to the target, where a tight focus ensures a fine spatial image resolution. Radar systems are favored as different reflecting planes along the target depth can be separated with coherent range-gating, leading to a clear target identification in a 3D image [162]. However, as discussed in Chapter 2, coherent THz systems are bulky, power-hungry, and non-scalable. In [162], the problem of imaging speckles was also noticed with radar based standoff imaging.

For all these reasons, incoherent THz reflection mode imaging still remains desirable yet elusive. A classical setup can be built by employing an unlocked THz source and a direct power detector in a confocal arrangement. However, this approach suffers from one major issue as illustrated in Fig. 3.16. The direct detector generates an output signal proportional to the radiation power integrated at its aperture. Based on the target surface properties, the power, wavefront, and direction of the reflected THz beam can change, all of which are interpreted similarly as a net change in the received power for a single direct detector. Therefore, the surface features do not exhibit a specific image contrast, leading to a false identification of the target that renders the whole exercise practically useless.

The fundamental idea behind light-field based confocal THz reflection mode imaging is to

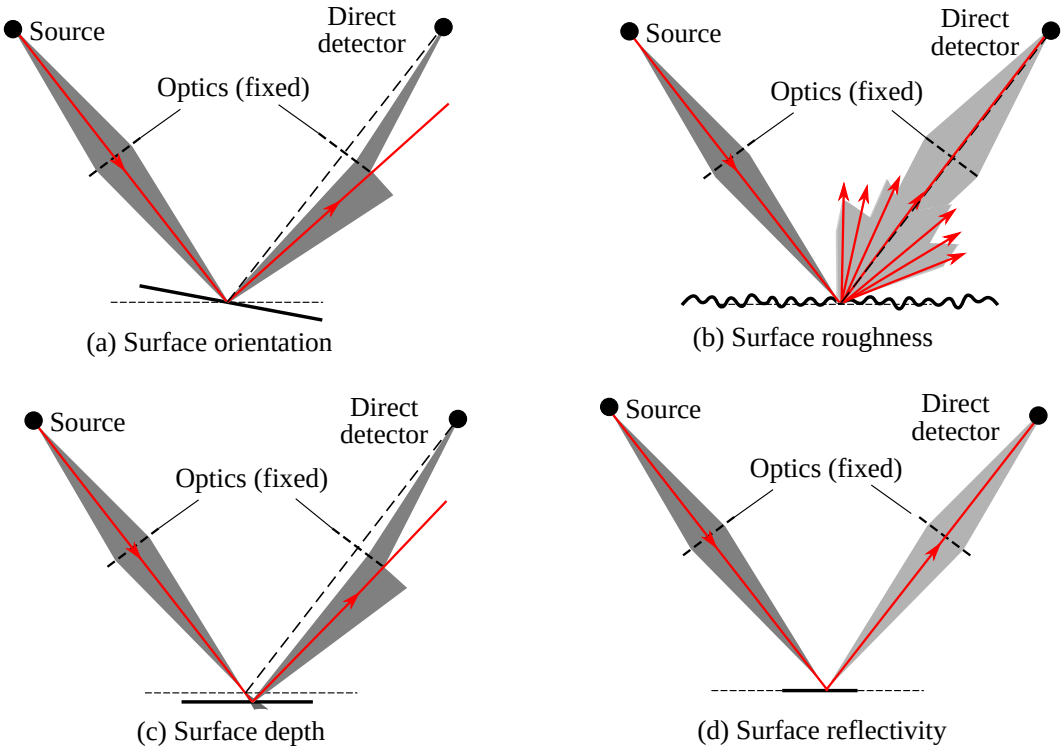


Figure 3.16: (a) Orientation, (b) roughness, (c) depth, and (d) reflectivity of a target surface induce similar change of power received at a direct detector in classical reflection mode imaging.

capture the spatio-directional disturbance of the reflected THz beam, by imaging it with a THz camera instead of a single detector. In post-processing, each sub-image can be reduced to certain parameters contrasting specific surface features optimally.

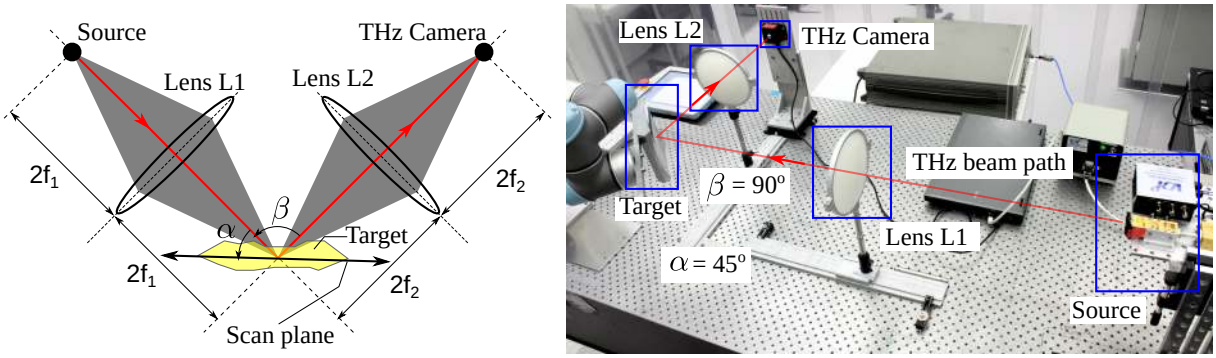


Figure 3.17: (a) Confocal THz reflection mode imaging setup with target scanning. Orientation angle α and bi-static angle β are also shown. (b) Actual picture of the experiment setup.

The imaging setup is illustrated in Fig. 3.17(a). The target is oriented at angle α to the incidence THz beam path. The source radiation is focused on the target by lens L1 with focal length f_1. After reflection, the beam is projected onto the THz camera by another lens L2 with focal length f_2. The incident and reflected beam paths are bi-static with angle β between them. The source, camera, and lenses are fixed leading to a stationary focal spot. The target is mechanically moved

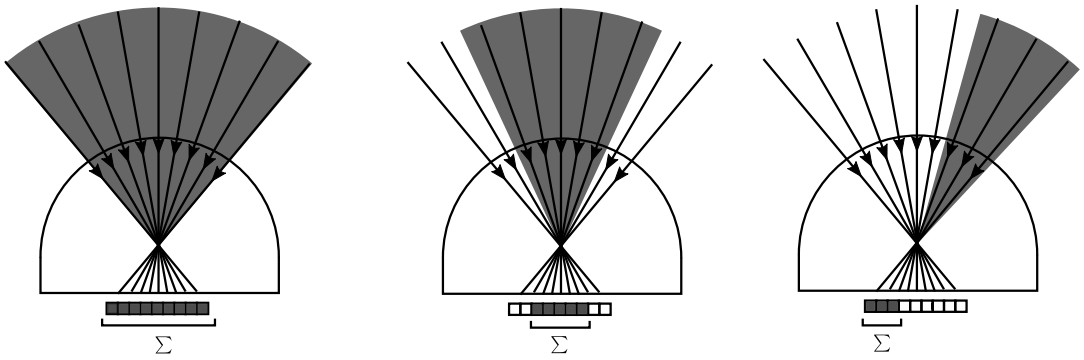


Figure 3.18: Adaptive aperture for an equivalent single detector constructed by integrating different sets of camera pixels in post-processing.

to scan $M \times N$ points in its plane, and the terminology from Fig. 3.9 applies.

A picture of the actual experiment setup is shown in Fig. 3.17(b). Here, a commercial CW AMC source from Virginia Diodes Inc. radiating $2\,\mathrm{mW}$ of output power with $25\,\mathrm{dBi}$ directivity at $0.65\,\mathrm{THz}$, along with the 1k-pixel THz camera from [109] were used. Custom-made biconvex high-density polyethylene (HDPE) lenses were used in both transmit and receive path. The HDPE material was selected due to its low-cost, high dielectric constant (≈ 1.54) and moderate attenuation coefficient ($\approx 0.25\,\mathrm{cm}^{-1}$) at around $0.65\,\mathrm{THz}$ [164]. Lens L1 was designed to have a focal length f_1 of $24\,\mathrm{cm}$ and a diameter of $15\,\mathrm{cm}$, resulting in around $2\,\mathrm{dB}$ of spillover loss from the $25\,\mathrm{dBi}$ source antenna placed at $2\mathrm{f}_1$ distance away from L1. The resulting distance between the source and the target was around $0.96\,\mathrm{m}$ ($\sim 4\mathrm{f}_1$). Also, L1 was thickest at $2.8\,\mathrm{cm}$ at its center exhibiting around $3\,\mathrm{dB}$ of attenuation. The focused beam waist diameter was approximated to be around $1\,\mathrm{mm}$. For L2, a large numerical aperture was desired to couple the reflected beam within full $\pm 23°$ FoV of the camera. However, to limit the lens thickness and attenuation, L2 was designed with a focal length f_2 of $12.2\,\mathrm{cm}$ and diameter of $15\,\mathrm{cm}$. This restricted the usable camera FoV to around $\pm 18°$ encompassing central 22×22 pixels at the FPA. The camera was placed at $2\mathrm{f}_2$ distance away from the lens, resulting in a separation of $0.48\,\mathrm{m}$ ($\sim 4\mathrm{f}_2$) between the camera and the target. At its principal axis, $5.8\,\mathrm{cm}$ thick L2 exhibited around $6\,\mathrm{dB}$ attenuation. The bi-static angle β between the transmit and the receive path was selected to be $90°$, and the target plane was oriented at angle α of $45°$ to the incidence beam. Note that this arrangement was selected only for an easier alignment at the optical breadboard, and the imaging techniques described later are generally valid for any orientation. The target was mounted on a Universal Robots UR5 6-axis robotic arm for scanning. This setup was used for all the measurements as reported later. More details on the lens design and imaging setup are available in [165].

3.3.2.1 Adaptive aperture

The first experiment demonstrates an optimization of the reflection FoV with adaptive aperture. The key idea is described in Fig. 3.18. An equivalent single detector with a programmable aperture can be synthesized by integrating different sets of camera pixels. This property can be used, for example, to select the specular reflections in a specific direction only. The distinct

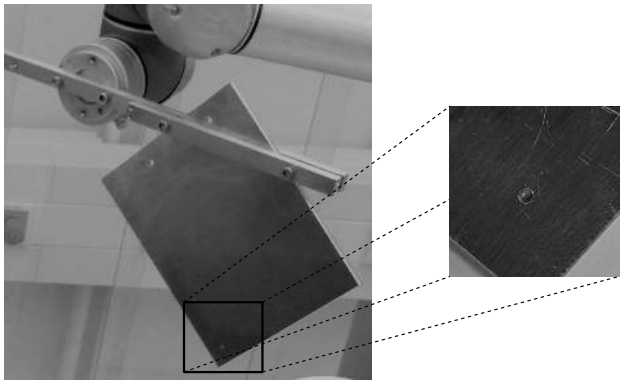


Figure 3.19: Mounted metal plate (the imaging target), with zoomed in area of interest including the orifice.

advantage is that all of this can be done in post-processing, so the technique provides a flexibility in terms of selecting the detector aperture after measurements. Generally any set of pixels can be integrated for unique detector apertures. In the presented experiment, pixels are integrated over a rectangular window, i.e. at each imaging position (m, n), output of the camera pixels are summed up along a window encompassing rows $\{a, b\}$ and columns $\{c, d\}$ at the FPA, denoted as $\Sigma V_{(a,c)|(b,d)}$. A smaller window with fewer pixels indicates a narrower FoV for the equivalent single detector.

To demonstrate the adaptive aperture, a metallic plate with an orifice shown in Fig. 3.19 was chosen as an imaging target. The raw light-field image data was acquired with a confocal setup and $1\,\mathrm{mm}$ step size while scanning the target in the uv-plane. The area of interest is around $3.1{\times}3.1\,\mathrm{cm}^2$, and consists of a circular orifice with diameter of $3\,\mathrm{mm}$. At each point, 16 frames were averaged, and the measurement time for the raw dataset was around $16\,\mathrm{min}$. The processed images are shown in Fig. 3.20. For all of these images, the background noise has been removed with threshold filtering. The maxima image is plotted in Fig. 3.20(a), and it does not show any orifice. This is because the reflected THz power scatters around the edges of the orifice and the scattered power still makes it into the camera. The power integrated around a central 16×16 pixel window at the FPA is shown in Fig. Fig. 3.20(b). The location of the orifice is visible in this picture, however, the scattered power still dominates in this region due to a relatively wide integration aperture of the detector. Subsequently, the size of the integration window is reduced to 8×8, 4×4, 2×2, and 1×1 pixels in Fig. 3.20(c)–(f) respectively. This corresponds to selecting an increasingly narrower angular integration aperture at the FPA. With this, the scattering artifacts are progressively filtered out, and a clearer picture of the orifice emerges. The image resolution is shown with the line profiles plotted in Fig. 3.21 for the cross-sections marked in Fig. 3.20. The trends indicate that the image resolution does not particularly improve. Instead, the image quality improves due to a selective angular filtering of the reflected light.

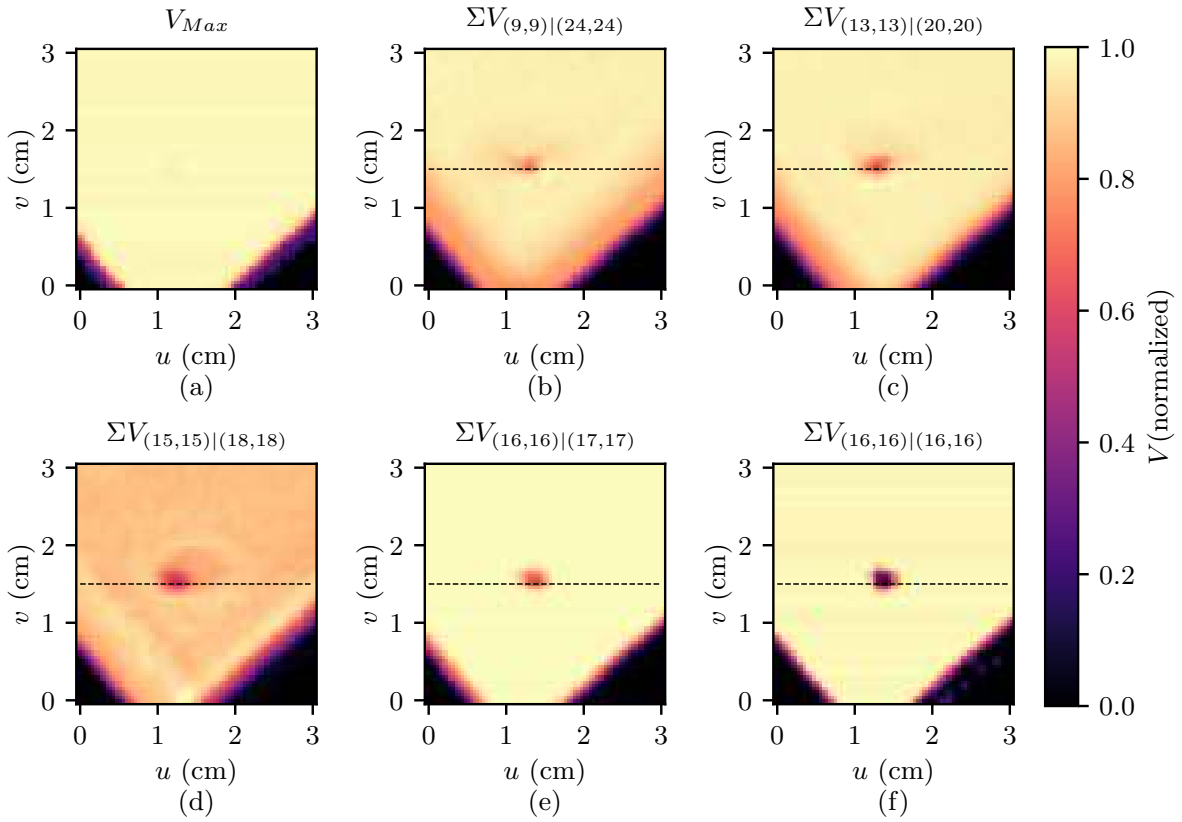


Figure 3.20: Different images formed by setting up different FPA integration apertures in post-processing. Notation $\Sigma V_{(a,c)|(b,d)}$ indicates signal integration across pixels enclosed within rows $\{a, b\}$ and columns $\{c, d\}$ at the FPA. Target is shown in Fig. 3.19. Dashed lines mark the cross-sections which are plotted in Fig. 3.21.

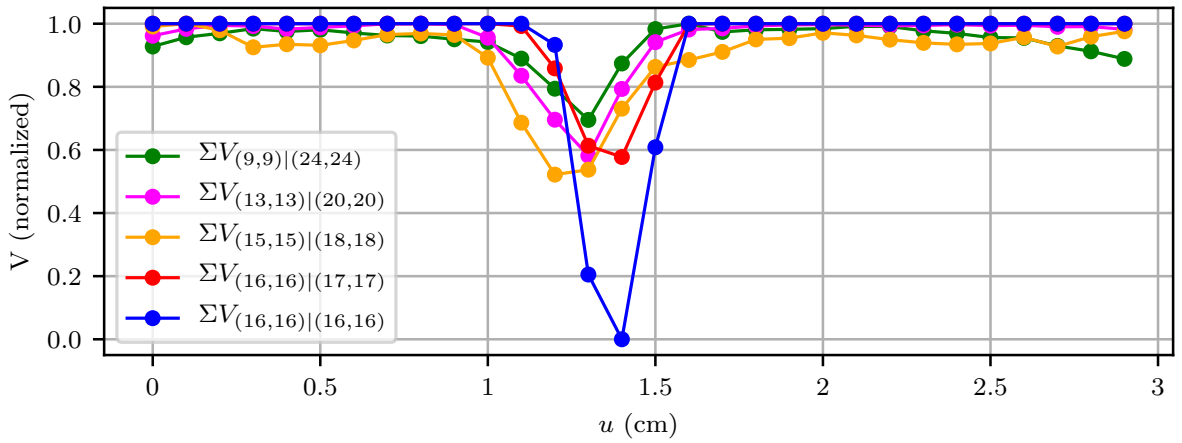


Figure 3.21: Line plots for the cross-sections marked in Fig. 3.20.

3.3.2.2 Statistical structure identification

In this measurement, a toy handgun shown in Fig. 3.22 was used as an imaging target. This target had a much more complex topology consisting of curves and different surface structures. The

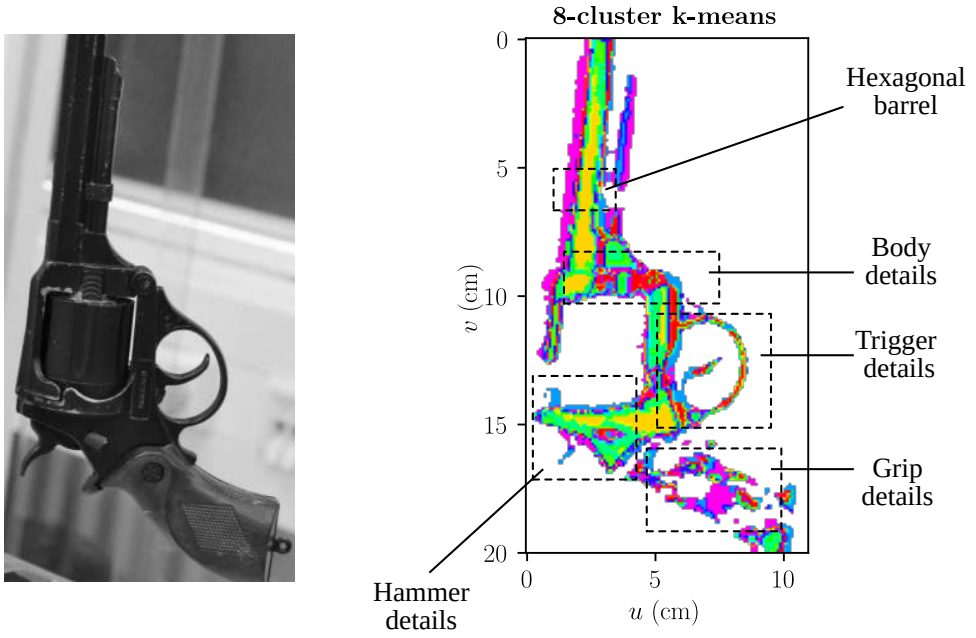


Figure 3.22: (a) A toy handgun used as an imaging target for statistical structure identification, and (b) final processed 8-cluster k-means image from the first four principal components PC1–PC4 (Fig. 3.23(b)). The hexagonal shape of the barrel, as well as the body and trigger structures are identifiable. The plastic cylinder is not visible in the reflection mode image.

goal was to contrast these surface features in the processed images in order to improve the target identification. The imaging was performed by the same setup shown in Fig. 3.17. The overall scanning area was $20\,\mathrm{cm}\times 11\,\mathrm{cm}$, with a step size of $1\,\mathrm{mm}$ and 16-frame averaging at each image point. The net imaging time was around $7\,\mathrm{h}$. After the data acquisition, the background noise was removed using a threshold filter. Due to a complex surface structure of the target, statistical processing was adopted to improve the image contrast. This included the following steps. First, the 32×32 pixel camera image acquired at each scan position was reduced to a certain extracted parameters. Here, four parameters were identified – the sum ΣV of response from all 32×32 pixels, the maxima V_{Max} of each image, and the row and column indices of the maxima pixel, i.e. (p_{Max}, q_{Max}). These parameters, shown in Fig. 3.23(a), refer to different contrast mechanism: ΣV captures the total reflected power at one image point, and V_{Max} indicates the strongest specular reflection with (p_{Max}, q_{Max}) indicating its direction. However, note that all these parameters are not always independent. For example, with reduction in the surface reflectivity, both ΣV and V_{Max} reduce. In order to generate the mutually independent or orthogonal set of parameters, the extracted parameters were applied to standard linear principal component analysis (PCA) method available with the MATLAB Statistics and machine learning toolbox. The resulting four PCA components, PC1–PC4 are shown in Fig. 3.23(b). Different types of contrasts can be noticed across all these PCA component images.

These components were then grouped in accordance with the k-means clustering method, which was also available with the MATLAB Statistics and machine learning toolbox. This

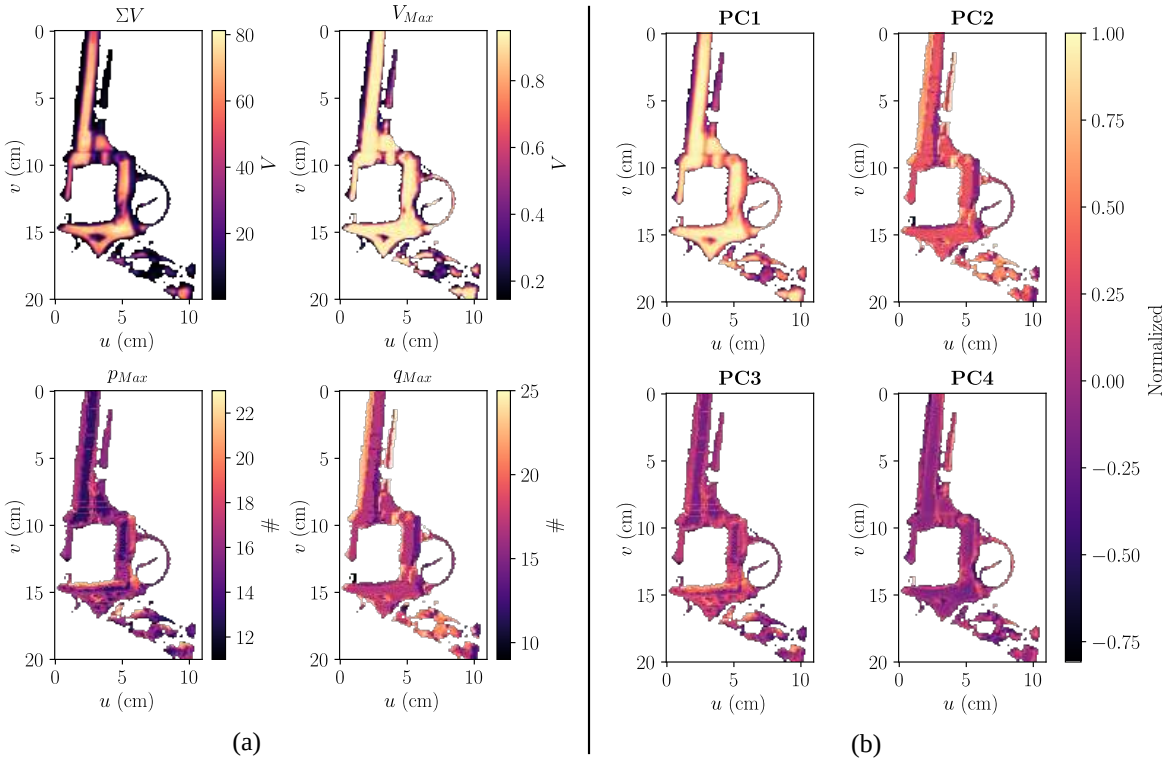


Figure 3.23: (a) Extracted image parameters, and (b) First four principal components PC1–PC4 generated from the extracted image parameters. All datasets have been normalized individually.

statistical technique partitions a set of N-dimensional observation (here N=4 for four principal components) into a number of clusters, by assigning each observation to a cluster with the nearest mean. An 8-cluster k-means image thus computed is shown in Fig. 3.22(b), where the hexagonal barrel, as well as details on body, trigger, grip, and hammer can be distinctly noticed. From manual observation, these details also seem to correlate to the physical structure of the target, although a more detail study is warranted to quantify this correlation.

3.3.2.3 Quantitative feature extraction

In this measurement, a $17.4\,\mathrm{cm}\times12.4\,\mathrm{cm}$ elliptical paraboloid mirror shown in Fig. 3.24(a) was selected as the imaging target. Its analytical surface profile is also shown in Fig. 3.24(b) which was extracted with a coordinate-measurement machine. The objective was to extract these 3D surface curvatures of the mirror along the central axial planes (also marked in Fig. 3.24(b)) from the reflection-mode confocal light-field imaging dataset. The target was scanned in a $20\,\mathrm{cm}\times15\,\mathrm{cm}$ with a step size of $2\,\mathrm{mm}$ and 16-frame averaging, for a total measurement time of around $160\,\mathrm{min}$. Again, the background noise was removed from the raw dataset with a threshold filter.

The pixel sum image ΣV is plotted in Fig. 3.25(a). The specular glint at one side of the image is due to the target geometry. This also highlights how different target surface geometries create target identification issues. The maxima V_{Max} image plotted in Fig. 3.25(b) shows a more

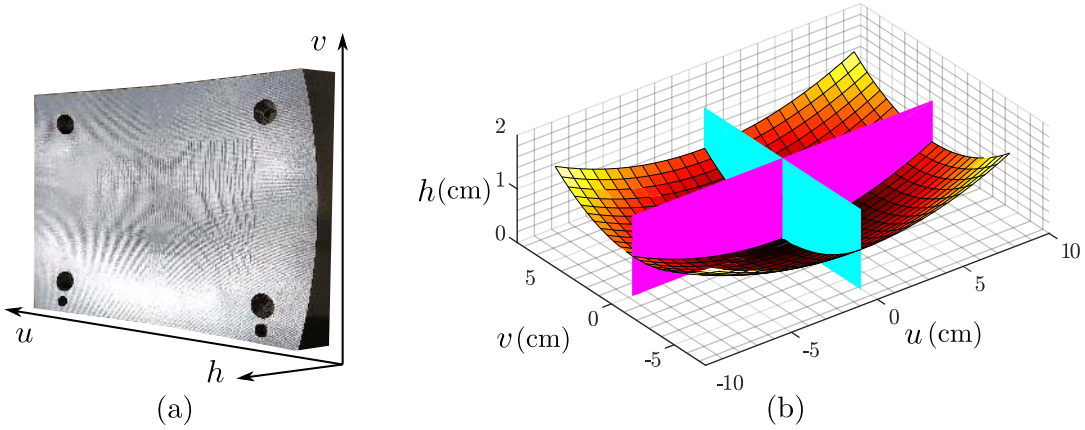


Figure 3.24: ((a) Paraboloid mirror target with reference axes. (b) Centered analytical surface profile $h = 0.9692u^2 + 1.909v^2$ (meters) with marked axial planes. After [159] © 2018 IEEE.

uniform magnitude indicating that the surface of the target has a uniform reflectivity. This is of course true as the mirror is composed of a single metal block. The maxima row index p_{Max} and column index q_{Max} are plotted in Fig. 3.25(c) and Fig. 3.25(d) respectively. These profiles show a gradual variation in the index values, indicating that the direction of reflection progressively changes at the object surface due to its curvature across both latitude and longitude. This change in maxima pixel index can be quantified to extract the actual radius of curvature of the target. Two cross-sections, marked as $p_{Max}(v_0)$ and $q_{Max}(u_0)$ in Fig. 3.25(c) and Fig. 3.25(d) respectively, were selected to extract the curvature profiles along the axial planes. Also note that the profile $q_{Max}(u_0)$ is at an offset from $u = 0$ because of the $45°$ angular orientation of the object with respect to the incident and reflected beam (Fig. 3.17).

The object curvature extraction procedure has been described in extensive detail in [159]. Here, the maxima pixel indices are first mapped to camera incidence angles as per the pixel-to-angle mapping described earlier in Eq. (2.6). These angles are then mapped to the surface-tangent slope of the target with a geometrical ray-mapping [46]. For example, Fig. 3.26(a) shows the row index profile $p_{Max}(v_0)$ mapped to camera reception angle $\theta_c(v_0)$, which is transformed to the surface tangent slope $\theta_0(v_0)$ shown in Fig. 3.26(b) in accordance to $\theta_c = -2\theta_0$ [159]. Also note that due to a finite FoV of the reflection optics, the pixel index profile saturates. Therefore, a linear fit has been employed in Fig. 3.26(b) to predict the variation of surface-tangent slope with the axial dimension u.

The surface curvature radius $r(v_0)$ can thus be calculated from the surface-tangent slope $\theta_0(v_0)$ using standard mathematical relation $r(v_0) = (1 + \theta_0(v_0)^2)^{3/2} \cdot |d\theta_0(v_0)/du|^{-1}$ [166]. The calculated radii for the extracted surface-tangent slopes along both principal axes, and on their respective linear fits, are shown in Fig. 3.27. The root-mean-square errors (RMSE) as compared to the actual analytical profiles are also reported. The extracted slopes show a larger RMSE errors due to the pixel discretization and FoV saturation. However, the radii extracted from the linear-fit are very close to the actual surface curvature.

Therefore, in the three imaging experiments reported above, we have shown different avenues

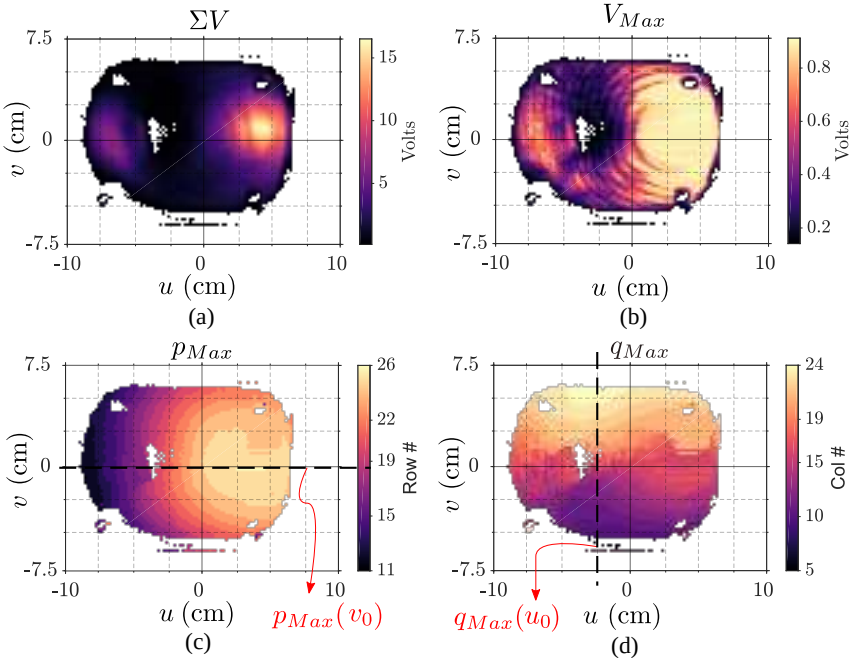


Figure 3.25: (a) Camera sum image ΣV, (b) maxima image V_{Max}, (c) maxima row index q_{Max}, and (d) maxima column index q_{Max}. The index profiles $p_{Max}(v_0)$ and $q_{Max}(u_0)$ marked with dashed lines are used for curvature extraction. After [159] © 2018 IEEE.

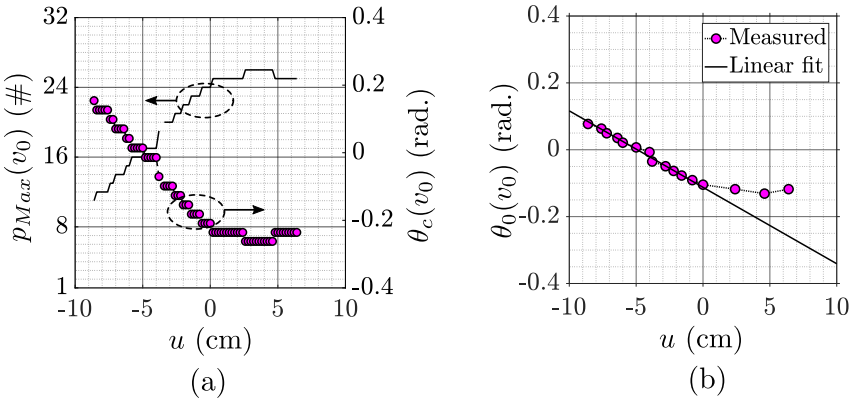


Figure 3.26: (a) Row index profile $p_{Max}(v_0)$ mapped to the camera reception angle in azimuth $\theta_c(v_0)$. (b) Extracted target surface slope $\theta_0(v_0)$, and corresponding linear segment fit, along u-axis for target referred cartesian system (u, v, h). After [159] © 2018 IEEE.

for improving the target identification in reflection mode confocal THz light-field imaging. First, adaptive apertures were utilized to filter out the scattered power. Later, a statistical method was shown for image contrast improvement. At last, actual 3D profile of a curved surface was also extracted quantitatively. All these experiments were done with simple, incoherent hardware, without utilizing any phase information. These experiments serve as a foundational proof-of-concepts for reflection mode THz light-field imaging which may form the basis of more advanced imaging modalities in the future.

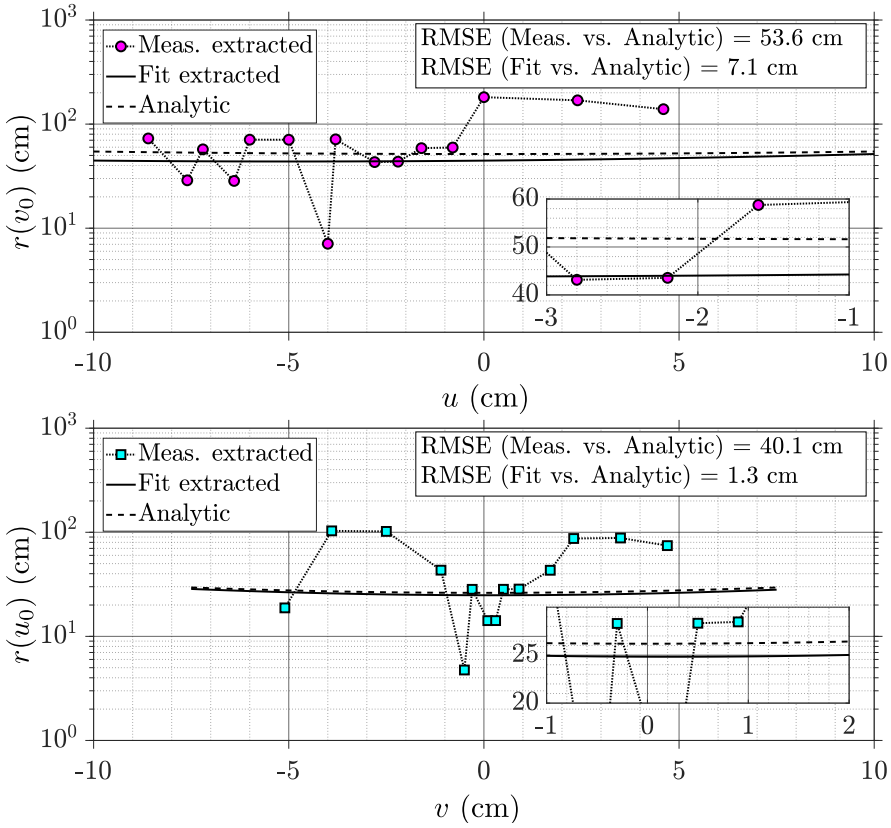


Figure 3.27: Extracted vs. analytically calculated surface curvature radii $r(u_0)$, $r(v_0)$ for the target axial planes (marked in Fig. 3.24(b)) with respective RMSE. Linear scale magnified views are also shown in the insets. After [159] © 2018 IEEE.

3.4 Summary

In this chapter, we have explained the basics of light-field imaging. The differences between the visible-light and THz light-fields, and the key challenges for latter have been outlined. We have also discussed the mathematical and conceptual formulation of light-fields in the form of 4D plenoptic function and rayspace representation respectively, and these ideas have been specifically presented for quasi-optical THz sources and detectors. Scanning based THz light-field imaging experiments based on a 32×32 pixel CMOS THz camera have also been described. In transmission mode, THz light-fields were utilized for radiation pattern characterization of a THz source, as well as lens-less imaging. In the reflection mode, a confocal imaging setup was presented and light-field properties were utilized to solve the crucial problem of target identification by different proof-of-concept experiments, to filter out the scattered power, statistical clustering of image parameters for target recognition, and for extracting the 3D profile of a curved metallic surface. These results are the first ever demonstration of light-field imaging at THz frequencies.

Chapter 4

THz source-array SoC

This chapter discusses the design of a THz source-array SoC for computational THz imaging (CTI). The details have been published in a peer-reviewed conference [167] and a journal [46]. The source was originally designed for single-shot reciprocal imaging with a single-pixel camera (SPC). The design also follows the idea of multi-chip integration already outlined in Sec. 2.3. As discussed in Chapter 7, such source SoC can be used in THz MIMO light-field imaging systems for exponentially increasing the imaging pixel count. Here, the conceptual idea of a single pixel camera is first described and discussed, before embarking on the discussions about the SoC design objectives, details, experimental characterization, and the imaging results.

4.1 Single-pixel THz camera

Conventional THz single-shot imaging is achieved by scaling the pixel count at the sensor FPA. As already discussed in Chapter 2, this comes at the cost of sensitivity as only direct power detectors can be integrated in arrays, and these are at least six orders of magnitude worse in sensitivity as compared to the heterodyne detectors. An SPC is an alternative approach for single-shot THz imaging, where the source illumination is itself divided into multiple pixels, while a single detector is used at the receiving end. An imaging process involves several sequential measurements upon modulating the source pixels. Sparse computation techniques such as compressive sensing (CS) can be used to reduce the number of sequential measurements thus speeding up the imaging process [168]. A highly sensitive single-pixel detector such as a heterodyne detector can be used in an SPC which thus provides an inherent SNR advantage.

The traditional approach for designing THz SPCs has involved a single THz source and some external THz spatial light modulator (SLM) device to permit spatially configurable transmission and attenuation of the THz wave. Modulation speed and modulation depth are the two most relevant metrics for THz SLMs, where a higher modulation speed indicates a faster imaging rate while a larger modulation depth allows a larger SNR. For example, in [169], hundreds of 32×32 pixels masks were mechanically replaced in front of an external fiber-coupled pulsed THz source

for the SPC demonstration. The modulation speed was below $1\,\mathrm{Hz}$ while the modulation depth was $100\,\%$. In [170], an 8×8 pixel THz SLM was constructed with metamaterial arrays composed of n-doped GaAs switches. Here, the modulation speed and modulation depth were $12\,\mathrm{MHz}$ and $10\,\%$ respectively, and an imaging rate of 1 fps was demonstrated. Recently, micro-machined metasurfaces for broadband 0.1–$1.5\,\mathrm{THz}$ power switching with $70\,\%$ modulation depth and $20\,\mathrm{kHz}$ modulation speed [171], and GaAs based metamaterial switches with $36\,\%$ modulation depth and $10\,\mathrm{MHz}$ modulation speed [172] were also reported. Another popular approach for external THz SLMs is spatial plasmonic switching where an optical light pattern is projected onto a semiconductor wafer placed in the THz beam path. The optical pulses change the plasma frequency of the semiconductor material, thus modulating the THz radiation. For example in [173], a $0.35\,\mathrm{THz}$ SPC system was demonstrated which consisted of an off-the-shelf waveguide based THz source, halogen lamp, a commercial 1024×768 pixels digital light projector, and a Germanium wafer as a plasmonic THz switch. The modulation depth and modulation speed were $45\,\%$ and $333\,\mathrm{Hz}$ respectively. An alternative reciprocal imaging system was proposed in [174] where the authors envisaged encoding the illumination pixels into different chopping frequencies, which could be identified and decoded at a single receiver.

The THz source-array SoC presented here unifies the THz signal generation and spatial modulation within a monolithic circuit. The approach is based on incoherent or unlocked source arrays where different pixels can be switched on or off individually. As discussed in Chapter 2, incoherent integration of source pixels also allows a better scaling of power for the single chip and multi-chip systems as compared to the coherent arrays. The SoC also allows chopping frequency division multiplexing (FDM) for reciprocal imaging. In this mode, the radiation from each source pixel can be electronically modulated at a different chopping frequency, which can be identified at the baseband frequency spectrum of the single pixel detector for image formation.

4.1.1 Spatial modulation and compressive sensing

The whole idea of THz SPC based on spatial modulation is illustrated in Fig. 4.1(a). In this case, the assumed generic transmission mode imaging setup constitutes an $n{\times}n$ pixel source-array SoC and a single-pixel direct detector. Any 'switched-on' arrangement of arbitrary source pixels projects a spatial illumination pattern. Here, it can be readily assumed that each source pixel can be turned off entirely, i.e. the radiated output power from each individual pixel can be binary modulated with 100% modulation depth. The spatial pattern, after transmission through an object, is integrated over the detector. Assuming a linear integration of the pixel power at the detector, its output voltage Y can be expressed as the following:

$$Y = R_v P_o \cdot \sum_{k=1}^{n^2} \phi_k \alpha_k \tag{4.1}$$

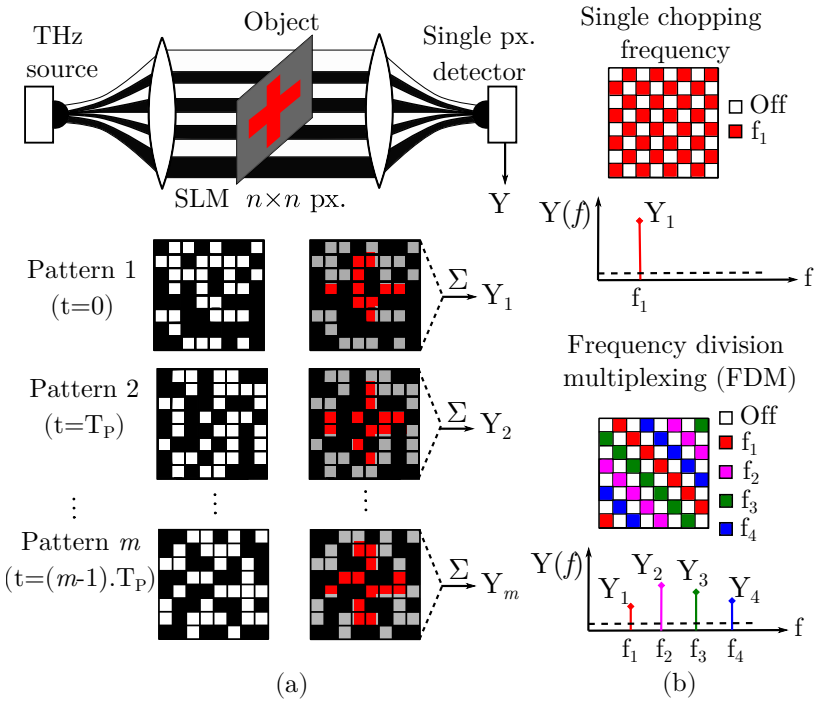


Figure 4.1: (a) Conceptual diagram of a transmission mode THz SPC with a binary SLM source and a direct power detector. Here m sequential measurements are done with the switching period T_P between different spatial patterns. (b) FDM concept. Different pixels can be chopped at different frequencies (color-coded) for their simultaneous acquisition in the detected signal spectrum. From [46] © 2020 IEEE.

Here, k is the index for pixel vector of size $n\times n$, P_o is the radiated power for each pixel (assumed same for all the pixels), $\phi_k \in \{0, 1\}$ is the switching status of k^{th} pixel, and α_k is the fraction of radiation power of the k^{th} pixel that is transmitted through the object cross-section. A power $P_o\phi_k\alpha_k$ reaches the detector, and assuming $100\,\%$ detector efficiency, this power is converted into a baseband signal in proportion to the detector responsivity R_v. The overall response signal Y is composed of a linear algebraic sum of the signals detected from all the source pixels after transmitting through the object. Now, note that a single measurement of Y does not distinguish between the individual pixels, and thus does not form an image. Therefore, spatial illumination restructuring is required. In this case, multiple spatial patterns are projected in a sequence with a switching period T_P, and the corresponding values of signal Y are arranged in a measurement vector. If m number of patterns are projected in a total time of $(m-1)T_P$, the construction of the measurement vector can be denoted as:

$$\begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_m \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} & \cdots & \phi_{1n^2} \\ \phi_{12} & \phi_{22} & \cdots & \phi_{2n^2} \\ \vdots & \vdots & & \vdots \\ \phi_{m1} & \phi_{m2} & \cdots & \phi_{mn^2} \end{bmatrix} \cdot \begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_{n^2} \end{bmatrix} \tag{4.2}$$

or,

$$\boldsymbol{Y}_{m\times 1} = \boldsymbol{\Phi}_{m\times n^2} \cdot \boldsymbol{X}_{n^2\times 1} \tag{4.3}$$

Here $\mathbf{\Phi}$ is the pattern matrix where each row denotes one spatial pattern, and $\boldsymbol{Y}$ is the measurement matrix. The vector $\boldsymbol{X}$ indicates the required transmission mode image, as its entries are proportional to the fraction of power transmitted by the object cross-section, i.e. $X_k = P_o R_v \alpha_k$ when compared to Eq. (4.1). As $\mathbf{\Phi}$ and $\boldsymbol{Y}$ are known, $\boldsymbol{X}$ can be calculated in post-processing as:

$$\boldsymbol{Y}_{m\times 1} \cdot \mathbf{\Phi}^{-1}_{m\times n^2} = \boldsymbol{X}_{n^2\times 1} \tag{4.4}$$

For $\boldsymbol{X}$ to be a unique solution, the pattern matrix $\mathbf{\Phi}$ must have a full rank and non-zero determinant. Thus, $\mathbf{\Phi}$ must have orthogonal rows, and the number of patterns m must be equal to the total number of pixels $n{\times}n$. In the simplest case, only one source pixel can be turned on for each measurement, leading to a time division approach where $\mathbf{\Phi}$ is an identity matrix. $\mathbf{\Phi}$ can also be the Hadamard matrix which is another orthogonal matrix [170]. For this, the entries of $\mathbf{\Phi}$ must belong to $\{-1, 0, 1\}$ which calls for a phase-intensity modulation. When only binary modulation is available, such matrix can be achieved by subtracting two patterns [170]. Also, the SNR for the image signal Y increases with the number of pixels switched on in a pattern. Some numerical simulations of this imaging process have been presented in [175].

Note that the measurement time is directly related to the number of patterns required. As the pattern matrices are mostly sparse, the compressive sensing (CS) technique often accompanies such SPCs to reduce the required number of patterns for faster imaging. Here, a solution to Eq. 4.4 is approximated with error minimization [168]. Interestingly, in the most extreme case, a binary (yes or no) decision about object identification can also be made with a single pattern acting as an optical neural network [176]. Nevertheless, a fast pattern switching and a high radiation power benefit the imaging speed and SNR, respectively. Each source pixel might also produce different power due to PVT variation and undesired mutual coupling, which is further impacted by the optical system aberrations. In this case, an image calibration step is necessary [173]. To further differentiate and calibrate the PVT related source power variability, mutual coupling, and the optical aberrations, a built-in power test (BIST) like scheme becomes invaluable to estimate the power radiated by each source pixel directly on the chip.

4.1.2 Chopping frequency division multiplexing

The spatial modulation and compressive sensing described above can be considered analogous to code-division multiple access approach prevalent in communication systems. As multiple users share the same medium in multiple access communication, multiple image pixels also share the same receiver in an SPC. Another approach can be a frequency-division multiple access, which can be done by chopping frequency-division multiplexing (FDM). This idea is illustrated in Fig. 4.1(b), where four mutually exclusive patterns are modulated at four different, non-overlapping chopping frequencies, and their responses are read out simultaneously from the baseband frequency spectrum $Y(f)$ of the detector. The chopping frequencies must be orthogonal to avoid mutual interference. For example, in the case of a square-wave chopping, the non-overlapping chopping frequencies can be assigned within the spectra between the first

and the third harmonics of the lowest chopping frequency.

Chopping FDM can be useful for optimizing the imaging speed and SNR in several cases. A chopping frequency larger than the noise corner of the detector can mitigate its large flicker noise. Any decision to use chopping FDM over SLM is also based on the readout front-end of the detector. For example, many modern digital signal processors (DSPs) have fast sampling ADCs storing data in a buffer, along with slower data transfer interfaces. In such cases, it makes more sense to sample and build the spectrum on the DSP and to transfer only the relevant Fourier coefficients for image formation. Specially for large pixel count SPCs, the number of measurements can be directly reduced in proportion to the number of frequency tones applied for the chopping FDM. Note that a large number of FDM tones can also degrade the imaging speed due the required frequency resolution. Also, fewer 'on' pixels in a chopping tone encoded pattern lead to a lower SNR at the detector.

While the imaging process in Fig. 4.1 is illustrated with a direct detector, both the SLM and FDM techniques would also work with a heterodyne receiver. Since each of the unlocked source pixels radiates at slightly different frequencies and random phases, the IF signal at the heterodyne detector must have sufficient bandwidth to pass the down-converted components with a fixed LO drive, and integration of this IF signal over this bandwidth results in the signal Y. Since the IF detector noise increases in proportion to the integration bandwidth, a narrower frequency distribution of the source pixels leads to a higher imaging SNR. Nevertheless, silicon heterodyne detectors have a much higher sensitivity than silicon direct detectors, and even more sensitive heterodyne receivers can be constructed in III-V processes as only a single receiver pixel is required [177]. For chopping FDM, the LO frequency can be modulated at different rates for the lock-in acquisition of different modulation components.

4.2 Design objectives

The THz source-array SoC to be presented soon targets CTI in SPC configurations. Multi-chip scaling is also a required feature to increase the source pixel count. In this regard, the following design objectives can be derived from the previous discussions:

1. **Compact layout of the source SoC** while integrating numerous pixels (smaller pixel area), with a low dc power consumption and a high THz radiation power, i.e. a high dc-to-RF conversion efficiency. This calls for the selection of an appropriate process technology and oscillator topology.
2. **Diverse pattern reconfiguration** including SLM and chopping FDM, both programmable through a simple digital interface. A fast switching between different pattern configurations is also necessary. At each pattern configuration, the SoC should also be able to trigger the data acquisition at the detector.
3. **High pattern fidelity** which requires low mutual pixel coupling, along with some in-pixel BIST for in-situ calibration and monitoring of the radiated power.

4. **Multi-chip scaling** which requires low-complexity packaging with serial, sharable data interface and common dc bias lines.

The source-array SoC architecture that was aimed to meet the above broad objectives, as well as the circuit design and operation details, are discussed in the next section.

4.3 SoC design

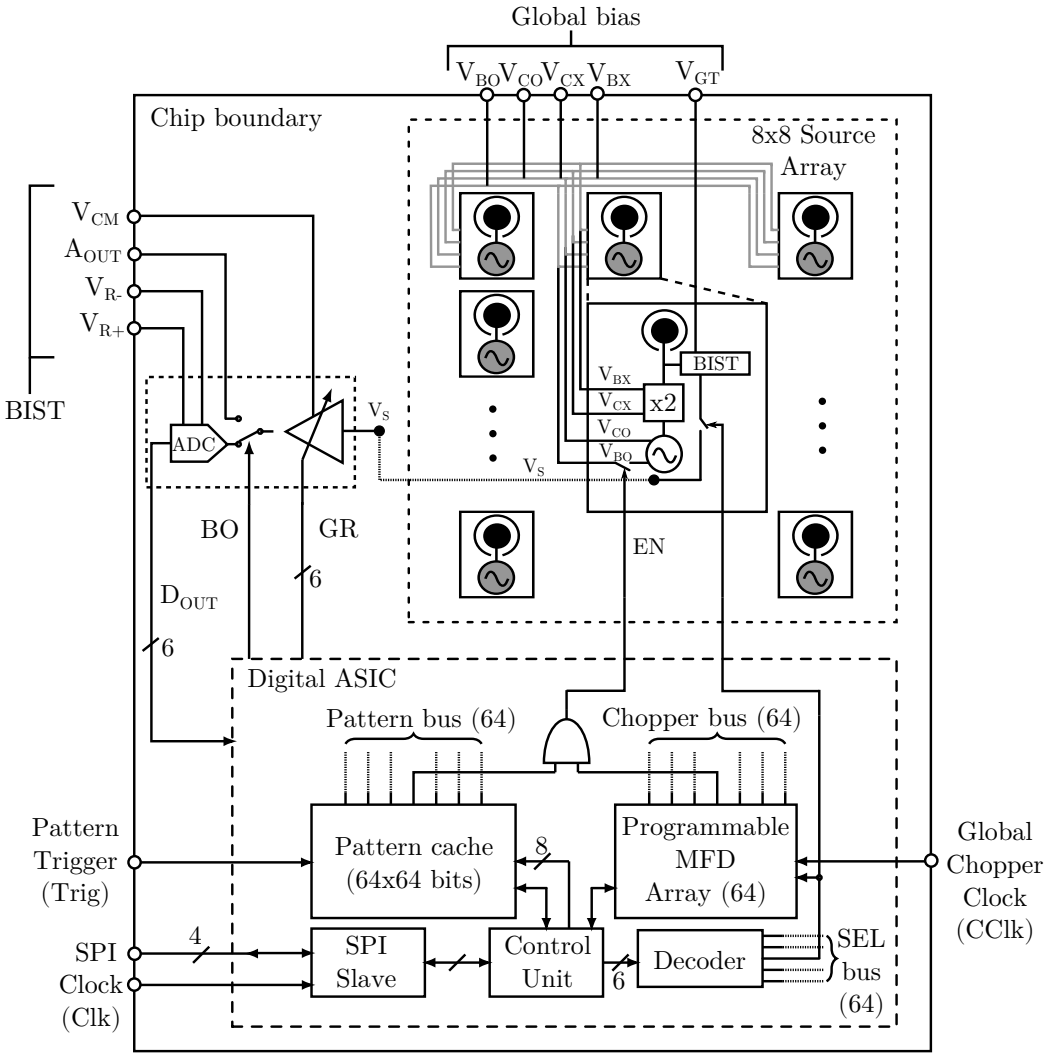


Figure 4.2: Block diagram of the 8×8 pixel THz source SoC with global biasing, BIST monitoring, and SPI interface. External trigger (Trig) is used for projecting the next cached pattern from the memory, and global clock (CClk) with 64 elements MFD array performs the FDM. From [46] © 2020 IEEE.

A block diagram of the source-array SoC is shown in Fig. 4.2. The SoC was implemented in $0.13\,\mu m$ SG13G2 SiGe:C BiCMOS process from IHP Microelectronics GmbH. It consists of 8×8 array of unlocked or free-running source pixels, each constituting a free-running fundamental oscillator with differential Colpitts topology, a differential to single-ended common-collector frequency doubler, and a circular slot antenna. The antenna is intended to be attached to a silicon lens, which allows for pixel area minimization. Also, a BIST is incorporated into the

antenna feed line at each pixel. The circuit design details of the pixel are presented later. Each pixel has five main analog biases, including biases V_{CO} (3.6–4.2 V) and V_{BO} (1.0–1.4 V) for the fundamental oscillator, biases V_{CX} (1.6–1.8 V) and V_{BX} (0.5–0.6 V) for the frequency doubler, and bias V_{GT} (0.6–1.2 V) for the BIST. These biases are globally shared by all the pixels, and they are supplied externally. The BIST output is multiplexed to a shared readout consisting of a programmable gain amplifier (PGA) with 6-bit gain register 'GR' and externally supplied common-mode voltage V_{CM} (0.3–0.9 V). With an internal flag 'BO', the output of this PGA can either be multiplexed to an external signal pad A_{OUT}, or to an integrated 6-bit flash ADC (FADC), with externally supplied range-voltages V_{R+} and V_{R-} (0.3–1.2 V). The digital output D_{OUT} of the ADC is sent to an integrated ASIC to be read out via an SPI operating at a clock signal 'Clk'. The whole BIST circuitry and digital logic operate at the technology VDD of 1.2 V.

The pixel is switched on or off with a flag 'EN' which switches the V_{BO} supply node at each fundamental oscillator individually. The 64-bit wide bus composing these switching signals is supplied via the ASIC. The ASIC can store 64 switching patterns, each with 64-bit size, into a pattern cache memory, and the preloaded patterns can be projected via a pattern trigger signal 'Trig'. Along with this, the ASIC also includes an array of 64 modulo-frequency dividers (MFD) to generate an individually programmable chopping signal for each pixel derived from a global chopper clock 'CClk'. Last but not the least, the ASIC also integrates decoder logic to select the pixel whose BIST output is multiplexed to the shared readout.

4.3.1 ASIC architecture

In order to further explain the pattern reconfiguration capability of the source-array SoC, the ASIC architecture is illustrated by a programming model shown in Fig. 4.3. The pattern cache has been designed as a circular first-in first-out (FIFO) queue of 64-bit registers PR0–PR63. Since the SPI transfers one byte of data in ten cycles of the 'Clk' signal, loading a pattern register requires eight SPI byte transfers. This results in a large latency for an interactive operation, where a pattern is immediately sent to the pixel array after programming it into the memory. The pattern cache allows a faster operation with a batch-mode upload, where all the pattern registers can be first loaded with required configurations. These can then be sent to the pixel array in a rapid sequence with an external 'Trig' signal that also increments the FIFO read pointer (Ptr.). After reading the register PR63, the read pointer resets to register PR0 and the process continues. Therefore, once the pattern cache is full, the SoC can be operated in a free-running mode by supplying fast trigger pulses to change the projected patterns.

Delving deeper, we see that the pattern register read by the 'Trig' signal is uploaded to a 64-bit selected pattern (SP) register parallelly feeding a pattern bus. The MFD array is another crucial part of the ASIC which creates programmable chopping signals for all the pixels. Each MFD block, from MFD0–MFD643, is identical and contains a fractional frequency divider based on modulo-arithmetic. To summarize its operation, the global chopping clock 'CClk' is divided in frequency by a factor $K_i = 2(2^8\text{-}M_i)/N_i$ at each MFD, where M_i and N_i are 8-bit local registers.

This allows programming of any frequency division ratio in range of 2 – 512 at each pixel. The output duty cycle is exactly $50\,\%$ for an even division ratio and close to $50\,\%$ for an odd division ratio. Fractional division ratios result in varying duty cycles and thus these are not recommended. The MFDs can also be programmed over SPI, and the whole MFD array can be enabled or disabled using an 'Enable divider' (ED) flag. A 64-bit wide chopper bus is derived from the MFD array, which is bitwise-ANDed with the pattern bus to generate the pixel switching bus 'EN'. This whole logic together provides a very flexible and high speed pattern reconfiguration for the source-array SoC, which proved crucial for CTI system implementations as discussed later.

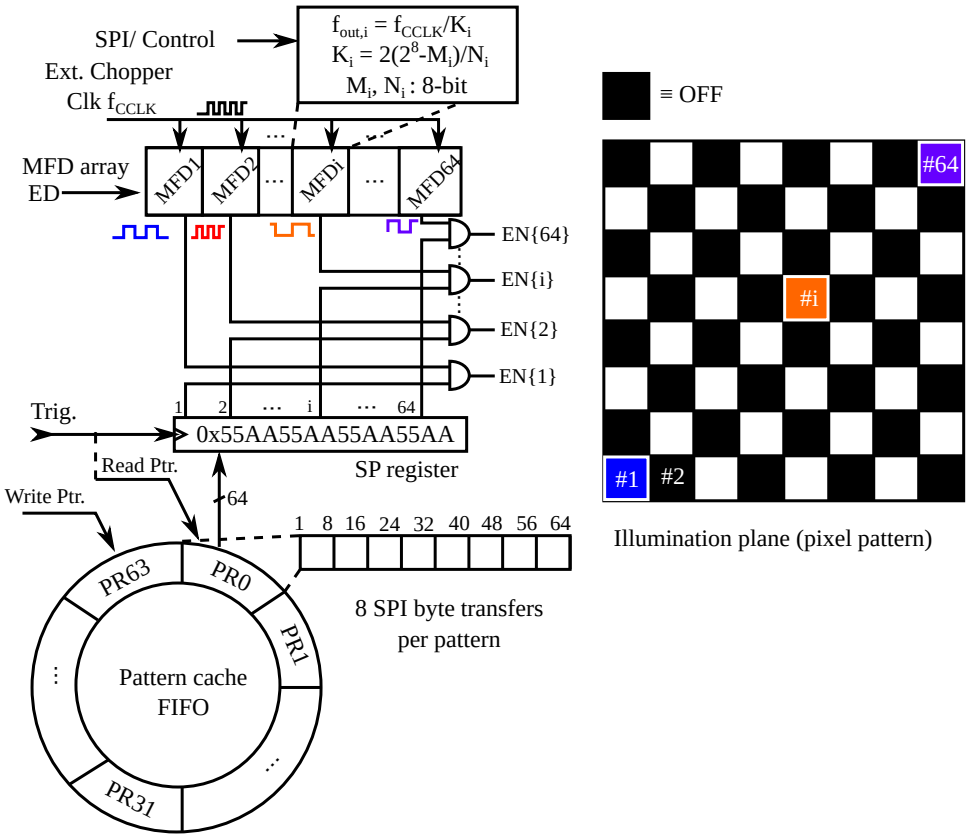


Figure 4.3: Digital programming model for the SoC. The 64-pattern cache memory is configured as a circular FIFO. The working pattern is triggered into the 64-bit SP register, which is bitwise-ANDed to a reconfigurable 64-element MFD array, thus providing different chopping frequencies for each pixel. After [46] © 2020 IEEE.

4.3.2 Pixel and BIST circuit design

Fig. 4.4(a) shows the circuit schematic of one source pixel, which is based on the $0.43\,\mathrm{THz}$ single pixel source that was presented in [80]. In the SoC implementation, the layout of transmission lines has been modified to fit the pixel into a compact area for a close-to-square aspect ratio. The pixel switching logic and BIST power detection has also been added. The THz signal is generated by a fundamental differential Colpitts oscillator composed of HBTs Q_1 and Q_2. The process technology provides HBTs with fixed emitter area of $0.12 \times 0.96\,\mu\mathrm{m}^2$ [63] and a transistor size is

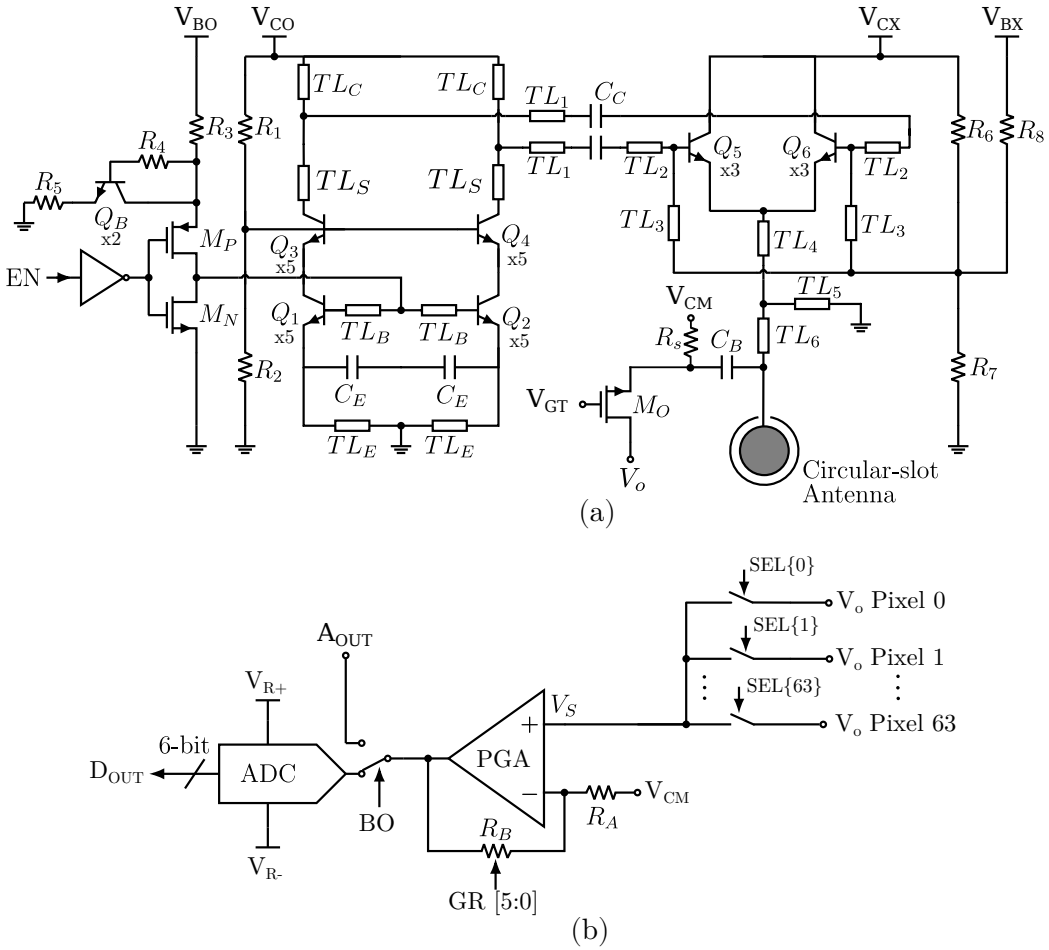


Figure 4.4: (a) Source pixel schematic with a differential Colpitts oscillator, common-collector doubler, switching circuitry, on-chip circular slot antenna, and integrated power detector for BIST; (b) shared BIST readout with the PGA and the ADC. From [46] © 2020 IEEE.

modified by lining a number of HBT devices in parallel. Fig. 4.4(a) thus indicates the number of emitter fingers used for each transistor. Transistors Q_3 and Q_4 form a cascode stage which isolates the oscillator output from its input. Microstrip transmission lines TL_S, TL_C, $TL_{1,2}$, and TL_3, along with AC coupling MIM capacitor C_C forms the interstage matching network between the oscillator and the balanced common-collector doubler composed of transistors Q_5 and Q_6. The doubler is designed to provide a reactive feedback of the second harmonic at the base-emitter junction to boost the second harmonic current [80]. Note that this design also ensures a minimal fundamental leakage by using a differential topology and providing an isolating doubler stage between the antenna and the oscillator, thus impeding any mutual RF cross-coupling between the pixels. The circular slot antenna, implemented in the TM1 layer of the process, has the circular center patch and radiating slot diameters of $106\,\mu\mathrm{m}$ and $152\,\mu\mathrm{m}$, respectively. Transmission lines TL_4 and TL_6 transform the capacitive impedance of the antenna to an optimum second-harmonic termination for the doubler emitter output. The antenna supports linear polarization, and the impedance values are similar to the ones that are reported in the original design from [80]. The biasing is handled by resistive voltage dividers

composed of polysilicon resistors R_1 – R_8. Each source pixel consumes 365×250 µm^2 of die area excluding the dc bias mesh. At the ambient temperature (27 °C), the simulated radiation frequency and power for the pixel over biases V_{BO} and V_{CO} are shown in Fig. 4.5. A maximum radiated power of $-1.66\,\mathrm{dBm}$ was simulated at a radiation frequency of $439\,\mathrm{GHz}$ for V_{BO} and V_{CO} of $1.05\,\mathrm{V}$ and $4.4\,\mathrm{V}$ respectively. In these simulations, biases V_{CX} and V_{BX} were kept fixed at $1.7\,\mathrm{V}$ and $0.45\,\mathrm{V}$ respectively. The simulation results in Fig. 4.6 also show thermal throttling of the pixel. These results, simulated for the maximum power bias, show more than $10\,\mathrm{dB}$ of output power roll-off, and about $10\,\mathrm{GHz}$ reduction in the radiation frequency, when the pixel ambient temperature changes from room-temperature to $80\,°\mathrm{C}$. These results become significant when multiple pixels are turned on simultaneously in the array, as shown in the measurements later.

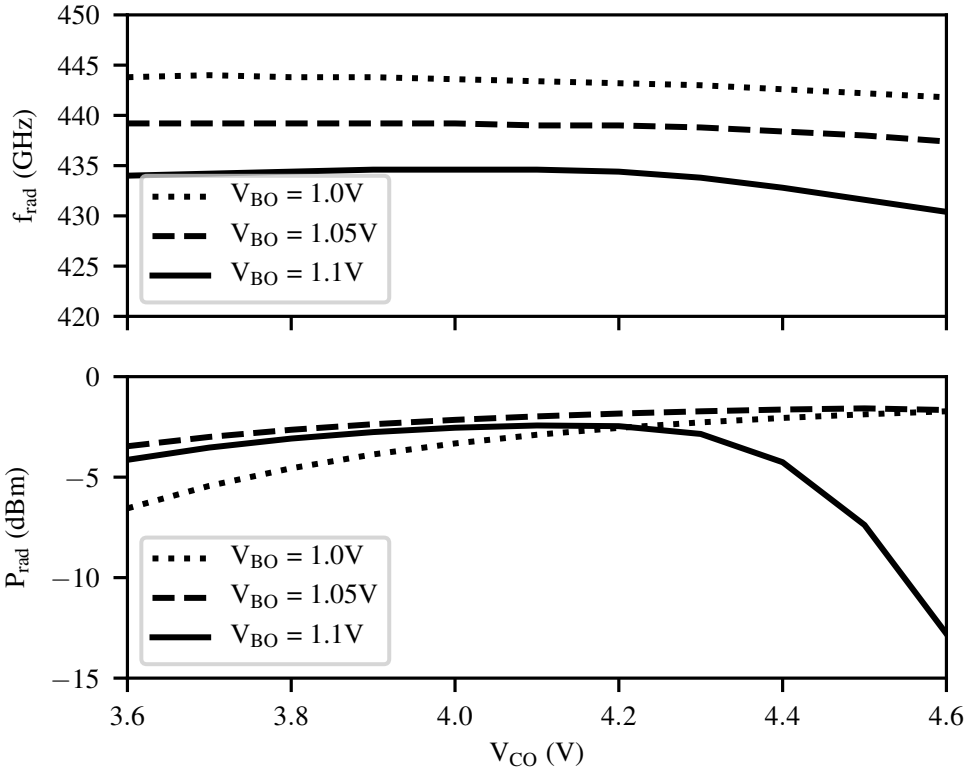


Figure 4.5: Simulation results for the radiated frequency f_{rad} and radiated power P_{rad} for a source pixel with varying V_{CO} and V_{BO}. Biases V_{CX} and V_{BX} were kept fixed at $1.7\,\mathrm{V}$ and $0.45\,\mathrm{V}$ respectively.

A pixel is switched on or off by changing the base bias of transistors Q_1 and Q_2 responsible for oscillation. The oscillator bias is supplied through a diode connected transistor Q_B which also provides a low impedance node to sink any instantaneous charge carriers during switching. The switch, composed of a CMOS pair with transistors M_P and M_N, sets the oscillator bias to zero (ground) when flag 'EN' is set to 0, effectively turning off the oscillator and thus the pixel. The switching speed is limited by the time constant of this network. Fig. 4.7 shows a time domain simulation showing the delay between pixel switching and actual beginning and quenching of oscillations. Greater delay is observed while switching on the oscillator, where the voltage

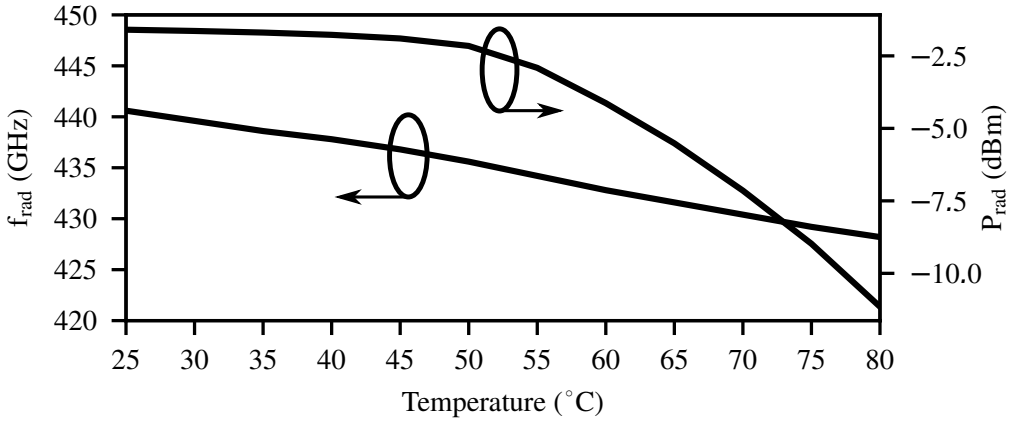


Figure 4.6: Simulated thermal throttling of the oscillator pixel for the maximum power biasing.

signal at the base reaches $99\,\%$ of its final amplitude in $6\,\mathrm{ns}$ after setting the 'EN' flag.

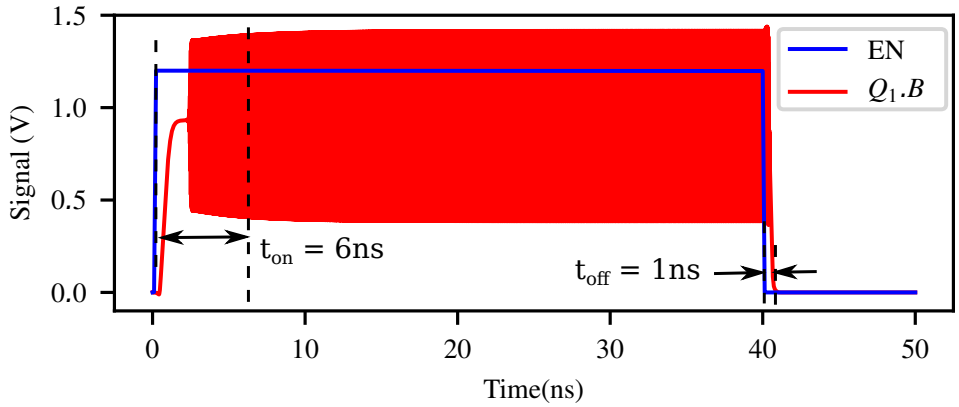


Figure 4.7: Time domain simulation of the oscillator pixel showing the application of switching signal EN and the onset of oscillations at base node of transistor Q_1, i.e. $Q_1.B$.

The in-pixel BIST circuit is implemented with a 1µm /0.13µm NMOS transistor M_O in a common-gate configuration [109] with a coupling capacitor C_B. This capacitance of around $1.3\,\mathrm{fF}$ manifests in form of a 32 μm^2 MOM stack between the antenna feed-line at layer TM1 and the layer M5. The simulated power coupling was around $-15.1\,\mathrm{dB}$ at $400\,\mathrm{GHz}$. For best sensitivity, transistor M_O must be biased at a gate-source voltage of around $0.3\,\mathrm{V}$ with around zero drain-source voltage. For this, the source terminal of M_O is biased at with voltage V_{CM} in the common-mode range of the readout PGA, and the biasing resistor R_S acts as an RF choke. For V_{CM} of $0.6\,\mathrm{V}$, the gate voltage V_{GT} for M_O should be around $0.9\,\mathrm{V}$.

The shared readout scheme for the BIST is further shown in Fig. 4.4(b). The BIST pixel is selected by a 'SEL' switch from the ASIC decoder, which is fed to the PGA with 6-bit programmable voltage gain of 3–29 dB (GBW ≈ 1.25 MHz, simulated). The 6-bit FADC shows a measured effective number of bits of 5.85 and a maximum sampling rate of $7.3\,\mathrm{MHz}$ [178].

4.3.3 Mutual pixel coupling

This is a key concern while designing an unlocked source array for SPC applications. For different spatial patterns to be entirely independent of each other, it is highly desired that each pixel should also operate independently, i.e. there should be no form of coupling between any two pixels of the source-array.

Mutual pixel coupling can arise from three different causes. First is the RF coupling, which can arise when the RF signal from one pixel leaks to another pixel, changing its effective oscillation frequency and radiated power. Also, RF coupling is likely to injection lock two or more pixels at the same oscillation frequency. This coupling can originate from the parasitic EM fields between two nearby antennas, or because of the substrate modes resulting from the substrate reflections.

In the source array, grounding shields have been placed around the pixels to prevent the EM field leakage. The ground shield and the antenna were designed together using full-wave simulations. The other issue is mitigated by using the hyperhemispherical silicon lens at the backside of the chip. This lens acts as a semi-infinite substrate and prevents the formation of substrate modes [112]. In [100], it was found that the coupling between shielded antennas in an array atop a silicon lens is in the order of -25 to $-30\,\mathrm{dB}$. In the source-array, further isolation is provided by the pixel architecture, i.e. the frequency doubler after the oscillator prevents any out-coupling / in-coupling of the fundamental oscillator signal. Fig. 4.18 in Sec. 4.5.2 presents an experiment to show that the neighboring pixels in the source-array have negligible RF coupling.

Another mechanism of mutual pixel coupling can be the transient charge generated during pixel switching, which can leak to the neighboring pixels. This is handled with a low-impedance switch composed of transistors M_P and M_N inside each pixel (Fig. 4.4). Moreover, this coupling is also expected to be transient in nature, and any adverse impacts can be avoided by introducing the required time delay between pixel switching and image signal measurement.

The most severe case of coupling originates from the dc wiring in the array. Each source pixel can consume up to $20\,\mathrm{mA}$ of dc current. Since all the pixels are routed to a common bias, the path taken by dc current changes based on the location and number of pixels that are switched on, resulting into different voltage drops due to a finite wiring resistance. Therefore, each pixel receives a slightly different bias which changes with the applied pattern.

The dc coupling is minimized by using thick wires with a mesh based dc routing. In the source-array, dc lines are routed in the thickest top metal layer with a sheet resistance of around $11\,\mathrm{m\Omega}$. The mesh routing is also important for current distribution. In fact, the first design of source array had a bus routing for V_{BO} bias which resulted in huge pixel coupling and reduced performance [167], and the dc routing had to be changed to a mesh by modifying the TM1–TM2 layers of the design [46]. Some extent of dc coupling is still expected to remain in the array due to the shared dc biases. In these cases, the in-pixel BIST becomes indispensable. Any relative change in the radiated power of a pixel can be monitored using the BIST and can be calibrated during post-processing of the image data.

4.4 Chip micrograph and Packaging

The chip micrograph for the source-array SoC is shown in Fig. 4.8, along with a zoom-in view of one of the source pixels. The overall die area is $12\,\mathrm{mm}^2$, including $2.1\,\mathrm{mm}^2$ area for the ASIC. The chip thickness is $150\,\mu\mathrm{m}$.

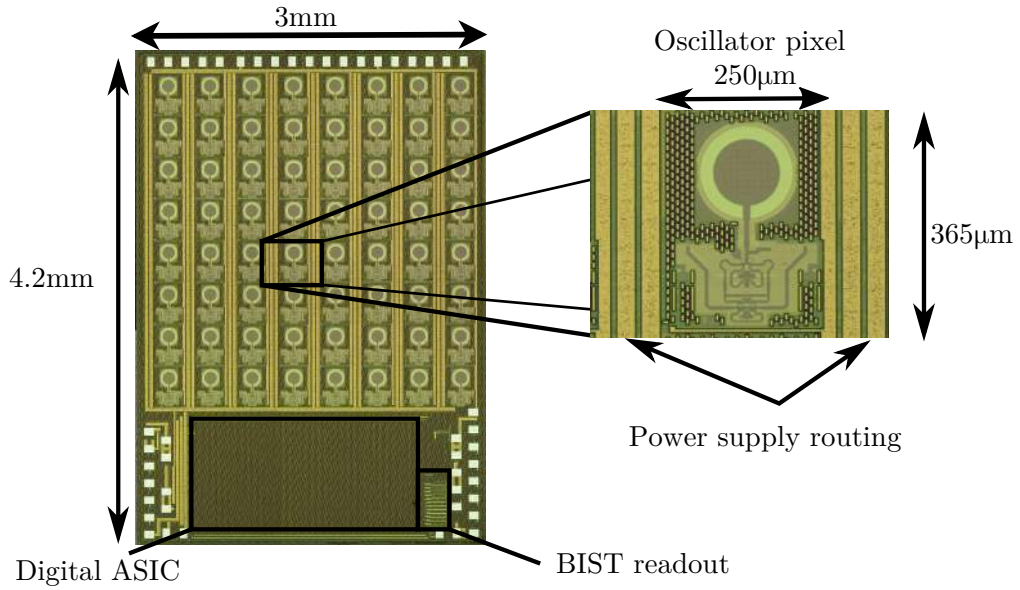


Figure 4.8: Die micrograph for the source SoC with a zoom-in view of the source pixel. From [46] © 2020 IEEE.

The packaged source module is shown in Fig. 4.9(a). Here, the SoC is glued from the backside to a $15\,\mathrm{mm}$ silicon lens with an elliptical extension. To assist with the heat dissipation, a passive copper heat sink is also attached to the lens with a thermal epoxy. The hardware block diagram implementing the whole control scheme is shown in Fig. 4.9(b). The control board has an FTDI 232R based USB-to-serial interface IC. The UART and SPI interfaces, as well as global chopper clock 'CClk' generator, are implemented on an FPGA (Xilinx spartan-6) driven by a $100\,\mathrm{MHz}$ crystal oscillator (XTAL), which supplies the required digital control and clocking signals to the SoC. The signals 'Trig' and 'CClk' can also be provided externally by configuring the solder jumpers J1 and J2 at the control board. The bias signals are provided through a separate board, and back-to-back connectors are used to connect all the PCBs. Overall, the packaged module has a volume of 5.8×5.8×5 cm^3. It is particularly noteworthy that all the PCBs are implemented with low-cost FR-4 material, and the source module doesn't need any external RF signal or component. At the PC, a programming interface is provided through a Python class. The steps to operate the source module include connecting the dc supplies, connecting the USB cable to the PC, and writing a Python code to perform the desired functions.

The source-array SoC with a silicon lens also follows the pixel-to-angle mapping that has already been described in Section 2.2.3. From the ideal model, the $15\,\mathrm{mm}$ lens aperture with a $2.83\,\mathrm{mm}$ elliptical lens extension leads to a central beam directivity of $36.4\,\mathrm{dBi}$ (HPBW $\sim 2.72°$)

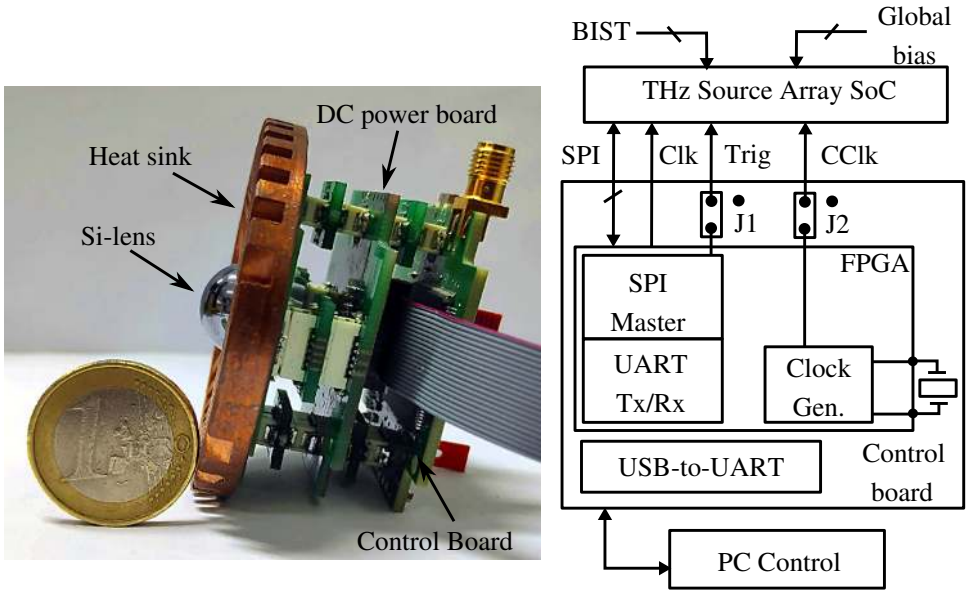


Figure 4.9: (a) Packaged source module with a 15 mm silicon lens of elliptic extension and a passive copper heat sink. A 1-euro coin is shown for scale. (b) Block diagram for the control scheme used to operate the module from a PC. From [46] © 2020 IEEE.

at $0.42\,\mathrm{THz}$. The calculated total fan-out angle or the FoV is $68°$ with approximately $7.6°$ beam separation angle.

4.5 Performance characterization

The most important performance metrics for the source-array relate to its radiated power and frequency, as well as the dc power consumption and the dc-to-RF conversion efficiency. For the SPC applications, additional parameters such as the modulation speed, pixel-to-pixel variability, and radiation pattern profiles, also become important. In this section, these characterization results are discussed in detail along with the experimental procedure.

Different experiment setups that were used for the free-space characterization are illustrated in Fig. 4.10. The power measurements were conducted with either a waveguide horn antenna coupled PM4 Erikson calorimeter from Virginia Diodes Inc. (Fig. 4.10(a)) or with a photo-acoustic absolute THz power meter from TK instruments (Fig. 4.10(b)). When comparing these two instruments, the PM4 meter shows a better sensitivity ($-30\,\mathrm{dBm}$ versus $-23\,\mathrm{dBm}$ for TK), and a high isolation to any lower frequency or fundamental leakage below WR-2.2 (330–500 GHz) band because of the sharp waveguide cutoff. The PM4 however is sensitive to higher frequency background thermal radiation which requires periodic compensation. The TK power meter, on the other hand, is sensitive to all the signals with frequencies below $3\,\mathrm{THz}$, and a chopping-mode measurement is necessary for rejecting any background noise. Even more significant difference arises in the power capturing apertures of the two meters. The PM4 has a narrow aperture due to the horn antenna, and it can only couple to a single source pixel. The TK meter has

a large $3{\times}5\,\mathrm{cm}^2$ aperture which can collect the radiated power from multiple source pixels simultaneously. In both cases, near-field measurements are necessary due to the limited sensitivity of the power meters and a large far-field distance ($63\,\mathrm{cm}$ at $0.42\,\mathrm{THz}$ for $15\,\mathrm{mm}$ lens aperture) of the source module.

The setup to characterize the radiation frequency is shown in Fig. 4.10(c) where a ×18 harmonic mixer HM500, from RPG-Radiometer Physics GmbH, down converts the RF signal from the source to an IF signal based on the supplied LO frequency. This mixer has a large IF bandwidth of around $3\,\mathrm{GHz}$ which makes it easier to observe the RF frequency even in the case of thermal drifts and pixel-to-pixel frequency variation. This mixer couples to a waveguide antenna and shows a rather high $50\,\mathrm{dB}$ conversion loss. Therefore, near-field measurements become necessary, and only one pixel can be measured within one alignment. More sensitive vector network analyzer extender (VNAX) modules were also available in the laboratory. However, since these modules are primarily intended for small-signal S-parameter characterization, they feature a narrow IF bandwidth ($< 1\,\mathrm{GHz}$) and a low saturation power (related to a low conversion loss). Some of these modules were used for qualitative analysis of the fundamental leakage, phase noise, and parasitic RF coupling between pixels, as specified later.

The far-field relative power measurements were conducted with a SiGe HBT based direct THz power detector that was also developed at IHCT [104]. Fig. 4.10(d) shows this setup. The detector is broadband, and it has a sensitivity of approximately $-80\,\mathrm{dBm}/\sqrt{\mathrm{Hz}}$ or $8\,\mathrm{pW}/\sqrt{\mathrm{Hz}}$ at around $0.43\,\mathrm{THz}$. In this case, the source module was mounted on a robotic arm to rotate it in 3D while acquiring the radiation patterns.

4.5.1 Single pixel characterization

The measured radiation power and frequency over the bias V_{CO}, for a single arbitrary source pixel at the center of the array, are plotted in Fig. 4.11. In these measurements, all the other pixels were kept switched off. Owing to the IR drop over the metal lines, the bias V_{BO} was around $1.2\,\mathrm{V}$ in comparison to the simulated optimum value of $1.05\,\mathrm{V}$ in Fig. 4.5, while biases V_{CX} and V_{BX} were set at $1.7\,\mathrm{V}$ and $0.45\,\mathrm{V}$ respectively. The peak power was measured at V_{CO} of $4.4\,\mathrm{V}$, with PM4 and TK reported values of $476.2\,\mu\mathrm{W}$ and $472\,\mu\mathrm{W}$ respectively. A close agreement between these values also points to a negligible fundamental leakage. The PM4 and TK values differ at lower bias voltages. The reason for this deviation is not entirely clear, and it is suspected to originate from the standing wave and reflections in the near-field setup. Also note that because of a resistive biasing, the source module consumes a static dc power of $0.8\,\mathrm{W}$ when all the voltages are applied yet no pixel is switched on. Each pixel consumes about $100\,\mathrm{mW}$ of power in the active state while sinking around $20\,\mathrm{mA}$ of current from V_{CO}. The measured RF frequency was in the range of 418–$421\,\mathrm{GHz}$. The maximum measured BIST responsivity was $115\,\mathrm{V\,W^{-1}}$ with respect to the peak radiated power. The measured radiation pattern showed a Gaussian beam with $34.7\,\mathrm{dBi}$ directivity and $-14\,\mathrm{dB}$ side lobes [46].

In order to check the variation in radiation frequency and power across different pixel switching

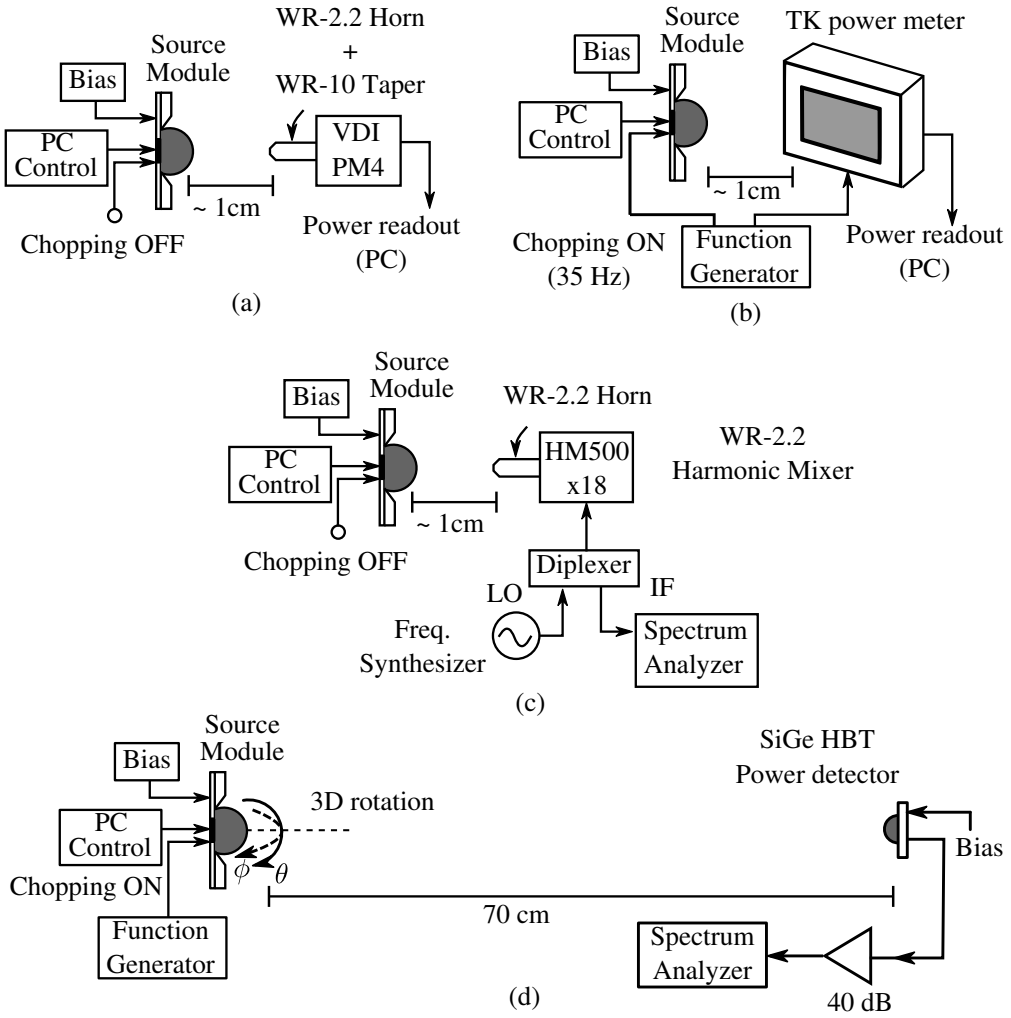


Figure 4.10: Different free-space characterization setups used in this work. (a) Power measurements in the near-field with an Erickson calorimeter (PM4); (b) Power measurements in the near-field with a photo-acoustic absolute THz power meter (TK); (c) Frequency measurements with a ×18 harmonic mixer (HM500); (d) Antenna pattern characterization in far-field with a SiGe power detector. From [46] © 2020 IEEE.

events, the pixel was switched on and off a hundred times in front of the HM500 harmonic mixer. The time series of the measured radiation frequency and IF power at the mixer are plotted in Fig. 4.12. The output frequency varies by $200\,\mathrm{MHz}$, while the output radiated power variation is under $1.5\,\mathrm{dB}$. This indicates that this source-array does not suffer from the switching power instabilities.

The modulation speed of this pixel was characterized using the far-field setup shown in Fig. 4.10(d). The source pixel was chopped with an external function generator which was bandwidth limited to $30\,\mathrm{MHz}$. The minimum division ratio for MFDs is 2, so the radiation could be chopped only up to $15\,\mathrm{MHz}$. The SiGe HBT detector output was connected to a $200\,\mathrm{MHz}$ bandwidth amplifier with a short SMA cable to minimize the baseband signal attenuation. The power detector output versus radiation chopping frequency is plotted in Fig. 4.13, showing a $3\,\mathrm{dB}$ roll-off at $10\,\mathrm{MHz}$. Conservatively, this is considered as the modulation speed limit for the

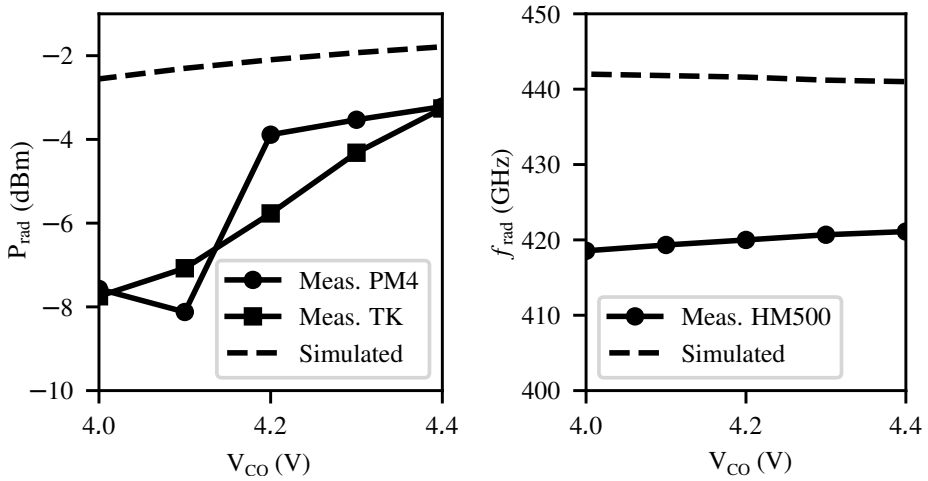


Figure 4.11: Measured radiation power and frequency for a single source pixel. The corresponding measurement setups are shown in Fig. 4.10. From [46] © 2020 IEEE.

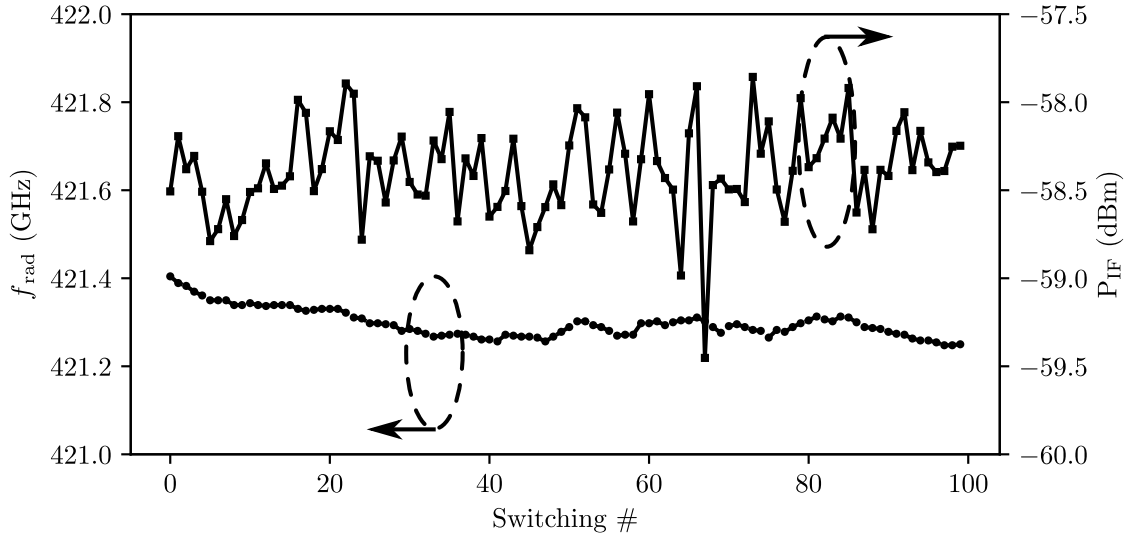


Figure 4.12: Radiated frequency f_{rad} and IF power P_{IF} measured at the HM500 mixer for switching the same pixel 100 times.

source module.

Additionally, the radiated second harmonic RF frequency (the desired component) and fundamental leakage were also investigated using the available VNAX modules. The second harmonic, measured with a WR-2.2 module from Virginia diodes Inc. is shown in Fig. 4.14(a). The source was placed at a far-field distance of $63\,\mathrm{cm}$ away from the VNAX. The propagation and conversion loss add to around $44\,\mathrm{dB}$. The IF signal shows a broad spread indicating a large phase noise, which results from the unlocked nature of source-array. The fundamental leakage was measured with a WR-3.4 (220–330 GHz) VNAX module from OML Inc. which was attached to a circular horn antenna. This was placed at $25\,\mathrm{cm}$ away from the module, which is the far-field distance for the fundamental. The measured IF spectrum is shown in Fig. 4.14(b) which indicates a fundamental radiation power level of $-50\,\mathrm{dBm}$ after calibrating for a net $21\,\mathrm{dB}$ of

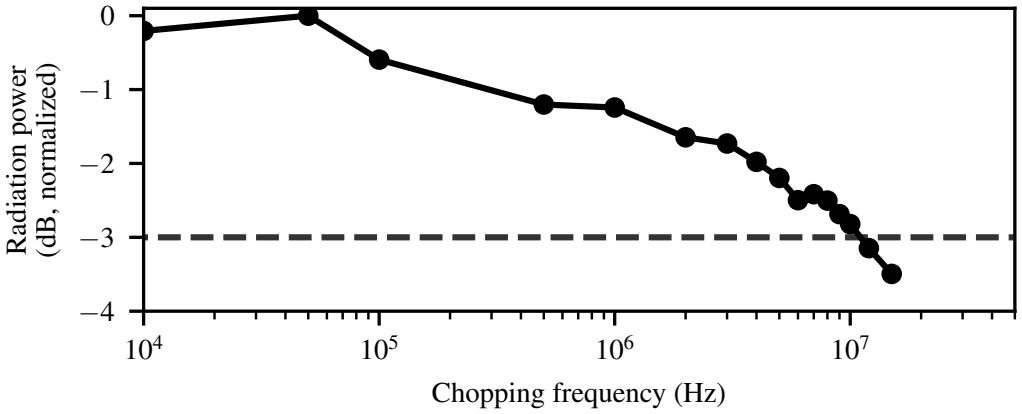
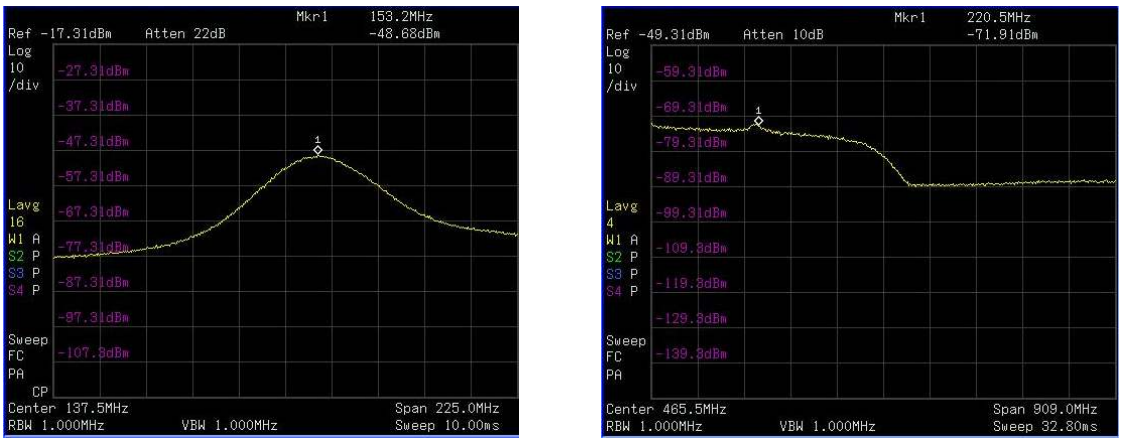


Figure 4.13: Relative radiation power vs. chopping frequency for a single pixel, measured with the setup shown in Fig. 4.10(d). Dashed line marks the -3dB level. From [46] © 2020 IEEE.

path and conversion loss.



(a) (b)

Figure 4.14: Screenshots of the spectrum analyzer showing IF spectrums for: (a) desired second harmonic from a single source pixel, measured with a WR-2.2 VNAX module with $420.116\,\mathrm{GHz}$ LO signal and $44\,\mathrm{dB}$ net path and conversion loss, and (b) fundamental leakage signal, measured with a WR-3.4 VNAX module with $210.15\,\mathrm{GHz}$ LO signal and $21\,\mathrm{dB}$ net loss.

4.5.2 Array characterization

Next, the net radiated power was measured over an accumulative number of active pixels to understand aggregate behavior of the source-array. This is shown in Fig. 4.15 where source pixels were sequentially and incrementally turned on, and the radiated power was measured with the TK power meter. The measured trend points to a saturation of the radiated power with increasing number of pixels. The measured peak radiation power was $10.8\,\mathrm{mW}$ or $10.3\,\mathrm{dBm}$. Initially, the power rises by around $472\,\mu\mathrm{W}$ ($-3.54\,\mathrm{dBm}$) per pixel, which matches the power measured for single pixel characterization. The $1\,\mathrm{dB}$ and $3\,\mathrm{dB}$ saturation points arrive upon switching on 24 and 48 pixels respectively. In order to ensure that this power saturation was originating from the SoC and not because of some measurement artifact at the TK power meter,

the array BIST response (BIST response summed up for all the pixels) was also measured. As plotted in Fig. 4.15, it also follows the saturation behavior.

Thermal throttling was discovered as the key reason behind this saturation. The source module temperature was verified with thermal imaging. Fig. 4.16 shows the temperatures for three different cases. When half of the pixels are active, and they are chopped globally at 1 MHz, the silicon lens temperature approaches 55 °C for 2.8 W dc power consumption. It further extends to 67 °C when all pixels are active and chopped with 4.5 W dc power. Note that the simulation results in Fig. 4.6 also predict this thermal throttling. This leads to a diminishing return in terms of radiated power while integrating more number of pixels on the same die, and thus multi-chip integration becomes necessary. The net radiated power can be further improved with active chip cooling.

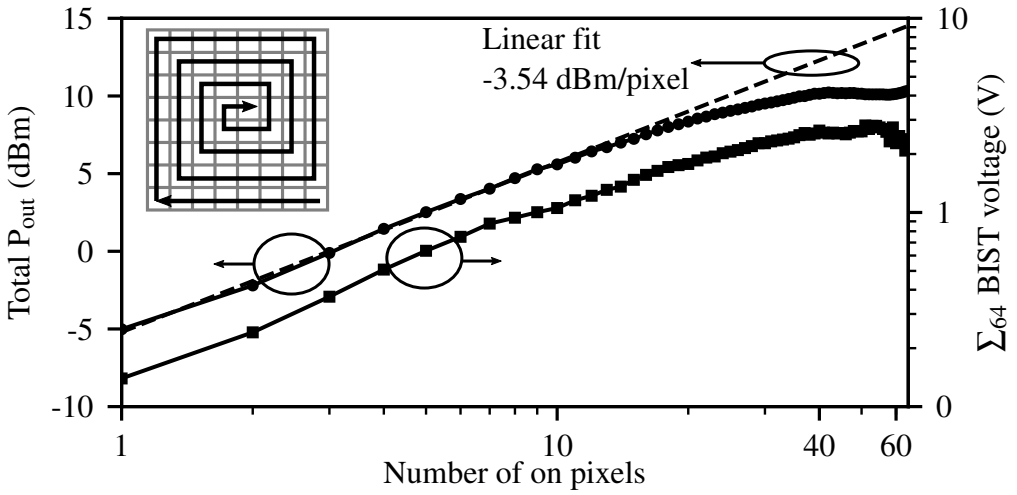


Figure 4.15: Net radiation power for cumulative pixel switching, measured with the setup shown in Fig. 4.10(b). Inset shows the pixel switching sequence. A 30 seconds cool down period was maintained between two subsequent patterns. Dashed line shows a linear fit over ten initial pixels. Right Y-axis shows the corresponding BIST response signal sum over the whole array measured with PGA voltage gain of 7.2 dB (GR = 2). From [46] © 2020 IEEE.

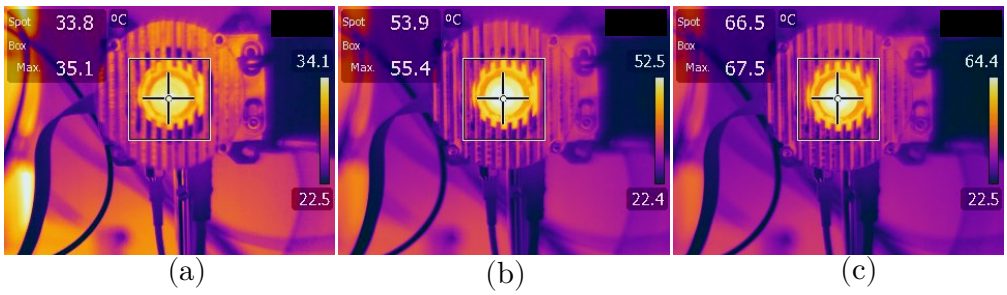


Figure 4.16: Thermal images of the source module with 1 MHz global chopping for three different operation states: (a) no pixel turned on (P_{DC}=0.8 W); (b) 32 alternate pixels turned on (P_{DC}=2.8 W); (c) all pixels turned on (P_{DC}=4.5 W). From [46] © 2020 IEEE.

The Fig. 4.17 shows the dc power consumption and conversion efficiency over the accumulative number of active pixels. The maximum power consumption is 6.85 W with 0.17 % dc-to-RF

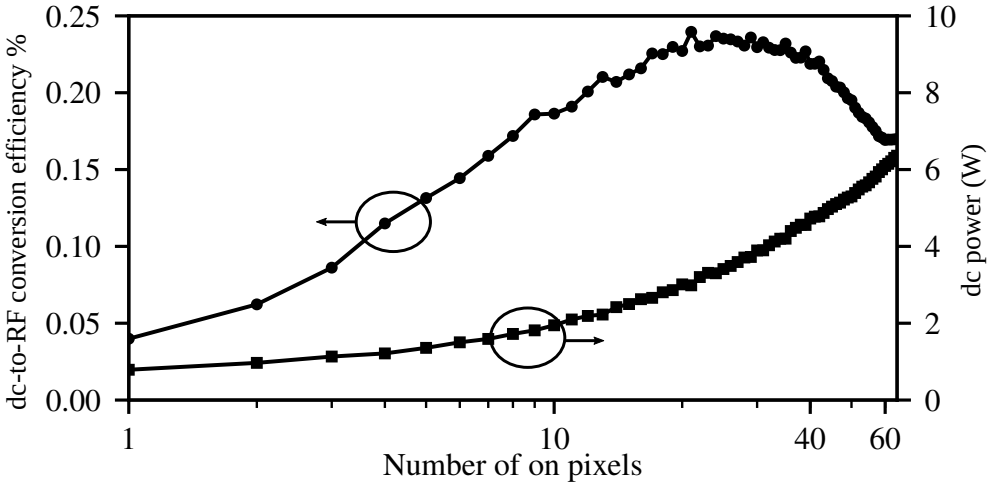


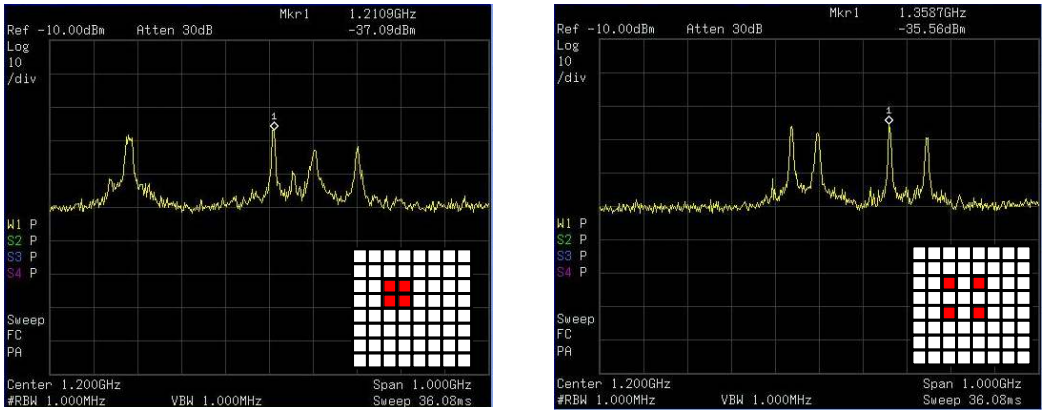
Figure 4.17: Overall dc power consumption and dc-to-RF conversion efficiency for the cumulative power measurement shown in Fig. 4.15. After [46] © 2020 IEEE.

conversion efficiency when all pixels are active. The peak efficiency is $0.24\,\%$ which is reached at around 24 pixels. Note that the dc power reported here was measured for a non-chopped condition. In case the pixels are chopped, the average dc power reduces to around half of the reported value.

A full quantitative characterization of the mutual coupling between the source pixels is challenging due to the shared pixel bias, some degree of dc feedback between the pixels, and the lack of appropriate instrumentation. Still, the following experiment was conducted to qualitatively verify the low mutual RF coupling between pixels. The WR-2.2 VNAX module and the source-array were placed at opposite $2f$ points of a convex polytetrafluoroethylene (PTFE) lens. With this setup, more than one source pixels could be sent to the VNAX. As the mutual coupling is expected to be largest between the neighboring pixels, two different test cases were measured. In the first case, four immediate neighbor pixels were turned on, while in the second case, the four active pixels were mutually separated by one intermediate inactive pixel. In both conditions, four distinct tones were observed at the VNAX IF output, indicating that the RF frequencies radiated by the active pixels were distinct or mutually unlocked. These results are shown in Fig. 4.18. It was also observed that the four tones moved together upon changing the supply V_{CO} slightly.

The PVT related output power variation of different source pixels was measured using the BIST power monitoring. The BIST values are plotted in Fig. 4.19 for each of the 64 pixels turned on separately, which indicates a pixel power variation within $3\,\mathrm{dB}$ across the array. Also, no specific correlation was observed between the BIST signal and the pixel position, indicating a uniform distribution of the shared dc bias. Any PVT variation in the BIST power detector itself is expected to be within $1\,\mathrm{dB}$ based on past measurement experience on large pixel-count CMOS integrated FPAs [160].

The overall radiation pattern when all pixels are active is shown in Fig. 4.20, which was measured



(a) (b)

Figure 4.18: IF spectrum observed from an antenna coupled WR-2.2 VNAX module when four different source pixels were turned on simultaneously. Insets highlight the pixels that are turned on with red marking.

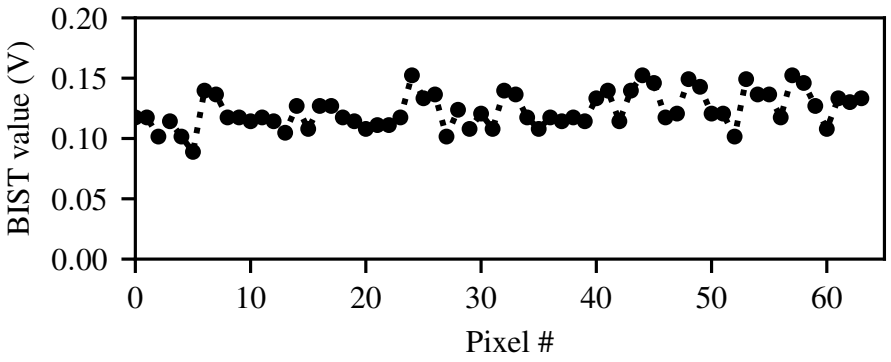


Figure 4.19: BIST response measured individually for each of the 64 pixels with PGA voltage gain of 7.2 dB (GR = 2). From [46] © 2020 IEEE.

at $1\,\mathrm{MHz}$ global chopping. To prevent thermal saturation, the chip was left inactive (all pixels off) for $20\,\mathrm{s}$ before each measurement point. All source pixels are recognizable at the antenna pattern with more than $20\,\mathrm{dB}$ isolation between the neighboring pixels. The radiation pattern cross-sections are shown in Fig. 4.20(b), where the mutual beam separation is seen to be around $7.5°$.

4.6 SPC imaging experiments

Leveraging the source-array SoC, SPC experiments were conducted with a transmission mode imaging setup shown in Fig. 4.21. The same SiGe HBT based broadband THz power detector from 4.10(d) was used here as a single-pixel receiver. PTFE lenses were used to form a collimated beam, covering the $68°$ fan-out angle of the source-array SoC, and $15°$ aperture of the detector (attached to a $3\,\mathrm{mm}$ silicon lens with directivity of $22.2\,\mathrm{dBi}$). The overall attenuation loss along the optical axis was approximated to be $9\,\mathrm{dB}$. The setup was carefully aligned to ensure the coupling of all source pixels to the power detector, and the detector baseband output was assumed to be linear with incident power. For 8×8 source pixels covering a circular aperture

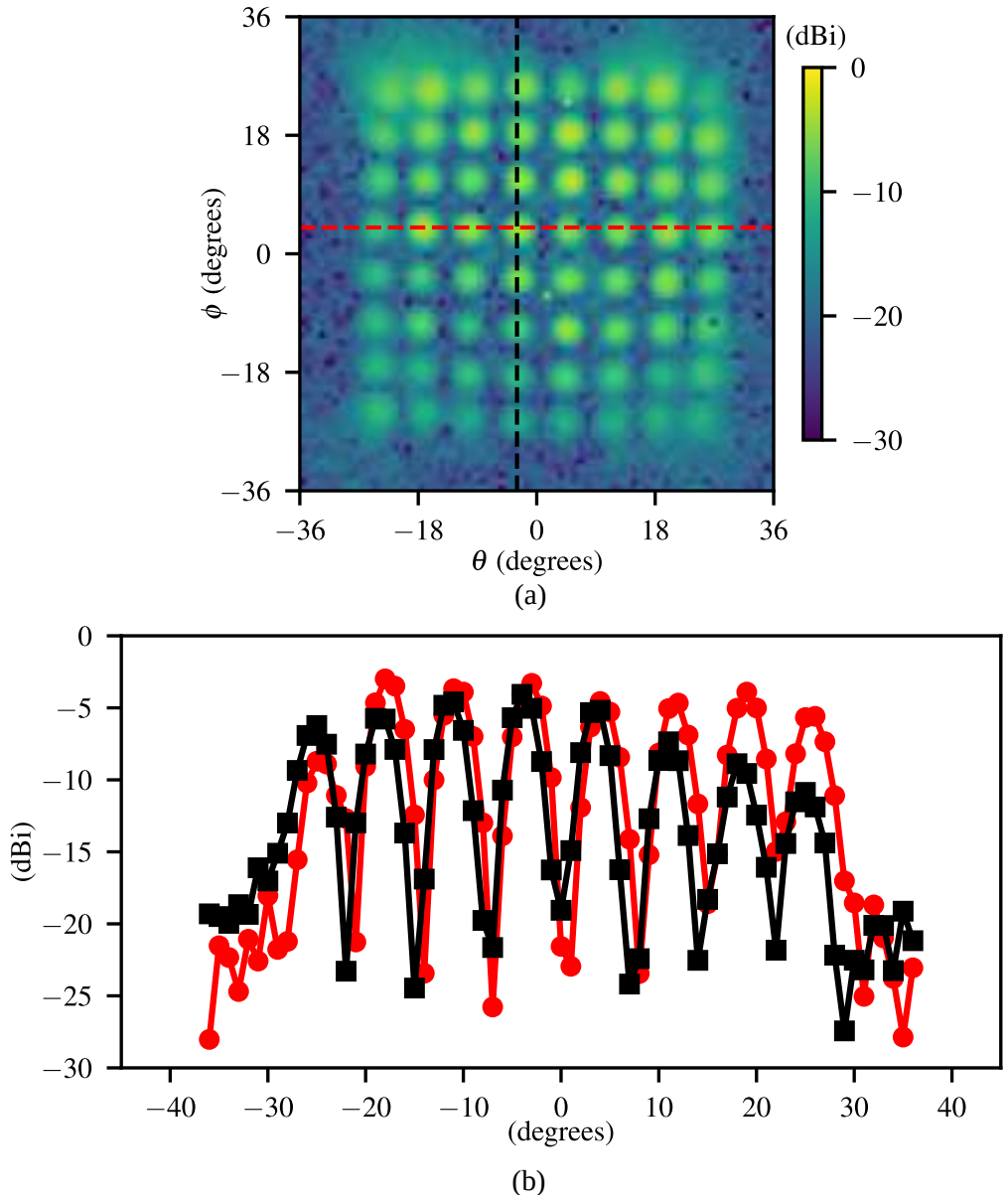


Figure 4.20: (a) Measured far-field antenna pattern for the whole array, and (b) Normalized radiation power along the cuts marked in (a). From [46] © 2020 IEEE.

of $5\,\mathrm{cm}$ diameter, the spatial resolution is calculated to be $6.25\,\mathrm{mm}$. The imaging target was an aluminum stencil sandwiched between two cardboard sheets, which was placed in the collimated beam path between the two PTFE lenses. The detector response in frequency domain $Y(f)$ was read out with a spectrum analyzer post $40\,\mathrm{dB}$ voltage amplification. Note that a direct detector was employed since a suitable heterodyne detector was not available, yet the latter is expected to provide a much improved image quality due to its higher sensitivity.

4.6.1 SLM based imaging

For SLM-based imaging, a single pixel switching scheme was preferred. In this case, the pattern matrix $\mathbf{\Phi}$ in Eq. (4.3) becomes an identity matrix. The saturation power level for the detector is

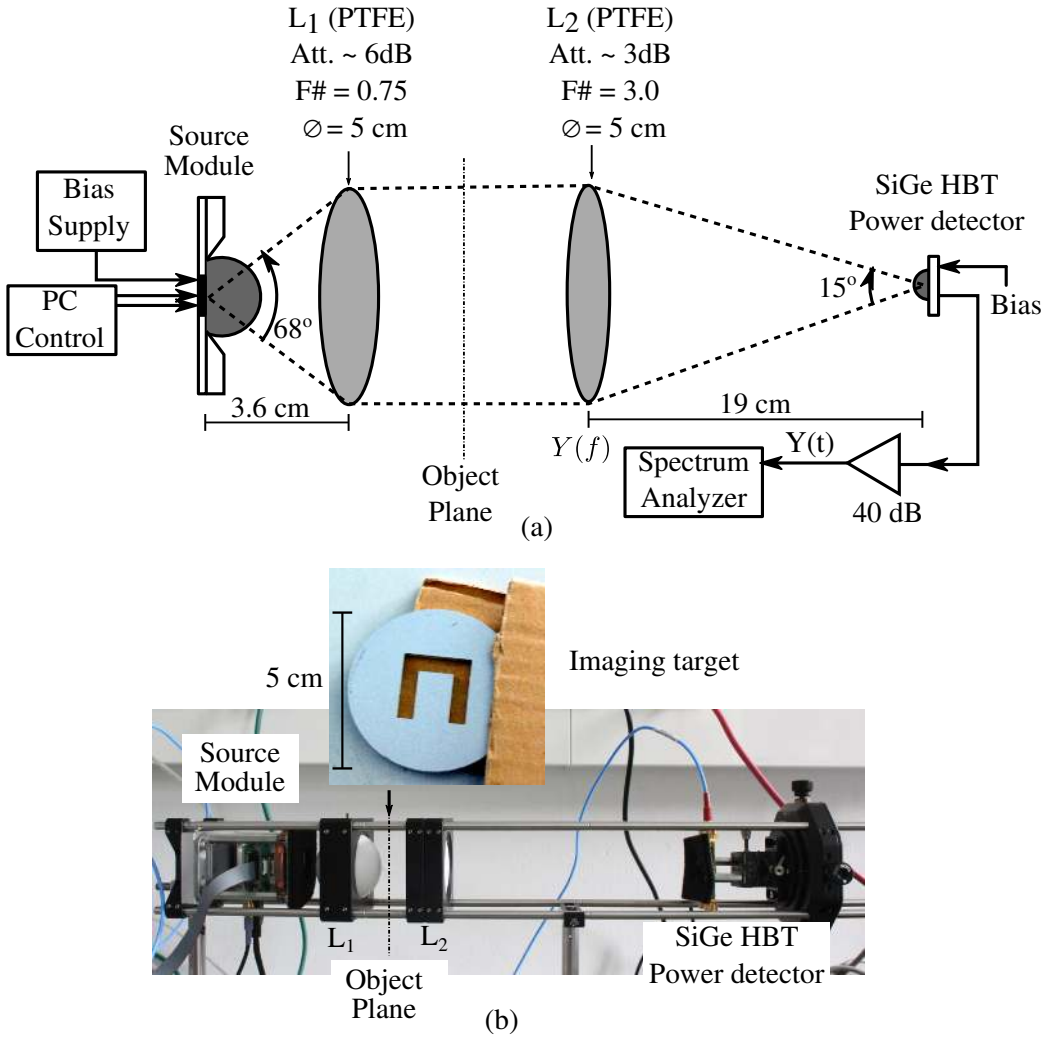


Figure 4.21: (a) Optical setup diagram for the SPC. (b) Actual picture of the SPC including the source module, single pixel detector, and PTFE lenses. Inset shows the imaging target which was an aluminum stencil concealed between two cardboard sheets. From [46] © 2020 IEEE.

unknown, yet it is expected to be below $0\,\mathrm{dBm}$. A Hadamard pattern matrix requires $50\,\%$ of the total (i.e. 32) active pixels at each mask, which may easily saturate the detector. Therefore, such a matrix was not used. The pattern matrix was preloaded into the memory cache of the SoC, which was then triggered to allow an electronic scanning of the scene. A $1\,\mathrm{MHz}$ global chopping was employed to bypass the flicker noise of the power detector. The trigger for the next pattern and the acquisition of the $1\,\mathrm{MHz}$ tone at the detector baseband were synchronized in software. The 64 values thus acquired for 64 source pixels were arranged in an 8×8 grid to form the image. One such image is shown in Fig. 4.22(a). The primary bottleneck was the readout time for spectrum analyzer, which resulted into a minimum 100 ms acquisition period for each 64-pixel image, yielding a 10 fps imaging speed. A voltage dynamic range of up to $60\,\mathrm{dB}$ was observed in this case.

In [175], 70 fps imaging was demonstrated with single-pixel switching, by connecting a fast

ADC card at the detector output, along with utilizing a hardware trigger. However, due to a non-chopped operation, the image SNR was found to be poor. Further optimization of the detector readout for even faster imaging is under investigation. Theoretically, the imaging rate can be extended to thousands of fps since the source-array SoC provides a high radiation power with a fast pattern switching. Faster frame rates lead to slow motion THz imaging, which can be of useful for commercial applications such as quality control over high throughput assembly lines in manufacturing and packaging industries.

4.6.2 FDM based imaging

Since the SLM based imaging speed was limited by the readout time of the spectrum analyzer, FDM based imaging proved crucial to extend the frame rates. With this, all source pixels could be captured within one data acquisition from the spectrum analyzer. Each source pixel was chopped at a different rate, by programming different frequency division ratios in range of 17 to 34 into the MFDs, with $25\,\mathrm{MHz}$ 'CClk' signal supplied from the control board. All the chopping frequencies were placed between the fundamental and the second harmonic of the lowest component (0.73 MHz). From the detector baseband spectrum, individual source pixels were identified from their known chopping frequencies. The spectrum analyzer span and resolution were adjusted to record these chopping tones into different frequency bins with minimum sweep time. Ultimately, an image acquisition period of $40\,\mathrm{ms}$ could be achieved which corresponds to a 25 fps video-rate imaging. Instances of the baseband spectrum and the acquired image are shown in Fig. 4.22(b) and Fig. 4.22(c) respectively. A slightly inferior voltage dynamic range of $40\,\mathrm{dB}$ resulted from the adjustments done at the spectrum analyzer, illustrating a speed-SNR trade off.

4.7 Comparison with the state-of-the-art

The performance of the source-array SoC is compared with the performance of other state-of-the-art silicon integrated THz sources, both coherent and incoherent, in Table 4.1. The design explores a new paradigm for THz sources, as most of the existing research has been focused on coherent power combining of the integrated source pixels. A detailed discussion on the coherent versus incoherent approach has already been presented in Chapter 2. The source-array SoC shows the highest radiated power for any silicon integrated THz source above $0.3\,\mathrm{THz}$, which is more than 3× larger than the highest power reported for a coherent source in [93], and more than 10× larger than the highest power reported for an incoherent source [60].

The source-array SoC can be particularly compared with the other incoherent $0.53\,\mathrm{THz}$ source-array [60] that was reported by IHCT in the year 2014. This array has 4× fewer number of pixels. While it allows programming a spatial pattern for SPC and CS based imaging [3], the programming latency is much larger due to the absence of any cache memory and integrated interface [161]. Also, the triple-push oscillator layout suffers from the problem of switching power stability [161]. Due to the careful choices in terms of oscillator topology and SoC

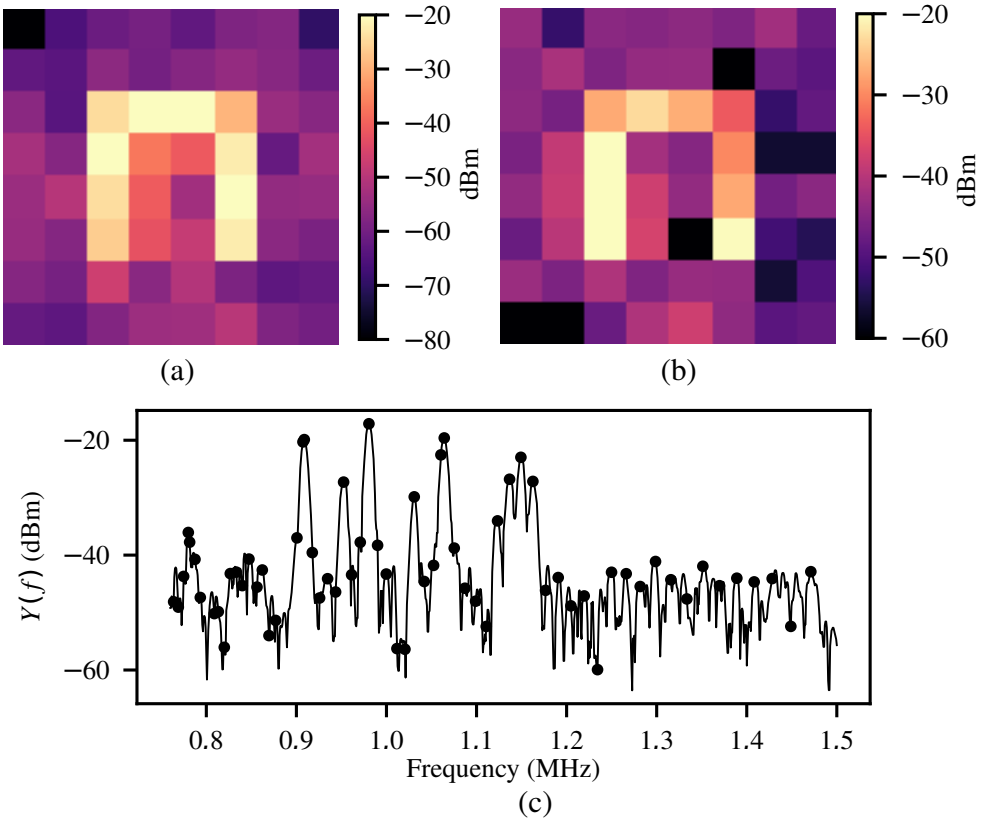


Figure 4.22: (a) Image created with single pixel switching (acq. time $\sim$ 100ms); (b) Image created with full FDM modulation (acq. time $\sim$ 40ms); (c) Baseband spectrum for full FDM modulation used to create the image in (b). Dots indicate the received power from different pixels at different chopping frequencies. The signal levels in dBm are the real values observed at the spectrum analyzer. From [46] © 2020 IEEE.

architecture, these problems have now been mitigated with the current source-array design. Also, novel functionality related to FDM and BIST has also been added to the source-array for the first time.

4.8 Conclusions and future work

In this chapter, the design and characterization of a $0.42\,\mathrm{THz}$ source-array SoC has been presented. This SoC represents a new milestone for silicon-integrated THz sources with a record radiation power and novel programmability. Due to its incoherent nature, high power intensity, and a simple dc biased operation, the SoC is analogous to the first THz light-bulb. The design further allows multi-chip scaling for boosting the radiated power and imaging aperture. While the SoC was originally designed for SPCs, the lens defined pixel-to-angle mapping, as well as FDM and multi-chip scaling functionalities, make it a crucial component for future THz light-field imaging systems. This is further explained in Chapter 7. Note that the multi-chip scaling of the source-array is not yet demonstrated. Still, it is a very rewarding endeavor, which will follow the ideas similar to those discussed in Chapter 6, with additional complexities that may arise because of the cooling requirements.

In all possibility, the SoC will be used in several novel imaging systems because of its illumination diversity and programmable reconfigurability, while the existing SPC imaging systems would also continue to improve. Investigations into THz MIMO light-fields, slow motion THz imaging, and combining the source beams for a uniform illumination, call for special attention. In the future, the SoC design can be further improved by incorporating a multi-level THz power modulation, possibly along with a tunable bias individual to each pixel, and auto power level control using feedback from the BIST.

Table 4.1: State-of-the-art in silicon integrated THz sources. After [46] © 2020 IEEE.

	This work [46]	[60]	[93]	[95]	[84]	[86]	[97]	[87]	[94]
Technology	130nm SiGe BiCMOS	130nm SiGe	130nm SiGe	65nm bulk CMOS	45nm SOI CMOS	130nm SiGe	40nm bulk CMOS	40nm CMOS	65nm CMOS
Freq. (GHz)	420	530	317	338	420	1010	586.7	660.8–676.6	416
P_{rad} (dBm)	**10.3**	0	5.2	-0.9	-10	-10.9	0.1	-16.1	-3
Coherent	**No**	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
EIRP (dBm)	**31.21**†	25†	22.5	17.1	3	13.1	24.1	7.4	14
Radiators	64	16	16	16	8	91	36	8	16
Power/radiator (dBm)	**-3.54**$^{\perp}$	-11.3$^{\perp}$	-6.84$^{\#}$	-12.9$^{\#}$	-19.03$^{\#}$	-30.05$^{\#}$	-15.5$^{\perp}$	-25.13$^{\#}$	-15.04$^{\#}$
Tuning (%)	0.7	3.2	0.06	2.1	10	–	0.7	2.36§	1.7
Efficiency (%)	0.24*/0.17**	0.04	0.54	0.053	0.014	0.0073	0.08	0.02	0.034
Area (mm^2)	12.6	4.2	2.1	3.9	10.26	1	0.68	0.862	4.1
Mod. rate*	**10 MHz**‡	–							
FDM¶	**Yes**	No							
BIST¶	**Yes**	No							
SoC¶	**Yes**	No							

†Single pixel; $^{\perp}$Incoherent; $^{\#}$Net coherent output power normalized to number of radiators; §Estimated ;

¶Applicable only to incoherent arrays; *Peak efficiency; **At peak power; ‡3-dB power roll-off.

Chapter 5

THz camera SoC

This chapter discusses the design of a CMOS based THz camera SoC. A comparison of SiGe versus CMOS THz detectors has already been presented in Chapter 2. Note that a state-of-the-art sensitivity below $5\,\mathrm{pW}/\sqrt{\mathrm{Hz}}$ with an ultra-wide bandwidth of 0.22–$1\,\mathrm{THz}$ has recently been reported for SiGe HBT THz detectors in [104]. It is entirely possible that such detectors would be leveraged in future THz cameras designed for passive THz imaging. However, apart from a high sensitivity and a large bandwidth, THz camera SoCs for multi-chip light-field array integration also require a small-footprint, a low complexity packaging, and a low dc power consumption (see Sec. 2.3). Therefore, the camera presented here is implemented with CMOS based detectors which do not require any channel biasing, resulting in a very small dc current flow and a negligible power consumption. The lack of large dc voltage and current offsets at the detector also simplifies the design of readout circuitry [109]. Also, the camera has been designed for a non-chopped operation. While a chopped operation can achieve a better sensitivity [115], [179], the requirement of the source modulation cannot be taken for granted.

5.1 Design objectives

A silicon integrated THz camera SoC was developed in the year 2012 at IHCT [109], [180], [181]. This first-generation design was implemented in a 65 nm CMOS process technology from ST Microelectronics with $8.4\,\mathrm{mm}^2$ die area. The rolling shutter readout was implemented on the chip, yet the amplification, ADC, and digital interface were packaged off-chip in a $5 \times 5 \times 3\,\mathrm{cm}^3$ metal housing. The camera was also designed to operate in a 0.7–$1.1\,\mathrm{THz}$ frequency band with a sharp sensitivity roll-off into the mid-THz band of 0.4–$0.7\,\mathrm{THz}$. This presents two major drawbacks. First, this camera has a limited usability for modern silicon THz sources radiating in the mid-THz band (Chapter 2), and second, its imaging FoV is under sampled since the beam width of each pixel is narrower than the beam separation angle [182]. Accounting for all of these concerns, the following primary objectives were considered for the design of a second-generation THz camera:

1. **Complete SoC integration** including on-chip amplification, ADC, digital data readout, and programming interface. This is necessary to allow for the low complexity, low power packages that are required for multi-chip array integration.
2. **Mid-THz operation** for ideal use of the camera with silicon integrated THz sources, along with an optimal FoV sampling.
3. **Lower cost process technology** implementation while maintaining at least the same pixel count and die area as the first-generation camera.

Note that these design objectives are not exactly compatible to each other. For example, any reduction in the operation frequency conventionally requires increasing the on-chip antenna size, which increases the die area thus offsetting any economic advantages associated with a lower cost technology. Also, the longer channel length associated with a lower cost process leads to a larger noise. The complete SoC integration also requires a better management of the dc pixel offset and variability. All such challenges are dealt with specific and unique design innovations that are described later in this chapter.

5.2 SoC design

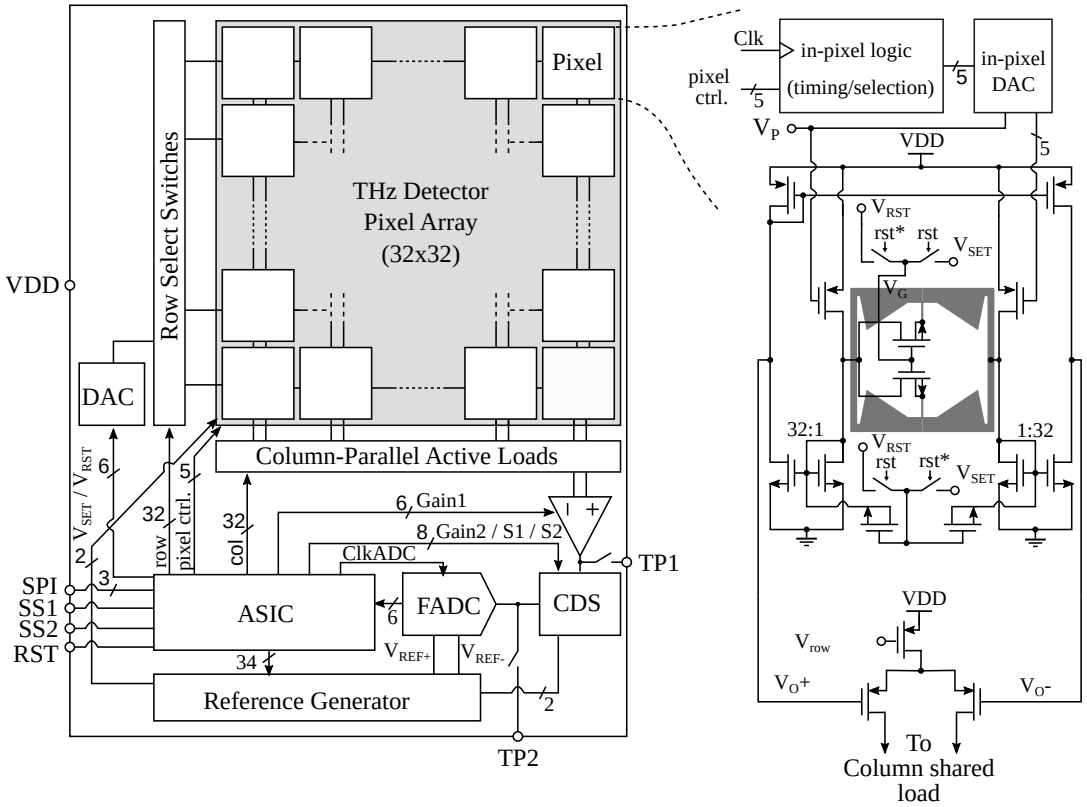


Figure 5.1: Block diagrams for the camera SoC and the detector pixel. After [47] ©2021 IEEE.

The block diagram of the second-generation camera SoC is presented in Fig. 5.1. It is implemented in the $0.13\,\mu\mathrm{m}$ SG13C CMOS process technology from IHP Microelectronics

GmbH. The SoC consists of 32×32 antenna-coupled CMOS THz power detector pixels. The pixel block diagram is also shown in Fig. 5.1. It consists of an isolated common-gate NMOS detector-pair. The source terminals in this configuration are driven differentially with a linearly polarized rectangular wire-loop antenna, also integrated within the pixel. This detector-antenna configuration allows an AC ground at the common drain output, creating a broadband RF short and mitigating the need of RF shunting capacitors [109]. The detector operation can be explained with the theory of distributed self-resistive mixing described in [107], [109]. A novel differential transimpedance readout is implemented at each pixel. The readout operation is explained in detail in Section 5.2.1. Like the source-array in the previous chapter and the first-generation THz camera in [109], the SoC is intended to be attached to a hyperhemispherical silicon lens which also provides a pixel-to-angle mapping (Sec. 2.2.3).

The pixels are activated in a rolling shutter mode with a row and column selection logic, and the PGAs, correlated double sampler (CDS) for offset cancellation, and ADC, are globally shared across all the pixels. Different biases for pixel and readout circuitry can either be generated with on-chip programmable bias generators or they can also be supplied externally. For chip programming and data readout, a standard SPI interface and a dedicated ASIC are integrated on-chip. Two select lines, labeled 'SS1' and 'SS2' allow the row and column multiplexed chip select logic for multi-chip arrays. With this design, the SoC requires only 8 pins (with on-chip bias generators) or 16 pins (with external biasing) in operation, resulting into highly compact IC packages.

5.2.1 Pixel design

The first step towards the development of a THz detector pixel is a co-design of the detector-antenna core circuitry [183]. It must be optimized to exhibit the lowest NEP over the required RF and baseband (integration) bandwidth. This involves maximizing the responsivity of the core circuitry by providing a complex-conjugate RF impedance match between the antenna and the detector, in addition to designing an optimal impedance baseband readout at the detector output. The noise generated by the NMOS transistor pair must also be minimized.

These design trade-offs have been extensively studied in several past publications [107], [109], [180], [183]. Here, we only summarize the general ideas without presenting any proofs. The detector sizing is done by selecting an appropriate channel width W and a channel length L. The minimum possible W and L are constrained by the technology limitations. A larger W indicates a higher input capacitance at the transistor, making it exceedingly difficult to achieve a broadband impedance match between the antenna and the detector [183]. A smaller (W/L) ratio provides a higher resistive impedance at the detector input, resulting into a larger RF voltage swing at the detector-antenna terminals which leads to a higher responsivity. On the other hand, a larger W increases the number of charge carriers in the transistor channel in the favor of responsivity [180]. A larger or a smaller value of the channel resistance, which is inversely proportional to the (W/L) ratio, also benefits the current-mode or the voltage-mode

readout respectively, both in terms of responsivity and thermal noise [180]. The low-frequency flicker noise is inversely proportional to the product of W and L [184]. The design of broadband on-chip antennas also becomes challenging due to the unfavorable dielectric stack of the silicon technology [185]. Due to the conduction losses, it becomes increasingly difficult to design compact, high-efficiency and broadband on-chip antennas with a large inductive impedance to tune out the input capacitive impedance of the detector. The antennas also need extra filling structures to satisfy the technology density rules, which may also prove detrimental to the antenna design [102].

For the presented design, one key goal was to extend the antenna operation bandwidth towards a mid-THz band (0.4–$0.7\,\mathrm{THz}$). The designed antenna, which is also visible in the pixel micrograph presented in Fig. 5.10(a), is shown in Fig. 5.2 with annotated structural details. It is a linearly polarized differential rectangular wire-loop antenna implemented in M1–M5 BEOL layers. The inductive impedance is created by the serpentine strip lines feeding the detector transistors. The additional tapered slots provide a longer RF current path to extend the antenna bandwidth towards lower frequencies, while the resonant slots extend the operation towards higher frequencies. Metal fillers are added along the H-plane of the antenna for density requirements. The power detector was implemented with NMOS transistors of width $W = 1\,\mu\mathrm{m}$ and length $L = 0.13\,\mu\mathrm{m}$ (minimum channel length for the technology) inside an isolated triple-well to minimize the AC switching and RF noise coupling. Fig. 5.3 shows the simulated antenna and detector impedance, as well as the simulated antenna radiation efficiency over an infinite substrate. Overall, the antenna shows a simulated optimum impedance match at 0.6–$0.7\,\mathrm{GHz}$ (see Fig. 5.9) with $> 70\,\%$ simulated radiation efficiency above $0.5\,\mathrm{THz}$.

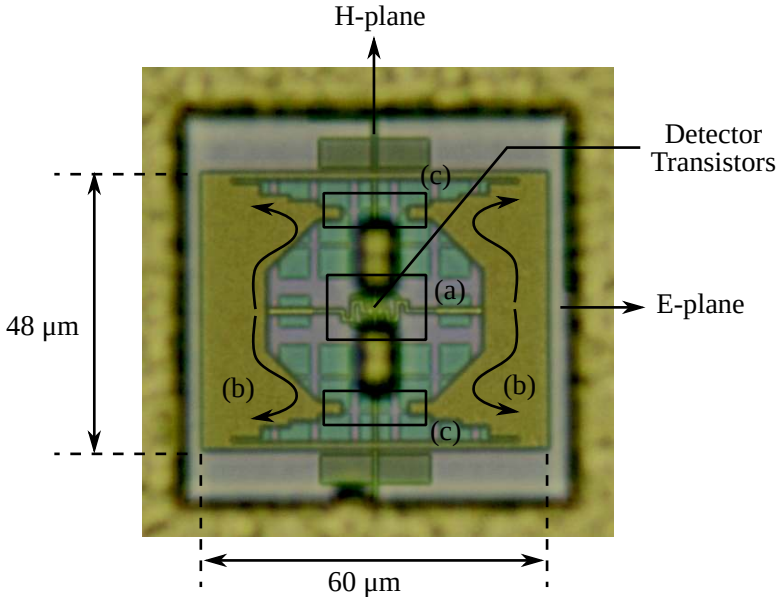


Figure 5.2: The in-pixel antenna with annotated bandwidth extending features: (a) serpentine RF feed lines for inductive impedance, (b) tapered slots for extending the antenna operation towards lower frequencies, and (c) resonant slots for extending the antenna operation towards higher frequencies.

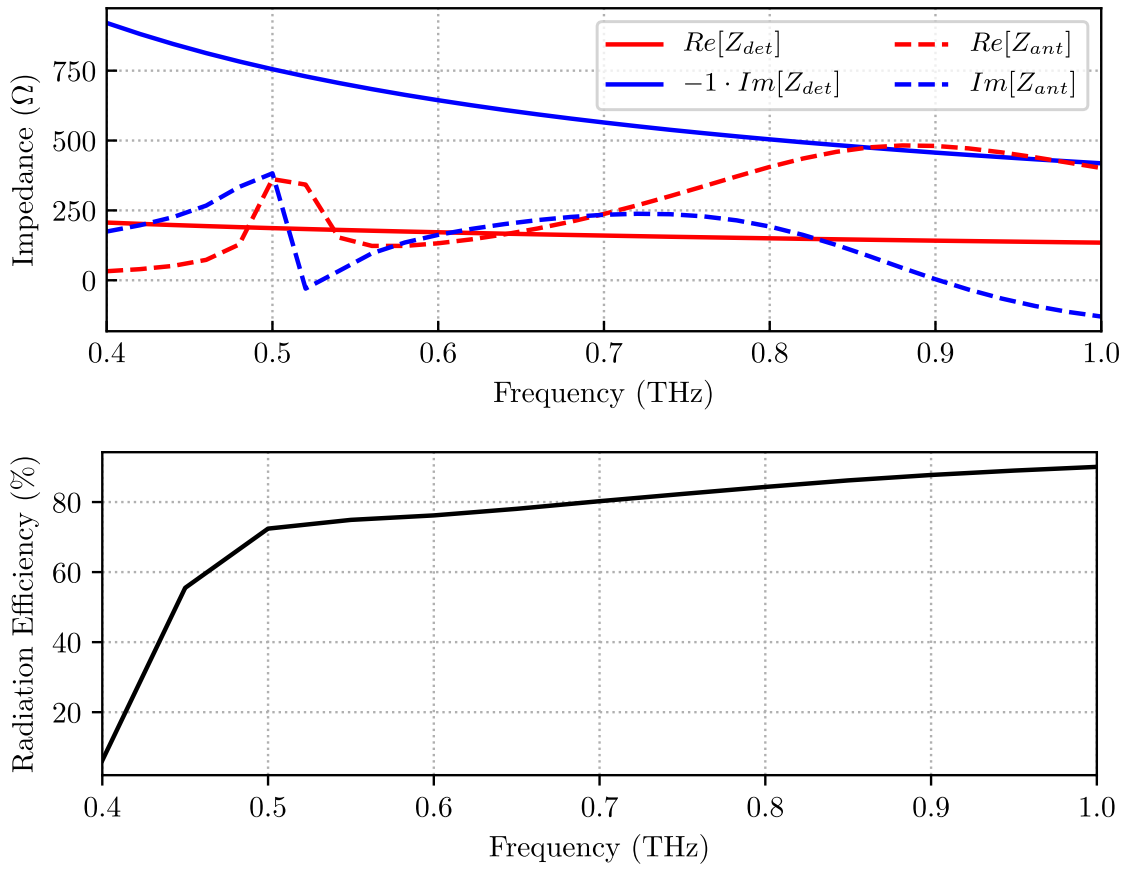


Figure 5.3: (Top) Simulated detector and antenna impedance for SG13C NMOS detector with channel dimensions $(W/L) = 1\,\mu m/0.13\,\mu m$ and gate-source bias of $0.3\,V$. Note that the detector input reactance is originally negative. (Bottom) The simulated antenna radiation efficiency over an infinite substrate.

The in-pixel readout circuit in operation is shown in Fig. 5.4. Here, the power detector is composed of transistors M_1, M_2 which share the gate and drain terminals, while their source terminals are connected differentially to the on-chip antenna feeding the RF signal. The dc bias at the source terminals is provided through the H-plane of the antenna. In order to detect the power of a THz signal fed from the antenna, the detector is biased with a voltage V_{SET} at the transistor gate terminals. Periodic deactivation of the detector is achieved by changing the gate voltage to V_{RST} (equal to the technology VDD [109]) for recording the dc pixel offset.

In the first-generation camera design, the detector output (common drain terminal of the transistors) was connected to a common-source amplifier with a high input impedance [109]. The bias for this amplifier was also provided through the antenna. In this configuration, the channel resistance of the detector transistor-pair appears in series between the gate terminal of the common-source amplifier transistor and its bias voltage. Since modulating the gate bias of the detector transistor-pair with V_{SET}/V_{RST} voltages also changes the channel resistance, such operation ends up impacting the bias voltage of the amplifier itself. Specially at bias V_{SET}, detector transistors are in a near-inversion condition where the channel resistance is high [107]. In this case, the gate of the amplifying transistor appears electrically floating, and its bias is set

by the parasitic capacitance at this terminal. Thus, such configuration creates the 'moving' dc offsets at the pixel output which must be accommodated by the subsequent readout circuitry. This reduces the overall achievable dynamic range of the integrated readout in view of its limited voltage headroom restricted by the technology VDD. Thus, in such designs, off-chip amplification is often required which increase the package size and dc power consumption, thus severely jeopardizing the multi-chip scaling approach.

This problem is solved by the differential transimpedance readout shown in Fig. 5.4. The source and drain terminals of the detector transistor-pair are connected differentially to the diode connected NMOS transistors M_3, M_4 with active PMOS load transistors M_7, M_8. Due to a differential, balanced configuration, all the node voltages remain well-defined and fixed irrespective of the detector bias, and thus the output dc offset remains fixed. The photocurrent I_{Ph} generated by the detector in response to a THz signal sinks from M_4 and sources to M_3 or vice-versa (the actual direction is irrelevant for this discussion). For a high transimpedance gain, this current must be converted to a large voltage swing, therefore transistors M_3, M_4 have to provide a large resistance. On the other hand, this resistance should be smaller than the channel resistance of the detector transistor-pair, otherwise a larger fraction of the photocurrent is wasted as a shunt current i' within the detector itself. In this design, the final transistor sizing was determined by the harmonic balance simulations. The transistors M_3, M_4 were designed with a narrow aspect ratio ($(W/L) = 0.3\,\mu\mathrm{m}/8\,\mu\mathrm{m}$) with a bias current and voltage of about $60\,\mathrm{nA}$ and $0.3\,\mathrm{V}$ respectively. This circuit is biased with a voltage V_P at the PMOS load transistors M_7, M_8, which can either be programmed internally with a 6-bit on-chip register, or it can also be supplied externally. The bias V_P, V_{SET}, and V_{RST} are shared across all the pixels. Also, a bias ΔV can be applied individually to each pixel with an in-pixel 5-bit DAC (Fig. 5.1), to compensate for up to $15\,\mathrm{mV}$ of PVT related voltage mismatch between M_3 and M_4. This range was determined from Monte-carlo simulation of the readout circuit. Finally, the photocurrent is mirrored to transistors M_5, M_6 with a multiplication ratio k of 32 established by the device sizing. The total power consumption of this circuit is around $5\,\mu\mathrm{W}$. The final differential voltage response V_O+, V_O- is fed to the shared readout scheme as explained next.

5.2.2 Shared readout scheme

The differential output of the in-pixel transimpedance amplifier is fed to another row-column shared amplifier, which in turn feeds a globally shared readout composed of a PGA, CDS stage, another PGA, and an ADC. The shared readout scheme is shown in Fig. 5.5. Each pixel integrates the PMOS transistor M_A biasing the transistor pair M_B–M_C, while the global bias voltage V_{row} is applied to a row with its 'rowsel' signal. The bias voltage V_{row} is generated by an on-chip current-steering 6-bit DAC, and it can also be supplied externally. The 'rowsel' signal is generated by the ASIC with an integrated decoder. The active load for this amplification stage is shared across a column, and it consists of NMOS transistors M_D, M_E, M_F, and M_G. With V_{row} voltage of around $0.6\,\mathrm{V}$, this amplification stage provides a simulated gain of around $7\,\mathrm{dB}$ with a simulated dc power consumption of $80\,\mu\mathrm{W}$ per column. The column output is multiplexed

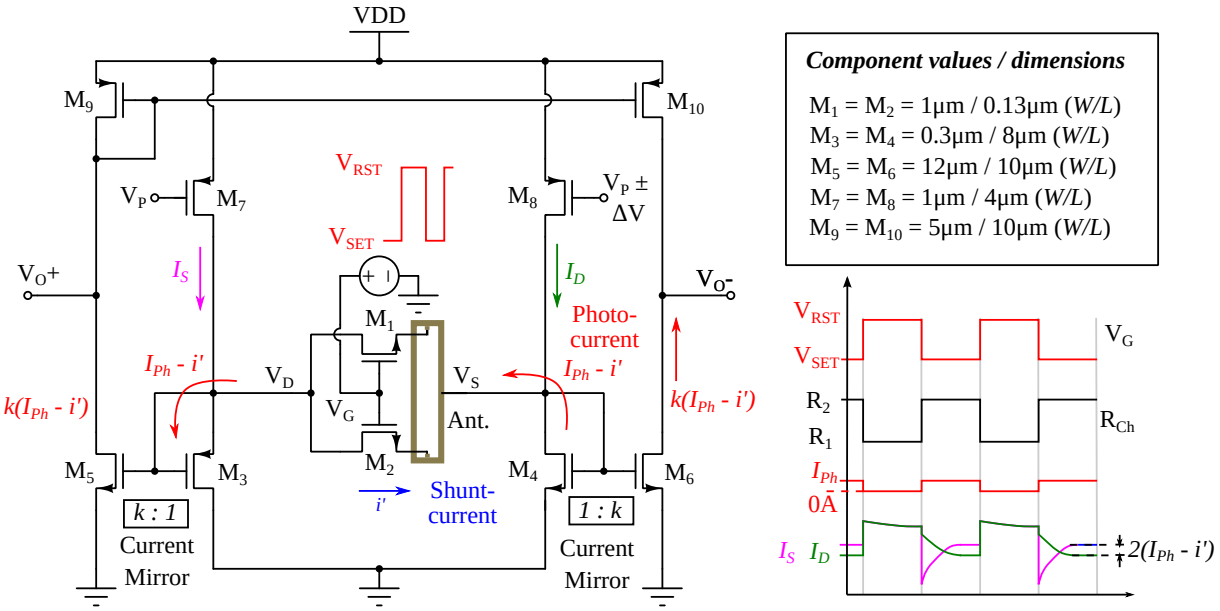


Figure 5.4: Operation of the in-pixel differential transimpedance readout circuit. Transistor pair M_1, M_2 represent the antenna-coupled detector, and current multiplication ratio $k = 32$.

with 'colsel' signal to the globally shared readout.

First, this voltage signal is amplified by a PGA with a gain A_{V1} that is programmable with a 6-bit register 'Gain1'. This gain can be programmed from $-16\,\mathrm{dB}$ to $22\,\mathrm{dB}$ (simulated) for 'Gain1' values from 0 to 63 (in decimal) respectively. The negative gain is facilitated to allow for signal attenuation in case of saturation in the readout chain. The common-mode voltage signal V_{OFF1} can be adjusted in the range of $0.3\,\mathrm{V}$ to $0.7\,\mathrm{V}$ to set the dc offset at the output. On-chip, this bias is fixed at $0.6\,\mathrm{V}$, and it can be supplied externally if a different offset is required. The output of this amplifier can be multiplexed to a test pad TP1 with switch T1. This is useful to characterize the pixel behavior for a chopped source radiation as discussed in section 5.4.1. The PGA consumes a simulated $480\,\mu\mathrm{W}$ of dc power. This is followed by CDS consisting of two sample-and-hold circuits to sample the signal and offset, corresponding to voltages V_{SET} and V_{RST} applied at the detector gate terminal respectively. The CDS output is fed to another PGA, identical to the first one. Here, the gain A_{V2} is controlled by the register 'Gain2' and the output can be multiplexed either to a test pad TP2 or to an integrated 6-bit FADC whose output D_{OUT} is the digital pixel response that is sent to the SPI. The common-mode voltage V_{OFF2} as well as the ADC range voltages V_{REF+}, V_{REF-} can either be programmed internally (each with a 6-bit bias register) or supplied externally. The ADC is identical to the one used in the source array SoC (Sec. 4.3.2). A timing diagram indicating the CDS and ADC operation is shown in Fig. 5.6. A pixel is selected for 10 SPI clock cycles (Clk), where the ADC conversion occurs at the end of 8^{th} clock cycle.

Fig. 5.7 shows the simulated response of a pixel over biases V_P and V_{SET} at $0.6\,\mathrm{THz}$. The RF port impedance in the harmonic balance simulation was set to the simulated antenna impedance at this frequency, with an input power of $-60\,\mathrm{dBm}$. The signal was extracted at TP2 and includes

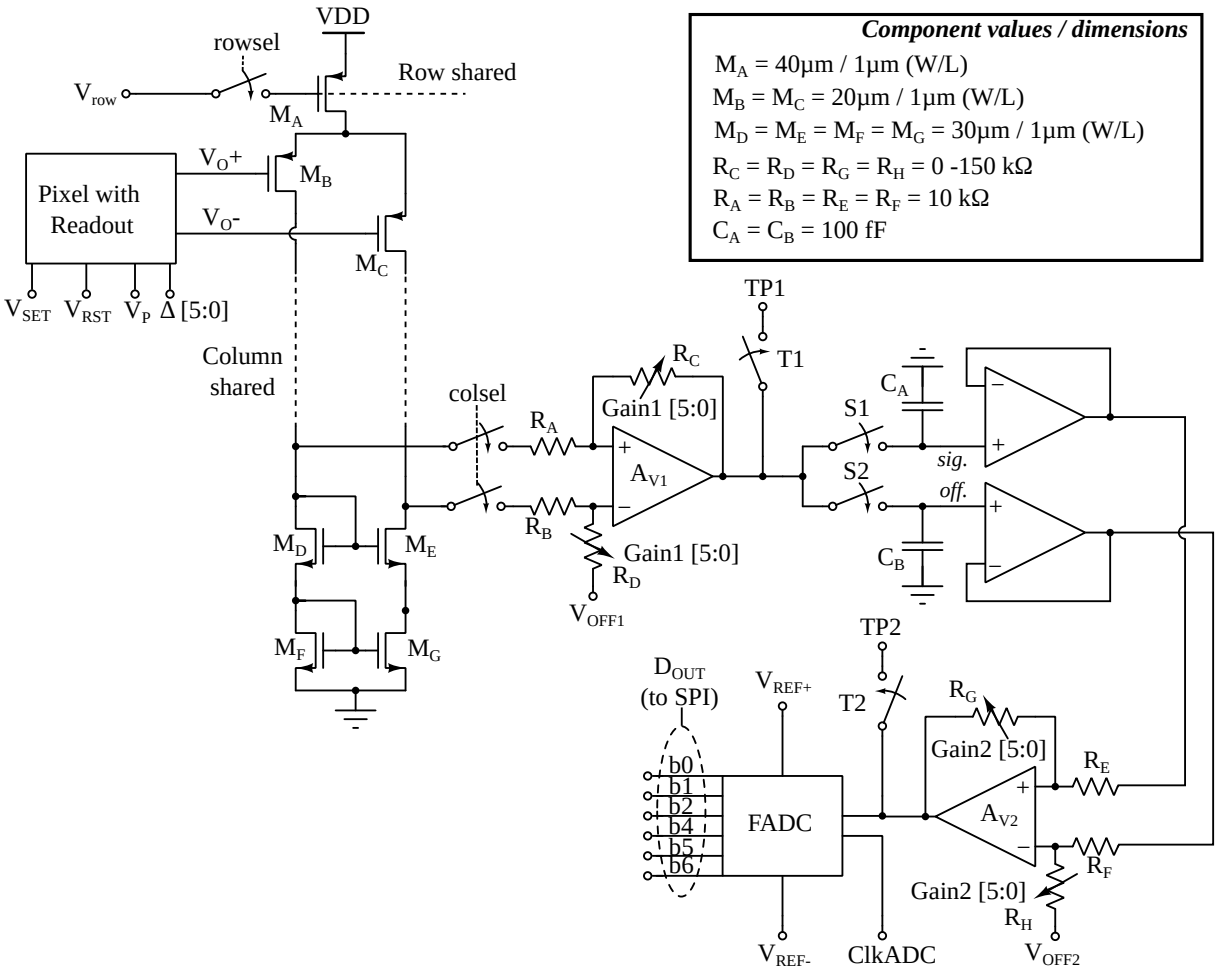


Figure 5.5: Shared readout scheme of the camera SoC. Component values and transistor dimensions are reported in the inset.

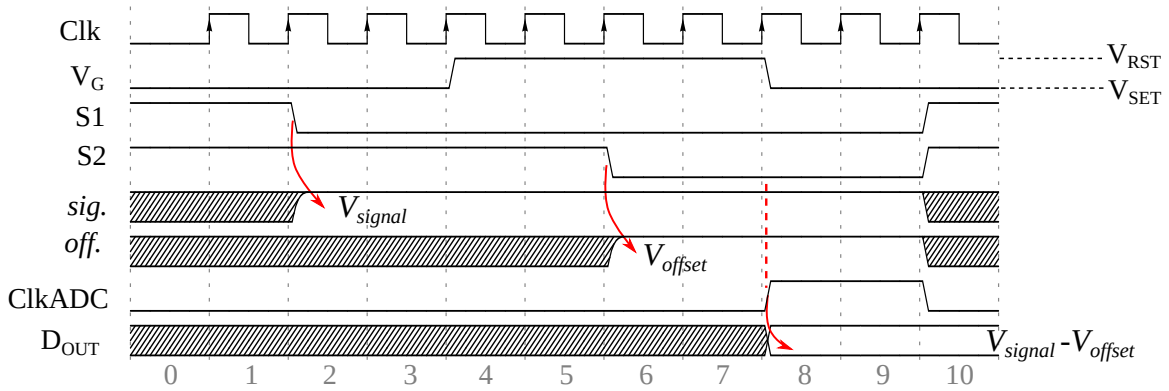


Figure 5.6: Timing diagram for the CDS operation and the pixel readout.

the whole shared readout chain up to the output of the second PGA. Note that while the optimal bias points and general trends match up to the measurements reported in the next sections, the simulations tend to overestimate the responsivity (and thus the NEP) since the antenna radiation efficiency, lens coupling efficiency, silicon-air reflections, and the exact behavior of CMOS transistors at THz frequencies [107], are all difficult to model and include in the simulations.

Therefore, quoting the responsivity and NEP numbers from simulations makes little sense. Fig. 5.8 shows the output noise voltage density over the baseband frequency. A $1/f$ noise corner at around $50\,\mathrm{kHz}$ can be observed, while the simulated 3dB baseband bandwidth is around $430\,\mathrm{kHz}$.

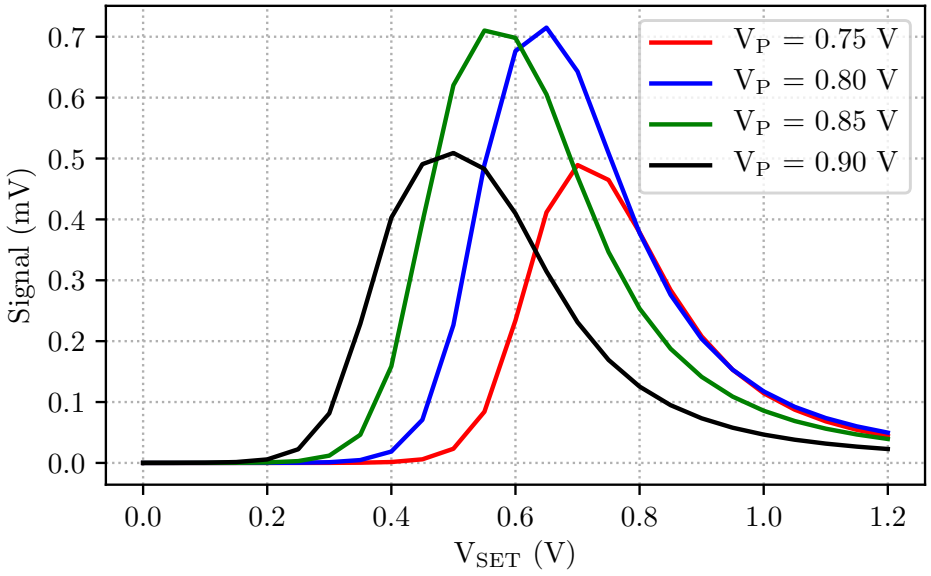


Figure 5.7: Simulated pixel response for an input power of $-60\,\mathrm{dBm}$ at $0.6\,\mathrm{THz}$, for different V_{SET} and V_P biases. The fixed bias and gain settings were $V_{row} = 0.6\,\mathrm{V}$, $V_{OFF1} = 0.3\,\mathrm{V}$, Gain1 = 5, and Gain2 = 6.

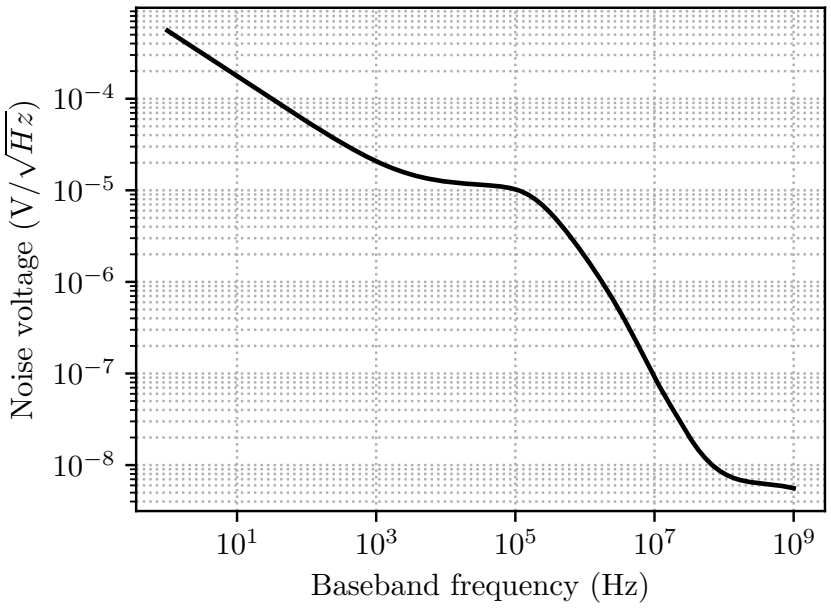


Figure 5.8: Simulated pixel baseband noise spectral density for $V_{SET} = 0.6\,\mathrm{V}$, $V_P = 0.87\,\mathrm{V}$, $V_{row} = 0.6\,\mathrm{V}$, $V_{OFF1} = 0.3\,\mathrm{V}$, Gain1 = 5, and Gain2 = 6.

Fig. 5.9 shows the simulated pixel response over the RF band of 0.4–$1.0\,\mathrm{THz}$. The simulated

antenna impedances over this band are included. These results show a peak response at $0.7\,\mathrm{THz}$ with a 3dB RF bandwidth of around $240\,\mathrm{GHz}$ (0.6–$0.84\,\mathrm{THz}$). These numbers are close to the measured values reported in Sec. 5.4.1 and Fig. 5.13. Note that the simulated response also shows a kink at around $0.5\,\mathrm{THz}$ due to some resonance in the antenna, which was also observed in the measurements.

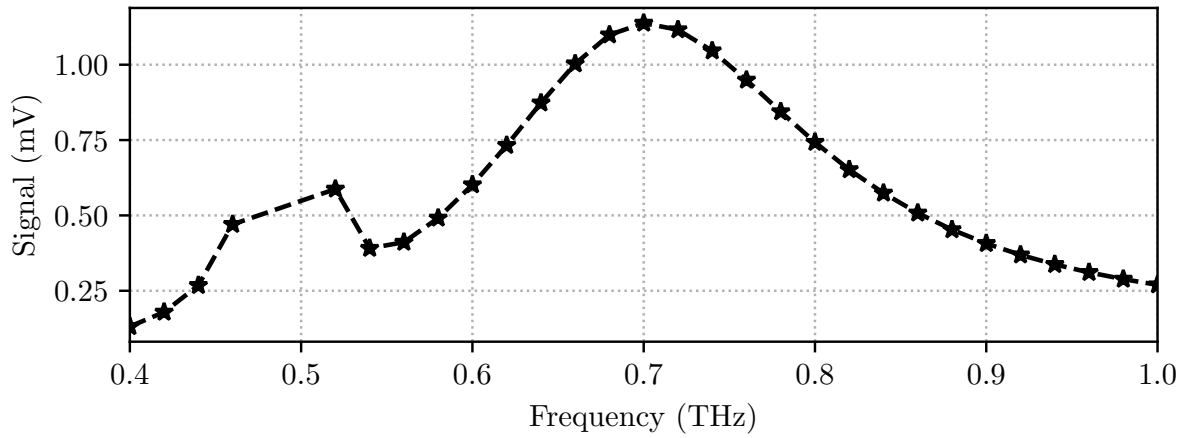


Figure 5.9: Simulated pixel response for the simulated antenna impedance (Fig. 5.3). An input power of $-60\,\mathrm{dBm}$ was applied at the RF port in harmonic balance simulation. Bias and gain settings were V_{SET} = $0.6\,\mathrm{V}$, V_P = $0.87\,\mathrm{V}$, V_{row} = $0.6\,\mathrm{V}$, V_{OFF1} = $0.3\,\mathrm{V}$, Gain1 = 5, and Gain2 = 6.

5.3 Chip micrograph and Packaging

The chip and pixel micrographs are shown in Fig. 5.10(a). The SoC has an $8.5\,\mathrm{mm}^2$ die area with $80\,\mu\mathrm{m}$ pixel pitch, while the chip thickness is $150\,\mu\mathrm{m}$. For the characterization and imaging results described in this chapter, the chip was packaged in the module shown in Fig. 5.10(b). Here, the chip was glued to the backside of a 15-mm silicon hyperhemispherical lens with an elliptical extension, and it was wire-bonded on an FR4 PCB with back-to-back connectors. The control logic was implemented in the same way as done in the source array module (Sec. 4.4). The control and the wire bonding PCBs were attached on the two sides of a motherboard PCB which provided the signal interconnections as well as SMA connectors for external biasing. Note that even before the design of this packaging scheme, some initial characterization was conducted with an Arduino controller instead of the FPGA. The single pixel wideband characterization described later in section 5.4.1 was conducted in this manner.

5.4 Performance characterization

The experimental characterization of the camera is divided into two parts: the wideband RF characterization and the digital characterization. The former was conducted with a chopped radiation and the response was read out at the test point TP1, while the latter was done with

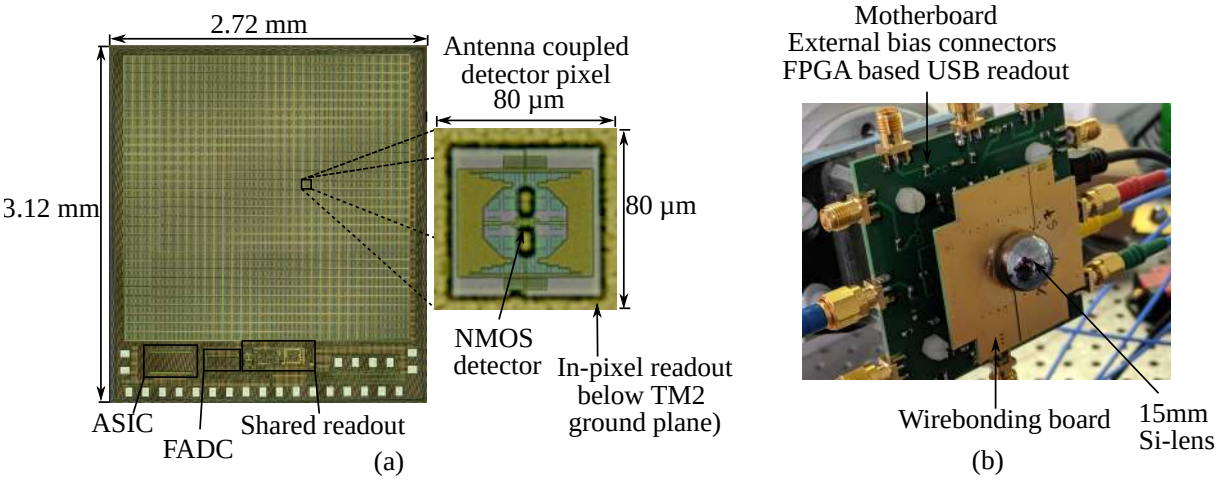


Figure 5.10: (a) Chip and pixel micrograph for the camera SoC, and (b) Packaged module used for performance characterization. After [47] © 2021 IEEE.

a non-chopped radiation and the response was read out from the digital data stream of the on-chip ADC.

5.4.1 Wideband RF characterization

For these measurements, the CW photoemitter source of the TeraScan 1550 system from Toptica Photonics was used. In this source, an InGaAs based photodiode converts the optical beat signal generated using two narrowly-detuned fibre-coupled distributed feedback (DFB) lasers into a monochromatic THz signal [186]. The radiation frequency of the source can be swept from $100\,\mathrm{GHz}$ (typical output power $\sim 100\,\mu\mathrm{W}$ or $-10\,\mathrm{dBm}$) upto $1.32\,\mathrm{THz}$ (typical output power $\sim 1\,\mu\mathrm{W}$ or $-30\,\mathrm{dBm}$) with a minimum frequency resolution of $10\,\mathrm{MHz}$ by thermally varying the offset between the two DFB lasers. The radiation can also be chopped electronically. The experimental technique to characterize a THz camera with this source was originally reported in [187].

The characterization setup is shown in Fig. 5.11. The radiation was chopped electronically at $40\,\mathrm{kHz}$, and the THz frequency was swept with a step size of $1\,\mathrm{GHz}$. The camera was placed in a collimated beam setup with $5\,\mathrm{cm}$ off-axis parabolic reflector to focus all the source power on a single detector pixel. The power incident on the camera chip was estimated by taking into account the free-space path loss and the lens spill-over loss. With this calculation, the effective THz power on a single pixel was $4.7\,\mathrm{dB}$ less than the total incident power on the chip [187]. The camera SoC was configured for a fixed selection of the detecting pixel (by disabling the Clk signal at the selected pixel, see Fig. 5.6), and the response was measured at the test point TP1. The bias signals were adjusted for the optimum (the best sensitivity) performance as reported later. The raw pixel response was also processed using a finite-impulse response (FIR) filter to remove the resonances associated with the internal lens reflections at the source. The raw and smoothed pixel responses are also shown in Fig. 5.12.

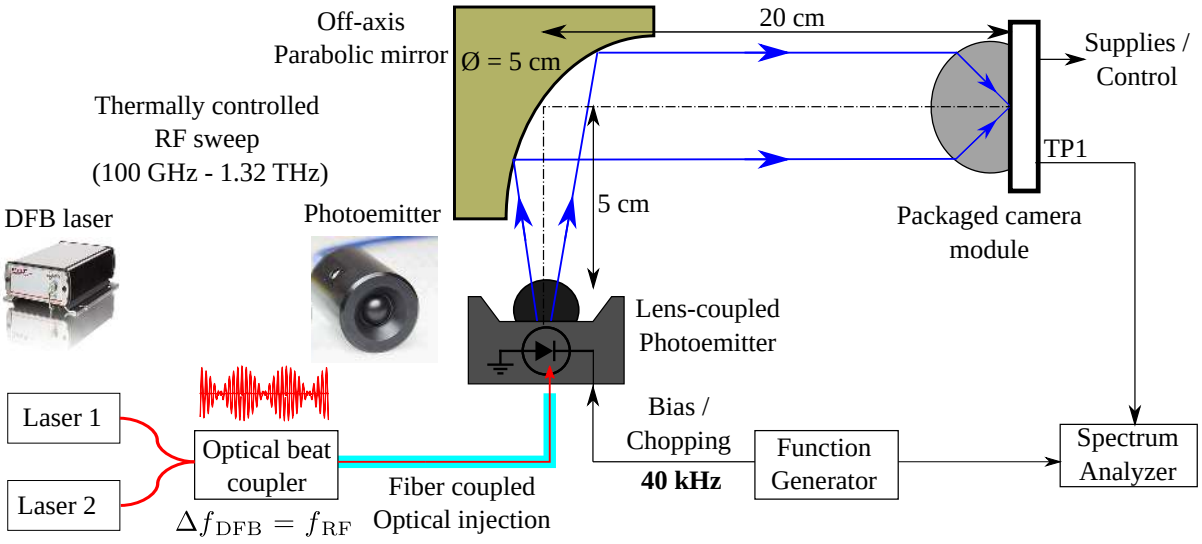


Figure 5.11: Experiment setup for the wideband RF characterization of the camera SoC.

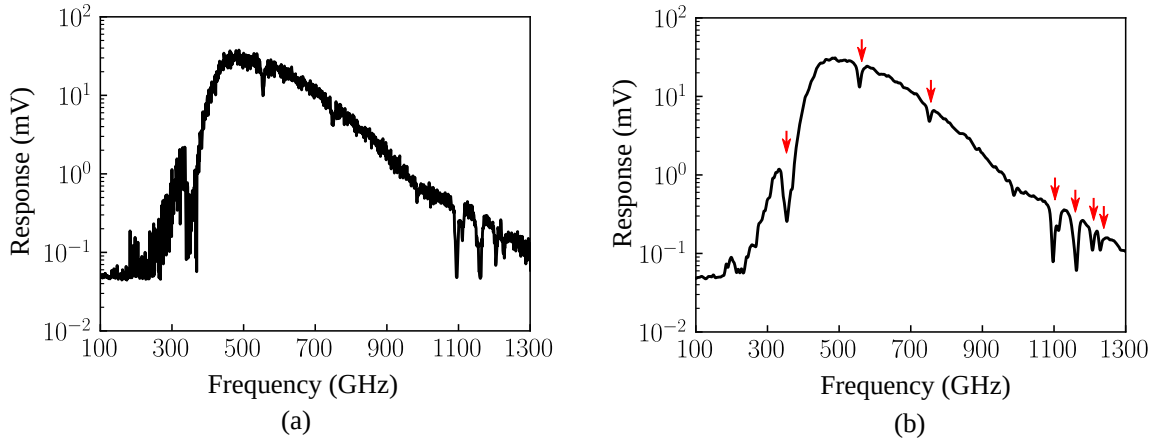


Figure 5.12: (a) Raw pixel response, and (b) filtered pixel response obtained for the wideband RF characterization. Atmospheric attenuation notches are marked with the red arrows in (b).

Fig. 5.13(a) shows the measured responsivity and NEP over the THz band for a single pixel with index (15, 14). Here, the optimal bias voltages V_P and V_{SET} of 0.87 V and 0.6 V respectively were applied externally with low-noise dc power supplies. The offset voltage V_{OFF1} of 0.3 V was also applied externally, while the bias V_{row} of around 0.6 V was applied with the integrated DAC. The simulated readout gain upto that of first PGA (Gain1 = 4) was 128 dB Ω. Inclusive of this gain, a maximum responsivity of 35 kV W^{-1} and a minimum NEP of 262 $pW/\sqrt{Hz}$ were measured at 600 GHz for the selected pixel. The NEP remains below 3 dB of its minimum value within the 460–750 GHz band, and below 10 dB of its minimum within the 415–990 GHz band. Therefore, the measured 3 dB and 10 dB bandwidths are 290 GHz and 575 GHz respectively.

The NEP versus frequency curves for three different pixels of the camera are also shown in Fig. 5.13(b). Note that this set includes the pixel (15,14) that was also selected in the last measurement. Here, all the bias signals were applied internally with the programmable bias generators. In this case, the measured minimum NEP of pixel (15,14) was 645 $pW/\sqrt{Hz}$ at

600 GHz, which represents a 2.46× degradation as compared to the measurements with the external bias. This can be attributed to a larger noise contribution from the internal bias generators. The three pixels with indices (15,14), (14,14), and (10,10) showed an approximate 50 % variation in the minimum NEP. Also, the minimum NEP of 442 $\mathrm{pW}/\sqrt{\mathrm{Hz}}$ for pixel (10,10) was obtained at 747 GHz instead of 600 GHz. Ideally, a PVT variation should not result in such dramatic shift in antenna-detector impedance matching. Note that the NEP trend of pixel (10,10) is almost flat over the 0.6–0.8 THz frequency band, and a change in the optimum RF frequency can be a result of the measurement noise.

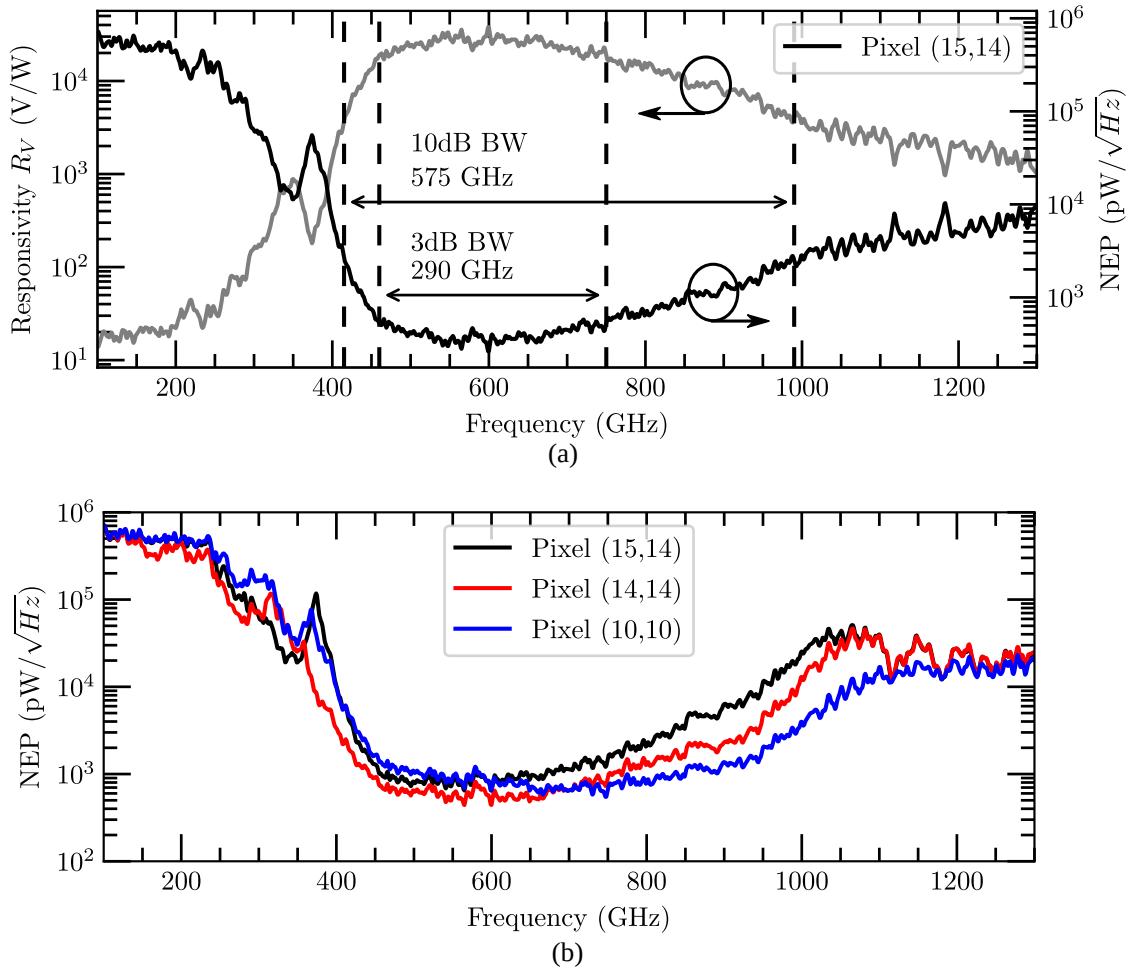


Figure 5.13: (a) Measured responsivity (maxima = 35 $\mathrm{kV\,W^{-1}}$ at 600 GHz) and NEP (minima = 262 $\mathrm{pW}/\sqrt{\mathrm{Hz}}$ at 600 GHz) for a single pixel with externally applied biases, for bias voltages V_{row} = 0.6 V, V_{OFF1} = 0.3 V, V_P = 0.87 V, V_{SET} = 0.6 V. (b) Measured NEP of three pixels with internal biases applied. Minimum values observed were 645 $\mathrm{pW}/\sqrt{\mathrm{Hz}}$ at 600 GHz, 442 $\mathrm{pW}/\sqrt{\mathrm{Hz}}$ at 600 GHz, and 547 $\mathrm{pW}/\sqrt{\mathrm{Hz}}$ at 747 GHz for pixels (15,14), (14,14), and (10,10) respectively. After [47] © 2021 IEEE.

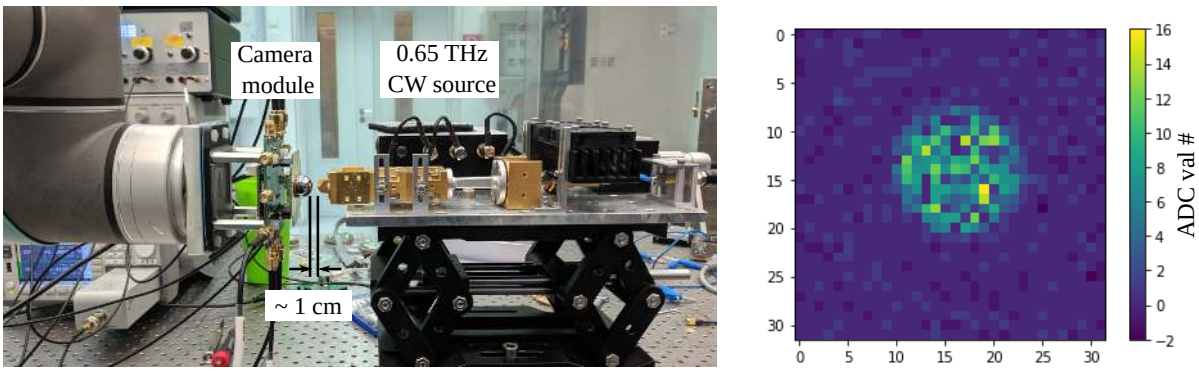
5.4.2 Digital characterization

For these measurements, a 0.65 THz waveguide coupled CW source from Virginia Diodes Inc. was used. This source radiates maximum 3 dBm or 2 mW of power. It also includes a bias port

for user controlled attenuation (UCA) of the radiated power by applying 0–$5\,\mathrm{V}$ voltage. In all measurements, the full-frame 1k-pixel digital image data was read out directly from the camera.

5.4.2.1 Sensitivity characterization

The first measurements were targeted towards the characterization of video-rate sensitivity of the camera. For this purpose, the camera was placed back-to-back near the source at a close distance of around $1\,\mathrm{cm}$. At this distance, it was assumed that the total radiated power from the source was available at the camera SoC. Note that this is an ideal case and there could be unaccounted losses related to the reflections and standing waves. Nevertheless, such ideal assumption prevents any overestimation of the sensitivity. A picture of the imaging setup is shown in Fig. 5.14(a). To avoid saturation of the camera output, the source power was attenuated to $-8\,\mathrm{dBm}$ by applying a $3.0\,\mathrm{V}$ bias at its UCA port. The camera frame-rate was controlled by changing the duration of the main clock signal (Clk) at the SoC. The ADC was operated over the full-range ($V_{REF+} = 1.2\,\mathrm{V}$, $V_{REF-} = 0\,\mathrm{V}$), and all the bias signals except V_{row} were applied externally. Both PGA offsets V_{OFF1} and V_{OFF2} were biased at $0.3\,\mathrm{V}$.



(a) (b)

Figure 5.14: (a) Experiment setup for the digital sensitivity characterization, and (b) sample camera image obtained at 25 fps post calibration.

As outlined in [109], the minimum detectable power (or sensitivity) of the camera equals to the NEP of a single camera pixel. To characterize this, a number of frames (100–1000) were first streamed out of the camera with the source turned off. A large number of frames are necessary to calculate the statistical parameters with a high precision. From the frame dataset, a mean-value frame was derived to calculate the pixel offsets, while a pixel-wise standard deviation provided the RMS noise for each pixel. The noise of a single pixel v_n was calculated as an average of the RMS noise from all the pixels.

To calculate the responsivity, the source was turned on and same number of frames were again acquired. Post averaging, the mean pixel offsets calculated in the earlier step were calibrated out. One of such calibrated frame is shown in Fig. 5.14(b). Since the source power spills to several pixels, the average responsivity R_V for a single pixel can be calculated by summing up the signal from all the pixels in the frame, and dividing this sum by the source power [109].

The NEP can be calculated by dividing the average noise v_n calculated earlier with average responsivity calculated in this step. Note that that unlike the wideband RF characterization where the calculated NEP was spot-NEP (baseband noise measured at the chopping frequency with a noise bandwidth of $1\,\mathrm{Hz}$), the NEP calculated in digital characterization is the integrated NEP. This accounts for the baseband noise integrated over the readout bandwidth of the camera. More details on this characterization procedure can be found in [109] and [160].

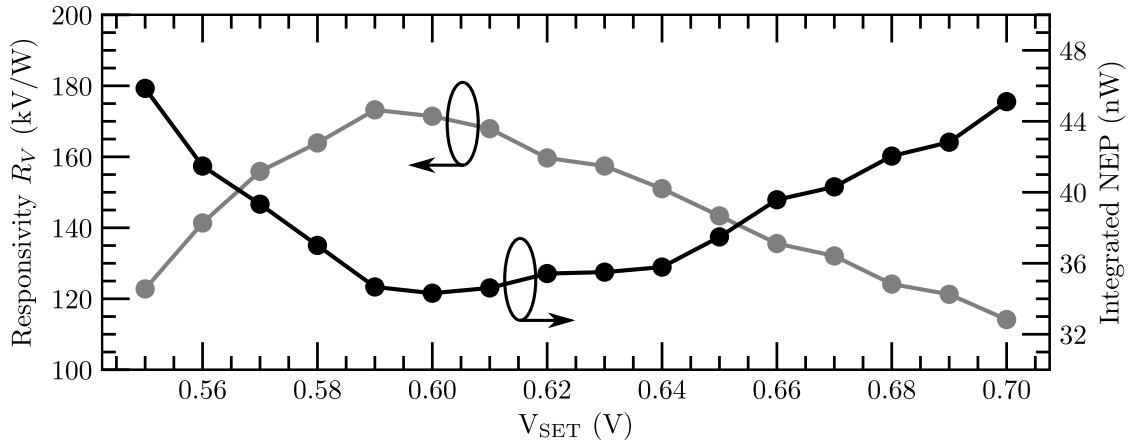


Figure 5.15: Measured responsivity (maxima = $171\,\mathrm{kV\,W^{-1}}$ at V_{SET} = 0.6 V) and integrated NEP (minima = $36\,\mathrm{nW}$ at V_{SET} = 0.6 V) for $0.65\,\mathrm{THz}$ at 25 fps. Biases V_P = 0.81 V, V_{OFF1} = 0.3 V, V_{OFF2} = 0.3 V, V_{REF+} = 1.2 V were applied externally. After [47] © 2021 IEEE.

The measured NEP and responsivity over the gate bias V_{SET} are shown in Fig. 5.15. The maximum responsivity was $171\,\mathrm{kV\,W^{-1}}$. Note that this corresponds to a simulated readout gain of $141\,\mathrm{dB\,\Omega}$ including both first and second PGA (Gain1 = 5, Gain2 = 6). The minimum NEP was $36\,\mathrm{nW}$ at a gate bias of $0.6\,\mathrm{V}$. The bias V_P in this case was $0.81\,\mathrm{V}$. In this case, the simulated 3dB readout bandwidth was $430\,\mathrm{kHz}$, which corresponds to an integration time of around $11\,\mu\mathrm{s}$ as per Eq. 2.2. Note that the above data was recorded at 25fps with 75fps data streaming and 3 frame averaging in post-processing. The maximum frame rate was capped at 90 fps due to the data rate limitation of the FT232R USB-to-serial IC packaged with the camera module. In digital mode, the net power consumption of the camera SoC was measured to be $13.5\,\mathrm{mW}$, with about $10.5\,\mathrm{mA}$ of current from $1.2\,\mathrm{V}$ power supply for the analog circuitry, approximately $100\,\mu\mathrm{A}$ current each at the offset biases V_{OFF1}, V_{OFF2}, and ADC supply V_{ref+}, and around $500\,\mu\mathrm{W}$ of power consumed by the digital logic. This implies a net power consumption of $13.3\,\mu\mathrm{W}$ per pixel including the digital readout. The PCB boards with control logic consumed about $28\,\mathrm{mA}$ of current from $5\,\mathrm{V}$ supply resulting into $140\,\mathrm{mW}$ of dc power.

5.4.2.2 Antenna pattern characterization

The antenna patterns of the camera pixels were also characterized in the digital mode. Here, the camera was placed at the far-field distance of $1\,\mathrm{m}$ away from the source. The source was operated at its full radiated power, and the camera was rotated along the azimuth and elevation

axis using a 6-axis robotic arm. The source was also turned off periodically for offset cancellation. The measured 2D antenna pattern for one of the center camera pixels is shown in Fig. 5.16. The HPBW estimated directivity is around $39.5\,\mathrm{dBi}$ as compared to lens aperture defined theoretical directivity of $40.2\,\mathrm{dBi}$, and first side lobe level is at -10 to $-12\,\mathrm{dB}$. Fig. 5.17 shows the antenna patterns for multiple adjacent pixels along a row, which show a beam overlap of about $-3\,\mathrm{dBi}$. This results in an optimal FoV sampling [182], which is related to our design choice of making the camera more sensitive in a lower frequency range, while having a small pixel pitch. Any closer or any farther beams would over sample and under sample the FoV respectively. Also, note that the antenna patterns of different pixels in Fig. 5.17 are normalized individually. The sixth pixel from left has a lower responsivity (due to PVT variations), leading to a lower SNR.

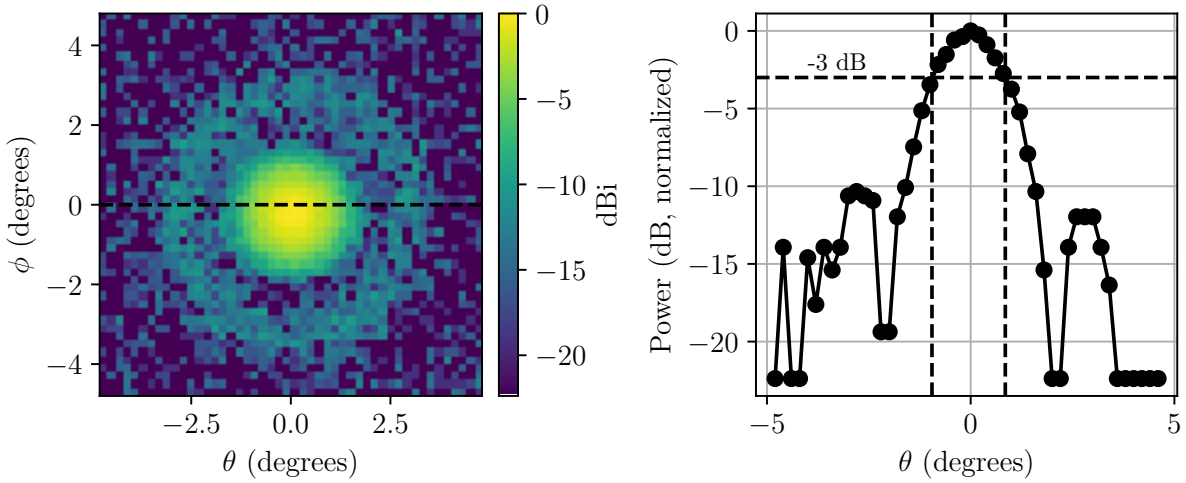


Figure 5.16: Measured antenna pattern for a single pixel in digital readout mode at $0.65\,\mathrm{THz}$. Full 3D pattern is shown on the left, while a 2D E-plane cross-section is shown on the right.

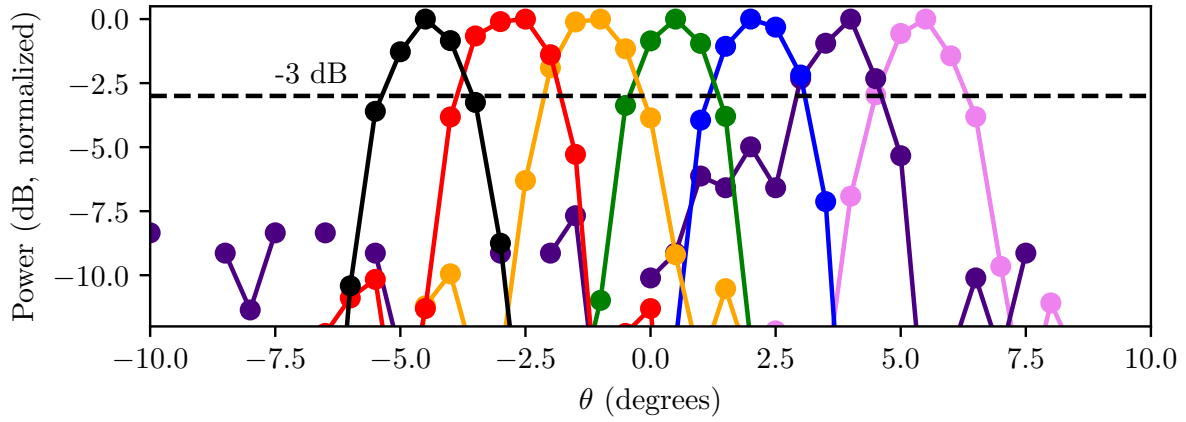


Figure 5.17: Measured antenna patterns at $0.65\,\mathrm{THz}$ for five adjacent pixels in a row at the center of FPA. Different pixels are delineated with different colors.

Fig. 5.18 shows the distribution of maximum signal that was detected by each pixel during a full rotation of the camera in far-field at the front of the $0.65\,\mathrm{THz}$ source. While around $90\,\%$ of

the pixels show a variability within $2\,\mathrm{dB}$, around $10\,\%$ of the pixels were found to be inactive. Also, these inactive pixels are located randomly around the array. We expect the technology PVT variation to be the reason of these inactive pixels. However, since only one sample was measured with this time-consuming technique, more accurate statistics on this variation could not be determined. Possibly the in-pixel DAC can be used to activate at least some of these pixels. More comprehensive measurements can be the subject of a future investigation.

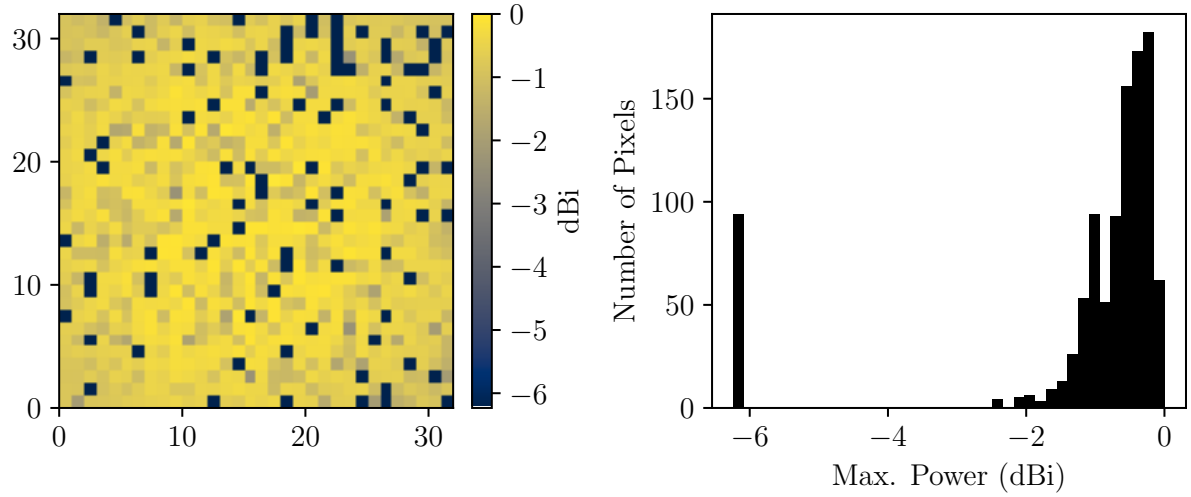


Figure 5.18: Relative maximum signal (in logarithmic scale) detected by each pixel in a full antenna pattern scan. The figure on the left shows the spatial distribution across the FPA, while the one on the right shows a histogram for the same.

5.5 Light-field imaging experiment

To show the light-field imaging capabilities of the camera, we selected the application of acquiring the 3D radiation pattern of the $0.65\,\mathrm{THz}$ CW AMC source. The WR-1.5 diagonal horn waveguide antenna at the source provided $25\,\mathrm{dBi}$ of directivity with about $10°$ of HPBW [188]. The source was operated with full $2\,\mathrm{mW}$ radiated power. The camera was placed at a distance of 20 centimeters away from the source, and it was scanned in a 2D plane in 11×11 steps to emulate a virtual light-field camera array. The imaging setup is illustrated in Fig. 5.19. The step size was $1.5\,\mathrm{cm}$ corresponding to the footprint of the silicon lens. The camera was operated at 25 frames per second with 100 frame averaging and offset cancellation for each sub-image. In chapter 6, we show the packaging of a real light-field camera array achieving similar lens-to-lens spacing. The overall imaging time was $35\,\mathrm{min}$, which can be reduced down to $17\,\mathrm{s}$ with an actual camera array of the same size, assuming all the cameras in this array can operate at the same speed of 25 fps.

The raw light-field dataset thus acquired is shown in Fig. 5.20(a). The antenna pattern

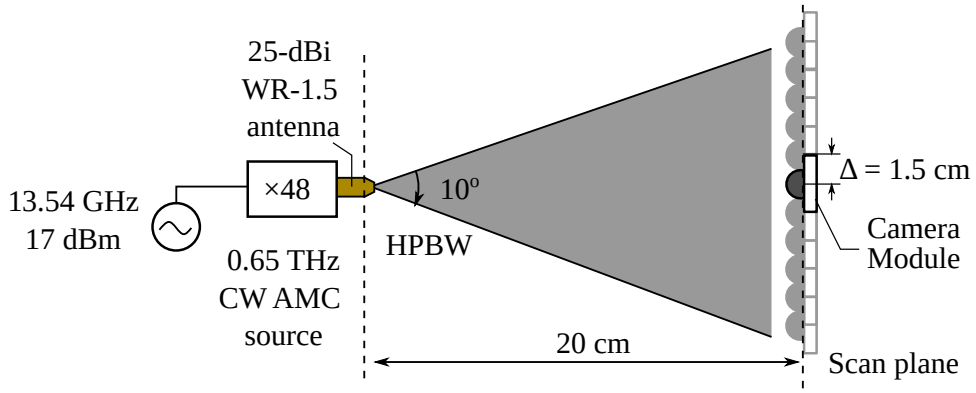


Figure 5.19: Imaging setup for the virtual light-field camera. The camera module is stepped into 11×11 positions with a step size of $1.5\,\mathrm{cm}$ corresponding to the silicon lens diameter.

reconstruction was done according to the following equation:

$$S(p,q) = \sum_{m=1}^{11}\sum_{n=1}^{11} V(m,n:p,q) \quad \forall \quad p \in [1,32], q \in [1,32] \tag{5.1}$$

Here, $S(p,q)$ is the reconstructed antenna pattern, where the pixel index (p,q) can be converted to the azimuth and elevation angles (θ,ϕ) as per the Eq. (2.6). It is also pointed out that the above equation follows the same terminology discussed in Fig. 3.9. As each camera pixel looks in a specific direction irrespective of the camera position, if the signal from this pixel is summed up across all the positions then an estimation is obtained for the power incident at this specific direction over the whole scan plane. In the above equation, this process is repeated for all pixels of the camera to create a 3D power versus direction plot. The reconstructed antenna pattern is shown in Fig. 5.20(b), with a cross-section shown in Fig. 5.20(c). The reconstructed pattern shows an approximate Gaussian profile with measured HPBW of $8°$ which is close to the actual HPBW of the source. The pattern quality and the beam width estimation can be further improved using an inter-pixel interpolation scheme, or with a finer scanning step size, or both. However, such enhancements were not added in the reported results in order to demonstrate the true quality of the raw data.

5.6 Comparison with the state-of-the-art

Table 5.1 shows a comparison of the performance of our camera SoC with other state-of-the-art silicon integrated THz cameras from the literature. The cameras in [115] and [189] have been implemented in an even cheaper 180nm CMOS technology. However, both designs integrate large and narrowband patch antennas resulting in around 8× large pixel area as compared to our camera. These patch antennas have also been designed for higher THz frequencies, possibly to limit the chip area. Also note that the camera in [115] presents a chopped readout thus requiring modulation of the source radiation which partially contributes to the excellent NEP performance. The camera in [179], implemented in a similar 130nm process technology as ours,

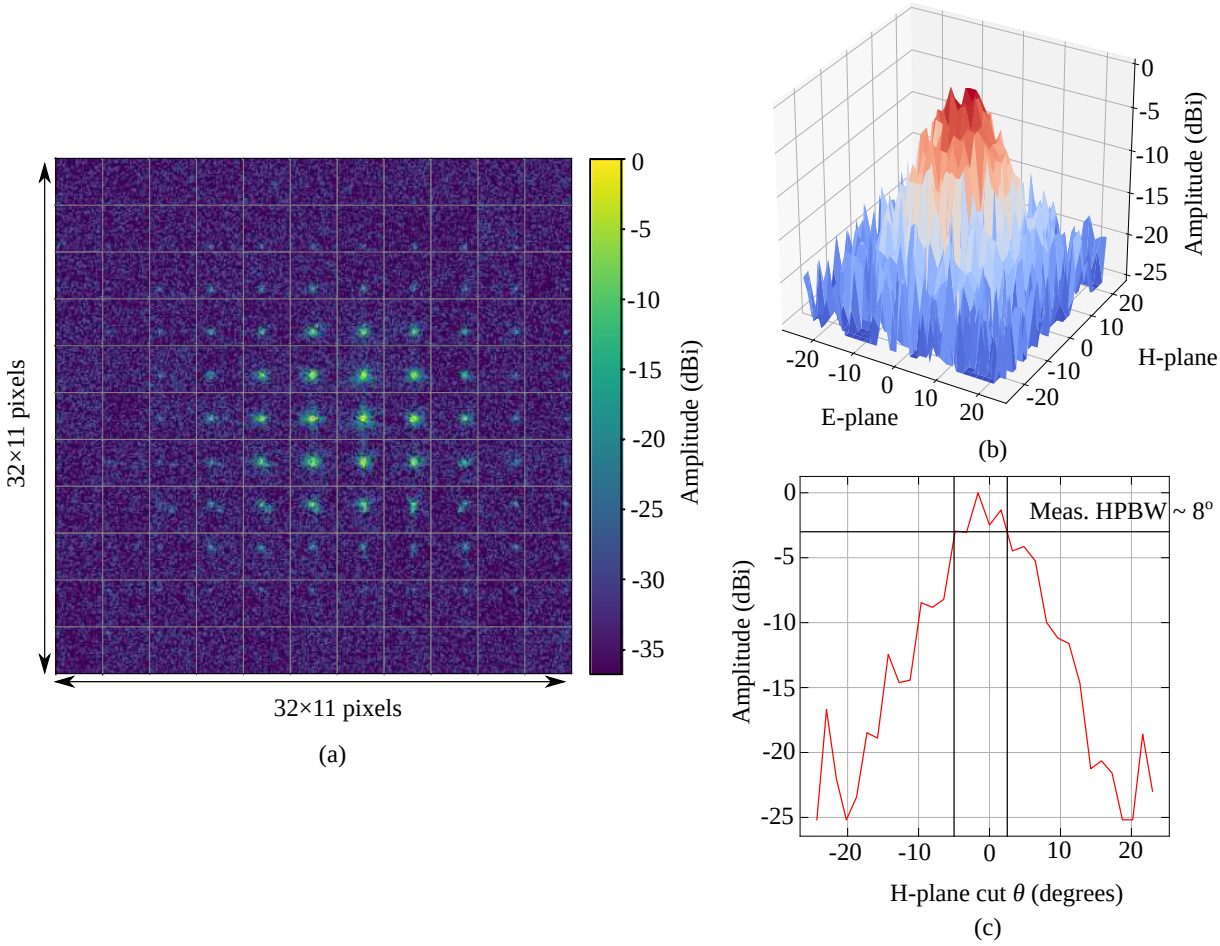


Figure 5.20: (a) Normalized raw light-field image data measured with setup in Fig. 5.19. (b) Reconstructed source antenna pattern using Eq. (5.1), and (c) One cross-section of the light-field reconstructed antenna pattern. Measured HPBW was 8° as compared to actual HPBW of 10°.

also integrates a chopped readout scheme and large bow-tie antennas which seem wideband as the NEP performance has been reported for two discrete frequency points 270 GHz and 600 GHz. The pixel size and the dc power consumption are around 9× and 13× larger than our camera respectively. The cameras in [115] and [189] integrated multiple on-chip ADCs in parallel, which results in a larger output complexity, while the camera in [179] does not integrate any on-chip digital readout. None of these cameras use an attached silicon lens, so they don't provide any light-field mapping in their packaged form unless accompanied by a bulky external dielectric lens. Therefore, while these designs implement several interesting readout innovations and record sensitivity numbers, they do not meet our design objectives related to the multi-chip THz light-field cameras.

The first two columns of Table 5.1 show the comparison between the second-generation, i.e. this camera SoC [47], and the first-generation camera [109] developed at IHCT. The new design manages a similar pixel count and chip area as the first-generation camera, while using a cheaper technology process. The operation frequency is reduced to the mid-THz band where

state-of-the-art silicon integrated THz sources are emerging. The new camera also integrates full digital readout on-chip, while off-chip ADC and amplifiers were required in the first-generation design. Note that the reported power consumption of 13.3 µW per pixel for our camera also takes into account its full digital readout scheme. The NEP has increased by 3× as compared to the first-generation design, which is an expected outcome of utilizing a cheaper process technology with longer transistor channels resulting into a larger noise.

Table 5.1: State-of-the-art in silicon integrated THz cameras. After [47] © 2020 IEEE.

	This work [47]	[109]	[115]	[179]	[189]
Technology	130nm CMOS	65nm CMOS	180nm CMOS	130nm CMOS	180nm CMOS
Array size	32×32	32×32	32×32	31×31	32×24
Pixel pitch	80µm×80µm	80µm×80µm	215µm×215µm	240µm×240µm	220µm×200µm
Power consumption	13.3µW/pix*.	2.5µW/pix.	4.5µW/pix.	174µW/pix.	–
Operation frequency	460–750 GHz**	790–960 GHz**	930 GHz	200 GHz, 270 GHz, 600 GHz	860 GHz
Antenna	Rectangular wire-loop	Ring	Patch	Bow-tie	Patch
On-chip gain	139 dBΩ + PGA 7–51 dB	50 dB	45 dB	31–71 dB	24 dB
NEP	36nW (int.) @ 653 GHz; 262 pW/Hz$^{0.5}$ @ 653 GHz, 40 kHz chopping	12nW (int.) @ 860 GHz; 100 pW/Hz$^{0.5}$ @ 860 GHz, 5 kHz chopping	91 pW/Hz$^{0.5}$ @ 930 GHz, 31 Hz chopping; 13.7 pW/Hz$^{0.5}$ @ 930 GHz, 100 kHz chopping	533 pW (int.) @ 270 GHz, 156 kHz chopping; 732 pW (int.) @ 600GHz, 156 kHz chopping	–
ADC	On-chip, 6b FADC	External	On-chip, 4×12b	External	On-chip, I-ADCs
Data interface	SPI	Analog	4×12b parallel	Analog	32 parallel I-ADCs
Readout chain	On-chip	External	On-chip	On-chip	On-chip
Operation mode	Continuous	Continuous	Chopped	Chopped	Continuous
Frame rate	25 fps	25 fps	400 fps	25–100 fps	25 fps
Optics	Silicon lens	Silicon lens	None	None	None
Light-field mapping	Yes	Yes	None	None	None

*Average including power consumption in the complete digital readout; ** 3 dB NEP bandwidth

5.7 Conclusions and future work

In this chapter, the design and characterization of a compact 1k-pixel broadband camera SoC was presented. The camera SoC is implemented in a low-cost 130nm CMOS process, and the chip architecture is aimed at multi-chip integration. The camera allows a full digital operation with a small pin-count package. A 3×3 multi-chip camera array consisting this SoC is presented in the next chapter.

The camera is specially designed to be used in all-silicon THz imaging systems, and therefore it is optimized for an optimum performance in the mid-THz band (0.4–0.7 THz) where state-of-the-art silicon integrated THz sources are emerging. A novel differential transimpedance based in-pixel readout was also discussed and demonstrated to solve the issue of moving offsets for CMOS based THz imagers.

The all-silicon, multi-chip light-field THz imagers henceforth enabled by this camera SoC are an ongoing area of research. Future cameras would continue to improve on the sensitivity and imaging speed. One interesting addition would be to incorporate a chopped readout along with a continuous one, so that the camera could be used in conjunction with the chopping frequency division multiplexing at the source-array.

Chapter 6

Multi-chip THz light-field camera

The necessity for multi-chip scaling has already been outlined in Sec. 2.3. In summary, multi-chip scaling represents an economic approach for improving the pixel count while efficiently handling the thermal and PVT variation bottlenecks for silicon integrated incoherent THz arrays. It is also necessary to provide the real-time spatio-directional sampling for THz light-field imaging.

6.1 Design objectives

While several approaches can be pursued for multi-chip scaling, all of them must be evaluated in terms of the following criteria:

1. **Packaging density:** The multi-chip integration must provide a close packaging of the ICs and the lenses (the macro-pixels) to allow a dense sampling of the spatio-directional light-field. On the flip side, a close packaging may also lead to an adverse mutual RF coupling between different ICs. However, such effects have not been studied so far.
2. **Precision alignment:** Since the light-field processing is based on geometrical models, an accurate placement of the lenses and the ICs at known positions becomes crucial for a correct calculation of the distances and the angles. Optimally, the packaging scheme must include some form of self-aligning or alignment guiding structures to help with this placement.
3. **Modular design:** The multi-chip integration must also be flexible enough to allow swapping (removal and insertion) of the individual macro-pixels. While this is not necessary, such modular design has inherent economic benefits. Also, the design approach should be scalable to accommodate different array sizes.
4. **Common interfaces:** The system comprising a multi-chip array must act as a single unit, i.e. it should provide a common interface for programming and data readout. Also, the dc biases should be shared among all the macro-pixels for the operational simplicity.

Along with these requirements, a low-cost packaging scheme is also desirable. For the source-arrays, some form of active or passive cooling must also be accommodated.

This chapter discusses the design of a multi-chip THz light-field camera, composed of a 3×3 array of individually lens-coupled THz camera SoCs (Chapter 5). The presented system is a realization of the multi-chip scaling that was envisaged in earlier in Fig. 2.7. A similar low-cost FR4 PCB based packaging can also be applied for designing multi-chip source-arrays, yet these may also present additional challenges related to the cooling and the large bias current requirements (Chapter 4).

6.2 Architecture and Implementation

Fig. 6.1 shows the system architecture for the presented multi-chip THz light-field camera. For a close packing, the camera SoC had to be assembled and wire-bonded over a lens-scale PCB. The signal and bias pads were castellated to create PCBs with such small form factors. The signals and biases were further routed on a separate 4-layer FR4 carrier PCB. The header pins on this board provided an alignment target for the lens-scale camera packages. The castellated camera PCBs were soldered on receptacles, which were in turn mounted on the header pins soldered on the carrier PCB. This ensued into a modular design with cold-swappable camera packages. The control logic was assembled on another FR4 PCB which consisted of an FPGA (Xilinx Spartan 6), with a commercially available breakout board providing a USB-C interface with FT232H USB-to-serial convertor IC. The 'SS1' and 'SS2' select signals on the camera SoC (see Fig. 5.1) were utilized to multiplex the array in a row-column format, thus reducing the IO requirements from the FPGA as shown explicitly in Fig. 6.1. The SPI interface was shared between all the SoCs. Note that this system clearly demonstrates the utility of integrated SPI into the camera and the source SoCs. Without such a shared interface, the IO connection requirements would quickly become unmanageable. The dc biases, shared among all the SoCs, were routed to on-board SMA connectors for attaching to the external supplies. In this whole scheme, the overall placement accuracy of the macro-pixels is expected to be within $100\,\mu\mathrm{m}$ which is limited by the dimensional tolerance of the PCB manufacturing process.

The lens-scale camera package, and the assembled multi-chip camera array, are shown in Fig. 6.2(a) and Fig. 6.2(b) respectively. The carrier PCB is $8\,\mathrm{cm}\times 8\,\mathrm{cm}$ large, and the lens-to-lens pitch is around $1.7\,\mathrm{cm}$. This is slightly larger than the lens diameter of $1.5\,\mathrm{cm}$ to allow space for soldering. Overall, the multi-chip array consists of about nine thousand imaging pixels.

6.3 Imaging demonstration

The camera array was used for a real-time imaging demonstration. The setup is shown in Fig. 6.3. The camera was placed in front of a $0.65\,\mathrm{THz}$ CW AMC source, and the light-field image data was streamed out in form of a video at a frame-rate of 4 fps. The imaging speed was limited by the controller implementation – individual commands were sent in sequence from a Python

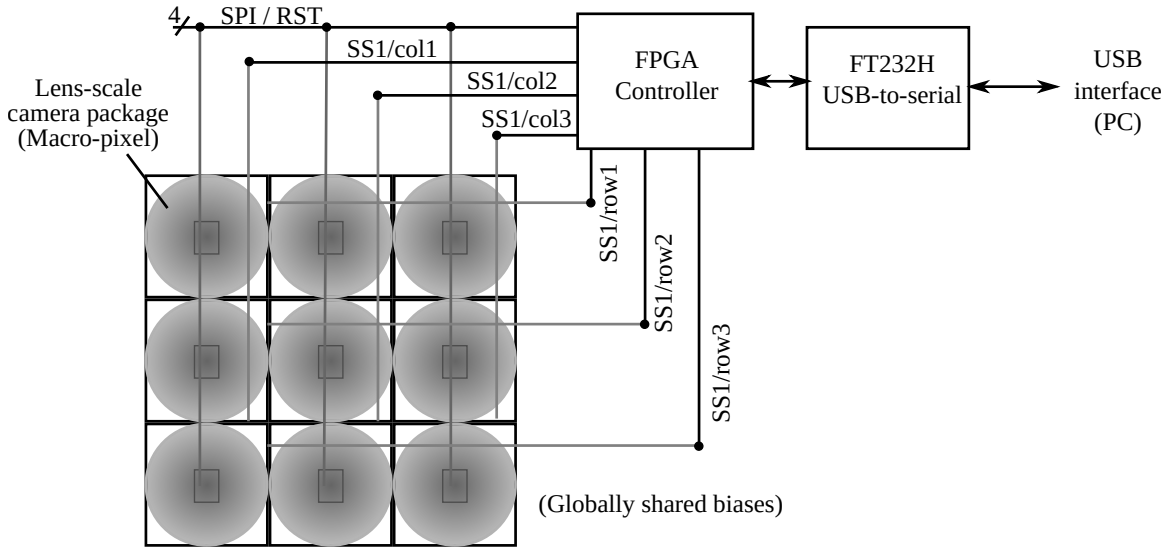
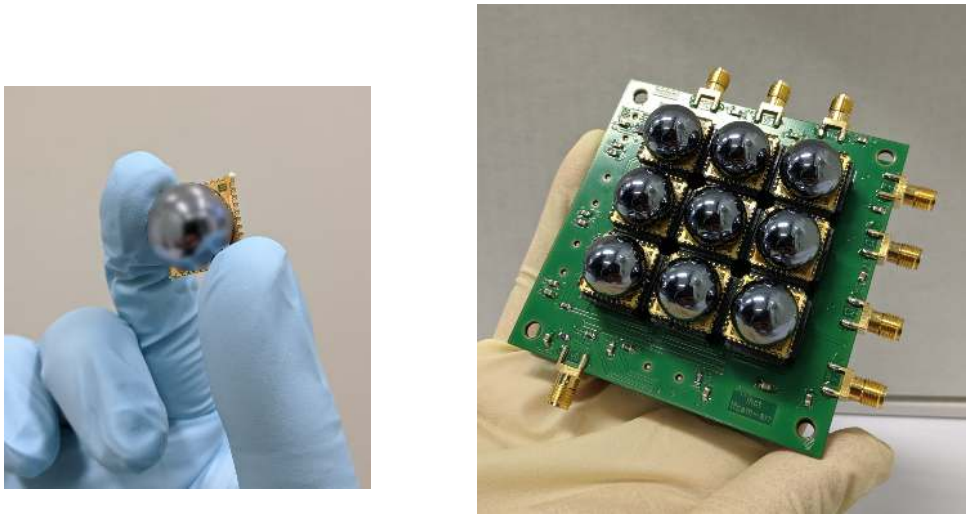


Figure 6.1: System architecture for a THz light-field camera composed of 3×3 multi-chip array of the THz camera SoC presented in Chapter 5.



(a) (b)

Figure 6.2: (a) Lens-scale camera package, and (b) multi-chip light-field camera module consisting a 3×3 array of lens-scaled packages assembled over a carrier PCB. SMA connectors are used for supplying the dc biases externally.

code on the PC to trigger the data acquisition from each camera. In this mode, each camera operates at around 36 fps, and therefore, nine cameras can be read out at an aggregate of 4 fps. The control logic on the FPGA can be optimized for an even faster readout. The fastest imaging speed of 90 fps was observed for a single camera, which should result in 10 fps imaging speed for the light-field camera array. Ultimately, due to a serial readout, the net imaging speed would always degrade when larger number of camera SoCs are added into the array. This can be circumvented by a selective readout of the most interesting pixels from the camera array. Such a logic can be implemented in the FPGA controller itself. Note that the light-field image dataset acquired from the setup in Fig. 6.3 will not be subjected to any quantitative investigations in

this chapter, as any such analysis proved premature at the time of writing this dissertation. The multi-chip THz light-field camera presents an entirely new capability of real-time THz light-field imaging, that was not available at the THz frequencies previously. Currently, ongoing efforts are focused towards effectively utilizing this camera for novel THz imaging applications.

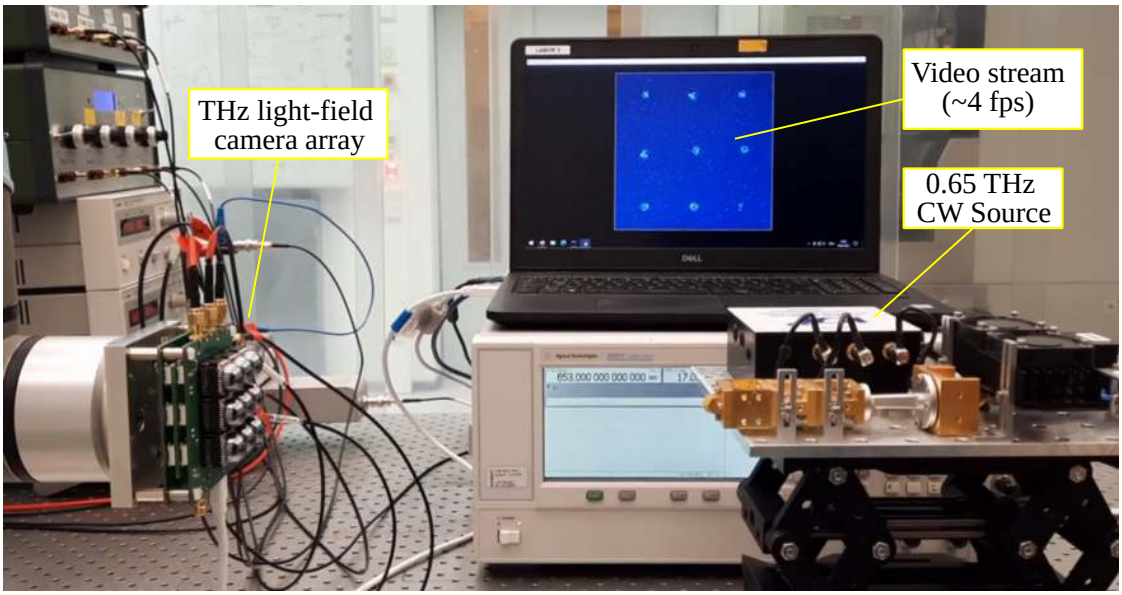


Figure 6.3: THz light-field camera array in operation, with 3×3×32×32 pixel video stream at 4 fps showing the mapped radiation pattern from a 0.65 THz source.

Chapter 7

Summary and Outlook

This thesis started with a discussion on THz imaging in general. Looking at the current state of THz systems and applications, a case was presented for developing incoherent, compact, and low-power silicon-integrated THz components, and the light-field methodology was proposed as a mean to achieve 3D THz see-through imaging. After this, we looked at the challenges and opportunities offered by the commercial silicon process technology for the THz systems. In these discussions, we looked at several approaches that are used to design THz sources and detectors. These approaches were particularly scrutinized for the implementation of integrated pixel arrays, concluding into the observation that unlocked THz source-arrays and direct power detectors are the best circuit candidates for this use case. The incoherent arrays, along with an attached silicon lens, inherently provide a directional or angular sampling. Building upon this, a multi-chip scaling approach was discussed as the practical, scalable, and cost-effective mean for creating spatio-directional THz arrays for light-field imaging.

The idea of light-field imaging was also comprehensively explored. The literature survey provides ample examples for visible-light light-field imaging, along with a handful of reports on the IR and the X-ray light-fields. However, THz light-field imaging was never explored in the past. We outlined the key challenges expected during the development of such approach. The mathematical and conceptual formulations for light-fields, available from the literature in form of the 4D plenoptic function and the rayspace diagrams, were discussed afresh from the perspective of THz radiation and quasi-optics. The THz light-field imaging, both in the transmission and the reflection mode, was actually demonstrated with a scanning-based imaging setup. These experiments yielded several important advantages of the THz light-fields that proved crucial for the demonstrated applications. Ultimately, radar like imaging was also demonstrated where the 3D surface profile of a physical object was quantitatively reconstructed from the incoherent THz light-fields without requiring any RF phase information.

Thereafter, we discussed the design of an 8×8 pixel $0.42\,\mathrm{THz}$ source-array SoC and a 32×32 pixel broadband THz camera SoC. Both have been designed to allow multi-chip scaling. The source-array SoC provides a record radiation power with a high integration density. While it

was specifically designed for THz single pixel cameras, the smart functionality incorporated in the form of fast spatial modulation, chopping FDM, and in-pixel BIST based calibration, is also useful for a range of THz imaging applications, including THz light-field imaging. The THz camera SoC is the first ever fully-digital silicon-integrated THz camera, also with the most compact form factor and the lowest dc power consumption. The camera SoC was implemented in a low-cost CMOS process technology, and the RF operation bandwidth was optimized to match the radiation frequency range of the existing and upcoming silicon-integrated THz sources. The novel in-pixel readout also serves as a major enabler for the digital SoC form factor as it allows a fixed dc pixel offset in the favor of a large on-chip baseband signal amplification. Leveraging on the SoC architecture, a multi-chip THz light-field camera array composed of 3×3 arrangement of the camera SoCs, was also designed and demonstrated.

It is now the first time that dedicated components have become available for silicon integrated THz light-field imaging. Several system-level challenges do remain. However, the hardware developed in this work will serve as the crucial foundation for building and testing new setups and ideas. Science and technology are nothing but a series of incremental improvements occasionally triggered by disruptive notions. We believe THz light-field imaging is one such disruptive approach, and now that the fundamental analysis, experiments, and hardware are available, the next steps would involve designing fully-fledged, real-time THz light-field imaging systems.

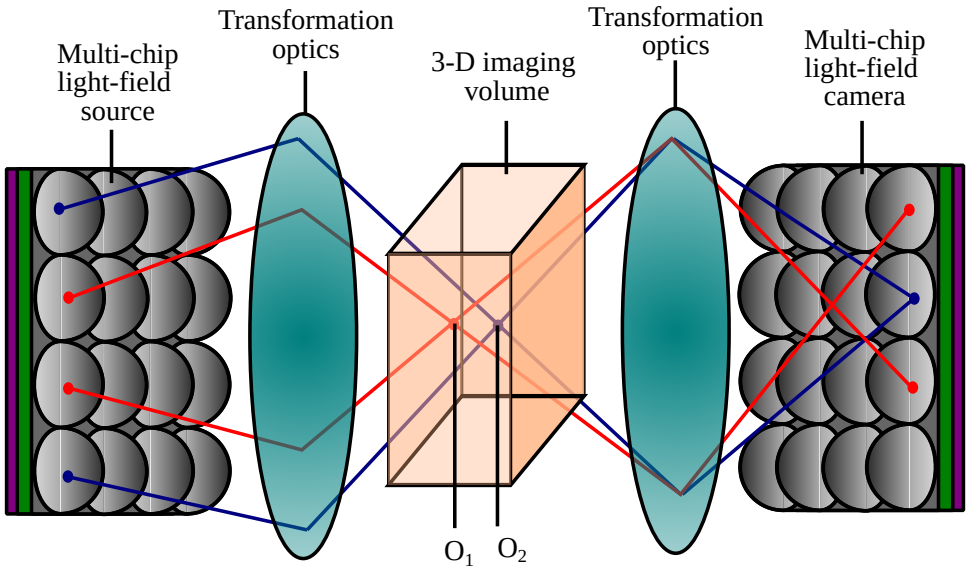


Figure 7.1: A THz MIMO light-field imager. All pixels at source provide an angular diversity while all pixels at camera provide a spatial diversity or vice-versa.

One important idea for such systems is that of THz MIMO light-fields. This was conceptualized alongside the development of multi-chip camera array. While a multi-chip system aims to increase the pixel count of either the source or the camera, such increment is still a linear function of the number of integrated chips. A limited number of pixels also restrict the achievable spatio-directional resolution for THz light-field imaging. For example, a system with nine 32×32

pixel THz cameras would have maximum 9216 pixels, with 9 pixels providing angular resolution and 1024-pixels providing spatial resolution or vice-versa. Similarly, a system with nine 8×8 pixels source-array would have 576 pixels in aggregate, with 64 pixel spatial resolution with 9 pixel angular resolution or vice-versa. The angular and spatial spaces can be interchanged using an objective lens.

A much larger spatio-directional pixel count is needed for realistic 3D imaging applications. For this, a THz MIMO light-field imaging system approach is proposed as shown in Fig. 7.1. It leverages the availability of spatio-directional fields at both the multi-chip source and the multi-chip camera arrays. With appropriate transformation optics, all pixels at the source multi-chip array can be used to provide the angular diversity, while all pixels at the camera array can be used for the spatial diversity, effectively boosting up the overall pixel count. Nine 64-pixel source arrays with nine 1k-pixel THz cameras would provide a total 5.3 million pixels at THz. This may correspond to 576 pixels angular resolution and 9k-pixel spatial resolution at each angular projection, or all 5.3 megapixels may be used in a 2D image. For THz MIMO light-fields, all camera pixels must capture each source pixel. The source pixels must be encoded in a different basis that is identifiable at the output of camera pixels. The source-array SoC readily allows encoding the pixel radiation in the form of a spatial or chopping multiplexing. Only the former is suitable for the presented camera SoC as its readout cannot capture and distinguish a chopped radiation. Such system-level research, along with further dedicated enhancement of the THz source-array and camera SoCs, remain some promising research directions for the future.

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