FACHBEREICH MATHEMATIK UND NATURWISSENSCHAFTEN
FACHGRUPPE PHYSIK
BERGISCHE UNIVERSITÄT WUPPERTAL

Studies on the Optical Readout for the ATLAS Pixel Detector

Systematical Studies on the Functions of the Back of Crate Card and the Timing of the Pixel Detector

Dissertation zur Erlangung des Doktorgrades

vorgelegt von
Tobias Flick

Juli 2006
WUB-DIS 2006-05

Überblick

Am europäischen Kernforschungszentrum CERN in Genf wird derzeit der Large Hadron Collider gebaut. An diesem Beschleuniger werden vier Experimente aufgebaut. Das größte wird das ATLAS Experiment sein. Der innerste Subdetektor des ATLAS Experimentes ist ein Silizium Pixel Detektor. Dieser Detektorteil wird über 80 000 000 Kanäle aufweisen, die mittels einer optischen Datenübertragungsstrecke kontrolliert und ausgelesen werden. Am detektorseitigen Ende dieser optischen Übertragungsstrecke wird ein Optoboard plaziert sein, das andere Ende im Kontrollraum bildet die Back of Crate Karte. Auf dieser Back of Crate Karte findet außer den opto-elektrischen Wandlung auch die komplette Justage des Zeitverhaltens des Pixel Detektors und seiner Auslese statt.

In dieser Arbeit wurde die Funktionalität der Back of Crate Karte in verschiedenen Testszenarien wie Produktionstests, Systemtests und Teststrahlaufbauten untersucht. Neben der Qualitätssicherung während der Produktion und dem Test der Funktion der Karte wurde entsprechenden Steuersoftware entwickelt und getestet.

In einem Teststrahlaufbau wurde die Back of Crate Karte mit dem Datennahmesystem integriert und unter ähnlichen Bedigungen wie später im ATLAS Experiment die Kontrolle des Zeitverhaltens und deren Auswirkung auf die Datennahme studiert.

Contents

Introduction

The particle physics is concentrating on the research of the structure of the matter which is observable in our world. How is this world built. Which particles exist, which are necessary to build up the world? How is this matter kept together, what are the interactions between the known particles?

The answers to these questions are obtained by observing the known particles, to study their properties, and to search new for particles. Models are developed to describe all the observations. Experiments are performed to proove the models. The best prooven model to describe many of the observations is the Standard Model. The Standard Model is elucidated in Chapter 1.1. It is tested very precisely by experimental measurements in the last years, but cannot explain all phenomena of nature. To discover the last not observed particle of the Standard Model, the Higgs boson, and to extend the model further experiments are needed.

To study the elementary particles machines and instruments are necessary to produce and measure the particles and their properties. In the last 50 years an enormous effort has been made to develop new machines to produce particles at always higher rates and energies. The more massive the particles are the more energy is needed to produce them. To increase the machine energy drives the physicists and engineers to develop new machines and experimental instruments.

The newest machine will be the Large Hadron Collider which is under construction at CERN in Geneva and will start operation in 2007. This machine accelerates protons in a ring to an energy of 7 TeV in opposite directions. These protons will collide at four interaction points. Here experiments will be installed to measure the products of the collisions: ALICE, ATLAS, CMS, and LHC-b.
The ATLAS experiment is the largest experiment. It is described in Chapter 2. This work has been done as a part of the development of the innermost subdetector of the ATLAS detector, the pixel detector. The pixel detector and its readout is explained in Chapter 3.

The steering and the data readout of the more than 80 000 000 channels of the pixel detector is performed through an optical data transmission line, the optical link. This optical link and espacially its off-detector interface, the Back of Crate card, is the central topic of this thesis.

The Back of Crate card has been studied in its function and its operation performance in

detail for this work. The card has been examined starting with the production (see Chapter 5), introducing it into system tests (see Chapter 6), and operating the card in a test beam experiment very similar to the final ATLAS experimental usage (see Chapter 7).

One important task of the Back of Crate card is the adoption of the timing for the pixel detector and its readout. The timing functionality of the pixel detector was studied for the first time in a real experimental environment using traversing particles in the test beam experiment. The behaviour of the Back of Crate card and the results for the test beam study promise a good performance in the final ATLAS experiment.

Finally this work and the results are summerised and an outlook to the forthcoming tasks is given.

Chapter 1

Top Quark Physics at ATLAS and LHC

1.1 The Standard Model

> ”The theories and discoveries of thousands of physicists over the past century have created a remarkable picture of the fundamental structure of matter: the Standard Model of Particles and Forces.” [1]

The Standard Model describes how the matter in our world is built up from small particles and held together by fundamental forces. It requires 12 matter particles and 4 force carrier particles to summarise all that we currently know about the most fundamental constituents of matter and their interactions, as they are described below.

1.1.1 Matter Particles

There are two kinds of matter particles – the quarks and the leptons – both point-like and apparently without internal structure.

There are six quarks, which are usually grouped in three pairs because of their mass and charge properties: up/down, charm/strange, and top/bottom.

There are six leptons, three with electrical charge – electron (e^-), muon (μ^-), and tau (τ^-) – and three electrically neutral ones – electron neutrino (ν_e), muon neutrino (ν_μ), and tau neutrino (ν_τ). While the charged leptons have a clear mass hierarchy, the electron is the lightest and the tau the heaviest, the mass hierarchy of the neutrinos is not well known up to now.

The e^-, the ν_e, the up quark, and the down quark are all that is needed to build up the stable matter in the Universe. They make up what is called the first generation of particles. But they are not all that was needed to build up the Universe; high energy processes produce a large variety of short-lived particles which exist because of the existence of ”heavier” particles. These are the muon and muon neutrino, the charm quark and strange quark,

Leptons	**1. Generation**		**2. Generation**		**3. Generation**	
Name	ν_e	e^-	ν_μ	μ^-	ν_τ	τ^-
el. charge $[e]$	0	-1	0	-1	0	-1
mass [MeV/c^2]	$< 3 \cdot 10^{-6}$	0.511	< 0.19	105.7	< 18.2	1777
Interactions	weak gravity	weak, em, gravity	weak gravity	weak, em, gravity	weak gravity	weak, em, gravity
Quarks	**1. Generation**		**2. Generation**		**3. Generation**	
Name	up	down	charm	strange	top	bottom
el. charge $[e]$	$2/3$	$-1/3$	$2/3$	$-1/3$	$2/3$	$-1/3$
mass [MeV/c^2]	$1-5$	$3-9$	1150 -1350	$75-170$	~ 175000	4000 -4400
Interactions	weak, electromagnetic, strong, gravity					

Table 1.1: The elementary particles known from the Standard Model. Leptons and quarks are sorted into three generations. The basic properties and the interactions of the particles are given, too [2].

which make up the second generation, and the tau and tau neutrino and the top quark and bottom quark, comprising the third generation.

Recent results from the LEP collider at CERN measuring the Z resonance have confirmed that the number of light neutrino species and therefore the number of generations is 3. The peak cross section of the Z resonance to any detectable final state f is sensitive to the number of neutrino species. It can be expressed through [3]:

$$\sigma_f^{peak} = \frac{12\pi}{M_Z^2}\frac{\Gamma_{ee}\Gamma_f}{\Gamma_Z^2}(1-\delta_{had}) \tag{1.1}$$

with

$$\Gamma_Z = N_\nu\Gamma_\nu + 3\Gamma_{ee} + \Gamma_{had} \tag{1.2}$$

Γ_x is the width of the decay into the state x. δ_{had} is the QED initial state radiative correction. It has been calculated to an accuracy better than 0.5%. This gave the possibility to fit the measured peak cross section with only N_ν and M_Z as free parameters. The result is $N_\nu = 2.9841 \pm 0.0083$ [4]. Thus the number of generations has been confirmed experimentally.

All second and third generation particles – apart from the neutrinos – are unstable and quickly decay into stable particles of the first generation. All the stable matter we observe today is formed by these first generation particles.

1.1.2 The Four Fundamental Forces

Fundamental particles bind together to form structures on all scales, from the proton built from three quarks, through atoms and molecules, liquids and solids, to the huge conglomerations of matter in stars and galaxies. They do this through four basic interactions, the forces.

The most familiar basic force is *gravity*, because it is well known from macroscopic effects. It keeps our feet on the ground and the planets in motion around the sun. On individual particles, though, the effects of gravity are extremely small. Only for matter in bulk does gravity dominate.

A much stronger fundamental force is the *electromagnetic* force, which manifests itself in the effects of electricity and magnetism. The electromagnetic force binds negative electrons to the positive nuclei in atoms, and underlies the interactions between atoms that give rise to molecules and to solids and liquids. Unlike gravity, it can produce both attractive and repulsive effects. Opposite electric charges (positive and negative) and opposite magnetic poles (north and south) attract, but charges or poles of the same type repel each other.

When looking inside atomic nuclei and at even smaller structures (inside nucleons), two unfamiliar forces come into play: the weak force and the strong force. The *weak* force leads, e.g., to the decay of neutrons and allows the conversion of a proton into a neutron (responsible for hydrogen burning in the centre of stars).

The *strong* force holds quarks together within protons, neutrons, and other particles. It also prevents the protons in the nucleus from flying apart under the influence of the repulsive electrical force between them. This is because within the nucleus, the strong force is about 100 times stronger than the electromagnetic one.

The strong force is quite special: it becomes stronger with distance. The quarks bound within particles, for instance, never appear alone; as you try to pull them apart, the force becomes stronger! This is unlike the more familiar effects of gravity and electromagnetism, where the forces become weaker with distance. The increase of the strength with distance is due to the self interaction of the exchange particles of the strong force, the gluons.

Force Carrier Particles

The standard model includes three types of forces acting among particles: strong, weak, and electromagnetic. Gravity is not yet part of the framework, but because its strength is several orders of magnitude smaller than the strength of the other forces it can be neglected to a good approximation (see Table 1.2).

The forces are communicated between particles by the exchange of special force carrying particles called bosons, which carry discrete amounts of energy from one particle to an-

Interaction / Force	**force carrier particles**	**Coupling**	**Strength (relative)**
strong force	8 gluons (g)	colour	1
weak force	W^+, W^-, Z^0	weak charge	$3 \cdot 10^{-1}$
electromagnetic force	photon (γ)	electrical charge	$7 \cdot 10^{-2}$
gravity force	graviton(?)	mass	10^{-43}

Table 1.2: The four fundamental forces and their force carrier particles [5].

other. Each force has its own characteristic bosons: the gluons (strong force), the photon (electromagnetic force), the $W^{\pm}$ and Z^0 bosons (weak force). For gravity the postulated exchange particle, the graviton, has not yet been observed.

A big success of the Standard Model is the unification of the electromagnetic and the weak forces into the electroweak force. This achievement is comparable to the unification of the electric and the magnetic forces into a single electromagnetic theory by J.C. Maxwell in the 19th century.

The Electromagnetic Interaction

The electromagnetic interaction is described by a gauge theory, Quantum Electrodynamics (QED). This force acts on every electrically charged particle. The equation of motion is the Dirac-Equation. It is valid for spin $\frac{1}{2}$ particles, the fermions. The Lagrange density is [6]:

$$\mathcal{L}_{QED} = i\bar{\Psi}\gamma^{\mu}D_{\mu}\Psi - m\bar{\Psi}\Psi - \frac{1}{4}F_{\mu\nu}F^{\mu\nu} \tag{1.3}$$

with:

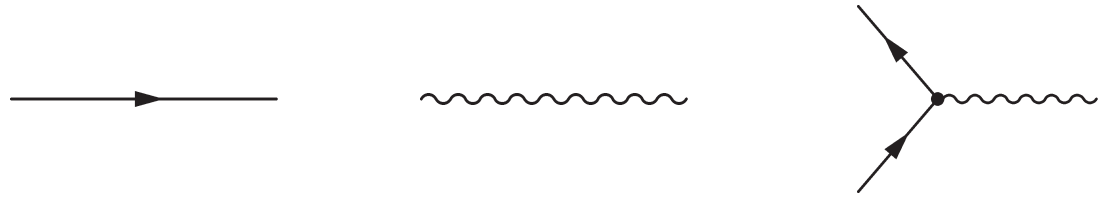
$$D_{\mu} = \partial_{\mu} - ieA_{\mu}(x) \tag{1.4}$$

the covariant derivative due to the local phase invariance [6]. And:

$$F_{\mu\nu} = (\partial_{\mu}A_{\nu} - \partial_{\nu}A_{\mu}) \tag{1.5}$$

which is the tensor of the strength of the field and describes the propagating field A^{μ}, which is to be identified with the photon as the exchange particle [6].

The subparts of this equation can be illustrated by Feynman diagrams following the Feynman rules: Terms which are quadratic in Ψ describe the propagators of the fermions (Figure 1.1(a)); terms quadratic in A describe the propagator of the photon, which is the exchange particle (Figure 1.1(b)); and terms quadratic in Ψ and linear in A describe the interaction between fermions and the photon (Figure 1.1(c)).



(a) (b) (c)

Figure 1.1: Fundamental Feynman graphs of QED: a) Fermion propagator, b) Photon propagator, c) Interaction vertex

The coupling constant for the electromagnetic interaction is α_{QED}, which is:

$$\alpha_{QED} = \frac{e^2}{4\pi\epsilon\hbar c} \simeq \frac{1}{137} \tag{1.6}$$

The Weak Interaction

The weak force acts on all particles. Neutrinos interact only through the weak interaction. The three exchange particles, the gauge bosons $W^{\pm}$ and Z^0, are massive particles. The mass of the W's is [2]

$$m_W = (80.419 \pm 0.056)\ \text{GeV}/c^2$$

and the mass of the Z is

$$m_Z = (91.1882 \pm 0.0022)\ \text{GeV}/c^2.$$

Because of their massiveness, the lifetimes of the gauge bosons are small. The small lifetimes of the force carrier particles are responsible for the short distance of the weak interaction.

Electroweak Unification

The electromagnetic and the weak interaction can be described through one theory, the electroweak theory. It is based on the group $SU(2) \otimes U(1)$. The invariance of the local gauge transformation leads to four gauge bosons: W^1, W^2, W^3 (from the SU(2)) and B (for the $U(1)$). W^1 and W^2 interact to form the gauge bosons W^+ and W^- through [6]:

$$W^{\pm}_{\mu} = \frac{1}{\sqrt{2}}(W^1_{\mu} \mp iW^2_{\mu}) \tag{1.7}$$

The combinations of the other gauge bosons W^3 and B:

$$Z_{\mu} = \cos\Theta_W W^3\mu - \sin\Theta_W B_{\mu} \tag{1.8}$$

$$A_\mu = \sin\Theta_W W_\mu^3 + \cos\Theta_W B_\mu \tag{1.9}$$

lead to the exchange particles Z^0 and γ (A_μ). The angle Θ_W is known as the Weinberg angle.

Spontaneous symmetry breaking introduces the mass of the W- and Z-bosons while the photon stays massless. Weinberg and Salam defined a weak isospin doublet:

$$\Phi(x) = \frac{1}{\sqrt{2}} \begin{pmatrix} \Phi^+ \\ \Phi^- \end{pmatrix} \tag{1.10}$$

The gauge bosons of the electroweak interaction couple to this field. This is the Higgs mechanism and gives a mass to the W- and Z-bosons. Additionally, it postulates a neutral scalar Higgs-particle H^0, which remains after the symmetry breaking. This Higgs particle is the only remaining particle of the Standard Model which has not yet been observed. The measurements at LEP have established a lower boundary for the Higgs boson mass of $m_H = 114.4\,GeV/c^2$ with a confidence level of 95% [7].

The Strong Interaction

The strong interaction is described by the Quantum Chromodynamics (QCD). It is based on the symmetry group $SU(3)$ which has 3 parameters, the three colours. The colours are defined as red, green, and blue. The exchange particles of the QCD are 8 gluons. They couple to the colours. The strong interaction only affects the quarks (q), carrying a colour, the antiquarks ($\bar{q}$), carrying an anticolour, and the gluons (g), carrying a colour and an anticolour. The necessity of this additional degree of freedom, colour, became obvious from the observation of the Δ^{++} particle, which is formed by three quarks of the same type (u-quarks). This seemed to be a violation of the Pauli principle. The solution for this problem is the introduction of colour for the quarks, so that the three up-quarks are different in colour. The observed particles – baryons (qqq) or mesons ($q\bar{q}$) – are always colour neutral. Baryons are comprised of 3 quarks, which each have a different colour. Mesons are built up from a quark and an antiquark, where the antiquark carries the anticolour of the quark. By experimental measurements the number of colours has been determined to be three, by measuring the R-ratio:

$$R = \frac{(e^+e^- \to q\bar{q})}{(e^+e^- \to \mu^+\mu^-)} \tag{1.11}$$

R is proportional to the numbers of colours and is measured as:

$$R = 3\sum_q e_q^2 \tag{1.12}$$

This result manifests the existence of the 3 colours.

The QCD is described by the Lagrangian:

$$\mathcal{L}_{QCD} = \bar{\Psi}(i\gamma^{\mu}\partial_{\mu} - m)\Psi - g_s \sum_a (\bar{\Psi}\gamma^{\mu}T_a\Psi)G^a_{\mu} - \frac{1}{4}\sum_a G^a_{\mu\nu}G^{\mu\nu}_a \tag{1.13}$$

where g_s is the coupling constant and T_a the fundamental description of $SU(3)$, with a representing the eight generators of $SU(3)$. The G^a_{μ} describe the gluons as gauge fields. Therefore, there are again two propagator Feynman graphs (Figures 1.2(a) and 1.2(b)), and the interaction vertex (Figure 1.2(c)). Because the gluons have colour and anticolour they can interact with each other. The 3-gluon self-coupling is shown in Figure 1.2(d). Through this self-coupling the strength of the force grows with distance, prohibiting the observation of free quarks.

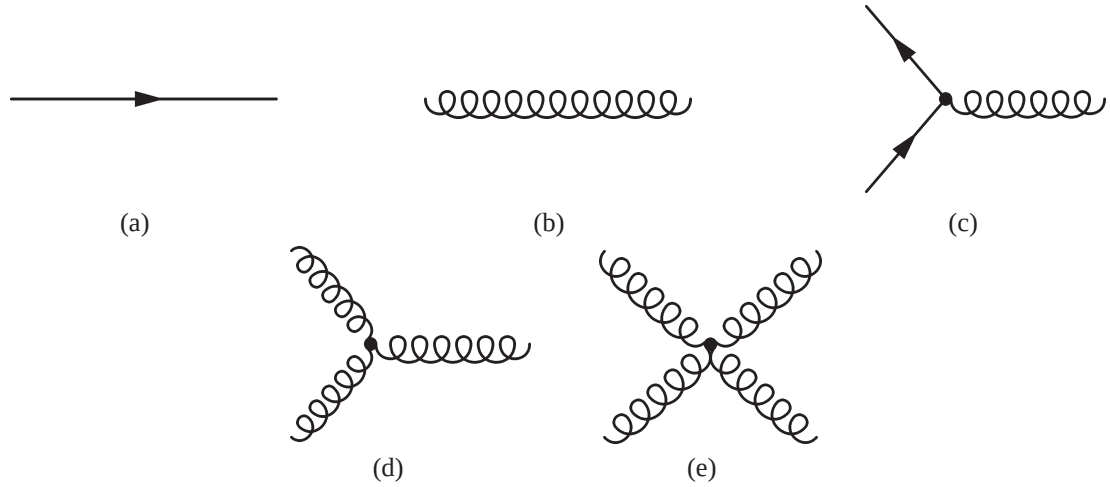


Figure 1.2: Fundamental Feynman graphs of QCD: a) Quark propagator, b) Gluon propagator, c) Interaction vertex, d) and e) Gluon self-coupling

The Cabibbo-Kobayashi-Maskawa Quark-Mixing Matrix

The quark mass eigenstates are not the same as the weak eigenstates. The mixing matrix relating these bases has been parametrised by Kobayashi and Maskawa in 1973 [8]. It is defined for six quarks. By convention, the mixing is often expressed in terms of a 3×3 unitary matrix V operating on the charge $-\frac{e}{3}$ quark mass eigenstates (d, s, and b) [9]:

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \tag{1.14}$$

The values of individual matrix elements can in principle all be determined from weak decays of the relevant quarks, or, in some cases, from deep inelastic neutrino scattering.

Using certain contraints at the tree-level discussed in [9] together with unitarity, and assuming only three generations, the 90% confidence limits on the magnitude of the elements of the complete matrix are

$$\begin{pmatrix} 0.9739 \text{ to } 0.9751 & 0.221 \text{ to } 0.227 & 0.0029 \text{ to } 0.0045 \\ 0.221 \text{ to } 0.227 & 0.9730 \text{ to } 0.9744 & 0.039 \text{ to } 0.044 \\ 0.0048 \text{ to } 0.014 & 0.037 \text{ to } 0.043 & 0.9990 \text{ to } 0.9992 \end{pmatrix} \tag{1.15}$$

The ranges shown are for the individual matrix elements. The constraints of unitarity connect different elements, so choosing a specific value for one element restricts the range of others.

1.1.3 But...

The Standard Model is by now a well-tested physics theory, used to explain and precisely predict a vast variety of phenomena. High-precision experiments have repeatedly verified subtle predicted effects. It is currently the best description we have of the world of quarks and other particles.

Nevertheless, physicists know that it cannot be the end of the story, because it cannot give answers to all questions. Some unresolved questions are:

- What's the origin of the mass of particles? Is the Higgs boson of Standard Model type or an extension?
- Can the electroweak and the strong forces be unified?
- What is "Dark Matter"?
- Why are there three generations of matter and where did antimatter go?

Such questions also relate to current mysteries about the Universe: "Is there more to the Universe than meets the eye? Why does matter dominate antimatter?" Obviously, there are still missing pieces and other challenges for future research to resolve, and that's why physicists search for *new physics beyond the Standard Model*, that will lead towards a complete *"theory of everything"*. And to do this new machines like the LHC with new experiments like ATLAS are necessary [1].

1.2 Proton-Proton Scattering

The collision of protons differs from the collision of electrons and positrons. Protons are not elementary particles but consist of quarks and gluons. The quarks are kept together

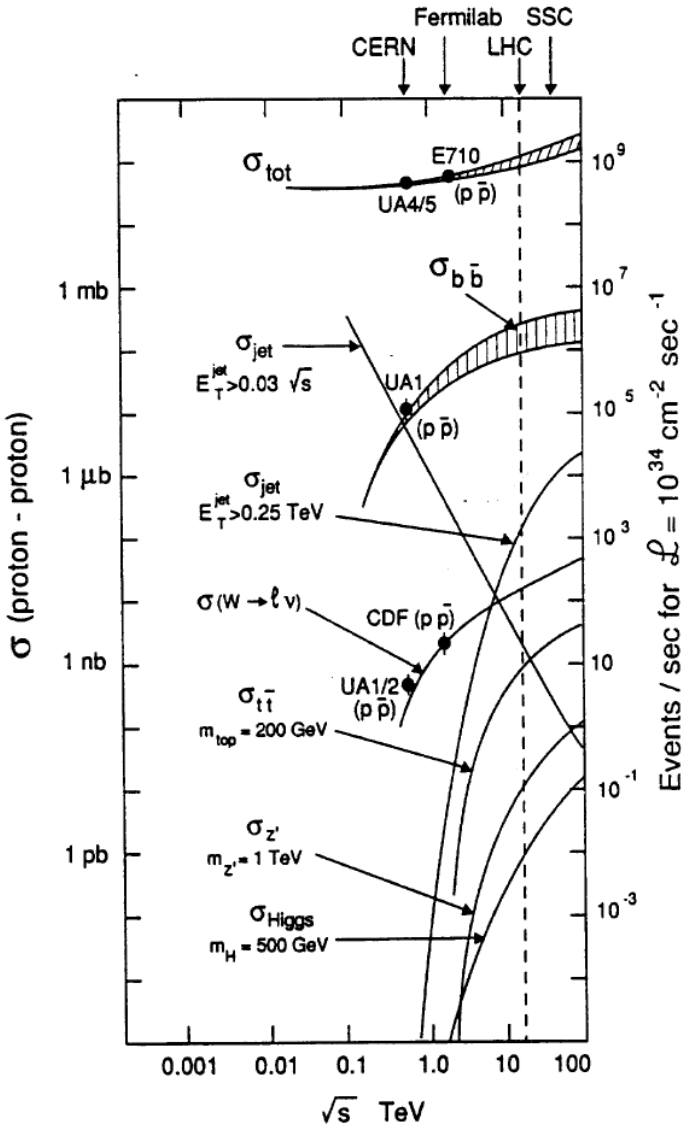


Figure 1.3: Energy dependence of some characteristic cross-sections from present colliders to the LHC [10].

by the strong force. The force carrier particles of the strong force are the gluons. These gluons may produce a virtual quark antiquark pair, the seaquarks. In collisions with a large energy transfer the quarks or gluons interact with each other. This implies that only the fraction of the centre of mass energy of the two protons which is taken by the interaction partners affects the collision. The momentum of the partons can be described as fraction of the proton momentum by the Bjorken variable x:

$$\sum_i \int dx x f_i(x) = 1 \tag{1.16}$$

where $f_i(x)$ is the parton density function (PDF). It is a measured function which depends also on the scattering energy. With its help the total cross section of the proton proton scattering can be calculated:

$$\sigma(S) = \sum_{i,j} \int_0^1 dx_i \int_0^1 dx_j f_i(x_i) f_j(x_j) \sigma_{ij}(S, \alpha_s) \tag{1.17}$$

Here $\sigma_{ij}(S, \alpha_s)$ is the cross section of the parton parton scattering, α_s is the coupling constant of the strong interaction, and $\sqrt{S}$ is the centre of mass energy. The total proton proton cross section depending on the centre of mass energy is shown in Figure 1.3.

The total cross section at LHC is about 100 mb. At the design luminosity (see next chapter) of $L = 10^{34} cm^{-2} s^{-2}$ there will be 10^9 collisions per second. The rate of $t\bar{t}$ pair production will be ten events per second and the Higgs boson will be produced with a rate of 0.02 events per second.

1.3 Top Quark Physics

The reasons for studying the top quark are numerous. The top quark is the heaviest fundamental particle. Its mass is an important parameter in the standard model. The top quark mass is related to the mass of the W boson, m_W, and the Higgs boson m_H through electroweak measurements. Precise measurements of the top quarks mass and the W mass provide constraints on the mass of the Higgs particle. The top quark is also of interest because its lifetime of $10^{-24}\, s$ is so short that the top will not hadronize before decaying. This gives a chance to study properties of a bare quark which are transported through the decay products.
The top quark was discovered in 1995 with the proton-antiproton collider Tevatron[a] at the Fermilab in the USA. Its mass is $m_t = 174.3 \pm 5.1\,\mathrm{GeV}/c^2$ and it carries a charge of $+2/3\, e$ [2]. The discovery took so long, because the colliders have to deliver the double of the top quarks resting mass to produce a top pair.

1.3.1 Top Quark Production

The top quark can be produced in pairs or singly. At LHC the production of the top quark will mainly happen by gluon-gluon fusion (in $\sim 87\%$ of the cases) while quark-antiquark annihilation will contribute with $\sim 13\%$. This is nearly opposite at Tevatron, because

[a] Tevatron is the main collider ring at the Fermilab in the USA

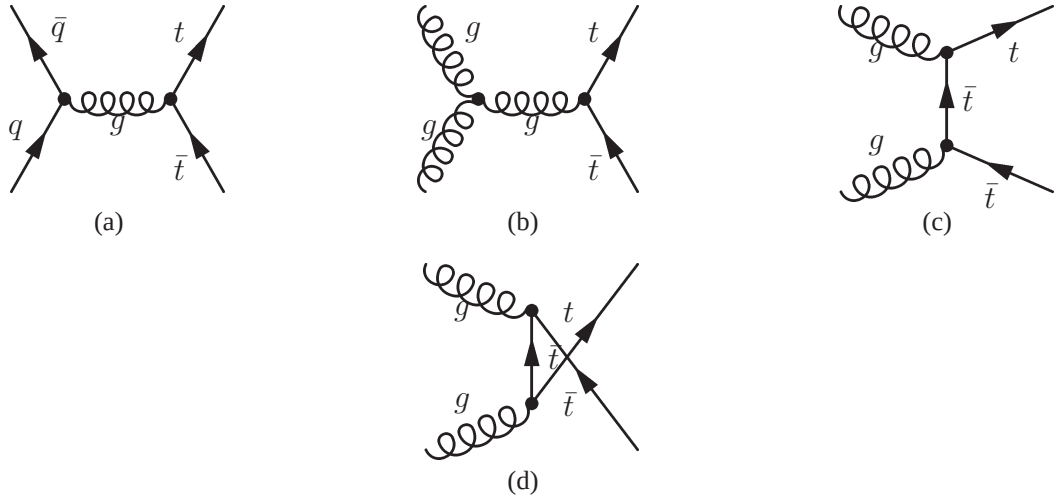


Figure 1.4: Main top quark production processes via strong interaction.

LHC collides protons and protons, while Tevatron collides antiprotons and protons at a lower energy. In Figure 1.4(a) the top-pair production through quark-antiquark annihilation is shown, while in Figure 1.4(b) the production by gluon fusion in the s-channel and in Figures1.4(c) and 1.4(d) the production by gluon fusion in the t-channel is presented. For single top production be referenced to the literature.
The cross section for $t\bar{t}$-production at the Large Hadron Collider (LHC) will be $\sigma_{t\bar{t}} \sim 800\,\text{pb}$. At LHC in the initial phase about 1 $t\bar{t}$-pair is produced each second, resulting in 10^7 $t\bar{t}$-pairs per year.

1.3.2 Top Quark Decay

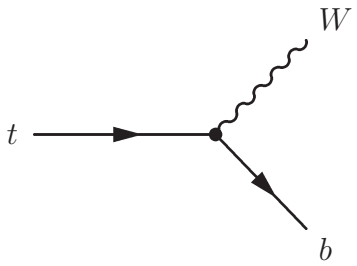


Figure 1.5: Main top decay mode: t→W+b

Because of its short lifetime the top quark does not hadronize. It decays after $\approx 10^{-24}\,s$. The time for hadronisation depends on the fraction $\frac{E_t}{m_t c}$. For the energies at the LHC ($E_t = 374\,\text{GeV}$ in average) the hadronisation time is about 10 times larger than the lifetime of the top quark [11].

The top quark decays nearly 100% of the time to b-W pairs. The b quark forms a jet, while the W boson decays either into a quark antiquark pair or into a lepton and a neutrino. The

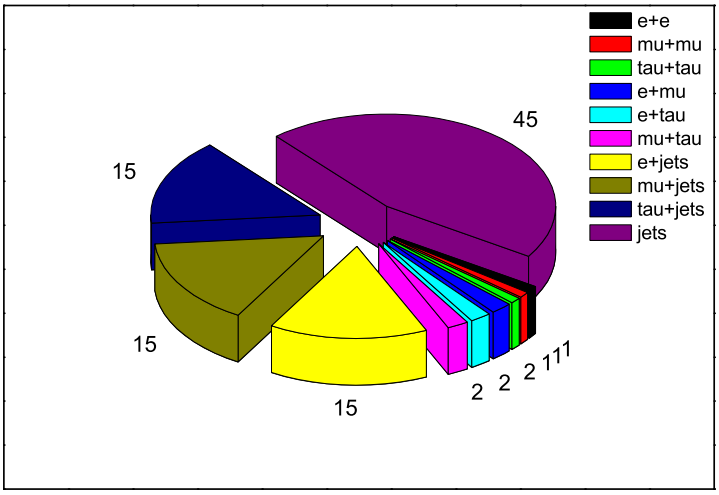


Figure 1.6: Branching ratios for the decay of the $t\bar{t}$ pair [12].

decay of a $t\bar{t}$ pair gives two b-W pairs. In 5% of the $t\bar{t}$ events the two W bosons decay into leptons and neutrinos, where the lepton is either an electron or a muon. This is called the di-leptonic channel. In roughly 30% the decay of the W bosons results in two quarks, a lepton (electron or muon), and a neutrino. This is the semi-leptonic channel. 45% of the $t\bar{t}$ pairs decay fully hadronically, meaning that both W bosons decay into quarks and antiquarks. The decay of the W into a tau and a tau neutrino is difficult to handle because the tau itself decays very quickly into hadrons (65%) or into leptons (35%). This is why the analysis dealing with the leptonical channels only takes care of e and μ. There are four types of decays distinguished: leptonic, semi-leptonic, hadronic, and $\tau + X$, see Table 1.3. All decay modes and their branching ratios are shown in Figure 1.6. The decay of the top quark into hadrons is the one with the largest branching ratio. In this decay channel there are 6 jets in which two jets come from the b-quarks and 4 from the W's. The four non b-jets have to be combined to the two W's correctly, which implies combinatorial

Decay type	**BR**	**Decay**
leptonically	5%	$t\bar{t} \rightarrow W^+bW^-\bar{b} \rightarrow l^+\nu b l^-\bar{\nu}\bar{b}$
semi-leptonically	30%	$t\bar{t} \rightarrow W^+bW^-\bar{b} \rightarrow l\nu q\bar{q}\bar{b}$
hadronically	44%	$t\bar{t} \rightarrow W^+bW^-\bar{b} \rightarrow q\bar{q}bq\bar{q}\bar{b}$
$\tau + X$	21%	one of the W's decays into $\tau + \nu_\tau$

Table 1.3: Top decay modes and their branching ratios (BR) [13].

uncertainties, especially if there are additional jets coming from gluon radiation. This decay channel has a large background coming from pure QCD effects and is hard to identify.
Very interesting and promising is the semi-leptonic decay channel. One can trigger on the isolated lepton and missing energy. There are 4 jets coming from the b's and the W. The two light jets have to be combined to reconstruct the W.
The purest decay is the leptonic decay channel, because it gives two isolated leptons, missing energy and two b-jets. It is possible to trigger on the leptons and missing energy (and do a b-tagging for the two jets), which should give the possibility to use this channel as well.

When dealing with jets from a b quark it is possible to perform b-tagging. This identifies a jet as coming from a b quark and reduces the combinatorial uncertainty. The result is a purer event sample.

For completeness the other decays of the top quark can be into an s or a d quark. But these decays are highly suppressed. The branching ratios are: 0.2% for the s quark channel and 0.01% for the d quark channel.

Chapter 2

The Large Hadron Collider and the ATLAS Detector

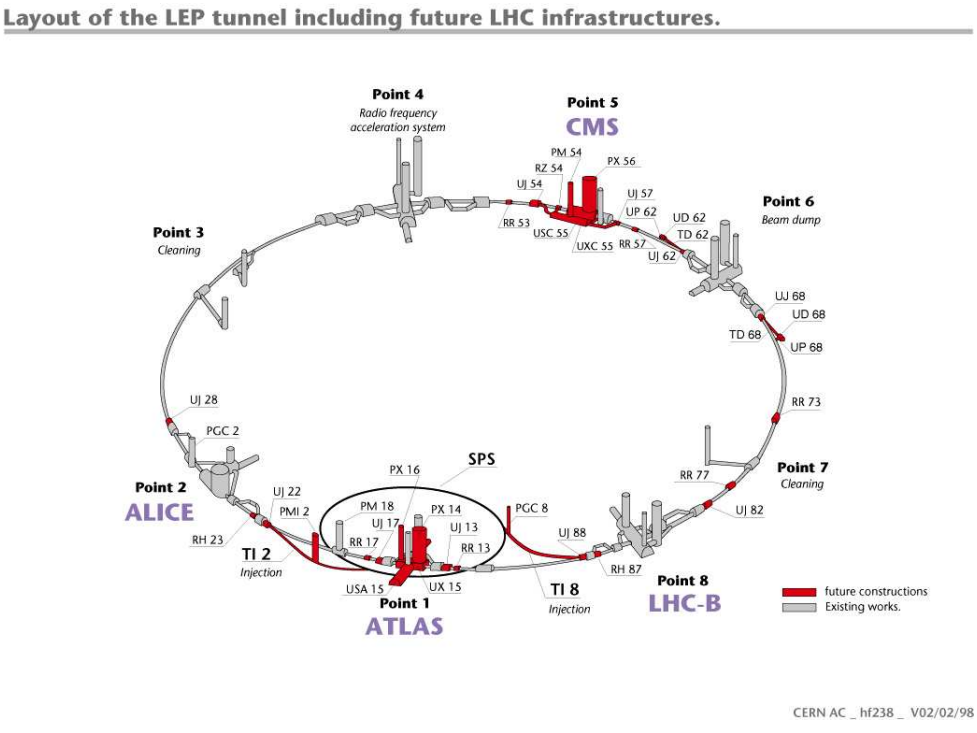


Figure 2.1: LHC accelerator with the experiments [14].

2.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is under construction at the European Centre for Nuclear Research (CERN) in Geneva. It will be installed in the tunnel of the former LEP[a] machine 100 m deep under ground. The tunnel is partly on French area and partly on Swiss area, between the Jura mountains and the airport of Geneva. The collider accelerates protons to an energy of 7 TeV. The collider system consists of different parts: there is a linear injector which first accelerates the protons, followed by the two ring accelerators, the PS[b] and the SPS[c] which accelerate the protons to 450 GeV. From the SPS the protons will be fed into the LHC using more than 500 magnets. The protons circulate in two vacuum beam pipes in opposite directions.

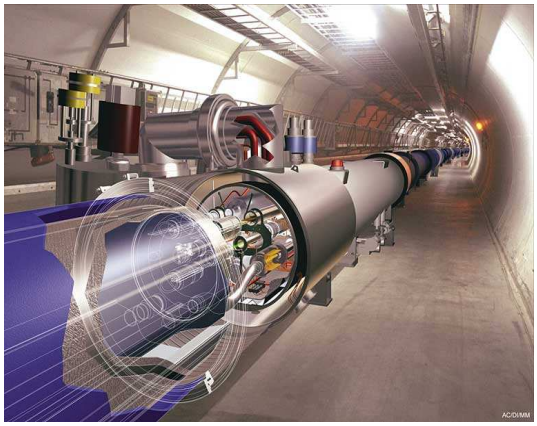


Figure 2.2: LHC pipe in the tunnel [14].

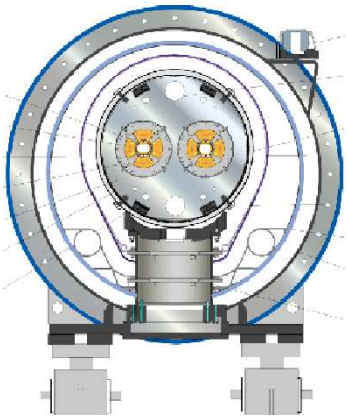


Figure 2.3: Cross section of the vacuum pipes inside a quadrupole magnet [14].

The LHC itself is a ring accelerator of 27 km circumference. The particles are normally protons, but heavy ions can be used, too. Each proton will reach an energy of 7 TeV. Table 2.1 provides an overview of some technical parameters of the machine.

The particles circulating inside the ring are divided into bunches of $\sim 10^{11}$ particles. 2808 of these bunches circumnavigate the ring and follow each other at separation of 7 m in length or 25 ns in time. The particles traverse the entire ring ~ 10000 times per second. At four specific points in the ring detectors will be constructed. At these points the two beams will cross and collide with a rate of 40 MHz. Four experiments will be installed at the LHC to measure the products of the particle collisions. Per event there are ≈ 20 inelastic scatterings which give nearly 1000 new particles.

[a] Large Electron Positron Collider, operated between 1989 and 2000
[b] Proton Synchrotron
[c] Super Proton Synchrotron

Circumference	$26658,883\,m$
Strength of magnets	$8,4\,\mathrm{T}$
Centre of mass energy for pp	$14\,\mathrm{TeV}$
Number of proton bunches	2808
Protons per bunch	$1.1 \cdot 10^{11}$
Beam energy	362 MJ
Separation between the bunches	$25\,\mathrm{ns}$
Collision rate	$40\,\mathrm{MHz}$
Luminosity	$10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

Table 2.1: Machine parameter of the LHC for proton operation for the proposed luminosity of $10^{34}\,cm^{-2}s^{-1}$.

The rate of the proton proton reaction inside the LHC machine depends on a the proton proton cross section and a machine parameter, named luminosity. The luminosity L is defined by Equation 2.1.

$$L = \frac{n_1 n_2 f}{A} \tag{2.1}$$

with:

$n_1,\, n_2$	number of particles in the crossing bunches
f	bunches per second
A	cross sectional area of a bunch

The LHC runs in two luminosity phases, the low luminosity phase with $L = 10^{33}\frac{1}{cm^2 s}$ and the high luminosity phase with $L = 2.3 \cdot 10^{34}\frac{1}{cm^2 s}$.

The produced particles are registered by the detectors. The momentum, the charge, the energy, and the track of the particles are measured. The measured information is used by the analysis software to reconstruct the events and analyse the physics.

There are four large experiments at the LHC, these being ALICE[d], ATLAS[e], CMS[f] and LHC-B[g]. ATLAS and CMS are general purpose experiments sensitive to all kind of processes, ALICE is a heavy ion experiment looking at the collisions of lead or gold ions. LHC-B is meant for doing B-physics, for example measuring the properties of the B mesons. While ATLAS, CMS, and ALICE are built up in a traditional manner with a tracker as the innermost detector, followed by a calorimeter and a muon system, the LHC-B experiment differs. LHC-B is built up only on one side of the collision target to have a longer view of the interesting particles.

[d] A LHC Ion Collider Experiment
[e] A Toroidal LHC Apparatus
[f] Compact Muon Solenoid
[g] Experiment for B-Physics at LHC: LHC-B

2.2 The ATLAS Experiment

This thesis is primarily focused on the pixel subdetector of the ATLAS experiment, so it will henceforth concentrate on the ATLAS experiment. The ATLAS pixel detector and its read out components are described in more detail in Chapter 3.1.

2.2.1 Goal of the ATLAS Experiment

The aim of the ATLAS experiment is to research the structure of matter, how it is built up and how it stays together. As described in Chapter 1.1, there are still open questions to address. With the highest energy ever produced with an accelerator, LHC will open new possibilities for studying already known processes and make another step in the search for new physics. The ATLAS experiment, as one of the general purpose experiments at the LHC, is meant for studying the quarks, especially the heavy quarks, as well as studying the CP-violation in the B-decay, searching for the Higgs, searching for super symmetric particles (SUSY), and more generally, physics extending the Standard Model [15]. The detector was designed according to these tasks to observe as many of the produced particles as possible. The structure is described below.

2.2.2 Structure of the ATLAS Experiment

The ATLAS detector is the largest detector at the LHC. It is 22 m in diameter and 44 m long. Its weight is about 7000 t. The detector is shown schematically in Figure 2.4.

Moving from the outermost to the innermost part, the ATLAS experiment is built up by a muon spectrometer (blue in the schematic), the hadronic (green) and the electromagnetic (orange) calorimeter, to a cryostat containing the inner detector consisting of a Transition Radiation Tracker (TRT, yellow), the Silicon Tracker (SCT, red) and the Pixel detector (rose). The inner detector is placed in a solenoidal magnetic field of 2 T strength, while the muon system is placed within a torroidal magnetic field of 0.5 T. The subdetectors of ATLAS are described in the next sections.

The coordinates in which the detector can be described are chosen to be Z, Φ, and η. Because the detector is symmetrical to the beam pipe this direction is chosen as the z-axis with the origin in the centre of the ATLAS detector. The two angles describing the other two dimension are the azimuthal angle Φ and the polar angle θ. While Φ is kept as a coordinate, θ is transformed into the pseudorapidity η by:

$$\eta = -ln(tan(\theta/2)) \tag{2.2}$$

This means $\eta = 0$ for the plane orthogonal to the beam pipe at z=0. Therefore the absolute value of η is used to describe a region of the detector symmetrically to the origin. Like the barrel region of the pixel detector is inside $\eta < 2$.

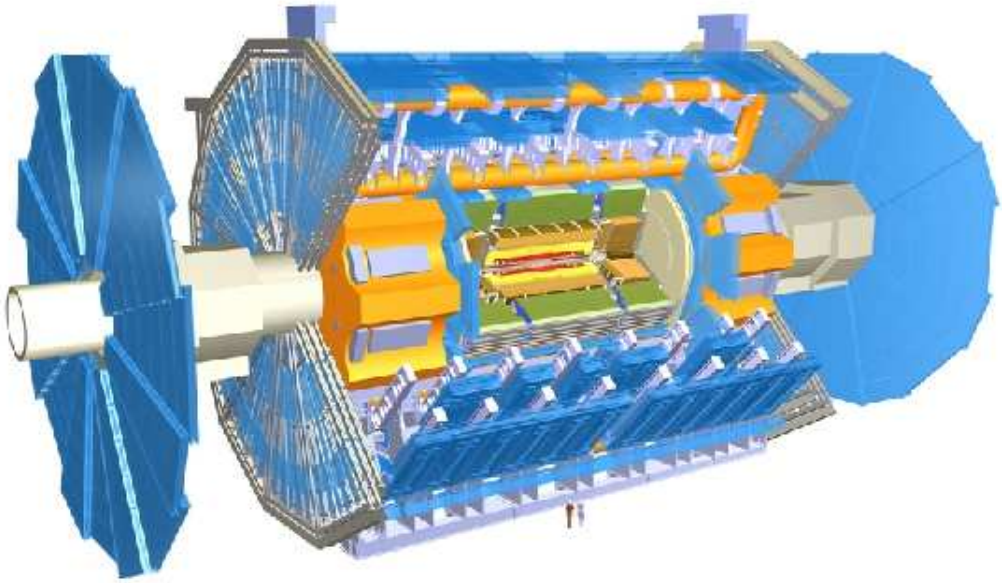


Figure 2.4: Schematic of the ATLAS experiment [14].

The Muon Detector

The muon spectrometer [16] is the outermost subdetector. It identifies muons and measures their track and momentum. To reach a precision on the order of $< 10\%$ in momentum for a muon with transverse $p_T = 1\,\text{TeV}$, the track of the muon has to be measured very precisely. The resolutions are $70\,\mu$m in z and $(0.1 - 1)$ mrad in Φ. The second purpose of this subdetector is to generate a trigger on muons, depending on their transverse momentum. The properties are summarised in Table 2.2.

The muon spectrometer is comprised of 4 different detector types: monitored drift tubes (MDT), cathode strip chambers (CSC), resistive plate chambers (RPC), and thin gap chambers (TGC).
The MDT's are foreseen for precision measurements. They are built of aluminium tubes of 30 mm diameter, $70 - 630$ cm length, with a tungsten wire in the middle. They are filled with an argon-methane-nitrogen mixture at 3 bar. The readout is done at the end of the tubes which are arranged in multilayers of 3 or 4 tubes. Figure 2.5 shows the carrier structure with the tube multilayers on top and bottom.

These MDT-chambers are arranged in the ATLAS detector as 3 barrel layers with 5 m, 7.5 m, and 10 m radius. In the forward and backward region there are 2 disks of MDT chambers on each side. The orientation is always parallel to the toroidal magnetic field for having the best measurement of the muon momentum.

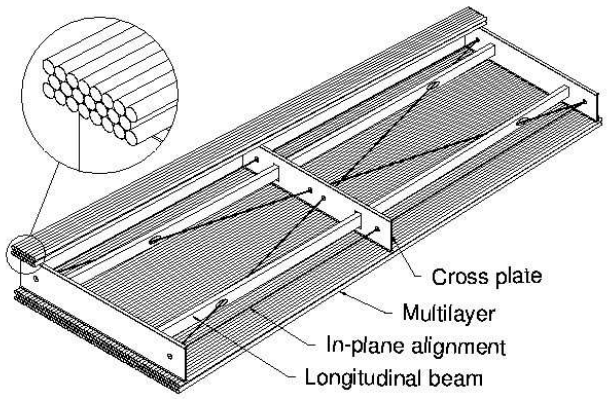


Figure 2.5: Monitored Drift Tube of the ATLAS muon System.

The CSC's are installed in the forward region very close to the beam pipe. In this region the MDT's cannot be used because of the high occupancy. They act like multiproportional chambers, where the signal is collected on strip segmented cathodes.

For generating the fast trigger signal, RPC's are built on top of the MDT's in the barrel region. They have a very short response time and measure a 2 dimensional trackpoint.

In the forward region the fast trigger signals are generated by Thin Gap Chambers.

Purpose	Precise measurement of the tracks of muons and generation of the muon trigger	
Detector type	Monitored drift tubes and different multistrip gas chambers	
Number	Barrel layers Disks	3 4
Dimensions	Radius Length	$5 - 10\,\mathrm{m}$ $7 - 21\,\mathrm{m}$
Resolution	z Φ	$70\,\mu\mathrm{m}$ $0,1 - 1\,\mathrm{mrad}$
Momentum resolution	$p_T < 100\,\mathrm{GeV}$ $100\,\mathrm{GeV} < p_T < 1\,\mathrm{TeV}$	2% $< 8\%$
Channels	CSC + MDT RPC + TGC	67000 + 370000 355000 + 440000

Table 2.2: Properties of the muon spectrometer.

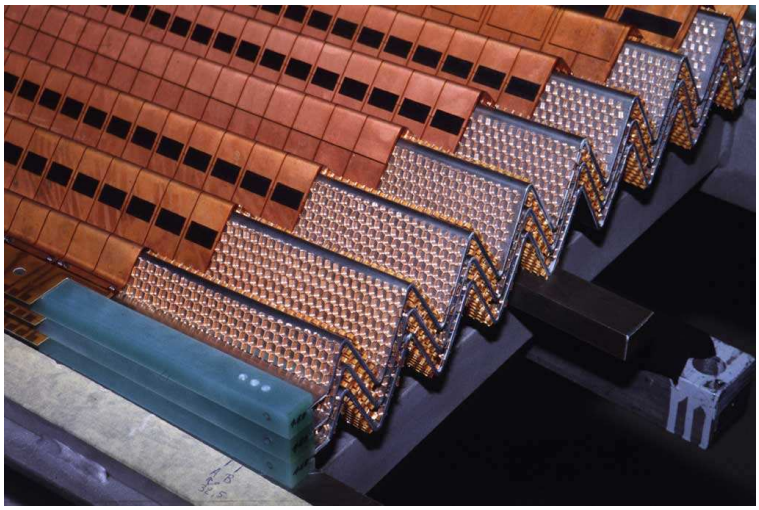


Figure 2.6: Liquid Argon Calorimeter in accordion structure

The Hadronic Calorimeter

The hadronic calorimeter measures the energy of hadronic particles. In addition, it delivers spatial information to match the hit to a track in the inner tracking detector. The calorimeter is comprised of a barrel section (tile scintillator calorimeter) and the end caps (liquid argon calorimeter). All calorimeters are sampling calorimeters. In the tile calorimeter, located in the barrel section, plastic scintillators are used as the active material and steel as the absorber material. All other calorimeters in ATLAS use liquid argon as the active material. They differ in geometry and in the absorber material. As absorber material tungsten is used as well as copper. The requirements are given in Table 2.3

Purpose	Measurement of the energy of hadrons and jets with spatial resolution	
Detectortype	Sampling calorimeter with liquid argon and plastic scintillators	
Granularity $(\Delta\eta \times \Delta\Phi)$	$0.1 \times 0.1 - 0.2 \times 0.1$	
Interaction length	$> 11\lambda$ at $\eta = 0$	
Energy Resolution	for $\lvert\eta\rvert < 3$	$\frac{\Delta E}{E} = \frac{50\%}{\sqrt{E}} \oplus 3\%$
	for $3 < \lvert\eta\rvert < 5$	$\frac{\Delta E}{E} = \frac{100\%}{\sqrt{E}} \oplus 10\%$
Dimensions	Radius:	$2.28 - 4.23\,\mathrm{m}$
	Length:	$11.46\,\mathrm{m}$
Number of channels in total	180000	

Table 2.3: Properties of the hadronical calorimeter.

Purpose	Measurement of the energy of electrons and photons with spatial resolution	
Detector type	Sampling calorimeter with liquid argon	
Granularity ($\Delta\eta \times \Delta\Phi$)	Barrel Layers	$0.003 \times 0.1 - 0.05 \times 0.025$
	Endcaps	$0.003 \times 0.1 - 0.1 \times 0.1$
Radiation length	$> 24X_0$	
Energy Resolution	Photons ($E_T = 50\,\text{GeV}$)	$< 1.6\%$
	Electrons ($E_T = 20\,\text{GeV}$)	$< 6\%$
Dimensions	Radius	$1.15 - 2.25\,\text{m}$
	Length	13.14 m

Table 2.4: Properties of the electromagnetic calorimeter.

The Electromagnetic Calorimeter

The electromagnetic calorimeter measures the energy of electrons and photons, and part of the energy of the hadronic jets. The calorimeter delivers a spatial information of the measured hit, using liquid argon as the active material and lead as the absorber. It is built in an accordion structure with alternating absorber and active layers. A schematic of the structure can be seen in Figure 2.6. The Properties are given in Table 2.4.

Transition Radiation Tracker (TRT)

The tracking system is located in a 2 T solenoidal magnetic field. It has to measure the tracks of charged particles very precisely to give information about the charge and the momentum of the measured particle. The precise spatial information obtained by the tracking system enables the reconstruction of the primary vertex, impact parameter, and secondary vertices. The radiation environment so close to the beam pipe is very severe. The components close to the beam pipe have to be extremely radiation tolerant. The tracking system is comprised of three different detector types.

The outermost of the tracking detectors is the transition radiation tracker (TRT). It is assembled from straw tubes. These are aluminium coated polyamid tubes of 4 mm diameter and a length of 1.44 m. Along the contral axis there is a $30\,\mu$m thick tungsten-rhenium wire. The tube is filled with a $Xe - CO_2 - CF_4$ gas mixture. Approximately 370000 tubes are included into the TRT, with 50000 in the barrel and 320000 tubes in the disks. On each detector side there are 18 disks. The properties of the TRT are summarised in Table 2.5.

As radiator between the tubes in the barrel there are polypropylene-polyethylene fibres, and in the forward region there are foils of polypropylene - polyethylene. As a result, the dielectric constant in the material alternates. Therefore, a charged particle traversing this material with a relativistic velocity emits transition radiation. The energy of the radiated

Purpose	30 spacepoints for the tracking of charged particles and electron identification	
Detector type	Straw tubes with PET/PP radiator	
Numbers	Barrel Layers	3
	Disks	18 on each side
Dimensions	Radius	558-1080 mm
	Length	$\pm$ 3396 mm
Spatial Resolution	$r - \Phi$	$170\,\mu$m
	z	-
Spacepoints		> 36 per track
Separation power e/π	Pion rejection	> 50
Channels	Barrel	50000
	Disks	320000
Track recognition	all tracks with $p_T > 0.5$ GeV within $\eta < 2.5$	

Table 2.5: Properties of the TRT.

photons is proportional to $\beta = \frac{v}{c}$. Because electrons and positrons will reach a very large velocity v and will emit a significant transition radiation, an identification of these particles is possible.

Silicon Tracker (SCT)

The silicon tracker (SCT) is located inside the TRT. In the barrel region the SCT consists of four layers. On each end it has nine disks in addition. The layers and disks are assembled with silicon strip detector modules. Each of them is comprised of by four silicon strip detectors, which are affixed in pairs on the top and the bottom of a carrier structure. The strips of the top and the bottom detectors are arranged with small angle of 40 mrad between the strips. This helps to resolve hit ambiguities. The sensors are $300\ \mu$m thick and have an active area of 6×6 cm^2. Two sensors are combined to one detector module with 768 strips of 12 cm length. The pitch between the strips is $80\ \mu$m. The properties are summarised in Table 2.6.

Pixel Detector

This thesis focuses on the pixel detector. The pixel detector and its read out structure is described in more detail in a separate chapter, see Chapter 3.1.

Purpose	More than 3 space points per charged particles	
Detector type	Single sided silicon strip detectors	
Numbers	Barrel Layers	4
	Disks	9 on each side
Dimensions	Radius	$300 - 520$ mm
	Length	$\pm$ 2788 mm
Spatial Resolution	$r - \Phi$	$23\,\mu$m
	z	$500\,\mu$m
Channels	Barrel	3200000
	Disks	3000000
Track recognition	all tracks within $\eta < 2.5$	

Table 2.6: Properties of the SCT.

2.3 The Trigger System

The trigger system [17] of the ATLAS experiment has three levels. The first level is implemented in custom made hardware. The second and third levels are programs running on computer farms. Because of the enormous amount of data the detector is taking, the trigger has to reduce it to an amount of data which can be stored. The trigger system has to reduce the rate of data taking (40 MHz) to the storage rate (200 Hz). The first level trigger reduces the rate from 40 MHz to about 75 kHz, the second level reduces this to 2 kHz, and the third level trigger finally to 200 Hz. The second and third trigger levels are referred to as the High-Level Trigger (HLT). They share a selection framework and differ mostly in the amount of data they handle and the speed of the algorithms.

To be sensitive to unknown processes of new physics, the trigger system is designed to be as inclusive as possible. The thresholds for fundamental objects are sufficiently low to be sensitive to decay products of new particles. And there is no topological criteria which would bias the trigger. Table 2.7 shows the trigger objects and the physics coverage.

Trigger Objects	**Physics Coverage**
Electron	Higgs, W'/Z', extra dimensions, SUSY, W, top
Photon	Higgs, extra dimensions, SUSY
Muon	Higgs, W'/Z', extra dimensions, SUSY, W, top
Jet	SUSY, compositeness, resonances
Jet + missing E_T	SUSY, leptoquarks
Tau + missing E_T	Ext. Higgs models, SUSY

Table 2.7: Example of trigger objects and their physics coverage.

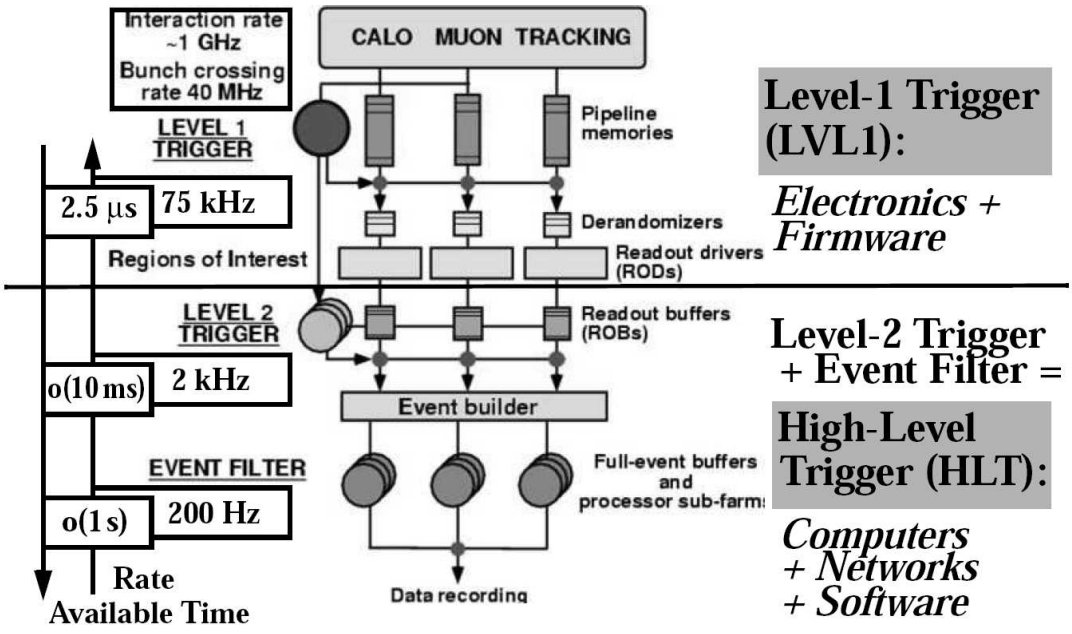


Figure 2.7: The overview of the ATLAS trigger and data acquisition system [18].

2.3.1 First Level Trigger

The first level trigger has to be very fast and is therefore implemented in custom hardware. Since the decision for a trigger can not be made within 25 ns, the detectors have to store the event data in a pipeline until the LVL1 trigger decision is made. The time for the trigger decision is $2.5\ \mu$s. After this time the data is lost if not read out. The LVL1 trigger is sent to the Read out Drivers (ROD) which will pass the read out data to the Read Out Buffer (ROB) where the data is stored until the LVL2 decision is reached.

The LVL1 trigger uses only information from the muon system and the calorimeters. These two items of trigger information are combined in a Central Trigger Processor (CTP) which makes the final decision and sends it via the Timing Trigger and Control (TTC) system to the subdetector ROD's. Additionally, the CTP sends information to the Region of Interest Builder (RoIB) which compiles a list of Regions of Interest (RoI) from the event for the LVL2 trigger.

Calorimeter Trigger

In the calorimeter system, trigger towers are used to make a trigger decision. The towers are in the region $|\eta| < 2.5$ and have a granularity of $\Delta\eta \times \Delta\Phi = 0.1 \times 0.1$. While the analog sums are done on detector, the information is fed into a preprocessor system followed by a jet/energy sum processor and a cluster processor, which identifies electrons and photons as well as taus and hadrons. With this an electron/photon trigger can be set,

as well as a tau or jet trigger. It computes the missing and the transverse energy and the x and y components of the missing transverse energy E_T to be used in the trigger decision.

Muon Trigger

The trigger chambers in the muon spectrometer are the RPC's and the TGC's. They provide three stations with 2 layers each in the barrel region. The trigger algorithm is based on a coincidence of hits in different layers with restrictions on their track. For detecting a low p_T muon, a successful trigger condition consists of three hits in the four inner layers, while a high p_T muon trigger requires an additional hit in the outer station.

The thresholds for momentum can be programmed independently for low and high p_T. The information from the muon system is passed to the CTP for the trigger decision.

2.3.2 High-Level Trigger

The High-Level Trigger (HLT) refers to the LVL2 trigger and the Event Filter (EF) system. They share the same trigger selection framework and many algorithms may be used by both of them. The boundary here is very flexible.

The High-Level Trigger software framework is based on the ATLAS offline framework Athena [19]. This makes it easier to use the HLT algorithms in the offline simulation. The HLT event selection software defines additional requirements on trigger algorithms compared to the offline algorithms. This is important for the LVL2, where data must be formulated as a Region of Interest (ROI). The trigger system is a stepwise system. Each step makes use of the data from the last step. And at each step the steering process can reject the event. This saves processing time and reduces the latency for events where a decision can be made based on some rather simple properties. The more time consuming algorithms are processed in later steps. An event can only be accepted after it has passed all the steps. For a more detailed description of the trigger system, please refer to [17] and [20].

Chapter 3

Components of the Pixel Detector System

3.1 The ATLAS Pixel Detector

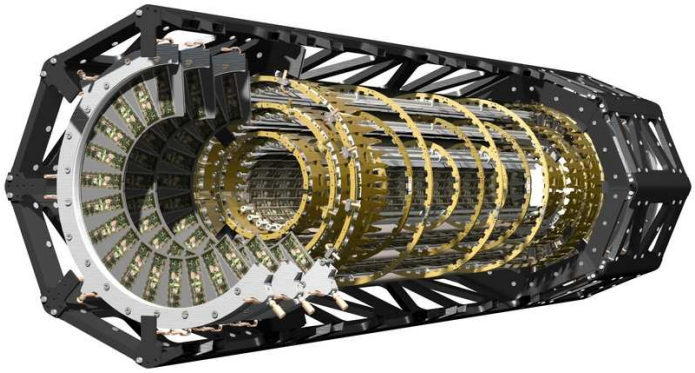


Figure 3.1: A schematic view of the pixel detector in its mounting structure [21].

The pixel detector is the innermost subdetector of ATLAS. Due to this, the requirements concerning radiation hardness, spatial resolution, two particle separation, and occupancy tolerance are rather severe. Even at the end of its lifetime the pixel detector has to deliver 3 spacepoints for each traversing charged particle. Its spatial resolution has to be < 15 μm in rΦ- and < 120 μm in z-direction. The detector is comprised of hybrid pixel detector modules which can be read out very fast and give true 3-dimensional spatial information

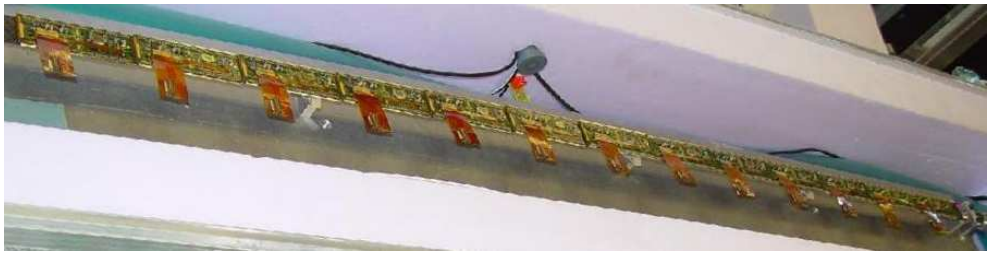


Figure 3.2: Loaded stave in a cooling box.

for each hit. The hybrid technique allows one to develop the sensor and the electronics independently and to optimise them separately.

The pixel detector (see Figure 3.1) has 3 barrel layers, 3 disks on the forward side, and 3 disks on the backward side. It records 3 spacepoints per charged particle, up to a pseudo-rapidity of $|\eta| = 2.5$. To reconstruct secondary vertices, means the location of a particle when decaying outside the primary interaction vertex, the spatial information close to the beam pipe is important. This information improves the resolution of the reconstruction and improves the analysis results. A secondary vertex can be observed if a B meson, containing a b-quark, decays. A reconstruction of this secondary vertex will allow one to tag a jet as a b-jet.

This is why the innermost layer of the barrel section is called *B-Layer*. The middle layer is *Layer1* and the outer one is called *Layer2*. Each barrel is comprised of staves, upon which the active elements, the pixel modules, are mounted. A stave is a carbon-carbon support structure having the cooling pipe underneath and the detector modules on top. It is 832 mm long and has a width of 18 mm [22]. Each stave will have 13 modules. The modules are arranged symmetrically about the centre with an inclination angle of 1.1°, and slightly overlap in the z-direction. Figure 3.2 shows a stave. The staves are combined pairwise, so that the smallest mechanical unit will be a bi-stave. They are arranged in a turbine like structure, so that the uninstrumented space is minimised.

The disks are divided into sectors (see Figure 3.3) which will have 3 modules on the front and 3 modules on the back. The modules on front- and backside overlap to provide complete coverage. Table 3.1 gives the dimensions and coordinates for the subparts of the pixel detector.

All staves are mechanically the same for all barrel layers and the sectors are identical for all disks. All staves and sectors are equipped with the same type of modules, 13 on the staves, 6 on the sectors. A selection of the staves for the B-Layer is based on the criteria of having modules which show the best performance without any rework procedure.

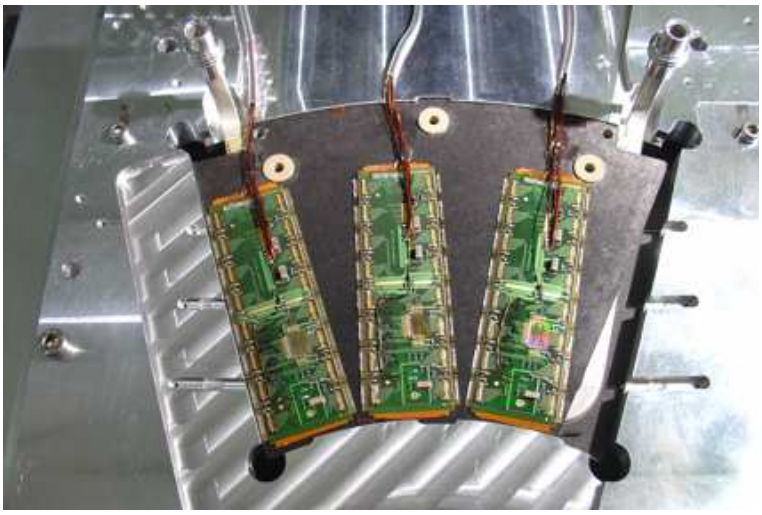


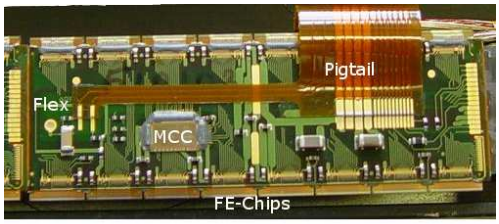
Figure 3.3: A sector on a test station. The sector is the smallest mechanical unit of a disk. A sector carries 6 module, 3 on the front and 3 on the back side.

3.1.1 Pixel Module

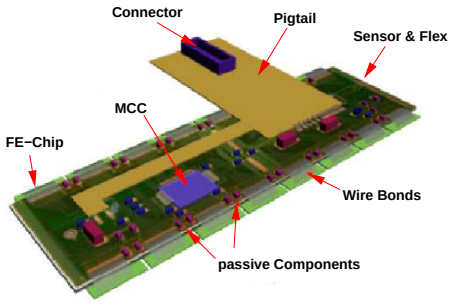
The smallest active detector unit of the pixel detector is a *pixel module* (see Figures 3.4(a) and 3.4(b)). It consists of a silicon sensor, the read out electronics, and the interconnection foil. The sensor is subdivided into 46080 pixels of an area of $50\,\mu\text{m}\times400\,\mu\text{m}$ or $50\,\mu\text{m}\times600\,\mu\text{m}$. Each of these pixels is connected to a single electronic cell via tiny solder bumps. The electronic cells are arranged in 16 special ASIC's, the Front End (FE) chips. In these chips the signals from the sensor is amplified and digitised. It is fed to the module control chip, the MCC, which communicates with the off detector readout electronics. The interconnections between the FE chips and the MCC are provided by $25\,\mu\text{m}$ thick wirebonds and a flexible capton foil, the "flex". The different components –

	Radius (mm)	**Staves**	**Modules**
B-Layer	50.5	22	286
Layer 1	88.5	38	494
Layer 2	122.5	52	676
	z-position (mm)	Sectors	Modules
Disk 1	±495	8/8	48/48
Disk 2	±580	8/8	48/48
Disk 3	±650	8/8	48/48
Total			1744

Table 3.1: Dimensions and coordinates for the ATLAS pixel detector subparts.



(a)



(b)

Figure 3.4: A pixel module. The 16 Front End (FE) chips are underneath as shown in the illustration. A flexible capton foil provides the interconnections between the FE chips and the module control chip (MCC) on top.

the sensor, the front end chips, and the module control chip – are described in the next sections.

3.1.2 Pixel Sensor

Basics of the Semiconductor Detector

As sensor material silicon as crystalline semiconductive material is used. A charged particle traversing a semiconductor loses energy in the crystal generating electron-hole pairs along its path. For silicon the mean energy to produce an electron-hole pair is 3.62 eV. To ionise an atom in the material one has to overcome the energy gap in the band structure of the semiconductor on one hand which is 1.12 eV for silicon and one has to account for the generation of phonons, thermal energy in the end, on the other hand.

The energy transfer of a charged particle in matter is described through the Bethe-Bloch-Formula 3.1.

$$-\frac{dE}{dx} = 2\pi N_a r_e^2 m_e c^2 \rho \frac{Z}{A}\frac{z^2}{\beta^2} \cdot \left[\ln\left(\frac{2m_e\gamma^2 v^2 W_{max}}{I^2} - 2\beta^2 - \delta - 2\frac{C}{Z}\right)\right] \tag{3.1}$$

with (values for silicon given in brackets):

dE/dx:	mean energy loss per track length
N_a:	Avogadro's number = 6.022×10^{23} mol^{-1}
r_e:	classical electron radius = 2.817×10^{-13} cm

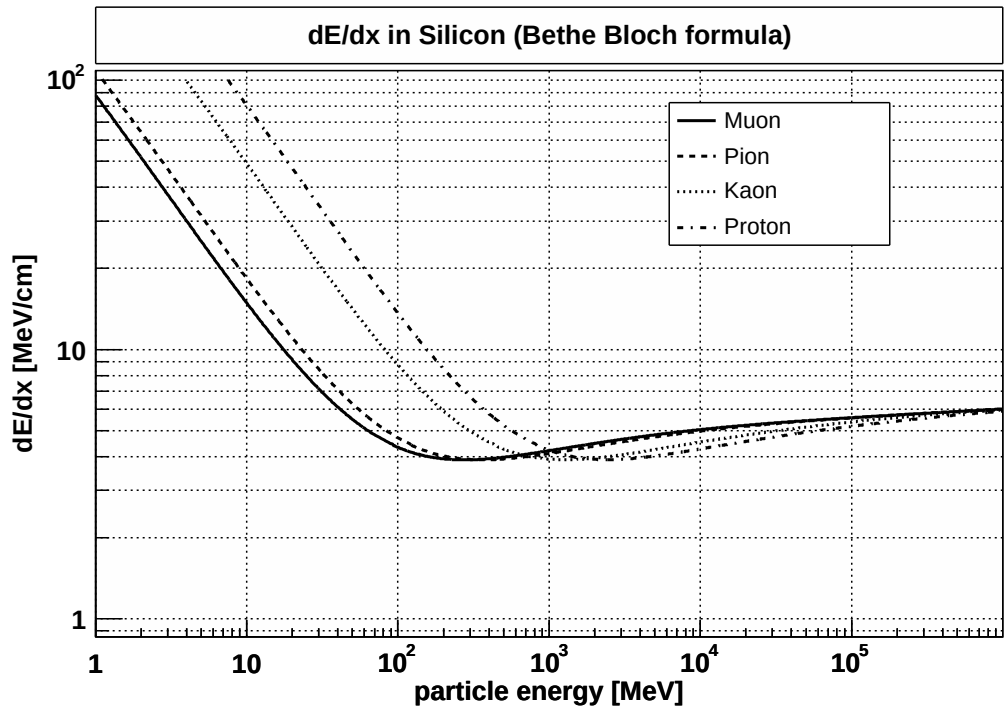


Figure 3.5: Energy loss of different types of particles according to the Bethe-Bloch equation, calculated for particles traversing 250 μm thick silicon [23].

m_e:	electron mass = 511 keV
ρ:	density of absorbing material (2.33 gcm^{-3})
I:	average effective ionisation potential (≈ 173 eV)
Z:	atomic number of absorbing material (14)
A:	atomic weight of absorbing material (28)
z:	charge of incident particle in units of e
β:	v/c speed of the incident particle in terms of c
γ:	$1/\sqrt{1-\beta^2}$
δ:	density correction
C:	shell correction
W_{max}:	$\simeq 2m_e c^2\beta^2\gamma^2$, if $M \gg m_e$ maximum energy transfer in a single head on head collision.

Formula 3.1 includes the density effect correction δ and the shell correction C and is valid down to $\beta \simeq 0.1$ [24].

The energy loss of a traversing particle is decreased by the density effect at high energies. The presence of the electric field leads to the polarisation of atoms along the path of the

particle and thus electrons far from the path are shielded from the full electric field. The density effect depends on the density of the absorbing material.

The effect of the shell correction is a small effect. It reduces the energy loss at low energies, because of the wrong assumption of a stationary electron in the absorber.

At around $v \simeq 0.96\,c$ or $\beta\gamma \simeq 3.5$ a minimum in the Bethe–Bloch formula is reached. Particles at that point are called *minimum ionising particles* (MIP).

As an example the mean energy loss in 250 μm silicon of an minimal ionising pion with the mass $m_{pi} = 139.57$ MeV is ∼97.5 keV, generating ∼27000 electron-hole pairs. This is different from the most probable energy loss, which is ∼69.9 keV, generating ∼19300 electron-hole pairs. This is due to the asymmetry of the energy loss density function, which is not gaussian but has a tail to higher energies, which is due to possible interactions with a higher energy transfer.

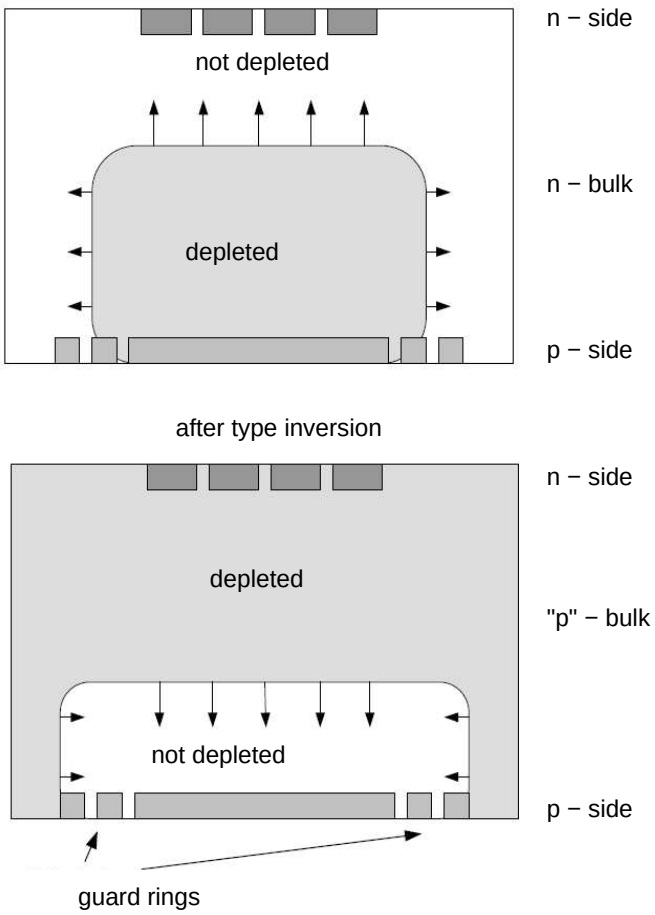


Figure 3.6: Type inversion.

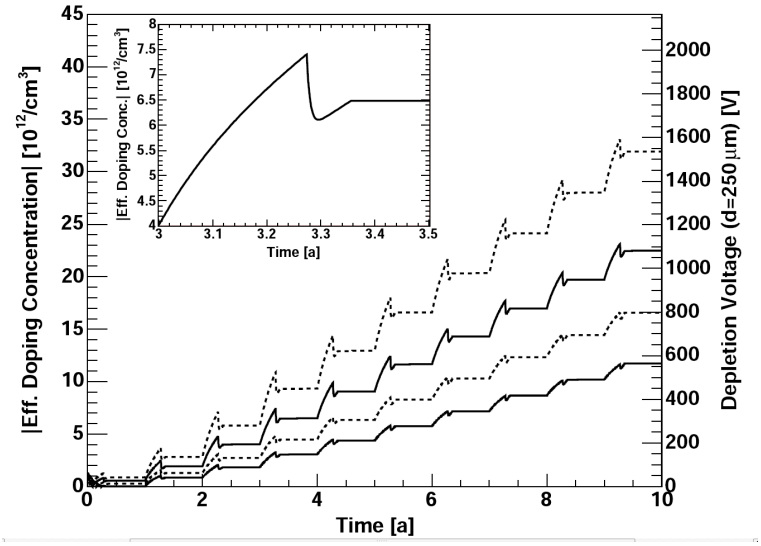


Figure 3.7: Sensor full depletion voltage under irradiation and annealing for the 10 years of ATLAS. The dashed lines are for pure silicon, the solid lines show the oxygen enriched silicon, which is used for the pixel detector. The upper two lines are for the B-Layer, the lower two lines are for Layer1 [27].

The ATLAS pixel sensor

The silicon sensor [25, 26] of the ATLAS pixel detector module has a size of $63 \times 18.6 \times 0.25\,\mathrm{mm}^3$. Its active area is $60.8 \times 16.4\,\mathrm{mm}^2$. It is subdivided into pixels to provide the 2 dimensional spatial information for each hit. The sensor is an n^+ on n type sensor. For this, both sides of the sensor have to be prepared, but this type of material has several advantages. The n^+ on n type sensor bulks undergo type inversion with irradiation (see Figure 3.6). This means that the concentration of the effective doping of the sensor material changes with an increasing radiation load. Thus, the type of the bulk inverts from an n-type into a p-like substrate. The change of the effective doping concentration implies that the depletion voltage needed for operation changes. While in an n-type bulk the depletion zone grows from the back side, after the type inversion the depletion zone grows from the pixel side. This implies that even with an incompletely depleted sensor the pixels are isolated against each other and operation is possible. The active volume of course increases with the depletion depth. The pixel supply system is designed to reach a depletion voltage of 700 V.

The radiation environment the pixel detector is located in is extremely severe. The pixel modules components have been tested to withstand this radiation level. Extensive research on sensor materials has shown that a controlled oxygen enriched silicon can withstand radiation better than normal silicon [28]. It is also known that temperature effects can improve or worsen the resistance to radiation damage. As a result, the operating temper-

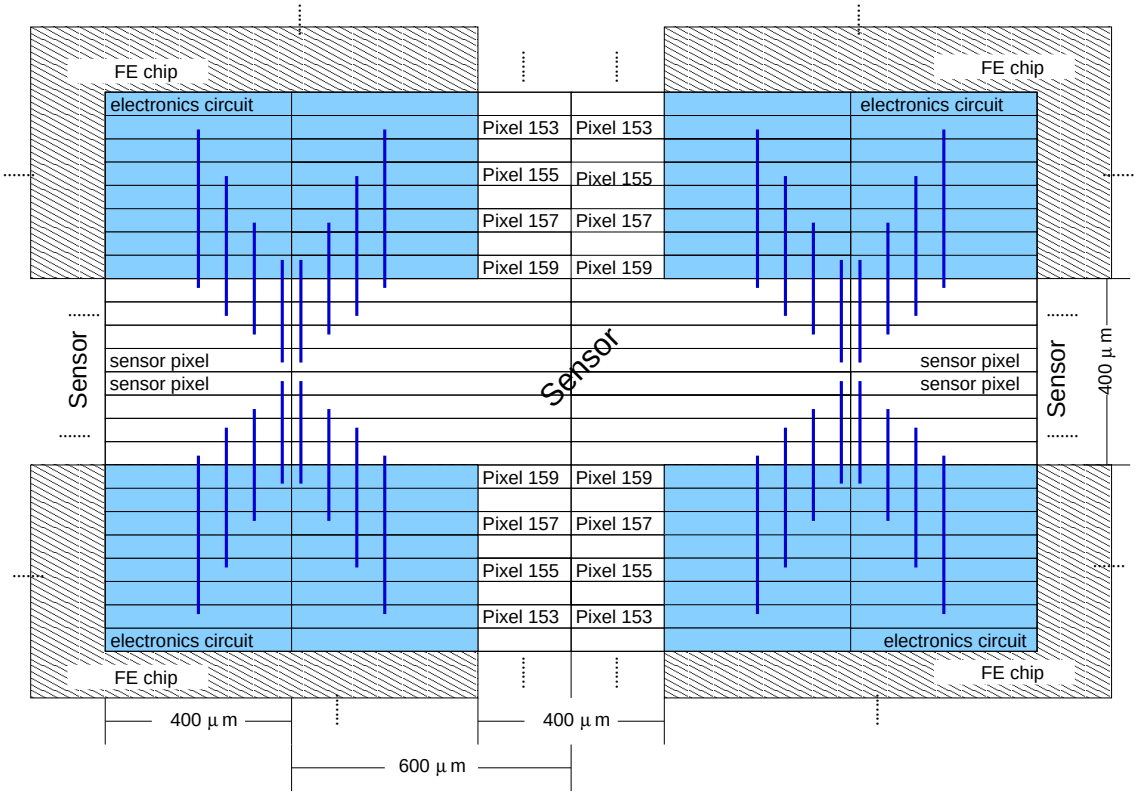


Figure 3.8: Ganged sensor pixels as view on the sensor top side. The pixels are the long horizontal structures. The vertical junctions are the connections of two pixel. The edges of the read out chips are sketches. A double connected cell always alternates with a single connected cell.

ature for the pixel sensor is -10° C. The silicon can repair itself at higher temperatures. This effect is called *annealing*. For a more detailed description, see [28]. The annealing improves the sensor first and turns into a reverse annealing after some time. This worsens the radiation damage again. The temperature has to be lowered to avoid this reverse annealing. Thus, during the inactive periods the pixel detector is kept at $+20^\circ$ C for 20 days and then at -10° C for the rest of the time. The resulting effective doping concentration of the silicon is shown in Figure 3.7. The plot shows the needed depletion voltage for the B-Layer (upper two curves) and for Layer1 (lower two curves). The dashed curve is for a pure silicon and the solid line shows the behaviour for the oxygen enriched silicon which is used for the pixel detector. It shows also that the oxygenated silicon sensor can be operated fully depleted after 10 years of ATLAS for Layer1. The B-Layer is foreseen to be exchanged after 5 years of operation.

The sensor pixels have a size of $50 \times 400\,\mu\text{m}^2$ for nearly all of the pixels. This leads to a spatial resolution of $15\,\mu$m in the rΦ-direction and $115\,\mu$m in the z-direction. Each

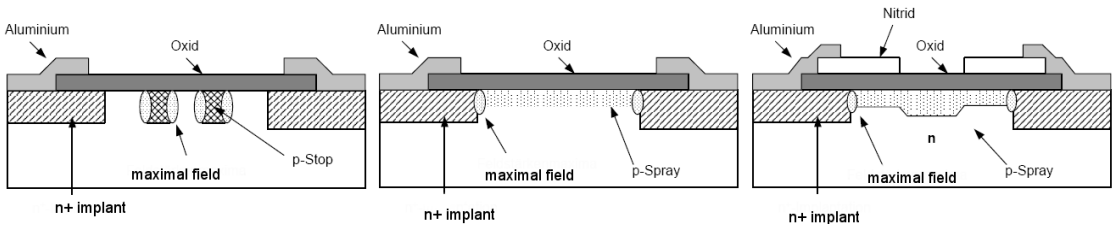


Figure 3.9: Cross sections of pixel isolation: on the left the traditional p-stop technique, in the middle the p-spray technique, and on the right the modified p-spray technique [26].

pixel is connected via a small bump with its own electronics circuit. These circuits are arranged in 16 Front End chips. Each chip has 18 columns and 160 rows of these circuits. On each long side of the module there are 8 chips. To avoid dead regions on the module, the area between the chips is specially designed. The pixels between the long sides of the chips are enlarged to $50 \times 600\,\mu\text{m}^2$. In the region of the short side of the chips there are 8 uncovered pixels. The uncovered pixels are combined to a connected pixel each, so there are 4 electronics circuits for each column in the FE chip which are connected to two pixels each. The top metallisation of the sensor is shown in Figure 3.8. The pixel structure can be seen and the chip edges are indicated. The connection between the pixels is visible.

As a result, one has to distinguish different types of pixels on the module. The normal cells ($50 \times 400\,\mu\text{m}^2$), the long cells ($50 \times 600\,\mu\text{m}^2$), the ganged cells which have two pixels connected to one electronics circuit, and the pixels which are long and ganged.

Isolation

On n^+ on n sensors the cells have to be isolated against their neighbours. The n^+ implants are in an n-type bulk, so there is an ohmic contact. For isolation there has to be a pn junction in between the pixel implants. The standard technique to isolate the pixels is the p-stop technique. It foresees an additional p-implant between the pixels. This highly doped p-implant stops the electron travel (p-stop). This technique has some disadvantages, such as an additional processing step (more expensive), and increasing field gradients with irradiation. To avoid this, the pixel sensors are isolated by the p-spray technique. Here the whole sensor surface is coated with a weak p-implant. The layer is sufficiently weak that the properties of the n^+ implants are not changed, but the space between the pixels is now filled with this p-implant, and this yields a pn-junction and suppresses electron travel.
A big advantage of this technology is that the effective doping of the p-spray implant is decreased by radiation due to surface effects. This lowers the field gradient between

the n- and p-implant, while the electron accumulating layer is shielded completely and the high voltage resistivity is increased. The p-spray used for the ATLAS pixel detector is a moderated p-spray, which means that the doping has a gradient from the middle between the pixel to the pixel implants itself. This increases the high voltage stability before irradiation.

Guard Ring and Bias Grid

The cutting edges of the sensor are electrically conductive. Therefore, it is necessary to isolate them from the high voltage on the sensor. This is done by a structure called "multiguard rings". It consists of 17 p^+ rings on a floating potential around the backside implant. The high potential is decreased from ring to ring and this prohibits a direct contact between the sensor edge and the implant for the high voltage.

For testing purposes all of the 46080 sensor pixel cells are connected to a bias grid. This allows one to bring all pixels to a defined potential for testing the cells without any electronic chips connected to the sensor. To avoid shorts between the sensor cells through the bias grid, the punch through effect is used. The resistance of the contact is high for low potentials and low for high potentials. In case of a disconnected pixel (missing bump) the punch through contact to the bias grid prohibits an uncontrolled high potential in this pixel [26, 29].

When connecting the read out chips to the sensor cell, the implant of the pixel is connected to the input potential of the amplifier and the bias grid is kept floating. The potential difference between pixel and bias grid is normally small and the pixels are not shorted by the bias grid.

3.1.3 Pixel Front-End Electronic

Sixteen ASIC's – the Front End chips – are placed on the pixel module. These chips have been developed especially for the pixel detector. They are designed in a radiation hard "deep submicron" technique [30] and are produced in a $0.25\,\mu$m-technology at IBM. Each chip has a size of 7.2×10.8 mm^2. It supports 2880 pixels arranged in 18 columns and 160 rows.

The supply for the chip is provided as a voltage of 1.6 V for the analog part (VDDA) and 2.0 V for the digital part (VDDD). The main ground connection between these two voltages is on the flex.

Requirements

The pixel detector must meet special requirements in terms of its environment and its functionality. It has to measure the passage of ionising particles with 3 space points.

The most probable energy which a MIP deposits in the $250\ \mu$m thick sensor results is a collected charge of around $20000\,e^-$. Assuming the particle crosses at 90° to the sensor plane, the charge can be shared between up to 4 pixels. In case of equal charge sharing the pixel cell has to recognise a charge of $5000\,e^-$. If this amount of charge is not recognised the hit is lost. Due to the geometry of the pixel detector setup inside the magnetic field the expection of cluster sizes is about 50% single hits and about 50% double hits.

Ideally the pixel detector is able to measure a charge of $5000\ e^-$. Two contributions have to be controlled for this. On the one hand there is a detection (discriminator) threshold which can be adjusted. Normally this threshold will be set to $4000\ e^-$. On the other hand the hit has to be associated to the correct bunch crossing, meaning to the correct 25 ns time frame. This is achieved for particles which deposit at least a charge of $1500\,e^-$ above the discriminator threshold. This effect is described in more detail later on in the timewalk description in this Section and in the test beam analysis (see Chapter 7). This leads to minimal charge which is measured in the correct trigger window of $5500\ e^-$. The module is able to compensate the wrong measured bunch crossing association internally, which is a feature of the Front-End chips, named *hit doubling*.

The discriminator threshold is necessary to reduce noise hits in the pixel cells as much as possible. The threshold values of the pixels on the module are gaussian distributed (threshold dispersion). Additionally, there is the noise of the electronics-sensor combination. For good performance the following equation should be valid:

$$\text{Noise}^2 + (\text{threshold dispersion})^2 \leq (500\ e^-)^2 \tag{3.2}$$

For a threshold of $3000\ e^-$ this is equivalent to a 5σ distance. For the ATLAS pixel detector the noise is required to be below $400\,e^-$ and the threshold dispersion below $300\,e^-$.

The spatial resolution of a pixel detector is dominated by the size of its pixel cells. The size of each pixel cell itself is limited by the area the electronics needed. The geometry determines the spatial resolution of a detector by:

$$\langle \Delta x^2 \rangle = \frac{1}{p} \int_{-p/2}^{p/2} x^2 dx = \frac{p^2}{12} \tag{3.3}$$

Where p is the pitch of the pixels. For the short side (Φ-direction) of the pixels this is $\langle \Delta x^2 \rangle = 14.4\ \mu$m and for the long side (z-direction) $\langle \Delta x^2 \rangle = 115.47\ \mu$m. To increase the resolution, the pixel electronic is able to measure roughly the deposited charge. From this measurement the precision of the position measurement can be increased for double hits to about $8\ \mu$m for the Φ-direction [31]. The detector orientation relative to the particle track is optimised for having 50% single hits and 50% double hits, taking into account the magnetic field the pixel detector is located in.

To minimise the uninstrumented region neighbouring modules overlap with each other. In addition, the deadtime for the pixels is required to be small. The hit rate for a pixel in

Physics Requirements	
spatial resolution in Φ	$< 15\,\mu$m
spatial resolution in z	$< 120\,\mu$m
efficiency	$> 94\%$
LHC Environment Requirements	
radiation tolerance	> 50 MRad or $10^{15}\,\frac{1\,\mathrm{MeV}n_{eq}}{\mathrm{cm}^2}$
time resolution	$< 25\,ns$ for $(100000\,e^- > q > 5000\,e^-)$
Requirements for the Electronics	
pixel size	$50 \times 400\,\mu\mathrm{m}^2$
noise	$< 400\,e^-$
threshold uniformity	$< 300\,e^-$
threshold	$\leq 3000\,e^-$
cross talk	$< 5\%$
power per FE chip	$< 250\,$mW
masking	all pixels individually
calibration	all pixels individually
leakage current compensation	up to $5\,$nA per pixel
Requirements for the Data Taking / Trigger	
deadtime	$< 2.0\,\mu$s
deadtime in the B-Layer	$< 0.5\,\mu$s

Table 3.2: Requirements for the pixel detector and its electronics [26]

the B-Layer is expected to be about 20 kHz. The deadtime has to be less than $0.5\ \mu$s per hit to be smaller than 1% of the hit rate.

All requirements for the pixel detector have been summarised in Table 3.2.

Pixel Cell

The pixel cell electronics, as shown in Figure 3.10 can be separated into an analog and a digital part. In the analog part there is a fast preamplifier which integrates the sensor charge into a feedback capacitor and discharges it with a constant feedback current. The outgoing signal is amplified in a second stage differentially. The second part of this signal comes from a replica circuit which reproduces the DC potential of the first amplifier part. The subsequent discriminator translates the analog pulse signal into binary hit information. On the starting and ending of the binary signal a time stamp is stored into a RAM which can be read out. The time stamp is generated by an internal counter which is synchronised with the 40 MHz system clock. Additionally, the binary hit information is fed to a hitbus. This hitbus is ”ORed” over each column and can be used as a trigger signal or for test purposes. The hitbus is not used in the physics data taking.

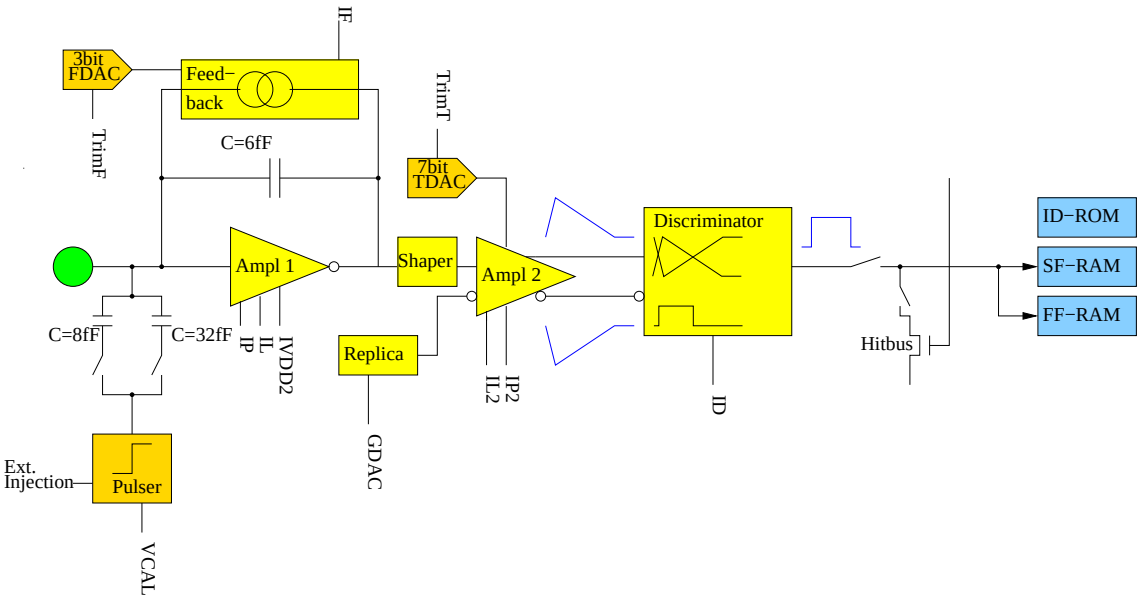


Figure 3.10: Schematic of the pixel unit cell.

The discriminator threshold can be set in two ways. The global threshold of the module can be set through a DAC (named GDAC) and each pixel has an individual 7-bit-DAC (named TDAC) to adopt the threshold and reduce the variation of the pixel thresholds over the module.

The analog information of the incoming pulse is translated into the length of the digital signal. A schematic of this is shown in Figure 3.12. Because of the constant discharging current the signals time above threshold is proportional to the height of the signal and, therefore, the duration of the digital signal is proportional to the deposited charge. This is called TOT, for Time Over Threshold. The TOT is measured in clock cycles of $25\,\mathrm{ns}$ length and can be up to 255 clock cycles (8 bit).

To reduce the variation of the TOT behaviour through out the module there is the possibility of adjusting the feedback current and with this the steepness of the discharging curve in each pixel by setting the FDAC's.

Each pixel has a 14 bit memory in which the pixel settings are stored. Seven bits are reserved for the TDAC settings, 3 bits for the FDAC settings, and the remaining 4 bits are used for enabling the pixel for different scenarios: The *enable* bit enables the pixel for readout, the *hitbus* bit sets it on the hitbus line, the *kill* bit disables the preamplifier, and the *select* bit chooses the pixel for test pulses. The DAC's, their meanings, and the nominal values are giving in Table 3.3.

To test the pixel cells there are two capacitors C_{low} and C_{high} in each cell on which one can pulse a charge and bring a signal into the electronics without the sensor. The pulsing

DAC	Meaning	nominal Value
IP	preamplifier current	$8\,\mu$A
IL	load current of the preamplifier	$1.5\,\mu$A
IP2	current for the 2nd preamplifier	$4\,\mu$A
IL2	load current for the 2nd preamplifier	$3\,\mu$A
IVDD2	current for setting the reference voltage	$250\,$nA
IF	feedback current	$4\,$nA
ID	discriminator current	$5\,\mu$A
GDAC	global threshold setting	-
ITH1	alternative threshold setting 1	-
ITH2	alternative threshold setting 2	-
TrimT	stepsize for the threshold TDAC settings	-
TrimF	stepsize for the FDAC settings	-
MonADC	leakage current measurement	$(0.125 - 128)\,$nA
VCAL-I	calibration current	$(0.5 - 511)\,\mu$A

Table 3.3: The DAC's of the front and chip and their meaning [26].

can be done externally or internally by the chip itself triggered by a strobe signal. It can be pulsed into the analog part or directly into the digital part.

Figure 3.11 gives an overview of how the pixel cells are read out. If a pixel registers a hit, the timestamp of the raising edge is stored into a RAM, named RE-RAM, and the timestamp of the falling edge is stored into a RAM, called FE-RAM. These timestamps are generated by a counter running with the 40 MHz system clock. The readout logic is organised column pairwise, and after the hit registration inside the pixel is completed, a "hit-mark" is given to the double column control. This initiates the readout of the whole column pair connected to it. All hits which appeared in this double column are then read out into the memory buffer.

If a trigger is set, the difference between the trigger timestamp and the latency is calculated and all hits which conform to this timestamp are read out through the serialiser into the module control chip.

Timewalk

As described, the time stamp for the signal crossing the discriminator threshold in the electronics circuit is stored for assigning the hit to a certain LVL1 trigger and therefore to a certain bunch crossing. As visualised in Figure 3.12, the steepness of the rising edge of the signal inside the electronics depends on the collected charge (signal height), and with this on the deposited energy. The time between the start of the pulse and its maximum is for all hits the same. This means the position of the pulse maximum is always the same. This is why more charge collected in the electronics causes a faster rise of the pulse and

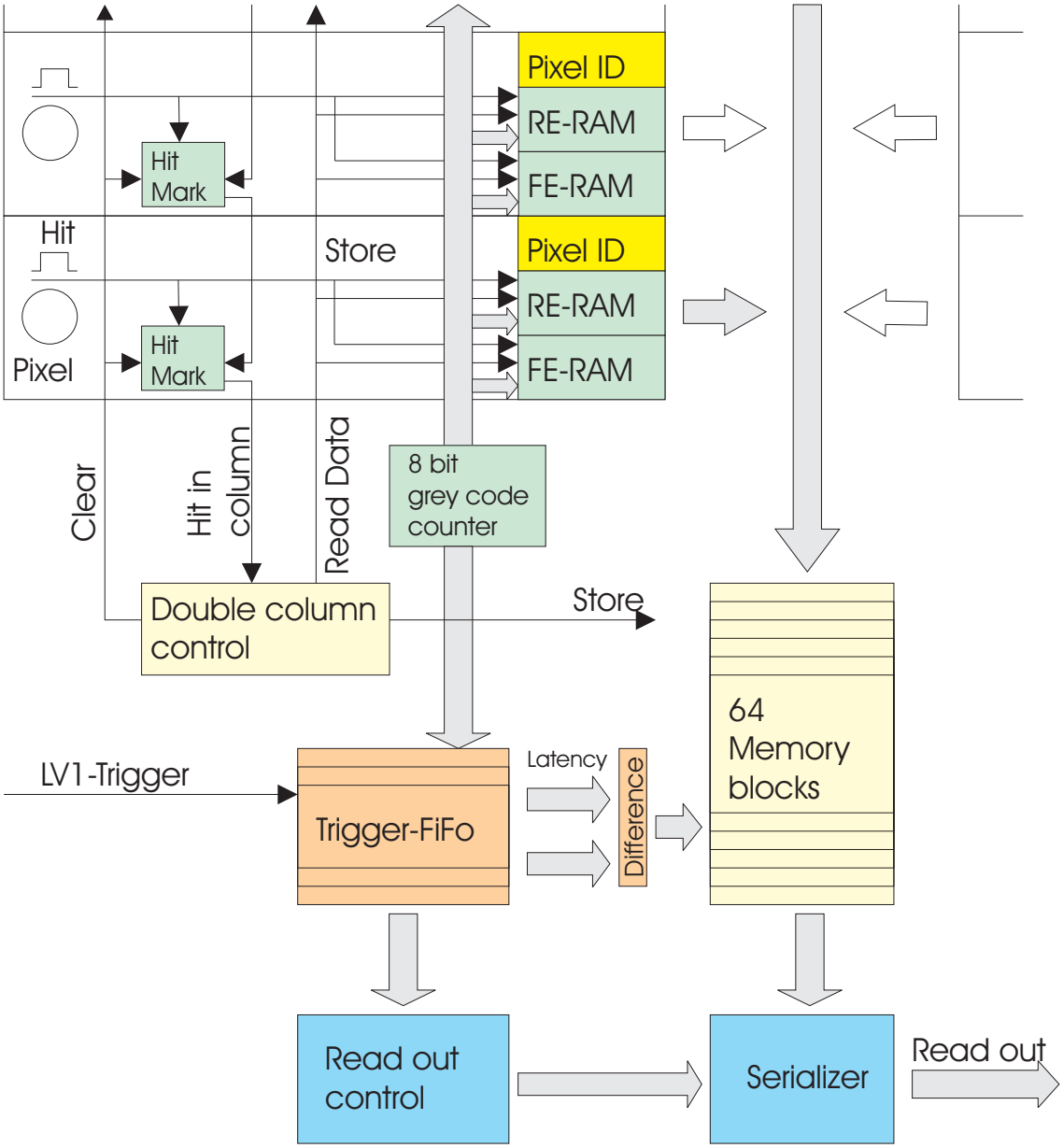


Figure 3.11: Schematical overview of the readout of hits from a pixel cell.

therefore a shorter time until the threshold is crossed, while less charge collected causes a slower rise of the pulse and therefore a larger time until the hit crosses the threshold. This leads to low energy hits coming from bunch crossing x, but being registered and read out for bunch crossing $x+1$, because of a slow rise time of the signal. As already mentioned, the timestamp is generated with a 40 MHz clock, so hits being registered inside a 25 ns window are assigned to the same bunch crossing. The timing of the module has to be

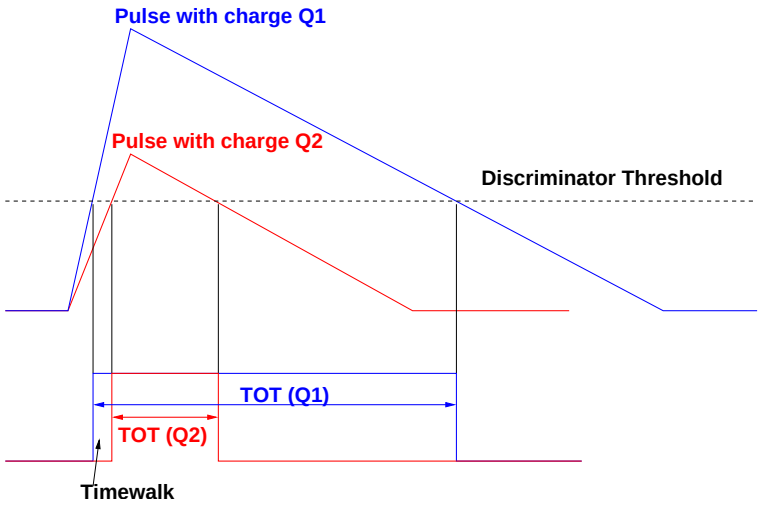


Figure 3.12: Schematic of hits with different energy deposition in the detector.

adjusted correctly to the bunch crossing to set the read out window optimal for registering as many hits as possible for the correct bunch crossing.

To determine the energy of the hits which get lost through a too long registering delay, a *timewalk* measurement can be performed. By timewalk, one refers to the minimal charge which can be associated to the correct bunch crossing. The measurement principle is shown in Figure 3.13.

The diagram shows a strobe signal which generates a pulse into the electronics circuit,

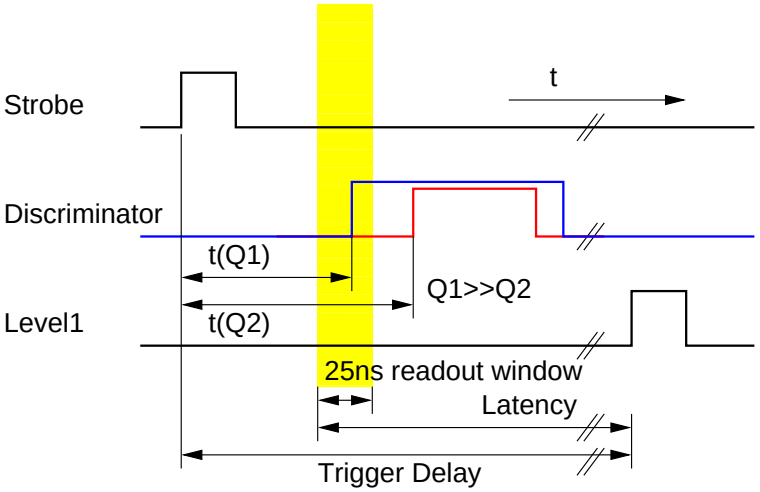


Figure 3.13: Principle of timewalk measurement [26]. The read out window (yellow) is shifted by the latency setting. Pulses of different height are illustrated (see Figure 3.12).

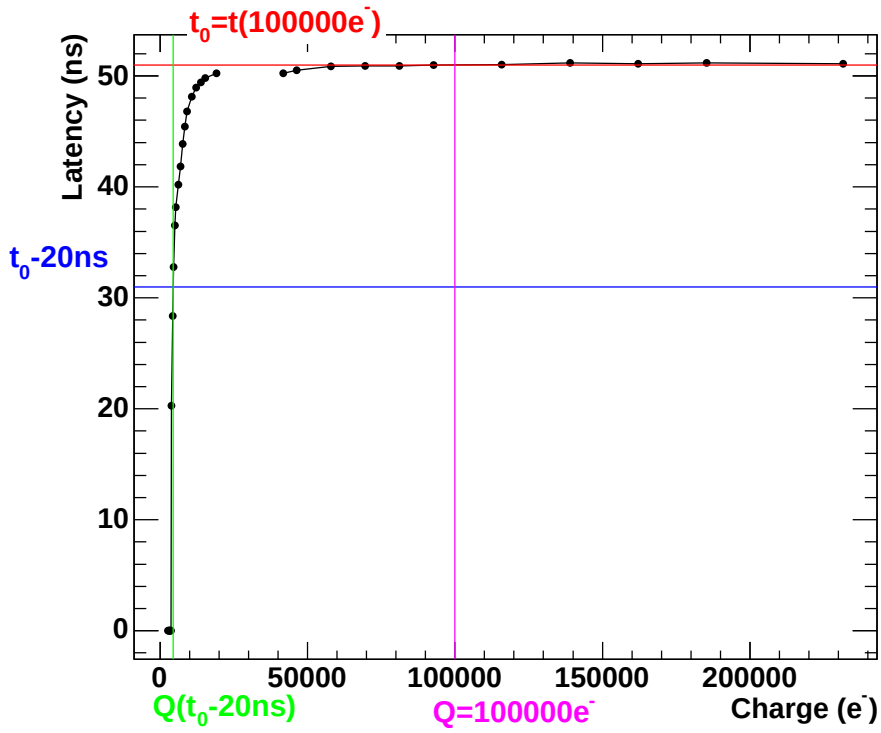


Figure 3.14: Measured timewalk of a single pixel with low and high injection capacity. The data reflects the latency at which 50% of the hits generating the given charge are registered.

a discriminator signal for two different pulse heights, and a Level1 trigger signal. The time between the strobe and the discriminator signal depends on the pulse height, which in turn depends on the charge generated in the sensor. The readout window is shifted against the Level1 trigger by shifting the latency. If the raising edge of the discriminator signal is inside the readout window, the hit will be read out. Measuring the percentage of registered hits against the shifted time, and plotting the time at which 50% of the hits are registered, results in a plot as shown in Figure 3.14[a].

For extracting the timewalk from this, the time t_0 at which 50% of a $100000\ e^-$ signal injected into the capacitor of the electronics circuit are registered is to be measured. Now the injected charge which starts to be registered 20 ns later is measured. This charge is the minimal charge which can be measured inside the trigger window, taking 5 ns as safety margin as a convention. The minimal charge which can be registered in the trigger window has to be less than $5000\ e$ to be able to register a MIP sharing its energy equally between four pixels, as described above. The timewalk behaviour and the possibility to

[a]This measurement is a superposition of two measurements with the two capacitors in the electronic circuit of each pixel.

Bit position	Name	Description
FE-FLAG[8]	HitOverflow	There has been a Hit overflow inside the corresponding receiver block.
FE-FLAG[9]	EoEOverflow	There has been an EoE overflow inside the corresponding receiver block.
FE-FLAG[10]	Lv1ChkFail	The LV1ID check inside the corresponding receiver has failed.
FE-FLAG[11]	BCIdChkFail	The BCID check between EoE words belonging to different FE's has failed.
FE-FLAG[12]	Lv1ChkFail	The LV1ID check between EoE words belonging to different FE's has failed.
FE-FLAG[15:13]	Empty	This three bits are always 000.

Table 3.4: Definition of the MCC generated warnings [32].

adjust the pixel module timing with respect to the system clock has been studied at a test beam setup. The measurements and results are discussed in Chapter 7.

3.1.4 Module Control Chip

The module control chip (MCC) [33] is the interface between the front end chips and the readout. It fulfils three main tasks: the chip receives the configuration, converts it, and passes it to the front end chips; it distributes the received trigger signals to the front end chips; and it reads the hit data from the front end chips per event (event fragment building) and sends it to the readout.

Trigger signals can be sent to the MCC for reasons of data taking (level-1 trigger) or for calibration and tuning runs (strobe signals). The MCC receives the trigger signal and distributes it to the 16 front end chips. Additionally, the MCC generates different reset signals to synchronise with the data acquisition and to reset the front end chips in case of errors.

For a given trigger the front end chips send the hit data to the MCC, which forms an event from it and passes this to the readout electronics.

Figure 3.15 depicts a block schematic of the MCC. It shows two ports, the module port as the interface between the MCC and the readout electronics, and the front end port as the interface between the MCC and the front end chips. The module port consists of 3 LVDS inputs for clock and data input and 2 LVDS outputs for returning the data. The data outputs DTO and DTO2 can be used in several modes: the MCC can send data in 40 Mb/s or 80 Mb/s on each line, so that the total transfer bandwidth can be 40 Mb/s (one data out with 40 Mb/s), 80 Mb/s (one data out with 80 Mb/s or two data out with 40 Mb/s), or 160 Mb/s (two data out with 80 Mb/s).

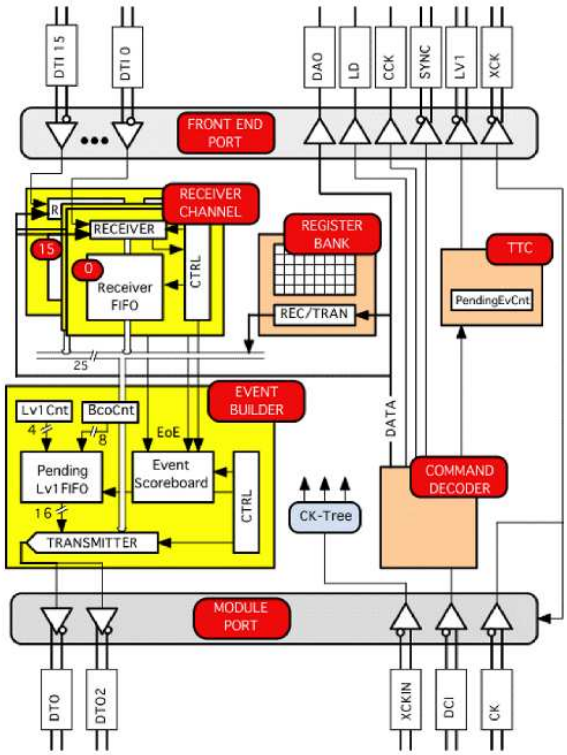


Figure 3.15: Block diagram of the MCC logic [33].

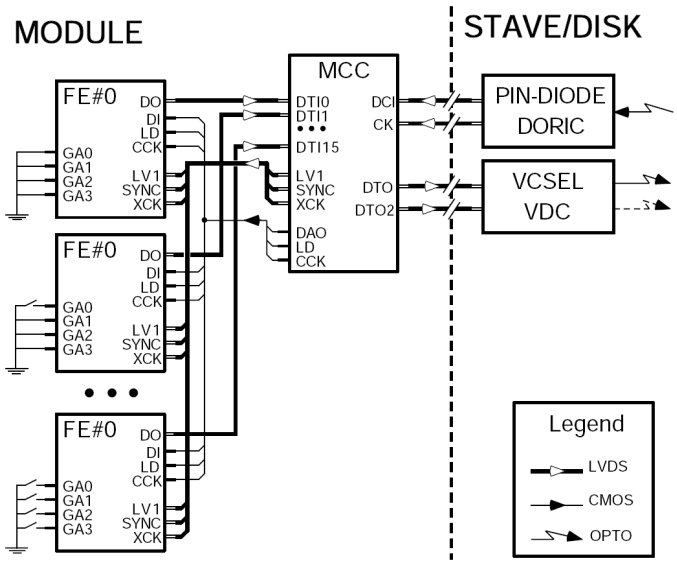


Figure 3.16: Sketch of the MCC to module communication [33].

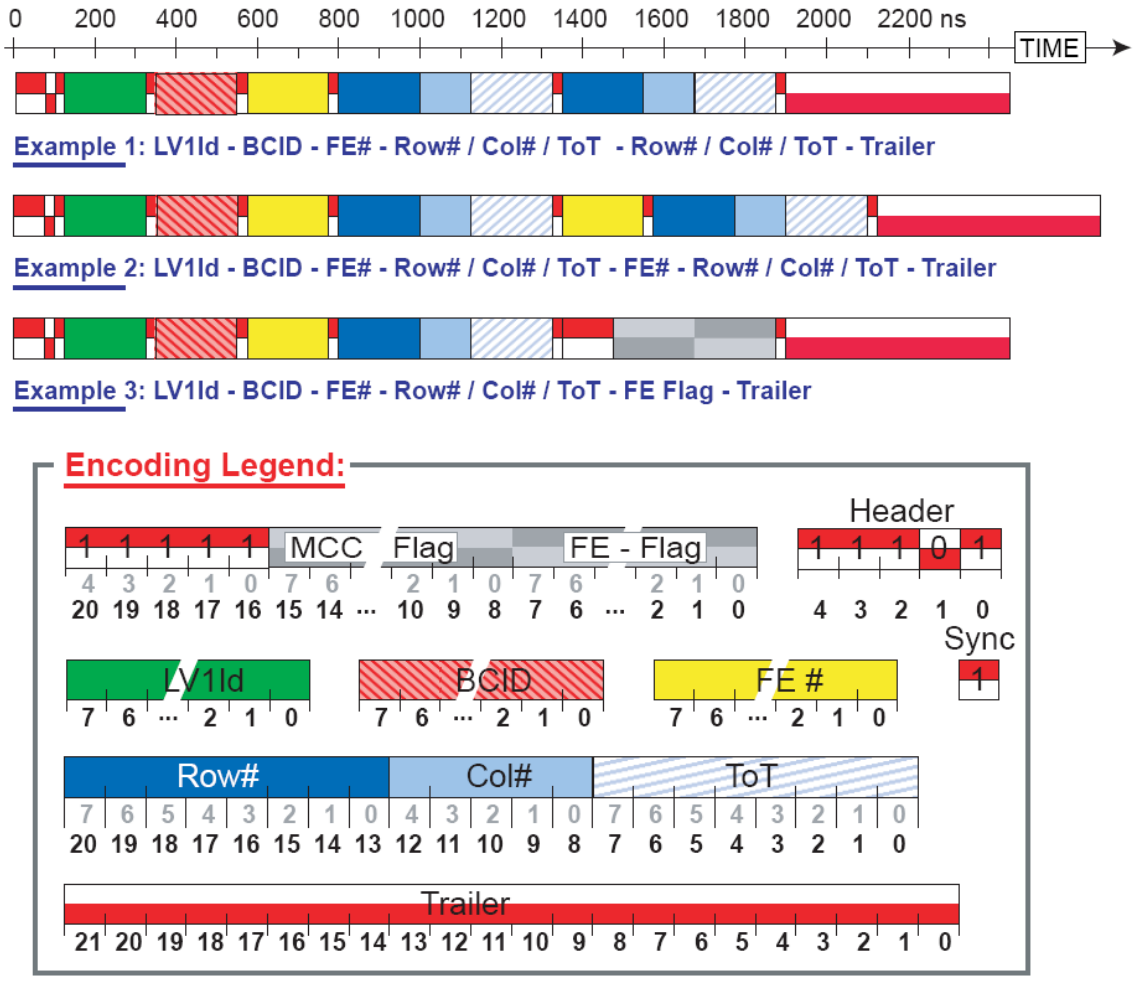


Figure 3.17: Data flow in the module control chip [32].

The front end port consists of 7 output lines and 16 input lines. While the signals DAO, LD, and CCK are distributed over single ended signals to the front end chips, the timing-critical signals XCK, LV1, SYNC, and STROBE are distributed via multidrop differential lines to the chips. The front end chip output is connected via a differential line per chip to the MCC. For each trigger the 16 front chips pass the hit data to the MCC. If a chip response misses for a given trigger signal, the MCC raises an error or warning flag in the data output. These flags are summarised in Table 3.4.

The data format of the communication of the MCC with the read out electronics is shown in Figure 3.17. First a header is transmitted followed by the Level1 ID and the bunch crossing ID. After this the front end number, the column, the row, and the TOT of each hit is transmitted per chip. If there have been any errors the error flags are attached and a trailer finalises the read out data.

3.2 The Pixel Detector Read Out: The Optical Link

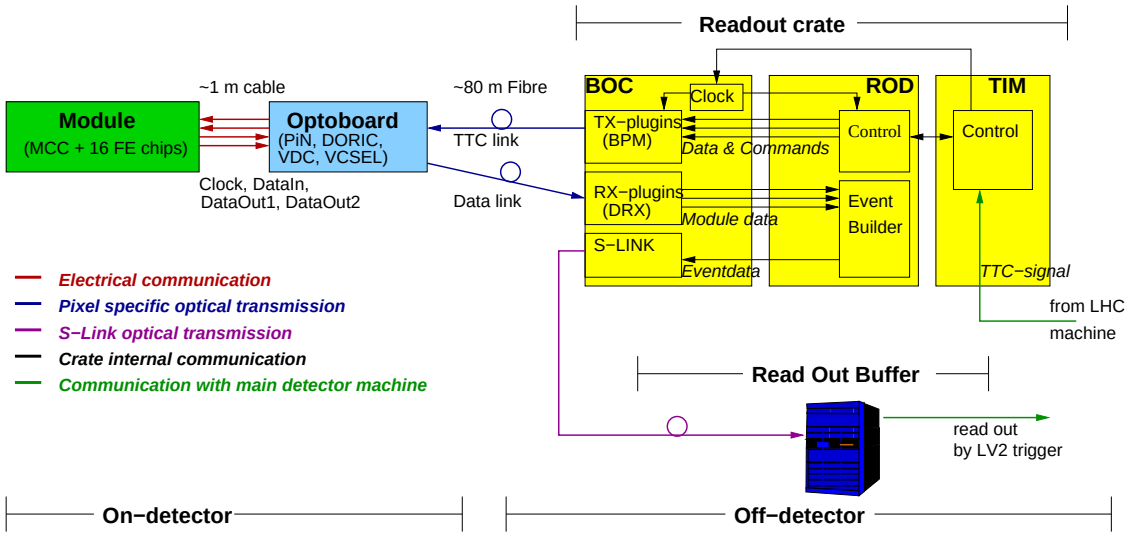


Figure 3.18: The readout chain of the pixel detector.

The communication between the pixel detector and the off-detector electronics in the counting room employs fibre optic data transmission. Therefore, on each side – on-detector and off-detector – an opto-electrical interface is needed. The on-detector interface is the optoboard, which is connected via optical fibres to the off-detector interface, the Back of Crate card (BOC). Each optoboard is connected to either a half stave or to a sector. Six or seven modules are connected to one optoboard. This ensures not to loose too many modules in case of an optoboard error on the one hand and not to install too much material in the detector volume on the other hand.

Per module one fibre is needed for the clock and command transfer from the off detector electronics to the module and one or, for the B-Layer modules, two fibres are needed for the data transfer from the module to the counting room. The fibres have a length of about 80 m. The data transmission is done unidirectional on each fibre.

The opto electrical interface in the counting room, the Back of Crate (BOC) card, is paired to a Readout Driver (ROD). Depending on the detector part and, therefore, on the used bandwidth, 1, 2, or 4 optoboards are connected to one BOC card. 132 BOC card / ROD pairs are needed for the read out of the ATLAS pixel detector.

The ROD‘s and BOC cards are localised in nine 9U VME crates which are controlled by a single board computer each. The single board computer has an ethernet connection to the computers steering the data acquisition. Additionally, in each crate there is one interface card for the timing and trigger commands coming from the LHC machine, the Timing

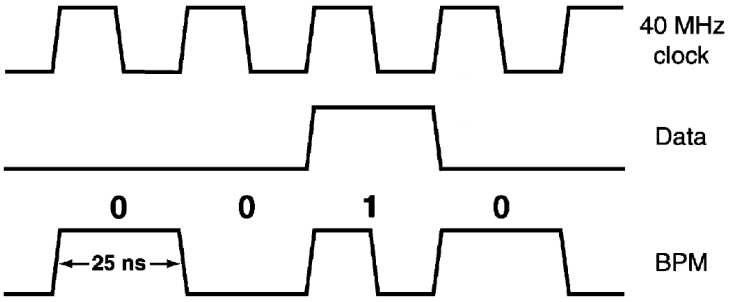


Figure 3.19: The principle of the bi phase mark encoding. The clock and the data signal are encoded into a BPM-signal

Trigger and Control Interface Module (TIM). For data storage, an optical transmission line will be established between the BOC cards and the Readout Buffer (ROB). All of these components and their functions are described in more detail in the next sections. For a schematic overview, see Figure 3.18.

A main feature of the pixel detector electronics is to have all timing capabilities in the off detector electronics. Each BOC card receives the clock from the LHC machine and distributes it to the paired ROD and each connected module. All timing adjustments are done on the BOC card. As already mentioned, the communication from the BOC card to each module is done via one single fibre. Therefore the clock and the data have to be encoded into a single signal. This is realized as a BPM[b] - signal. Figure 3.19 shows the principle of the BPM encoding.

The biphase mark encoding scheme is a DC balanced code which creates a transition for each rising edge of the clock and an extra transition for a data one on the falling edge of the clock [34]. The encoded signal is sent down to the optoboard optically.

3.2.1 Optoboard

The optoboard [35] is the opto-electrical interface in the detector area. It is a 2×6.5 cm^2 beryllium-oxide (BeO) printed circuit board. The optoboards are located on the patch panel 0 (PP0) near the pixel detector. Here the connections between the optoboard and the modules are realised. Six or seven modules are connected electrically to an optoboard.

In the pixel detector there will be two flavours of optoboards, the B-boards and the Disk-boards. The Disk-boards are foreseen to connect the modules on the Disks, Layer 1, and Layer 2 to the readout electronics, while the B-boards are designed especially for the B-Layer modules. The Disk-boards are equipped with one 8-way PiN diode array and one

[b] BPM : BiPhase Mark encoding

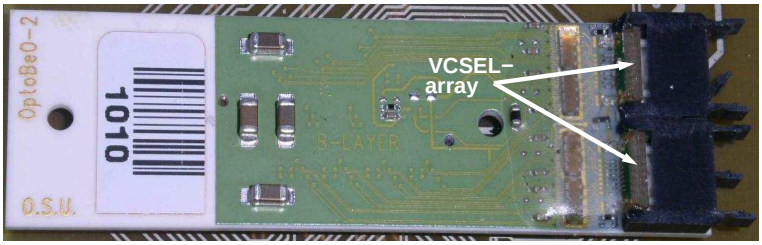


Figure 3.20: The optoboard. A B-Layer board is shown with two VCSEL-arrays. The dimensions are 2×6.5 cm^2.

8-way VCSEL[c]-array, while the B-board has one additional 8-way VCSEL-array. The B-Layer modules are read out at 160 Mb/s. This can only be performed by two data lines (DTO and DTO2) running at 80 Mb/s. Therefore, each B-Layer module needs two connections from the optoboard to the counting room. The modules on the Disks and Layer 1 are read out at 80 Mb/s, which uses only one data line and one fibre from the optoboard to the counting room. The Layer 2 modules transmit data at 40 Mb/s on one dataline and one fibre. In total, 272 optoboards – 44 B-boards and 228 Disk-boards – are built into the detector (see also Table 4.1).

The connection between the optoboard and the counting room is provided by optical fibres which are ribbonised into 8-way ribbons and will be described later. One ribbon is used for the transfer of the timing, trigger and command signals from the counting room to the detector, called the TTC-link, and one or, in case of the B-Layer optoboards, two ribbons are used for the data transfer from the optoboard into the counting room, called the data link. The communication is done channelwise for each module individually. In order to reduce the material inside the detector the clock and the commands for the module are encoded into one BPM signal which is sent to the optoboard. This way both signals are transmitted by one fibre and received by one PiN diode. The optoboard receives the BPM signal with a PiN diode per channel, and decodes the clock and the data in a special ASIC, the DORIC[d] (see below). The electrical clock and command signals are transferred separately to the module.

The module's MCC sends out the data electrically to the optoboard. The VDC[e] (see below) drives the VCSEL channelwise with the data from one module to send the data to the counting room. As already mentioned the data can be transferred with 40 Mb/s or 80 Mb/s as a "Non-Return-to-Zero"[f] (NRZ) signal on a single optical fibre.

[c] Vertical Cavity Surface Emitting Laser
[d] Digital Opto-Receiver Integrated Circuit
[e] VCSEL Driver Chip
[f] A non-return-to-zero (NRZ) line code is a binary code in which "1s" are represented by one significant condition and "0s" are represented by another, with no neutral or rest condition.

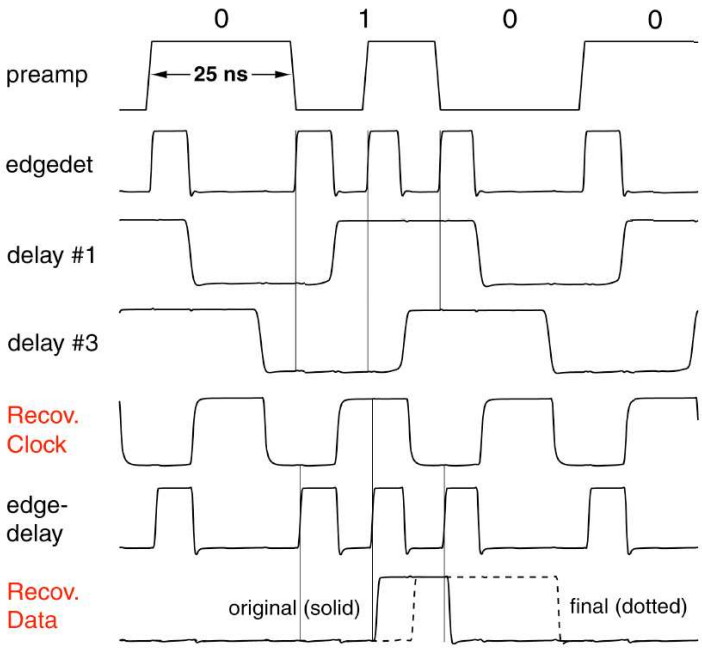
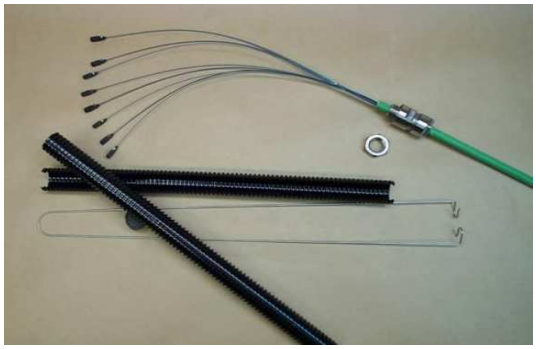


Figure 3.21: Biphase mark (BPM) decoding [35].

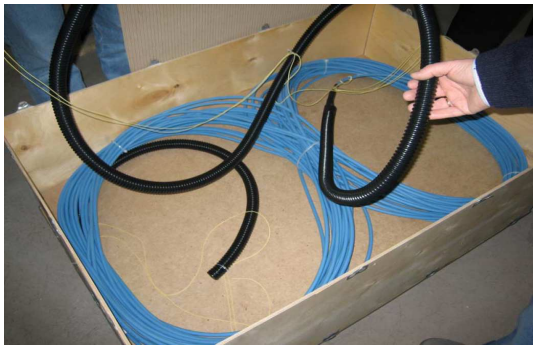
DORIC

The DORIC [35] receives the electrical signals the PiN-diode converts from the light signals. It is a four channel chip and its function is to decode the BPM encoded clock and command data. The working range of the DORIC is between $40\ \mu A - 1000\ \mu A$ input current. The reconstituted clock is required to have a duty cycle of $(50 \pm 4)\%$ with a timing error of less than 1 ns. The bit error rate of the DORIC circuit is required to be less than 10^{-11} after receiving a radiation dose of 50 Mrad.

Figure 3.21 shows a BPM signal decoding. In case of only zeros being encoded with the clock the signal looks like a 20 MHz clock. The ensure a correct locking into the right frequency the DORIC needs to be reset after power up. During this reset the DORIC has to receive a no-data signal to decode the 40 MHz clock correctly. The recovered 40 MHz clock is used as an input to a delay-lock loop which adjusts the internal delays until a 50% duty cycle is reached. After locking into the right frequency, the clock recovering circuit is blind to transitions in the middle of the 25 ns intervals. The data recovery circuit is sensitive to each edge of the input signal and recovers it as data if the recovered clock is high and as no data if the recovered clock is low. This signal is then synchronised to the recovered clock. Clock and data are transmitted to the connected module as differential signals (LVDS).



(a) The optical ribbons bundled into a cable.



(b) A final optical cable containing eight ribbons.

Figure 3.22: The optical fibres are arranged into ribbons (a) with 8 fibres each. Eight ribbons are bundled into a cable (b). Figure b) shows a 79.2 m long cable ready for installation into the ATLAS experiment is shown.

VDC

The VDC is also a four channel chip, and its function is to convert the LVDS signals coming from the modules into signals to drive the VCSEL channels. The output current of the VDC is contolled by an external current control and can be varied between 0 mA and 20 mA. To increase the switching speed of the VCSEL, a dim or standing current of ~ 1 mA is given always to the VCSEL. To reduce the electrical noise on the optoboard the current consumption of the VDC is kept independent from the laser state. If the laser is in the off state, a dummy load consumes the power which the laser consumes in the on state.

3.2.2 Optical Fibres

The fibres [36] which make the connection between the optoboard and the readout electronics are comprised of three parts. In the inner region of the detector they have to withstand a very high radiation level, while in the outer region of the detector the radiation level is less severe. Therefore, a combination of radiation hard and radiation tolerant fibres will be built in. The radiation hard fibre is a SIMM[g] fibre with a core diameter of 50 μm and the radiation tolerant fibre is a GRIN[h] fibre with two different core diameters. For the connection from the optoboard to the readout electronic a GRIN fibre with core diameter 62.5 μm is used and in the opposite direction a fibre with core diameter 50 μm is used.

Two connections have to be in the fibre routing. Outside the pixel detector support tube patch panel 1 (PP1) is located. At this patch panel all supply and data lines will have a

[g] stepped index multimode
[h] graded index multimode

connector. The pixel detector is the last subdetector which will be installed in the ATLAS experiment. Therefore, all fibres and cables from patch panel 1 to the control rooms are to be installed earlier and will be connected after the pixel detector will be in place. Between the optoboards at PP0 and the connectors at PP1 bare ribbons of eight fibres each will be installed. The length of the ribbons will be 2260^{+0}_{-60} mm or 2510^{+0}_{-60} mm depending on the position [37]. Between PP1 and the counting room optical cables [38] of $79.2^{+0.2}_{-1.7}$ m length will be installed. The cables are comprised of eight ribbons each. In total 84 cables will be installed into the ATLAS experiment.
The second connection is between the SIMM and the GRIN fibre. This connection is done by splicing. The splicing is done ribbonwise already at the vendor site. It is contained in the cables and will be located near the muon detectors, roughly 9 m away from PP1.

3.3 The Back of Crate Card

The BOC card is the main part of study for the work described in this thesis. It is therefore explained in more detail in Chapter 4.

3.4 The Read Out Driver

The Read out Driver (ROD) is the main card for data taking for the Pixel detector. Figure 3.23 shows a ROD. Its purpose is to generate the commands for the modules, format the event from the modules data, and provide monitoring capabilities during the data taking. Also, the trigger is received by the ROD directly from the TIM (next section) and passed to the connected modules. The main control on the ROD is done by a controller FPGA and a Master DSP. All actions of the ROD are initiated by these chips. The ROD receives the detector data from the BOC card in 8 formatter FPGA's. Here the format of the data is checked and a reformatting of the data arriving in multiple streams (for the higher bandwidth modes) is performed. The data is then handled by the event fragment builder FPGA. The event fragment builder checks the data for detecting errors in the header or trailer, MCC errors, FE chip error flags or to detect unphysical data. The event fragment builder rearranges the data according to the trigger and passes it to the router FPGA. The router formats the data to its final format and drives the data out to the Read out Buffers via the S-Link card on the BOC card. Additionally, parts of the data are copied to the Slave DSP's which perform histogramming for the online monitoring. These histograms can be read out via the VME interface.

132 ROD's are needed for the ATLAS pixel detector. Each ROD has its own optical interface, the BOC card. They are paired back to back in 9U VME crates, which can be equipped with up to 16 ROD's each.

Figure 3.23: Readout Driver (ROD) for the pixel detector.

3.5 The Timing, Trigger, and Control Interface Module

The TTC Interface Module (TIM) is the interface between the off-detector electronics and the ATLAS Level-1 trigger. Each readout crate contains one TIM which receives the TTC signals and transmits the required information to the ROD's via a custom backplane. The TIM can also enable the crate for a stand-alone mode by generating the signals as requested by the local processor.

TIM-3, as shown in Figure 3.24, is the final version of the TIM. 24 TIM's have been produced, 14 for SCT and 10 for the pixel detector needs.

3.6 The Readout Crate Controller

The ROD Crate Controller (RCC) is a single board computer. On this computer the local steering software for the cards in the crate is running. It controls up to 16 ROD/BOC pairs

[h]TTC: Timing, Trigger and Control

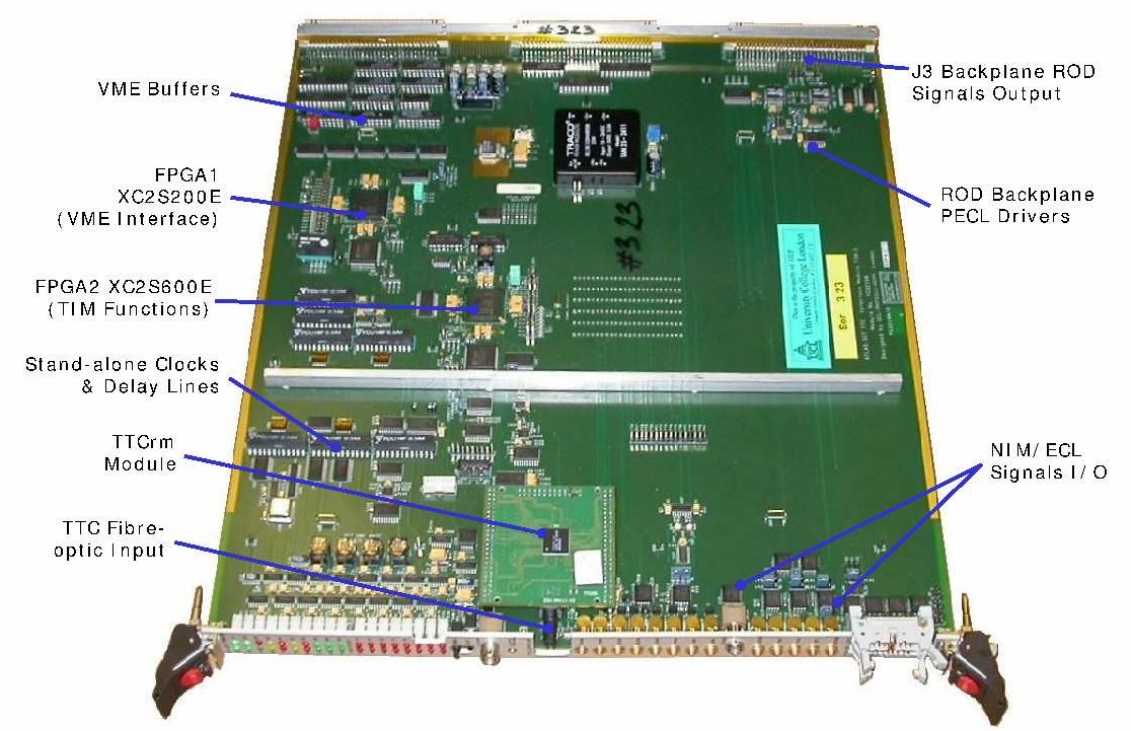


Figure 3.24: The TIM (TTC Interface Module) [39].

and the TIM. The controller is connected to the ATLAS data taking software over ethernet connections and has to operate on commands of the DAQ / DCS software. Additionally, it provides the functionality to operate the crate independently for configuration, calibration, and similar tasks.

Chapter 4

The Back of Crate Card

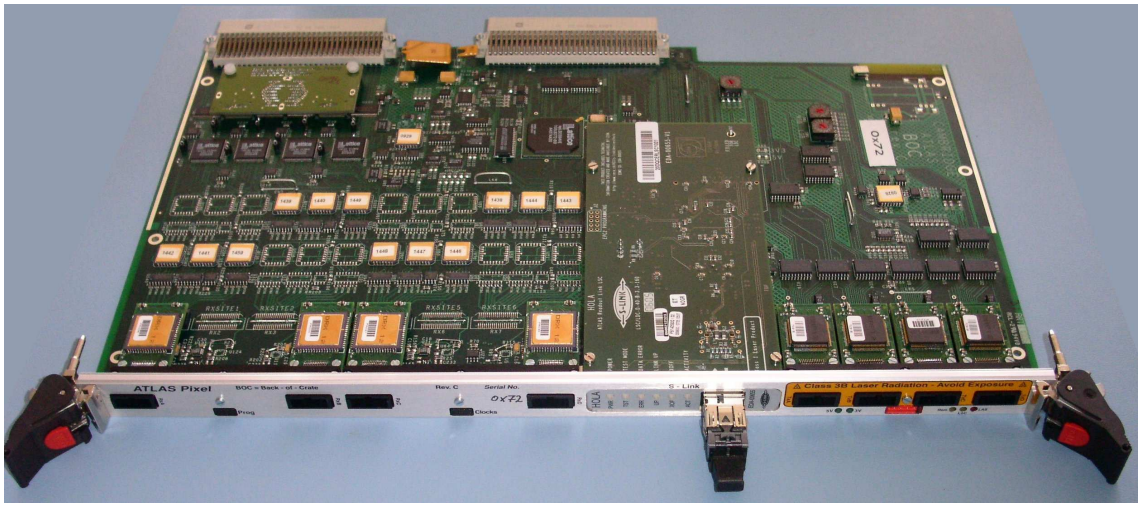


Figure 4.1: Back of Crate card in pixel assembly.

The Back of Crate (BOC) card is a main part of the optical data transmission line for the ATLAS pixel detector in the counting room. As can be seen in the description of the read out scheme in Chapter 3, the BOC card serves as the optical interface for the off detector part and provides the complete timing functionality for the ATLAS pixel detector and its read out. The functionality of the BOC card is the main topic of this work.

As part of this work the BOC card has been introduced into the read out chain of the system test in Wuppertal and its functions have been implemented in the system test software and in the data acquisition software for the final read out. Additionally the timing functionalities have been tested in a test beam setup at CERN, see Chapter 7. To get a better understanding of the work done with this card the BOC card is described in more detail in this chapter.

As the name indicates, the Back of Crate card is located on the back side of the ATLAS readout crates. 132 BOC cards are needed in total for reading out the ATLAS pixel detector. The cards are placed in 9 read out crates. At maximum 16 BOC cards can be situated in one crate. Each of the BOC cards is paired with a Readout Driver (ROD).

The BOC card is a 9U VME 64X transition card, which has been developed by the group of the Cavendish Laboratory in Cambridge. It interfaces the ROD to the detector electronics and to the Readout Buffers (ROB). Additionally the BOC card performs timing and data recovering tasks.

The BOC card has to provide the following functionalities:

- Receive and distribute the clock signal as provided by the TIM.
- Receive the electrical control signals for the modules from the ROD, convert them to Bi-Phase Mark encoded optical signals, and dispatch these down the clock and control fibres to the detector modules.
- Provide masking, timing, and laser current adjustment functions for the transmitted control signals.
- Receive the optical data packets from the detector modules via the fibre ribbons, convert them to electrical form, and pass them to the ROD.
- Provide a timing adjustment, threshold adjustment, and clock synchronisation for the received optical data.
- Take the data stream from the ROD in parallel form, and provide the S-Link path via the Readout Buffer to the DAQ.
- Provide a laser safety interlock.

The BOC card has been designed for two subdetectors, the SCT and the pixel detector in the ATLAS experiment. The board design is the same for both of them. Because of the bandwidths the Readout Driver can handle, the pixel BOC card will serve less modules than the SCT BOC card. The modularities and data transmission bandwidth used in the pixel detector has been adopted to the geometry and the occupancy of the detector. In addition, the SCT will have two connections from one module to the BOC card while the pixel detector will have only one. This leads to an unused section on the BOC card, which will not be assembled with components on the pixel BOC card. Due to the modularity described in Chapter 3, the optical-electrical converters for pixel provide eight channels instead of the twelve channels for SCT.

Each pixel BOC card can serve up to 32 pixel detector modules[a], while the SCT BOC cards serve 48 SCT-modules each. The number of channels used depends on which part

[a]Due to modularities not all channels will be used. Maximal 26 modules will be connected to one pixel BOC card.

Detector part	Staves/ Sectors	BOC cards	Optoboards		Comment
B-Layer	22	44	44	(B)	A half stave per BOC at 160 Mb/s
Layer 1	38	38	76	(D)	A full stave per BOC at 80 Mb/s
Layer 2	52	26	104	(D)	A bi-stave per BOC at 40 Mb/s
Disks	48	24	48	(D)	Two sectors per BOC at 80 Mb/s
Total		132	44(B) + 228 (D)		

Table 4.1: Number of parts to read out the complete ATLAS pixel detector, split up for the different detector parts. (B) and (D) indicates the optoboard flavour, B-boards and Disk-boards. The Numbers do not include the foreseen spare channels.

of the pixel detector the BOC card has to support.
For the B-Layer, one BOC card will serve a half stave, meaning six or seven modules, with one *clock and control* fibre for each module and two *data* fibres from each module to the BOC card. On each data fibre the module data is transmitted at 80 Mb/s. This is referred to as the 160 Mb/s mode, realised as a transmission at $2 \cdot 80$ Mb/s.
For Layer 1 and Disks, one BOC card serves a full stave or two sectors, meaning 13 or 12 modules, with one clock and control fibre and one data fibre per module. The transmission of the module data to the BOC card is performed at 80 Mb/s.
And for Layer 2 one BOC card will serve a bi-stave, meaning 26 modules. In this configuration one clock and control fibre and one data fibre is used per module. The module data is transmitted at 40 Mb/s to the BOC card.
In each case the clock and control signals are sent via 8-way ribbons to the modules and the data signals arrive via 8-way ribbons from the modules. These different ”configurations” are listed in Table 4.1.

The different transmission bandwidths on the data fibres to the BOC card imply a different data registering on the BOC card for each case. The BOC card has to operate at either 40 Mb/s, 80 Mb/s, or 160 Mb/s = $2 \cdot 80$ Mb/s bandwidths. Because the ROD has to receive the modules data on up to 32 input lines at 40 Mb/s only, the BOC card has to split the 80 Mb/s data streams into 40 Mb/s streams. This limits the used channels of the BOC card. This is explained in more detail in Section 4.2.3.

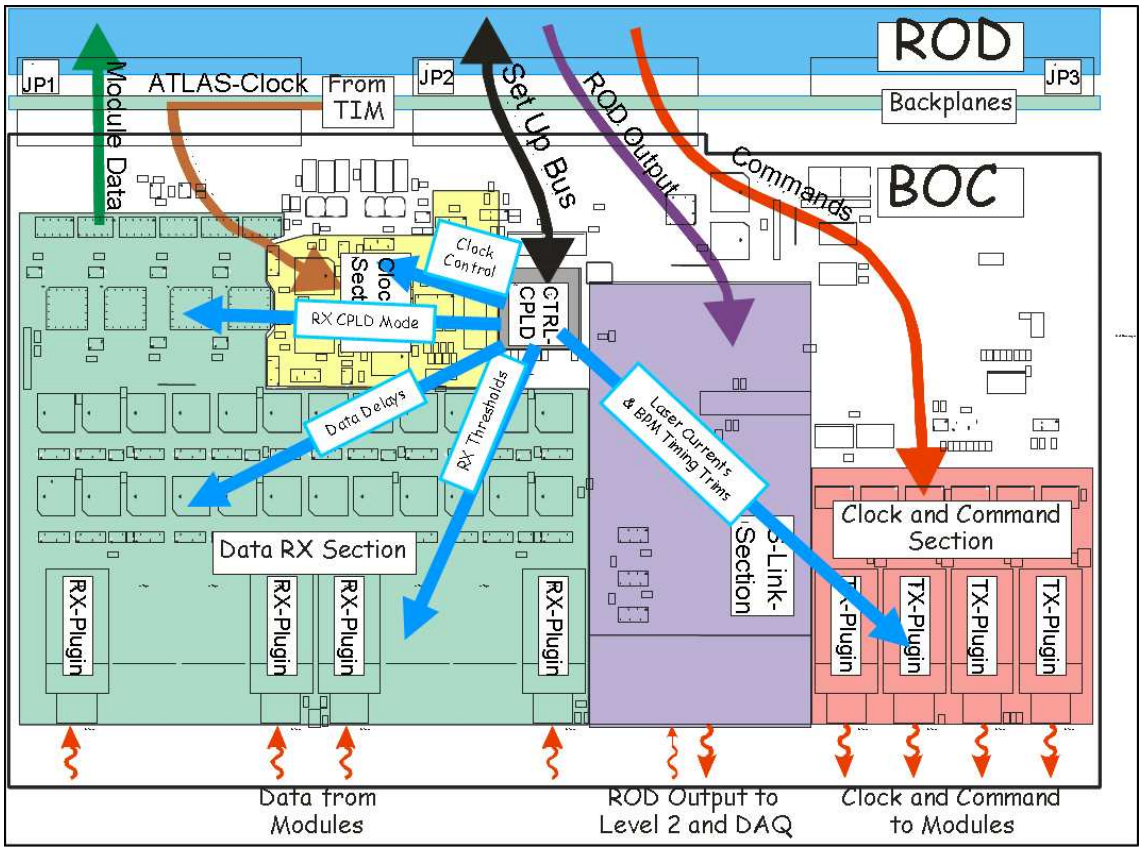


Figure 4.2: Schematical view of the Back of Crate card [40].

4.1 The Design of the Board

The design of the BOC card has been developed by the group of the Cavendish Laboratory at Cambridge. Its layout can be separated into several sections due to the functionalities of the card, as there are the clock section, the clock and command (transmission) section, the data receive section, and the S-Link section, see also Figure 4.2. The functionality will be described following this structure in the next sections.

The BOC card is supplied by two voltage lines with 3.3 V and 5 V. Additionally a 12 V supply is connected for the operation of the PiN diodes in the receiving part. The power consumptions of the BOC card are listed in Table 4.2.

The main functions are performed in seven CPLD[b] chips. These programable chips are loaded with a firmware each. There is one CPLD performing the main control of the board and the communication with the connected ROD. The communication between the ROD and the BOC card is done through a bus, named setup bus. All register access, writing and reading is done through this bus. There is a protocol for this communication to ensure a

[b]CPLD = Complex Programable Logic Device

Voltage line	typical current with no firmware loaded	typical current with firmware loaded	typical current with plugins assembled
3.3 V	2.2 A	2.6 A	2.8 A
5 V	0.45 A	0.45 A	0.9 A
12 V	0.1 mA	depending on light input	

Table 4.2: Typical current consumption of a BOC card, while no firmware has been loaded, after loading the firmware, and with plugins assembled.

safe operation, for example set the ROD ”waiting” until a task in the BOC card has been finished and reported. The state model of this ROD - BOC card communication is shown in Figure 4.3.

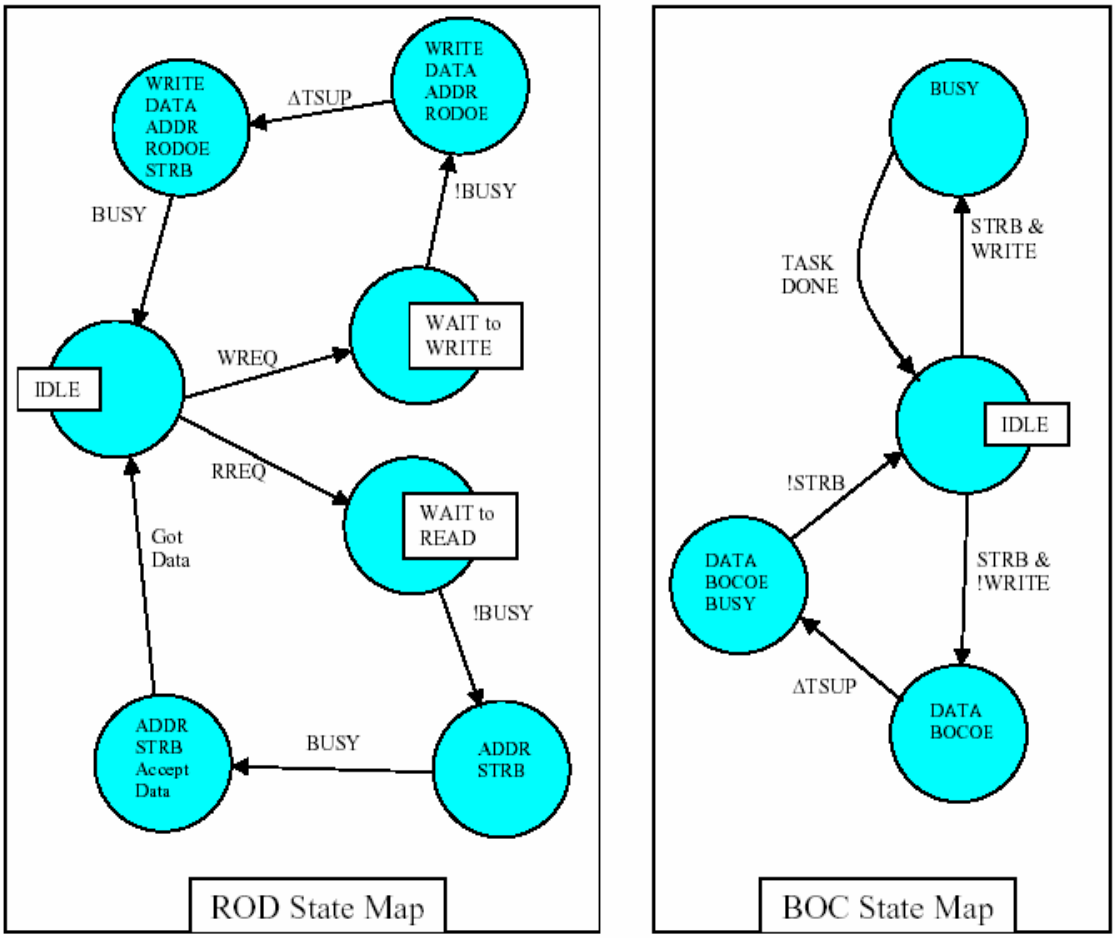


Figure 4.3: State map of the setup bus protocoll [40]. The communication between the ROD and the BOC card is performed using this protocol.

Four further CPLD's are foreseen to operate in the receive section for data registering and splitting the high bandwidth streams. The other two CPLD's are for communication with the RX- and TX-plugins (see below) and for controlling a certain clock for the data registering, which is the V-clock.

Each BOC card has its own serial number. Two hexadecimal rotari switches can be attached to this number. The serial number can be read out and identifies each individual BOC card.

4.2 The Sections of the Layout

4.2.1 Clock Section

The BOC card receives the 40 MHz system clock from the Timing Trigger and Control Interface Module (TIM) located in the same readout crate. On the BOC card this clock is multiplexed into 5 clocks. One of these clocks is passed directly to the ROD. Another one (named BPM- or P-clock) is sent to the transmission section and further on to the modules. One clock copy (named A-clock) is for the internal chip functionality. The other two clocks (named B-clock and V-clock) are foreseen for the data recovery, which is described in Section 4.2.3.

In order to adjust the timing of the modules the P-clock can be delayed by 0 to 24 ns in 1 ns steps. The B-clock, as part of the data recovery, can be delayed by 0 to 24 ns in 1 ns steps also. Because of data which is transmitted to the ROD is sampled by the B-clock, the B-clock has to be in a fixed optimal phase to the ROD-clock. The second clock for data recovery is the V-clock. This clock can be delayed by 0 to 49 ns in 1 ns steps, and additionally it can by delayed in 40 ps steps by 0 to 10.2 ns. A summary of the clocks is given in Table 4.3.

Clock signal	**Purpose**	**Delay Capability**
System clock	Clock received by the BOC from the TIM	-
A-clock	Clock for internal chip functionality	-
P-clock	Clock being encoded	BOC wide:
	into BPM for the modules	0 to 24 ns, 1 ns steps
B-clock	Clock for normal data recovery	0 to 24 ns, 1 ns steps
V-clock	Clock for 80 Mb/s sampling	0 to 49 ns, 1 ns steps
		0 to 10.2 ns, 40 ps steps
ROD-clock	copy of system clock for the ROD	-

Table 4.3: Clock description and delay capabilities.

4.2.2 Transmission Section

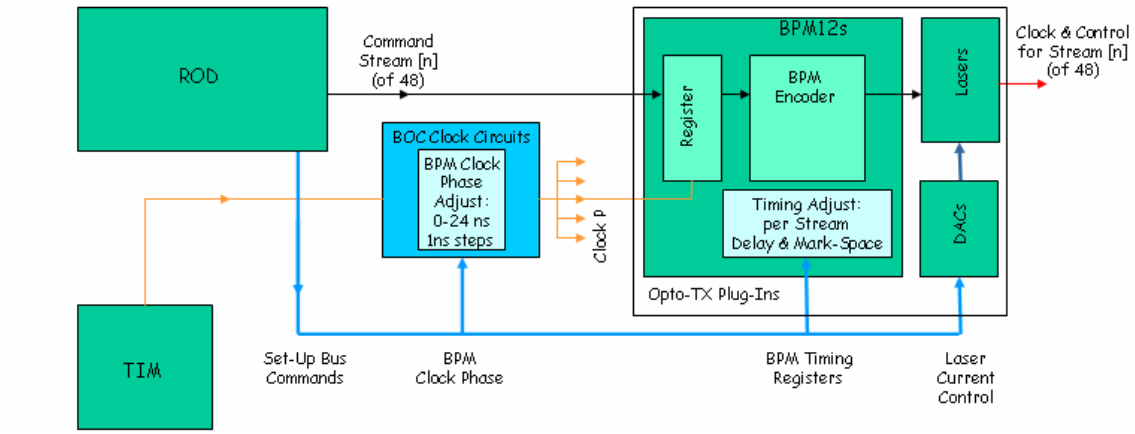


Figure 4.4: Schematical view of the command stream model in the Back of Crate card [40].

The transmission section of the BOC card receives the commands for the modules from the ROD. These are passed to four sites where TX-plugins [34] are located. Figure 4.5 shows such a plugin. The sites are named TxA, TxB, TxC, and TxD. Each of these TX-plugins is connected to one optoboard via an 8-way fibre ribbon. The data streams for each module are handled individually. The TX-plugin houses a BPM-chip [34] and an 8-way VCSEL [34] array. The data and the clock for one module are encoded into one signal by the BPM chip and sent to the module through one VCSEL channel. The BPM encoding of the clock and data signal is shown in Figure 3.19.

There are several tuning capabilities inside the transmission section. The delayable P-clock for the modules coming from the clock section is multiplexed for all module channels. Inside the BPM-chip one can add an additional delay to each stream for one module, there is a fine and a coarse delay. The fine delay can be set between 0 to 35.56 ns in 280 ps steps. The coarse delay can be set between 0 to 775 ns and has a stepsize of 25 ns. With this and the P-clock delay, each module can be timed individually against the bunch crossing (see Chapter 7).

There are more settings possible within the BPM, like an inhibit prohibiting the data to be encoded, and a mark space ratio setting for the outgoing signal. The laser current for the VCSEL's setting the outgoing light power can be controlled via two multi channel DAC's (MDAC) on the TX-plugin. The MDAC registers can only be written but not read. Therefore the values written to it are stored inside a RAM additionally. This RAM can be read again.

[b]MDAC: a Multi channel Digital Analog Converter from Linear Technologies (LTC1665)

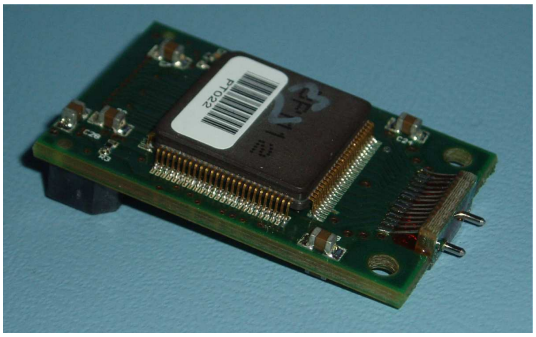


Figure 4.5: TX-plugin for transmitting the light from the BOC card to the opto-board. The size is 1.5×3.5 cm^2.

Parameter	Control Range	Function
BPM-clock	0 to 25 ns, 1 ns steps	Clock copy for all connected modules, BOC card wide
BPM inhibit	on / off	prohibiting the data to be encoded
BPM fine delay	0 to 35.56 ns, 280 ps steps	delay for the signal to the module, channelwise
BPM coarse delay	0 to 775 ns, 25 ns steps	delay for the signal to the module, channelwise
BPM mark space ratio	settings: 0 to 31	adjust the signal mark space ratio within a 30:70 to 70:30 range
laser current	settings: 0 to 255	setting the laser forward current between 0 and 18 mA

Table 4.4: Parameters to control the transmission section of the BOC card.

It has been observed that the settings inside the BPM chip influence each other, therefore, an interactive tuning has to be performed. The tuning necessity and the main idea of how to do this is described in Chapter 6.

The command stream on the BOC card is shown in Figure 4.4. The BOC card passes the commands received from the ROD to the TX-plugin. Here the decoding with the clock received from the TIM is performed. The delay capabilities are shown. To each individual module one clock and command signal is sent optically. There is one optical fibre per module. A summary of the parameters controlling the transmission section is given in Table 4.4.

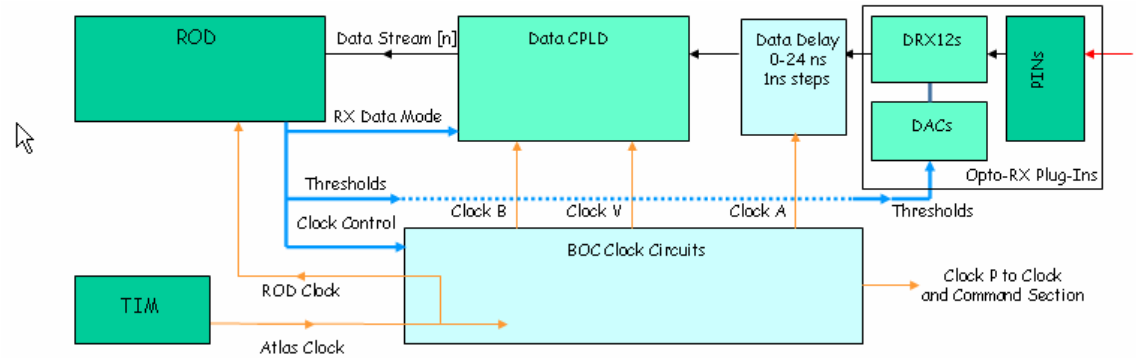


Figure 4.6: Schematical view of the data recovery circuit in the Back of Crate card [40]. The V-Clock is used for 80 Mb/s operation only.

4.2.3 Receive Section

In the receive section the BOC card receives the module data. The optical signals arrive at the RX-plugins [34] (see Figure 4.7). Up to four RX-plugins can be equipped on one pixel BOC card. Each RX-plugin serves 8 channels, so that up to 32 modules can be connected to one BOC card. The RX-plugin consists of an optical-electrical converter (a PiN diode) and an amplifier chip, the DRX[c] [34]. The light signals are received channelwise by an 8-way PiN diode array, which feeds the converted electrical signal to the DRX. The DRX is a 12 channel chip where 8 channels are used for the pixel detector read out. It has an internal threshold, which can be controlled via MDAC settings per channel. It amplifies the received electrical signals and passes them differentially onto the BOC card. Here the received data is set into a correct phase with respect to the ROD clock and passed out as 40 Mb/s data streams. To achieve this delay, chips (Phos4 chips) within the receive section enable certain delays to the data streams. They can apply a delay between 0 and 24 ns, in 1 ns step size, to each individual stream.

Each of the four CPLD's in the receive section handles the 8 streams of one RX-plugin. Inside these CPLD chips the data is registered and clocked out with the B-clock, to obtain a stable phase to the ROD clock. The whole receive chain is shown is Figure 4.6.

Depending on the detector part the modules are located in, the transmission bandwidth from the modules to the BOC card is increased. Layer1 and Disk modules operate at 80 Mb/s bandwidth and the B-Layer modules transmit the data at 160 Mb/s on two fibres at 80 Mb/s each.

In case of receiving 80 Mb/s optical data the BOC card performs a demultiplexing of the 80 Mb/s data streams into two 40 Mb/s streams each. This is done in the CPLD's. In

[c]DRX: Driving and Receiving IC

Figure 4.7: The RX-plugin is the optical to electrical converter housed on the BOC card. The size is 1.5×3.5 cm^2.

terms of demultiplexing, the 80 Mb/s and the 160 Mb/s, which is $2 \cdot 80$ Mb/s, modes are identical.

The demultiplexing, and with this also the doubling of the used streams, implies that for higher bandwidths less modules can be connected to the BOC card. In case of 80 Mb/s only two TX-plugins and two RX-plugins per BOC card are assembled. One BOC card in this configuration can serve up to 16 modules. In the 160 Mb/s = $2 \cdot 80$ Mb/s mode one TX-plugin and two RX-plugins per BOC card can serve up to 8 modules[d].

In order to split the 80 Mb/s signals into two 40 Mb/s signals, there are the two independent clocks, B-clock and V-clock, for the data recovery. The 80 Mb/s data streams are demultiplexed by registering every second bit with the B-clock – generating one stream – and the other bits with the V-clock (opposite to the B-clock) – generating the second stream. The two 40 Mb/s data streams are then clocked out to the ROD with the B-clock, see Figure 4.8

The BOC card output is fed directly into the formatters of the ROD. Eight formatters are available being able to handle 12 streams each. In order to balance the load on the ROD formatters there are always four streams used per formatter. In the 40 Mb/s operation on each stream the data of one module is sent to the ROD. This is shown in Figure 4.9. The RX-plugin sites are named RxA, RxB, RxC, and RxD due to the left out sites used only by SCT.

In the 80 Mb/s operation there are always two streams per module necessary, so that the data of two modules arrives into each formatter. And in the 160 Mb/s mode four streams are occupied by the data of each module. This means that each formatter receives the data of one module on four data streams.

[d]Due to the modularity of the optoboards connected to the modules only 6 or 7 out of the 8 channels are used. In case of a half stave read out either 6 or 7 modules are connected to one optoboard. In case of a sector read out 6 modules are connected to one optoboard

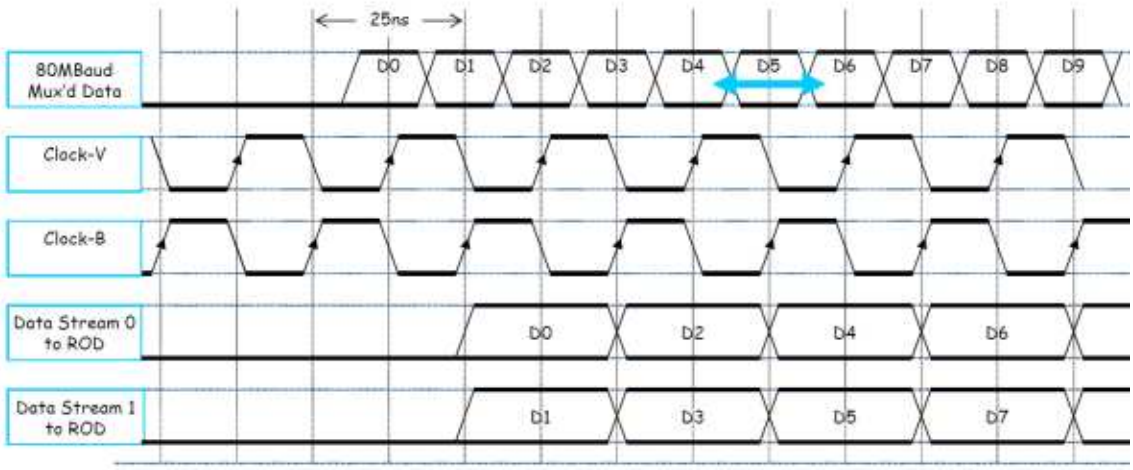


Figure 4.8: Demultiplexing of an 80 Mb/s stream into two 40 Mb/s streams [41].

To achieve the load balancing a small routing board is assembled to each pixel BOC card. It enables a routing between the CPLD's. With this the sorting of the data lines can be completely performed inside the BOC card. Figure 4.10 shows the routing of the streams in 80 Mb/s or 160 Mb/s mode. The only two used RX-plugin sites are named RxA and RxD. On each plugin there will be up to 8 optical signals arriving at 80 Mb/s. In the CPLD's the streams are split into two 40 Mb/s streams each and passed to the formatters on the ROD. To balance the load equally between these formatters each CPLD handles four 80 Mb/s streams. This is achieved by sharing the eight 80 Mb/s input streams per

Parameter	**Control Range**	**Function**
RX-Threshold	settings: 0 to 255	Threshold inside the DRX 0 to 250 μA control range, channelwise
RX Data Delay	0 to 25 ns, 1 ns steps	adjusting the phase of the data, channelwise
B-clock	0 to 25 ns, 1 ns steps	clock for sampling the data to the ROD, global
V-clock	0 to 49 ns, 1 ns steps	additional clock for de- multiplexing, global
V-clock fine phase	0 to 10.2 ns, 40 ps steps	fine adjustment for the V-clock, global

Table 4.5: Parameters to control the receive section of the BOC card. The clocks are controlled in the clock section but necessary for the data reconstitution.

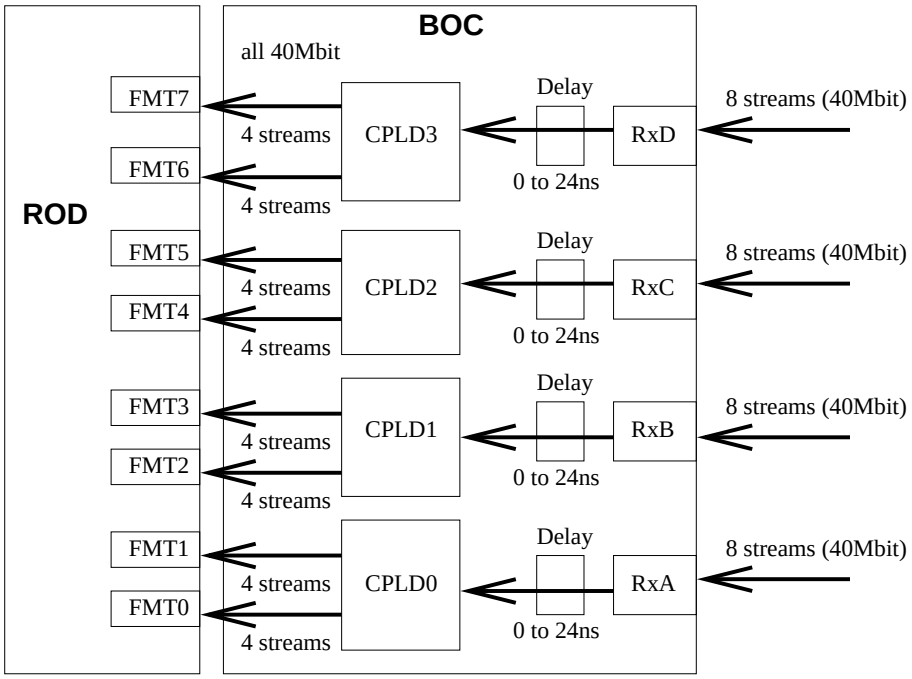


Figure 4.9: Data flow through the BOC card in 40 Mb/s operation.

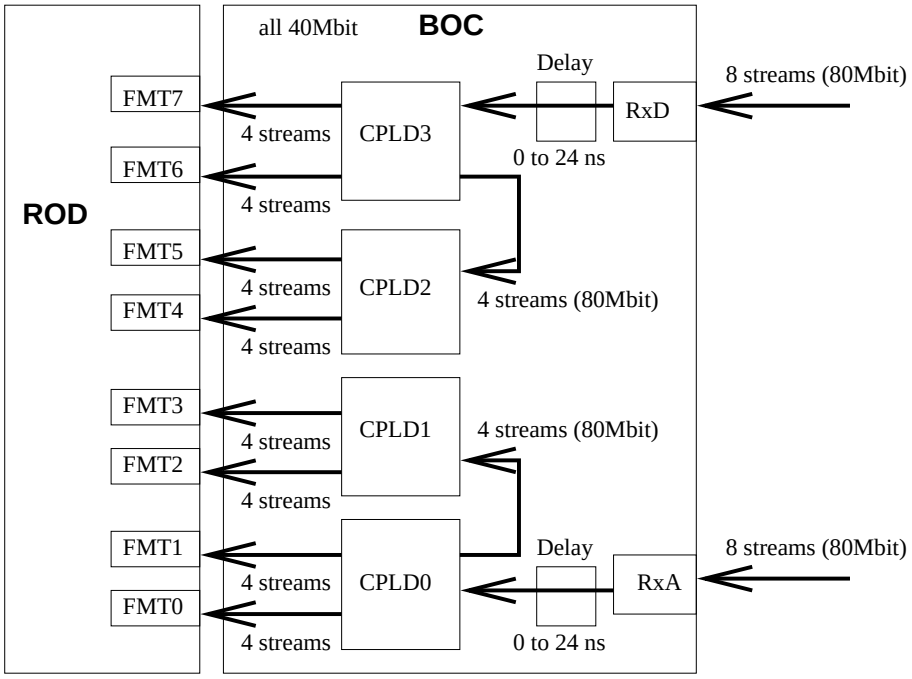


Figure 4.10: Data flow through the BOC card in 80 Mb/s or 160 Mb/s operation.

RX-plugin to two CPLD's. The routing of four streams to the neighbour CPLD requires a sending and a receiving of the streams which is sampled by the clock. In order not to have a timing difference between the streams belonging to the same trigger the not routed streams are clocked out and received in the CPLD as well. This causes all the sixteen 40 Mb/s streams to be parallel in time. All the available parameters to control the receive section are listed in Table 4.5.

4.2.4 S-Link Section

For sending the data out to the Read out Buffers, the BOC card carries the S-Link [42] card, or HOLA[e]. This card is plugged onto the BOC card. Its interface is specified for a data transmission with 32 bits in parallel at 40 MHz. On the BOC card itself there is no additional functionality for the S-Link interface other than driving the signals.

4.2.5 Further Functionalities

To obtain some information about the hardware of the BOC card some monitoring functions are available. The voltage and the current consumption on the 12 V lines for the PiN diodes on the RX-plugins can be read out. In addition two temperatures are accessible. The temperature below the TX-plugins and the temperature below the RX-plugins can be measured by an NTC[f].

The monitoring is reported as ADC[g] values which can be translated into the monitored data. Reading out this data the DCS can monitor the conditions under which the BOC card runs.

To provide laser safety the BOC card has to switch off the lasers of the TX-plugins in case of an interlock. Two interlock lines per crate are distributed via the back plane of the crate. Each BOC card in the crate receives the two interlock lines for switching off the lasers on the TX-plugins. The two lines are active low. On the BOC card the two lines are combined by a logical "AND". The lasers are only switched on if both lines are in state "high", meaning no interlock is set. One of the two lines is connected to the local interlock at the rack the crate is located in. The other line is used as a remote interlock connected to the on-detector interlock system. If any of the two interlocks is set the lasers on the TX-plugins are switched off immediately. For further information on the interlock system be refered to the description of the ATLAS pixel detector interlock system [43].

[e] HOLA: High speed Optical Link for ATLAS
[f] NTC: a resistor with a Negative Temperature Coefficient
[g] ADC: Analog Digital Converter

Chapter 5

Production of the Back of Crate Card

The Wuppertal group has taken the responsibility for the production of the ATLAS pixel BOC card and with this the responsibility to guarantee a functional card. To gain experience in handling and operating the Back of Crate card extensive studies have been performed either in standalone setups or in system tests. In Chapter 6 and 7 measurements with the Back of Crate card in system tests and in a test beam setup at CERN are described. The BOC card has been integrated into system test in Wuppertal, Bonn, Genova, and CERN. In this chapter the tests for quality assurance under production are motivated and explained. All the testing during the production has been performed in Wuppertal.

The functionalities of the BOC card, as described in the last chapter, have been tested during the production process. All cards are tested to check the proper behaviour of all functions. A short description of the tests and some results are given in this chapter.

5.1 The Tests during Production

Before running tests on the boards an inspection of the assembly is done to detect misplaced components or connectors and bad soldering. If this is completed, the current consumption of the card is measured for the 3.3 V and the 5 V line. The card is supplied with 3 voltages, 3.3 V, 5 V, and 12 V. The current consumption is measured for the main supply lines, while the 12 V line is for supplying the PiN diode on the 4 RX-plugins. The current on the 12 V line is therefore caused by the PiN diode receiving light signals. In this stage of the testing only the voltage is checked at the RX-plugin connectors. The limits for the currents on the different lines are given in Table 4.2. After passing this test the BOC card is installed into a read out crate for the further testing.

The test flow is shown in Figure 5.1. The testing splits up into two phases: the electrical testing and the optical testing. In the electrical test special test plugins are used to simulate the optical plugins and to provide some certain functions for testing some of the electrical

properties of the board. Before the optical test can be performed the mechanical housings for the connectors of the fibre ribbons have to be assembled. The optical plugins are fixated onto these parts. To achieve a good alignment of the fibres to the optical plugins an alignment of the mechanical parts is already necessary. The alignment of the plugins is part of the optical testing. The amount of light power coupled from the VCSEL's into the fibres and from the fibres into the PiN has to be more than 1500 mW. The tests which are performed under production are described in the next sections.

5.1.1 Electrical Tests

The different sections of the BOC card as described in Chapter 4 are tested explicitly. After loading the firmware to the programable chips of the BOC card all functions have to be available.

First checks are foreseen for the interlock and the power indicating LED's. The communication is checked by a read out of the serial number.

Clock Tests

The different clock signals available on the BOC card are listed in Table 4.3. To test these clocks, control features have been implemented into the BOC card firmware. It is possible that the delay chips will lock on half of the clock frequency, 20 MHz. This would lead to a larger step size in the delaying. A test of the correct locking is important. One can test the right clock behaviour including the correct delaying by performing scans shifting different clocks against one another. The A-clock and the V-clock can be used like data signals. They can be delayed by the delay chips. By sampling this clock with the B-clock the correct step size of the delays can be controlled.

If one or more of the delay chips are locked onto the wrong frequency it is possibile to reset the delay chips and check the correct locking again.

Shadow RAM and Multi Channel DAC's

On the opto-plugins there are multi channel DAC's (MDAC's) to control the current and threshold settings. These MDAC's are not readable. The BOC card has a shadow RAM to store the values written to the plugins. This RAM is tested by writing random numbers to it and then read back. There are 240 values (8 bit each) written and read back. No error in writing or reading is allowed.

Also the writing to the MDAC's itself is controlled. Special test plugins are used to receive the values written to the MDAC addresses. The TX test plugins can be read out again, so a check of the written data is performed directly. 5600 values (8 bit each) are written and read back. No error must be observed.

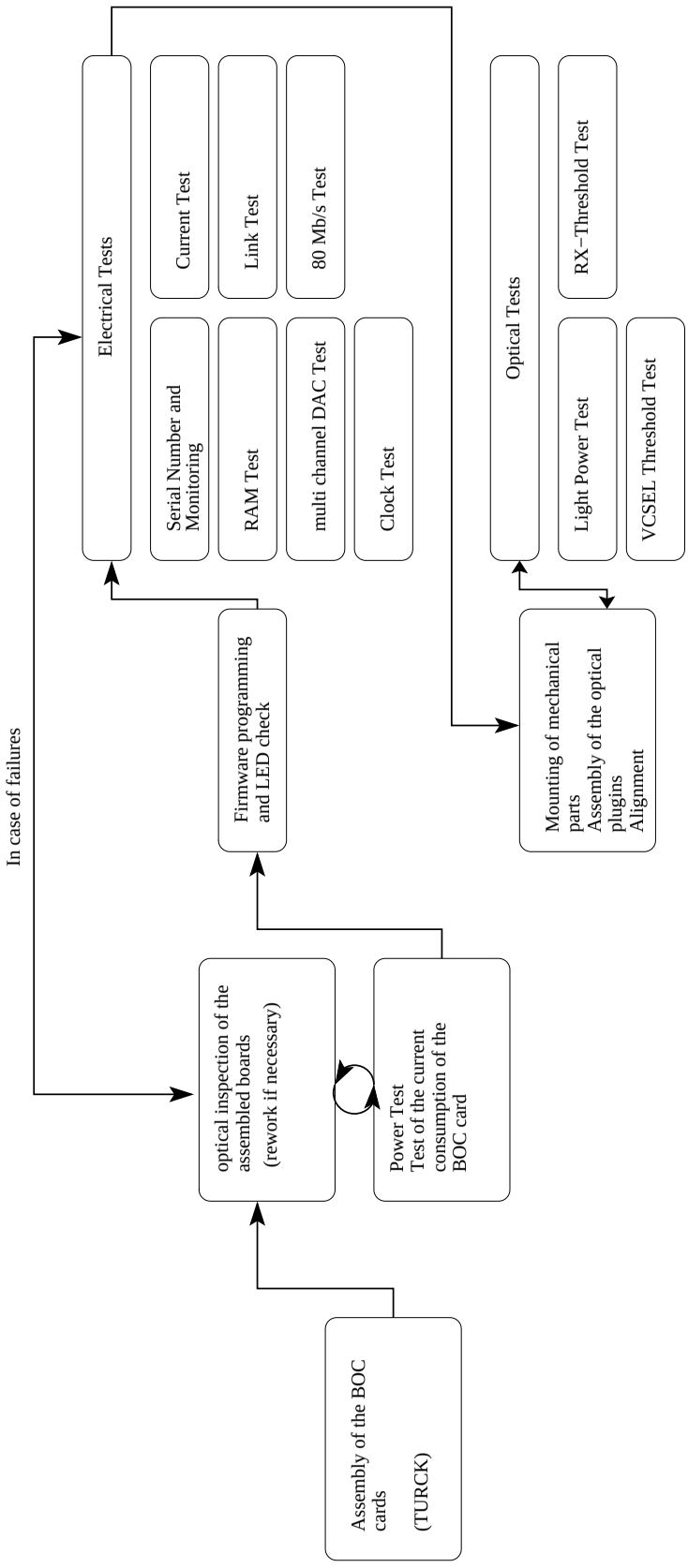


Figure 5.1: Production and test flow for the BOC card.

On the RX test plugins a current on the 12 V line is generated by writing to the MDAC addresses. Measuring the PiN current on the BOC card checks the writing to the MDAC addresses as well. Each RX site must show a linear MDAC setting versus measured current behaviour to pass this test.

Monitoring and Current Test

The monitoring of the PiN voltages is checked by comparison of the monitored voltages with manually measured voltages.

The currents are checked by using the test plugins again. A current ramp up is performed with the RX test plugins. A linear dependency between the used MDAC setting and the monitored current is to be seen, see Figure 5.2. At a certain current larger than 18 mA the BOC card switches the voltage off for safety reasons. The linearity and the switch off behaviour is checked by the test.

Link Connectivity Test and 80 Mb/s Test

To test the functionality of the routing for the data on the BOC card a link connectivity test is performed. Eight short data streams of 32 bits each are passed through a TX / RX test plugin pair and then through the receive section on the BOC card. Each link has to work properly and no losses of data due to shorts or open connections are to be observed.

In this configuration the function of the routing for the 80 Mb/s operation is tested as well. Again no data loss is allowed. This way all the electrical connections in the communication paths to and from the modules are tested. The connections over the additional plugin board for the inter CPLD routing and the propper operation of the firmware for the 80 Mb/s mode is checked in addition.

5.1.2 Optical Tests

Having the optical plugins assembled to the BOC card functionality checks for the plugins and their control are performed. The optical plugins have been tested separately, so the function can be guaranteed. On the BOC card there are the TX- and the RX-sections which need to be tested. This has to be done individually for all channels. For these tests the TX-plugins are connected to the RX-plugins via optical fibre ribbons. There is a connection between one TX- and one RX-plugin for all four sites.

The optical power emitted by the VCSEL's on the TX-plugins, the VCSEL threshold behaviour, and the RX-threshold behaviour of the DRX chips are to be tested.

In the power measurement the generated PiN current for each stream is measured for different laser current settings. At the maximum laser current setting the light power has to be above 1.5 mW in amplitude. Because of sending a 50% high – 50% low signal,

Test	**Result**	**Cut**
Power Test 3.3 V	Measured current	$I < 2.5$ A
Power Test 5.0 V	Measured current	$I < 0.5$ A
Serial number test	Function of serial number reading	correct reading of 0x00, 0x55, 0xAA, 0xFF
Monitoring test	Read back the monitored PiN voltages	$V_{mon} = V_{meas} \pm 0.3$ V
RAM test	Read back written values out of the RAM	no errors
TX multi channel DAC test	Read back written values on the test plugin	no errors
RX multi channel DAC test	Monitor generated current on the 12 V line (pluginwise)	Linear curve with slope $0.080 < s < 0.095$ mA/steps 18 mA $< I_{\text{break}} < 20$ mA
Clock Test	Check of the frequency logging for the delay chips	correct logging with maximal 1 reset
Link Test	signal through the receive section, channelwise	no shorts or open channels, every link working
80 Mb/s test	80 Mb/s routed signals	routing without errors, no shorts or open channels
Optical power test	maximal light power for a clock like signal	$P > 750\,\mu$W
RX-threshold test	minimal RX-threshold at $I_{PiN} = 0.25$ mA	find a threshold < 160
VCSEL threshold test	Laser current setting for generating 0.2 mA PiN current	find a threshold < 160

Table 5.1: Qualification cuts for the BOC card test procedures.

the measured light power is only half of the amplitude in average, it has to be larger than $750\ \mu$W.

The VCSEL's on the TX-plugin have a threshold. A certain driving current is necessary to get light out of the VCSEL's. This threshold is measured by scanning the laser current setting and measure the produced PiN current on the connected RX-plugin.

The RX-threshold behaviour is tested at a generated PiN current of $250\,\mu$A. The threshold is scanned starting from the lowest value until a working threshold is found. This has to function properly. Normally the minimal working RX-threshold setting is below 100. The cut value is 160 to provide a control range large enough for the threshold adjustment.

5.1.3 Qualification Criteria

The test routines described above are for testing the functionality of the BOC card. Each of the electrical properties and functions has to work without any failure.

Besides the functions which can be determined as working or not working, the tests using the BOC card monitoring circuit gives varying results in a certain range. There are limits to evaluate the results as correct.

The limits for the slope s of the curve measured in the current test are $0.080 < s < 0.095$ mA/steps. This ensures that all the cards behave similar and a global calibration can be used instead of calibrating each monitoring circuit of each BOC card individually. The overcurrent breakdown has to be seen in a current range of 18 mA $< I_{break} < 20$ mA.

In the optical testing of the BOC card it is mainly the function of the plugins that is checked. In addition the controlling of the plugins by the BOC card can be seen. In the threshold tests for the VCSEL's and the DRX the thresholds have to be found for settings less than 160.

The test of the light power is used as a test for the alignment as well. The lower limit for the light power of the VCSEL at the highest laser current setting is 750 μW for a clock like signal. Table 5.1 gives a summary of the tests and their qualification cuts.

5.2 Pre-Production Summary

In total 156 out of 175 printed circuit boards hav been assembled by the assembly site *Turck*[a]. The remaining boards will act as spare kits for repair and if necessary for post assembly purposes. 30 boards have been loaded as a pre production batch. 126 boards have been assembled in the main production batch. The test results for the pre production BOC cards show a good performance of the boards.

The testing of the preproduction batch was used to qualify the boards and the test software. All boards passed the working - non working criteria directly or after some minor rework.

All performed tests have been passed successfully by each board. In the current test using the RX test plugins for generating a current on the 12 V supply line, all boards show a linear curve and perform the voltage breakdown in the correct manner. Figure 5.2 shows the curve for the generated current against multi channel DAC setting. Figure 5.3 shows the multi channel DAC setting for the breakdown and the current reached before the breakdown. As shown in Figure 5.4 the mean slope of the current curve is $(0.0855 \pm 0.0015)\frac{\text{mA}}{\text{steps}}$. The spread of the slopes is indeed small, so the use of a global calibration of the monitoring circuits is justified.

[a]Turck: Firm doing the assembly of the pixel BOC cards.

The results of the power tests are shown in Figure 5.5. The distribution of the light power at highest laser current (0xFF $\equiv$ 18 mA laser forward current) coupled into the fibres is shown. The signal measured was a clock like signal. As a cut value $750\ \mu$W is applied. All VCSEL's on the TX-plugins reach this value. The mean value is 1.64 mW with an RMS of 0.39 mW. This ensures that all boards will be able to perform the optical data transmission even if the fibres are damaged by irradiation over 10 years of running the ATLAS experiment [44].

As a conclusion the light power of the signal transmitted to the modules provides a safety margin large enough to compensate damages of the fibres due to irradiation. The minimal current the DORIC is able to work with is $I = 40\ \mu$A. The responsivity of an irradiated PiN is about $R = 0.33\ \frac{A}{W}$ and the worst case attenuation of the fibres is 5 dB. This results in a required light power of the VCSEL on the TX-plugin of $P > 400\ \mu$W. The light power received by the PiN on the optoboard has to be around 300 μW (in amplitude) to produce an electrical signal the DORIC is able to work with. The light power can be adjusted channelwise. The measurement of the light power by DCS using the optoboard can be used to adjust the light power.

The RX-threshold test searches a minimal threshold for receiving the correct pattern sent to the RX-plugin. The amount of light sent by the TX-plugin VCSEL's is tuned to generate a PiN current which is within the dynamic range of the DRX. The measured thresholds are shown in Figure 5.6. For all tested RX-plugin channels the threshold could be found in the range between 20 and 100 showing a mean value of 50 with an RMS of 8.7. This means that the RX-thresholds work as expected and that there is enough space for increasing the RX-threshold in case of higher input light power.

The threshold of the VCSEL's on the used TX-plugins is determined by measuring the increase of the corresponding generated PiN current. The expected values are around 100. The VCSEL threshold is defined as the current setting value for which a PiN current of 0.2 mA is measured. The measurement shows a mean VCSEL threshold of 93.4 with an RMS of 10.1. This prooves the expectation to be correct, see Figure 5.7.

All in all the optical properties have been found to be in the expected range. This ensures the function of the optical transmission and receiving over the complete time of running. The possibilities of tuning which are foreseen, like increasing the light power or raising the RX-threshold are necessary to achieve an optimal performance of the system. The coupling of the lasers to the fibres and fibres to the PiN diodes are measured to be good. The capabilities of adjusting any parameter channelwise must be controlled per channel by the detector control system. The used monitor function of the BOC card are not absolutely calibrated but they can be used to determine the necessary properties of the card for tuning and monitoring. The BOC cards are tested to operate in the ATLAS experiment as foreseen and expected.

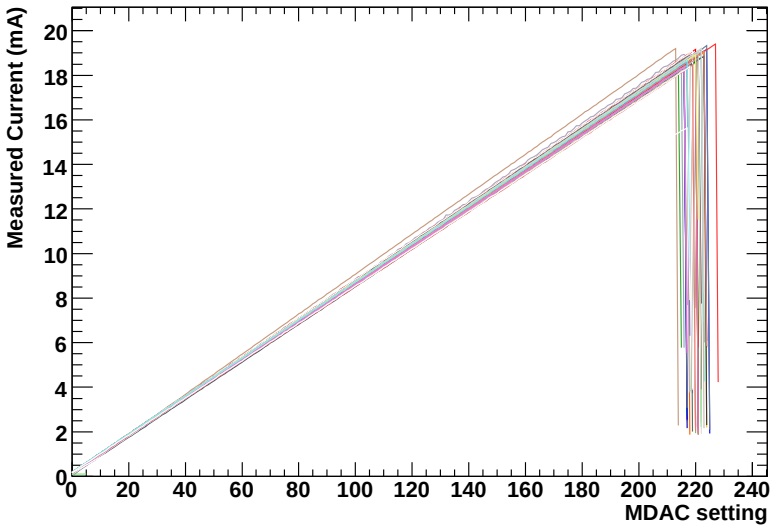


Figure 5.2: During the PiN-current test generated currents against the MDAC settings. At around 18 mA an overcurrent has to be observed to control the overcurrent safety option. The mean slope of the curves is $s = (0.0855 \pm 0.0015)$ mA/steps, see Figure 5.4.

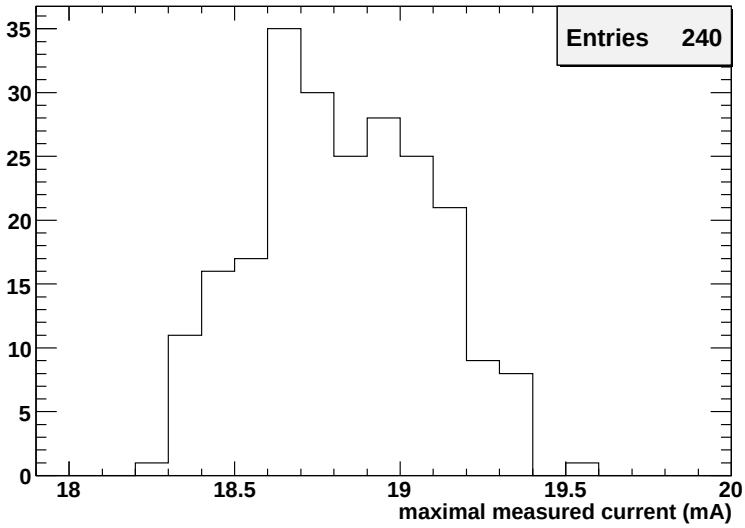


Figure 5.3: The maximal generated current before breakdown. The mean value is 18.83 mA with an RMS of 0.26 mA. The limits are 18 mA $< I <$ 20 mA. 240 RX-sites have been measured.

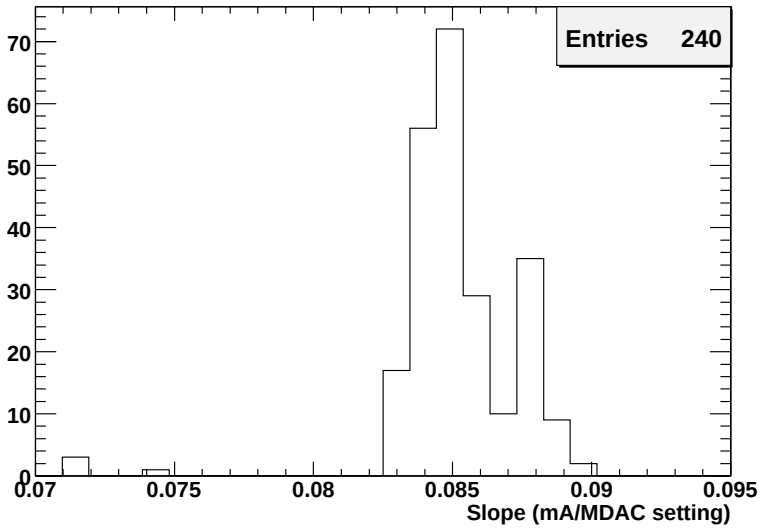


Figure 5.4: Slope of the current curves. The mean slope of the curves is $s = (0.0855 \pm 0.0015)$ mA/steps. The slope limits are $0.080 < s < 0.095$ mA/steps. 240 RX-sites have been measured.

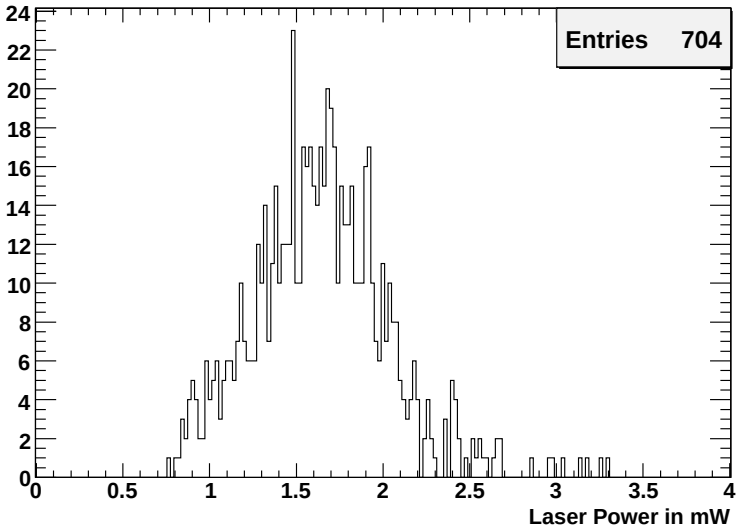


Figure 5.5: Distribution of averaged optical power generated by the TX-plugin VCSEL's at the highest possible laser current. The signal sent was a clock like signal, so the measured power value is about half of the signal amplitude. The mean averaged power is 1.64 mW with an RMS of 0.39 mW. The lower limit is 750 μW. 88 TX-plugins have been measured.

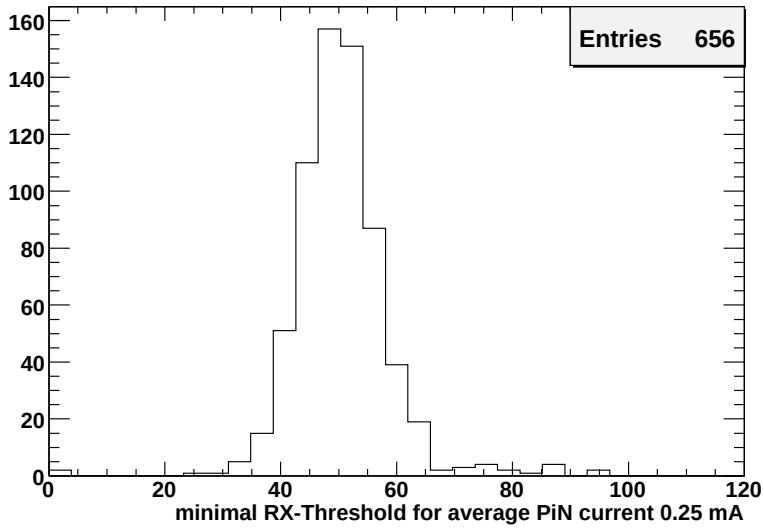


Figure 5.6: Distribution of the minimal RX-threshold for receiving the data correctly at a mean PiN current of $250\ \mu$A. The mean RX-threshold value is 50.14 with an RMS of 8.69. The minimal RX-threshold must be below 160. 82 RX-plugins have been measured.

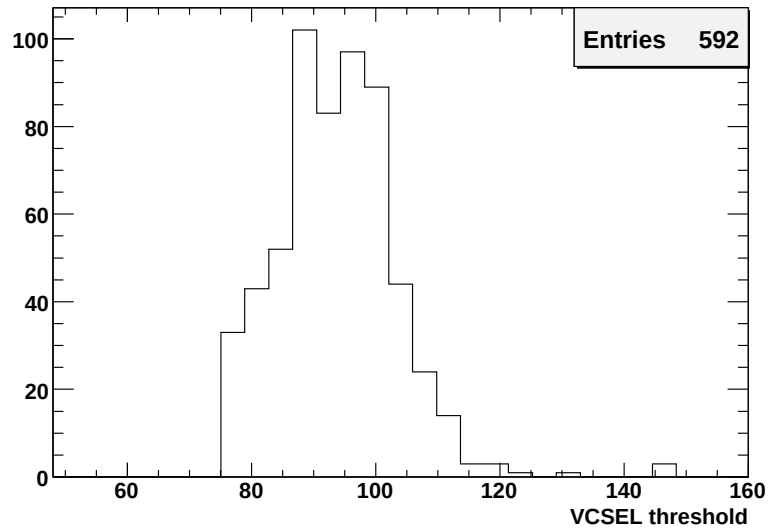


Figure 5.7: Distribution of VCSEL thresholds for generating a PiN-current of 0.2 mA.

Chapter 6

System Test

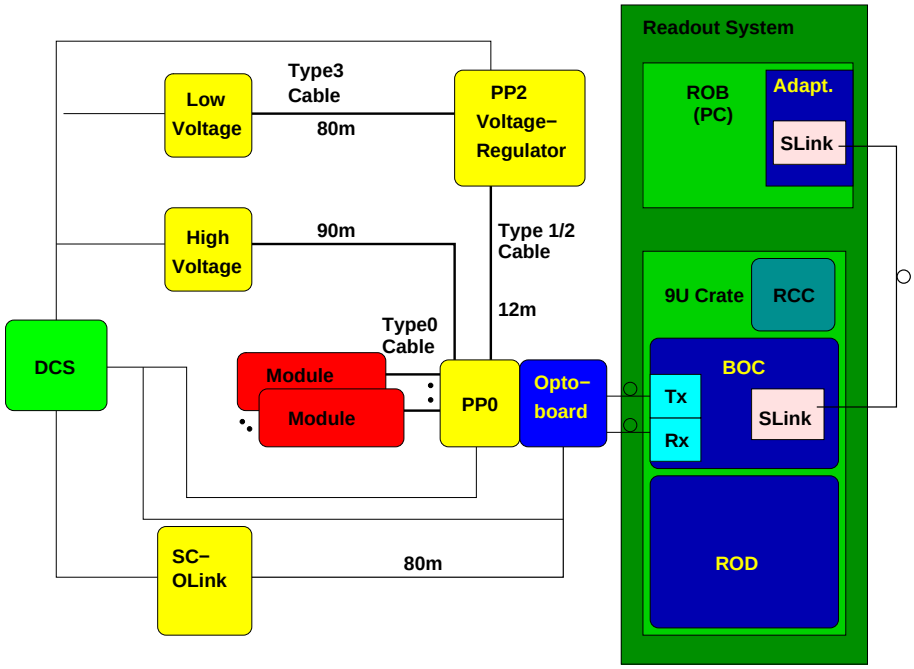


Figure 6.1: Readout scheme of the system test [45]. The parts of the power supply system are yellow, the readout system green and blue. This work will mainly focus on the readout system.

It is obvious that a system with as many different components as described thus far has to be tested intensively. In spite of the production tests of the individual parts, a system of all of the components needs to be tested, and this for all modes of operation that are foreseen to be used.

For the ATLAS pixel detector such a system test has been set up in Wuppertal to test the complete chain of modules, optical link - meaning optoboards, fibres, TX- and RX-

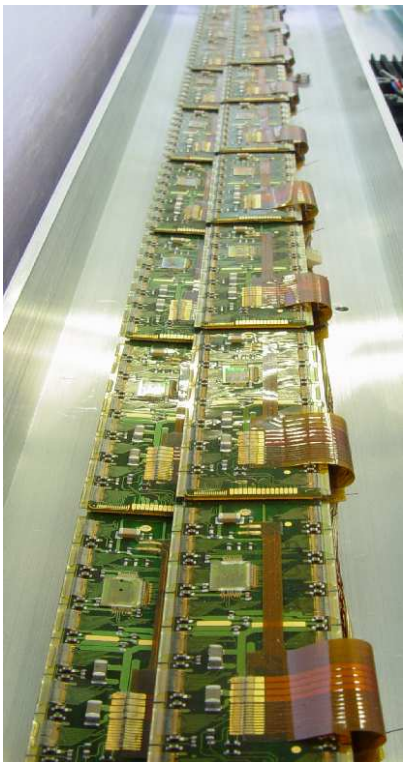


Figure 6.2: Bi-stave used as device under test in the Wuppertal system test.

plugins - a BOC card, a ROD, a single board computer, a control computer and the DCS[a] [46] for controlling and monitoring the voltages, currents, and temperatures.

Ideally the test software would be close to the final state, but because this is not the case much of software development is done during the testing phase, so all in all it is a test for hardware and software alike.

6.1 The Structure of the Wuppertal System Test Setup

Figure 6.1 gives an schematic view of the system test setup. In the Wuppertal system test setup a bi-stave with 26 modules is used (see Figure 6.2). Because the pixel modules have to be kept under temperature and humidity control, the bi-stave is built into an insulated box for cooling.
Six or seven modules of a half stave are connected electrically to an optoboard which is located on an interface card, the PP0 support board. This PP0 support board provides the connectors for one optoboard and the cables coming from up to seven modules, and performs the routing in between (see Figure 6.3).

[a]DCS: Detector Control System

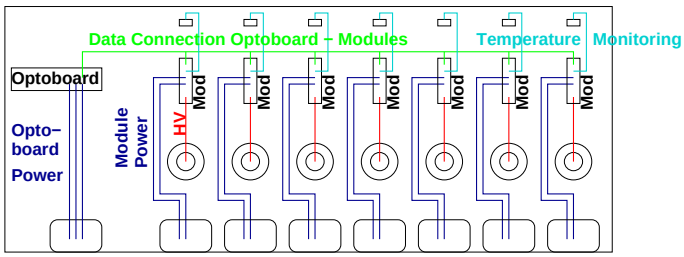


Figure 6.3: Schematic view of the PP0.

The PP0 support board is also the interface for the power connections of the optoboard and the modules. It provides the connections for the temperature control by the detector control system (DCS). The Wuppertal system test is equipped with two PP0 support boards housing one Disk-type optoboard each, to be able to operate two complete half staves.

The supply system of the modules is structured as in the experiment [47]. The power supplies are controlled by the detector control system. The sensor bias voltage of -150 V is supplied by an ISEG[b] power module and delivered through cables as long as shall be used in the experiment. They are connected to the PP0 support board modulewise. The supply voltage for the digital (2.1 V) and analog (1.7 V) part of the detector modules is delivered by a WIENER[c] power supply and regulated by a PP2 regulator board [48].

The PP2 regulator board consists of 16 voltage regulators. It receives one voltage line for the analog module supply, one voltage line for the digital module supply, and one voltage line for the V_{VDC} optoboard supply. From these the PP2 regulator boards regulate the voltages (analog and digital) for 7 modules and the optoboard. The regulator for the optoboard is foreseen to be redundant. For each half stave or sector one PP2 regulator board is needed.

In the system test for each half stave one Wiener supply channel per voltage and one PP2 regulator board is used. Again, long cables are used in the system test.

The two optoboards are connected with optical fibres to two TX- and two RX-plugins on one BOC card. The BOC card is placed in a VME-crate connected to a ROD. The crate is controlled by a single board computer which has an ethernet connection to a control machine. The control computer provides the connection between the readout system (data acquisition, DAQ) and its hardware (ROD/BOC card), and the detector control system (DCS) over a protocol named DDC[d] [46].

[b] ISEG: A vendor manufacturing high voltage power supplies.

[c] WIENER: A company developing mainframe crates and power supplies for industrial and scientific research.

[d] DDC: DAQ - DCS Communication

6.2 The Measurements during the System Test

The measurements done in the Wuppertal system test are designed to confirm the correct functioning of the complete system including the optical readout. Of special interest is the influence of the optical readout system on the detector module performance. Therefore, the measurements are done in different configurations, as in single module or multi-module readout, with separately or parallel powered modules to be able to compare the results to values obtained in the qualification phase before. The parameters to compare are obtained in several measurements:

- Test of the cabling between the modules and the readout electronics
- Digital tests of the modules
- Analog tests of the modules
- Usage of different bandwidths for data transfer
- Studies of the BOC card and optoboard parameters, like optical power, RX threshold, mark space ratio, data delay
- Studies of the DCS environment

The first two tests, cabling and digital, are mainly to ensure correct communication between the readout hardware and the modules.

The test of the DCS is an important task in the system test; for a description see reports by the Wuppertal DCS group, i.e. [49]. The tests concerning the optical system are described in more detail in the following sections.

6.2.1 Cabling Tests

After setting up the system some short tests are necessary to determine if the modules are connected properly to the supplies and readout. It is important to confirm the routing from the BOC card over the optoboard to the modules and vice versa, because there is no special error checking afterwards. Therefore, a short *link test* can be performed, checking the communication with the modules for each link separately. In this way problems in the optical cabling and the settings in the control software can be discovered and corrected.

Having the connections confirmed, the modules can be configured and the functionality of setting and reading registers inside the modules is tested by a *register test*. This ensures that the modules get the commands from the control system and can be read out properly.

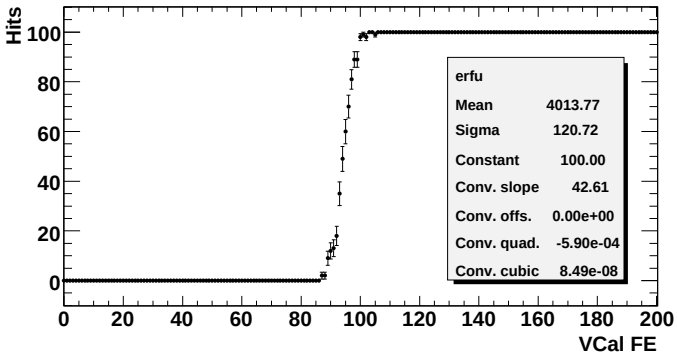


Figure 6.4: Result of a threshold scan for a pixel.

6.2.2 Digital Tests

The digital part of the pixel electronic cells of the modules can be tested separately. It can be pulsed directly and has to register each pulse as a hit, as if it comes from the analog circuit. If not all injected pulses are recognised, this indicates an error in the function of the electronics, a failure in the power supply, or damage of the module.

6.2.3 Analog Tests

In the *analog tests* the threshold and the noise of the module is determined. A voltage pulse is injected into the injection capacitor of the analog part of the electronics cell. This is equivalent to a certain charge which is collected from the sensor. By increasing the pulsed voltage the threshold and the noise of the electronic cell can be determined. The output of these scans is the distribution of the threshold and the noise over the complete module. This can be compared to measurements done earlier or in different setups.

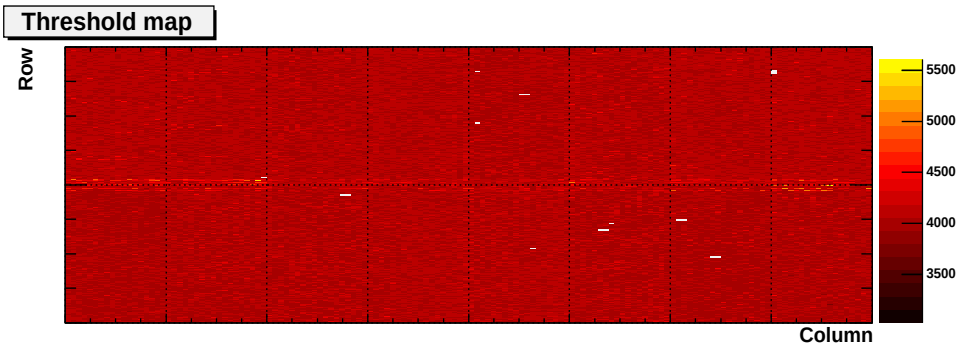
In Figure 6.4 the result of this measurement for a single pixel is shown. And Figure 6.5 shows a typical result of a threshold scan for the module in three different views, as a colour coded hit map giving the threshold for each pixel, as a distribution of the thresholds, and as a scatter plot. The voltage which is pulsed into the capacities is increased stepwise. For each step a selectable number of pulses is given. Figure 6.5 shows the distribution of the detected thresholds for all pixels of a module. It is visible that there is a spread in the threshold values. This spread, or threshold dispersion, can be tuned to be as small as possible by varying the tuning DAC's for the individual electronic circuits. The module scanned here shows a threshold of $4063\ e^-$ with a nicely small dispersion of $47\ e^-$.

The threshold of each pixel is not a specific value. It is smeared by noise effects of the electronics and the sensor assembly. Figure 6.6 shows the noise result of an analog scan. It is again devided into several views, the hit map shows the colour coded noise value

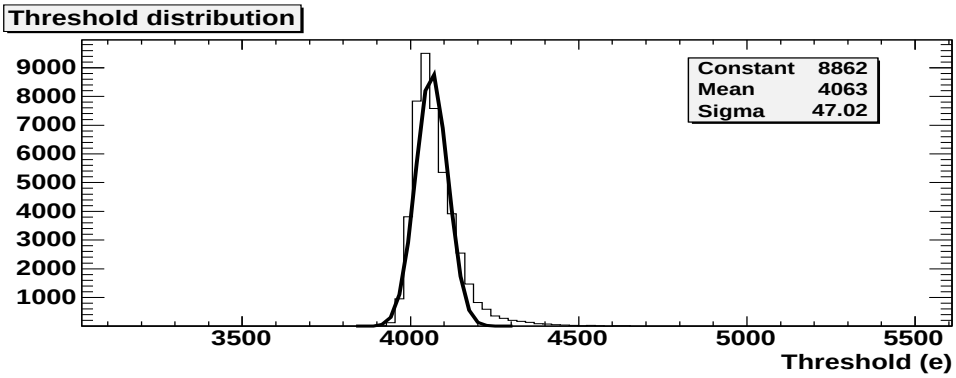
of each pixel, the distributions of the noise values for the different pixel geometries are given, and a scatter plot of the noise values is shown. When pulsing the electronic cell with pulses well below threshold the cell does not recognise any hit. Pulses well above threshold are recognised completely. The steps in between, near threshold, are affected by the noise. On this curve an error function is fitted (see Figure 6.4):

$$erf(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \tag{6.1}$$

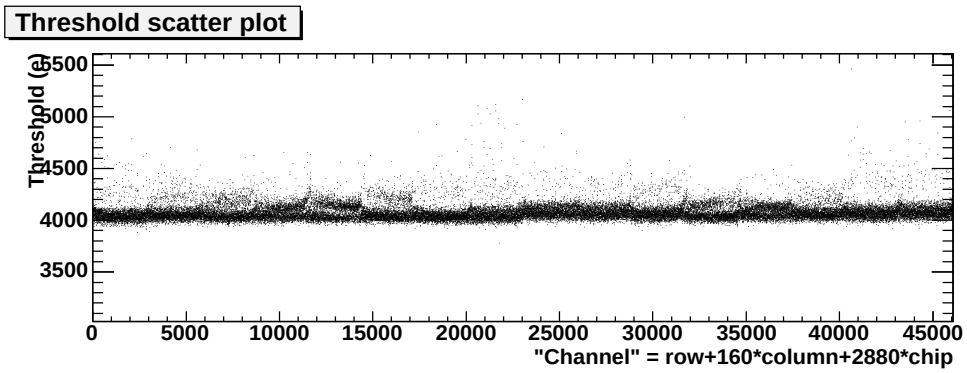
The mean of the underlying gaussian is the threshold value. The sigma of the fitted gaussian is taken as noise. In the noise result plot these sigma values are shown. They have a dispersion over the module, which is also shown. The scanned module shows a noise of $155\ e^-$ with a sigma of $6.9\ e^-$.



(a) Pixel threshold map.

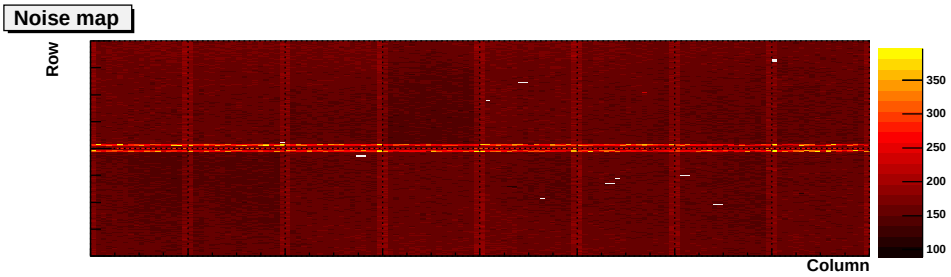


(b) Distribution of the pixel thresholds for the module.

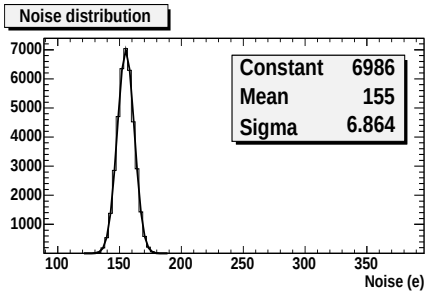


(c) Scatter plot of the pixel thresholds.

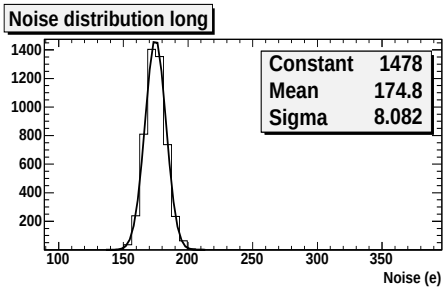
Figure 6.5: Typical result of a threshold measurement. The mean threshold is $4063\ e^-$ with a dispersion of $47\ e^-$ for module 510868 on the system test bi-stave.



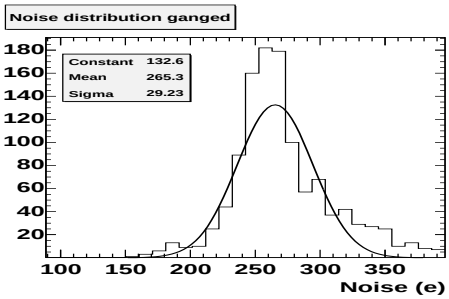
(a) Pixel noise map.



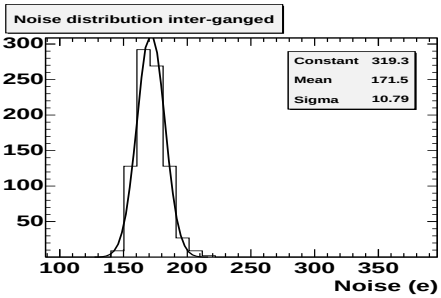
(b) Noise distribution of all pixels.



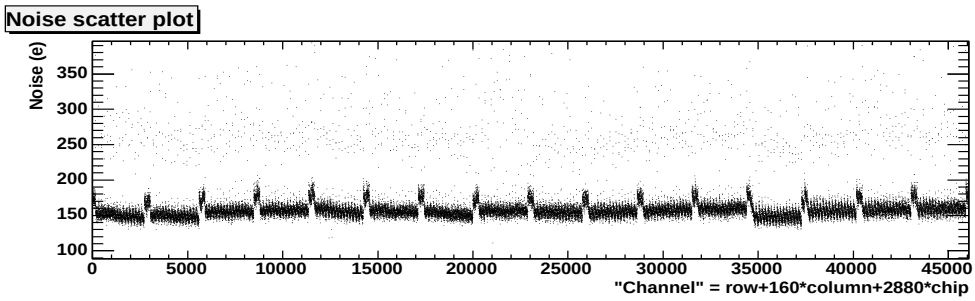
(c) Noise distribution in the long pixels.



(d) Noise distribution in ganged pixels.



(e) Noise distribution in the ”interganged” pixels.



(f) Scatter plot of the noise measurements.

Figure 6.6: Typical result for a noise measurement. Here the result for the separately powered module M510868 is shown. The mean noise value is 155 e^-.

6.3 The Development of Software

To include the BOC card into the system test the control of the hardware had to be included into the system test software. The data acquisition software is based on a library, named *PixLib*, which provides the support of the hardware on one hand and control, scanning, and tuning capabilities on the other hand. The BOC card control has been included into this library as a sublibrary, named *PixBoc*. The functions provided in PixBoc have been integrated into the steering software for the system test, STcontrol[e], and will be used for controlling the BOC card in the detector control later on. In this way a test of the card including the steering software is possible.

Additionally, a control program, BocControl, had been written which enables the configuration and control of the BOC card in the system test environment before STcontrol was able to handle the card. In this way BocControl potentiate first tests with the optical readout system. It was also used to integrate the BOC card into a test beam setup, see Chapter 7. Both tools, BocControl and STcontrol, have been used in the system test. It has been shown that the software controls the hardware correctly.

6.4 The Results of the System Test Measurements

To characterise the system with the optical link, threshold and noise scans have been performed under different conditions. The standard laboratory module test system provides reference data. This system is used during production of the modules for the characterisation and qualification of the modules. It is referred to as the TurboDAQ system.

The step from the TurboDAQ readout to the optical readout was studied. Because of only being able to test single modules with the TurboDAQ system, a test with only one module has been performed with the system test. In this test only one module has been powered at a time and was measured; this test is called ”separate powered”. Two further operational modes have been measured, these being a half stave and a full stave in parallel.

In Tables 6.1, 6.2, and 6.3, the results for the measurements in the different modes for the modules on stave 4008 are given.

Concerning the threshold of the modules, one can see a systematic change for all modules in the step from the TurboDAQ to the optical readout. The results are shown in Table 6.1 and Figure 6.7. All modules have been tuned to have a threshold of around $4000\ e^-$. This was done with the TurboDAQ system. After tuning the TurboDAQ system measures the threshold to be higher by around $160\ e^-$. The measured values for the three different configurations using the optical readout are relatively stabpm.jpgble. The measured threshold matches the tuning goal of $4000\ e^-$ within a range of 2%. This is a good result taking into account, that the measured value matches the aimed value. To

[e]STcontrol is maintained by the Bonn University group. The PixBoc functionalities have been ported into GUI applications by this group.

Readout Setup:	TurboDAQ	System Test	System Test	System Test
Power Scheme:	single module	single module	half stave	full stave
position / number	[e^-]	[e^-]	[e^-]	[e^-]
M6A / 510836	4196	4071	4060	4067
M5A / 510901	4175	4058	4054	4057
M4A / 510620	4163	4076	4057	4072
M3A / 510857	4159	4004	4004	4037
M1A / 510173	4166	4045	4019	4065
M0 / 510973	4172	4037	-	4029
M1C / 510868	4196	4063	-	4075
M2C / 510778	4185	4031	4084	4038
M4C / 510624	4182	4041	4078	4011
M5C / 510106	4173	4052	4019	4018

Table 6.1: Mean thresholds of the modules in the different measurements. Modules in position M0 and M1C have not been measured in the full stave configuration [50].

be able to check this result absolutely a source calibration of the threshold would be necessary. The possibility of performing this kind of scan is not yet given in the software. It has to be included into the software for the system tests at CERN. This will proove the difference in the results acheived with the two readout systems. The difference in the measurements has several contributing factors, such as the different readout hardware, the different control and fitting software, and differences in the environment circumstances

Readout Setup:	TurboDAQ	System Test	System Test	System Test
Power Scheme:	single module	single module	half stave	full stave
position / number	[e^-]	[e^-]	[e^-]	[e^-]
M6A / 510836	69	55	62	60
M5A / 510901	54	46	51	49
M4A / 510620	52	46	52	56
M3A / 510857	50	48	54	51
M1A / 510173	51	48	61	54
M0 / 510973	51	44	-	48
M1C / 510868	55	47	-	62
M2C / 510778	48	40	58	52
M4C / 510624	54	50	61	55
M5C / 510106	53	42	55	56

Table 6.2: Threshold dispersions of the modules in the different measurements [50].

Readout Setup:	**TurboDAQ**	**System Test**	**System Test**	**System Test**
Power Scheme:	**single module**	**single module**	**half stave**	**full stave**
position / number	**[e⁻]**	**[e⁻]**	**[e⁻]**	**[e⁻]**
M6A / 510836	183	159	160	160
M5A / 510901	181	154	164	158
M4A / 510620	178	157	158	159
M3A / 510857	175	149	151	152
M1A / 510173	174	152	155	154
M0 / 510973	184	160	-	165
M1C / 510868	185	155	-	158
M2C / 510778	184	158	170	159
M4C / 510624	181	153	157	153
M5C / 510106	179	152	155	154

Table 6.3: Noise of the modules in the different measurements [50].

like temperatures, voltages, and humidity. Given the stability of results for the different measurement configurations using the optical system, our trust in this system is increased. A long-term stability study for the readout system is currently being performed to study if the measurements are reproducible over a longer time [51].

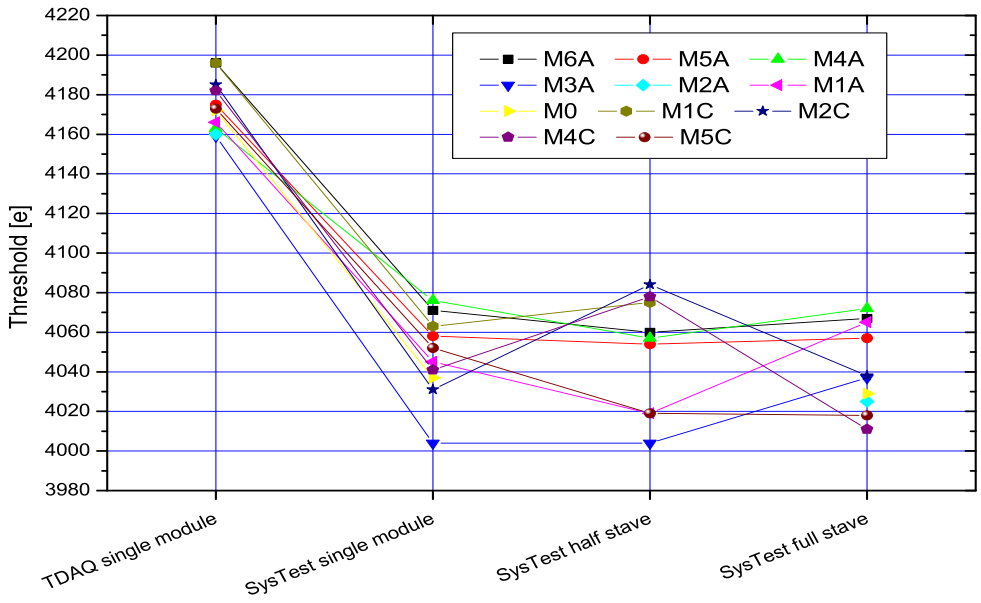


Figure 6.7: Mean threshold results for the modules on the system test stave 4008. The measurements were performed for different configurations of the powering and readout.

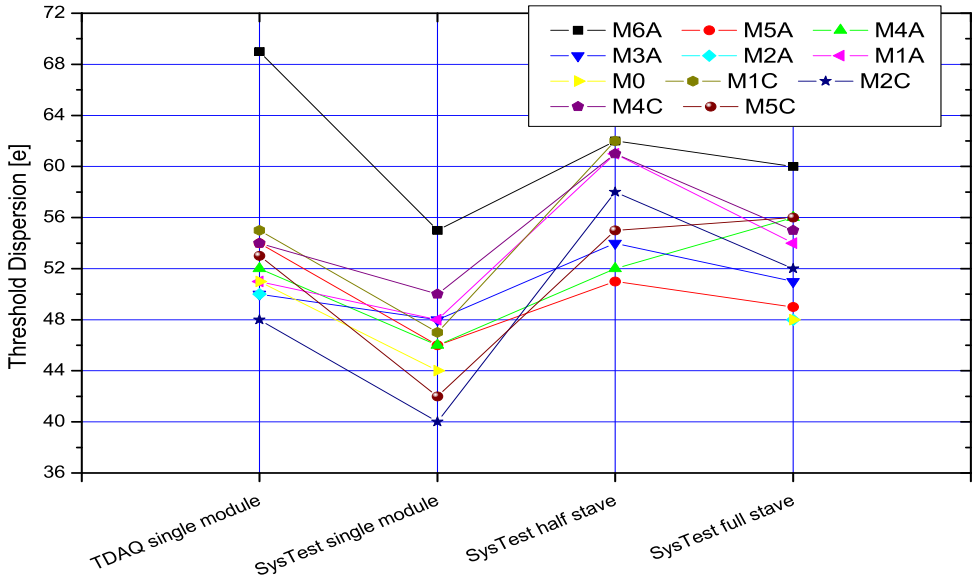


Figure 6.8: Threshold dispersion results for the modules on the system test stave 4008. The measurements were performed for different configurations of the powering and readout.

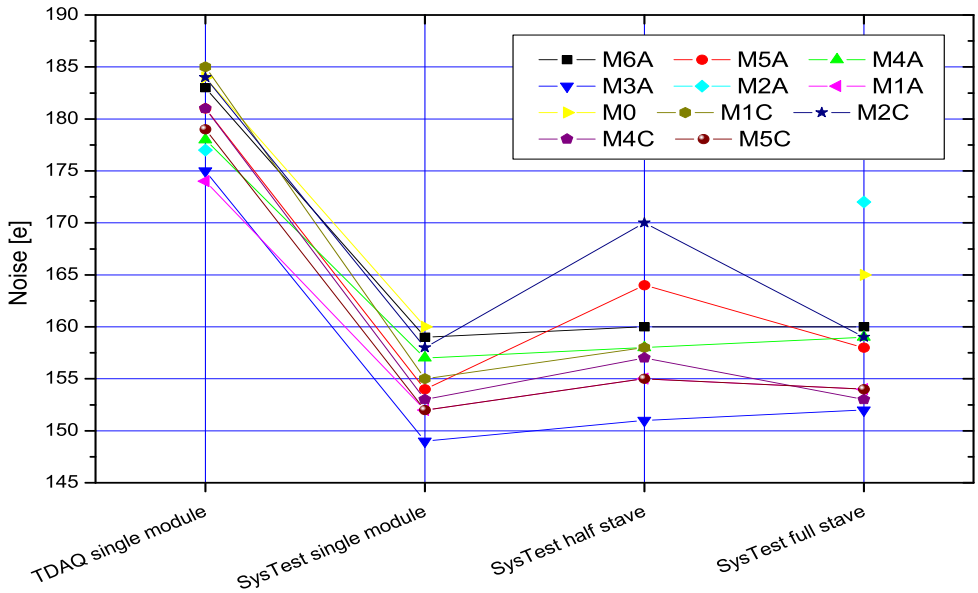


Figure 6.9: Noise measurement results for the modules on the system test stave 4008. The measurements were performed for different configurations of the powering and readout.

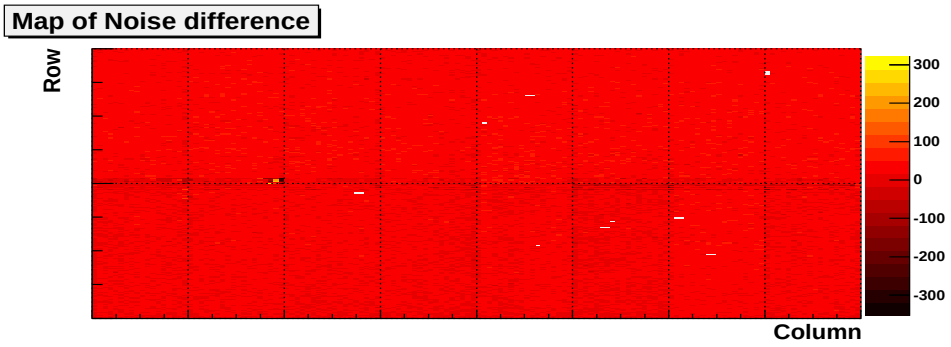
The dispersion of the threshold does not show the same behaviour as the threshold. Table 6.2 and Figure 6.8 show these results. In these measurements one can see temperature effects coming from different powering scenarios. While with the TurboDAQ system the temperature was around 25° C, the separately powered modules have been operated at 27° C, the half stave at 18° C, and the full stave at 20° C. The previously mentioned difference in the results of the measurements with TurboDAQ and the optical readout system for separately powered modules can be seen again. The system test results are systematically lower, although the operation temperature is nearly the same. The differences on order of 10 e^- for the measurements with the optical readout system are attributed to temperature effects. Because the tuning is performed at a given temperature, differences of a few electrons in the threshold dispersion are expected for the relevant temperature differences.

In Table 6.9 and Figure 6.3, one can find the results for the noise. The noise of the modules behaves in the same manner as the thresholds. A systematic change between the TurboDAQ and the optical system can be observed. The noise is measured to be lower for the optical system by around $30\ e^-$. The stability for different configurations has been shown to be within a range of about $10\ e^-$. The long term study will measure the noise change over a longer period.

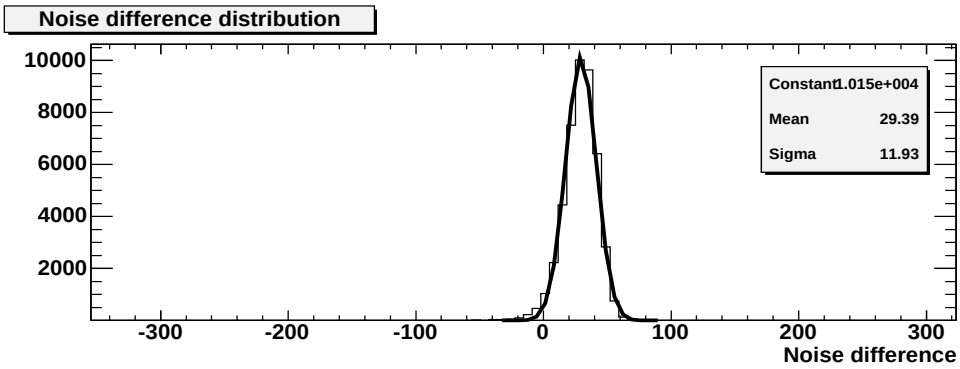
In Figure 6.10 a plot is shown which depicts for each pixel the difference of the noise between two measurements. The two comparable measurements of single modules with different readout hardware are subtracted for each pixel, and the result is plotted. One can see that the TurboDAQ measurement gives higher noise results by around $29\ e^-$.

Figure 6.11 shows the same for the threshold difference between the TurboDAQ measurement and the measurement with the optical system. The TurboDAQ system measures the threshold to be $\sim 132\ e^-$ higher.

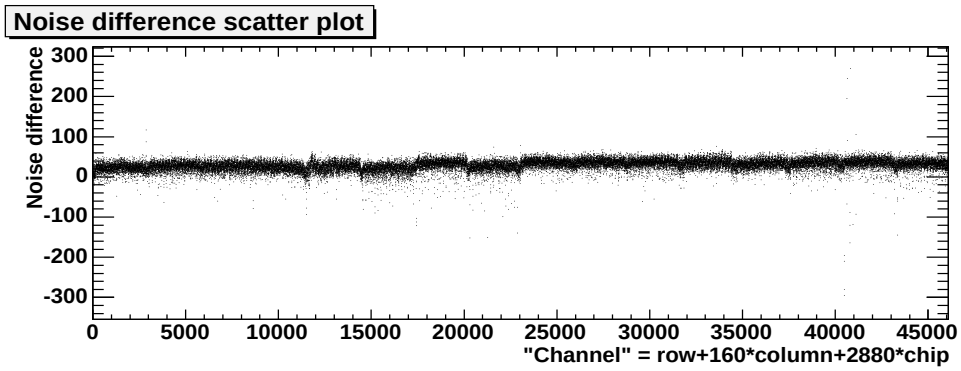
A first conclusion from the tests done so far is that the optical system reads out the modules stably after setting up the optical system correctly. The handling of the system during the measurements showed that a tuning and optimisation of the parameters is necessary to achieve optimal transmission performance. This is explained in more detail in Section 6.5 To be studied in terms of stability and cross talk is the case of having several readout parameters at the edge of the working range, but it is expected that in such a case the system becomes unstable rather quickly. Because the data sent by the modules must have a certain format, errors in the transmission are directly seen in unrecognised module data. The next step in testing the system is to study a fully loaded BOC card and a system with more than one BOC card and ROD. This is under investigation at CERN. A test facility of roughly 10% of the pixel detector is to be set up. It will provide the possibility to study a larger system, including all parts which are foreseen for the pixel detector.



(a) Pixel noise measurement difference.

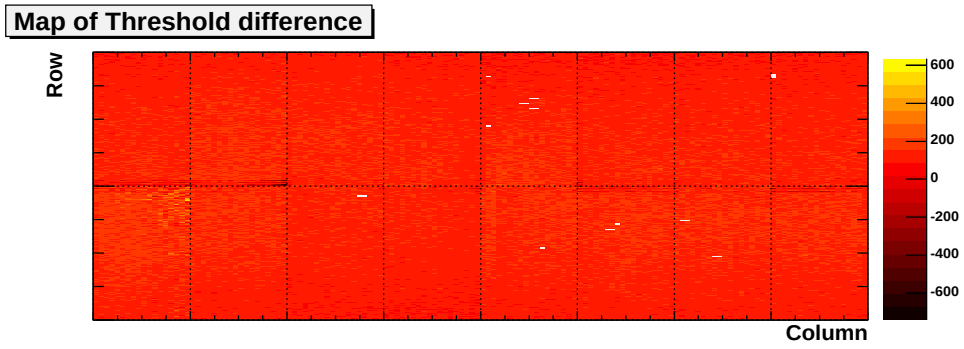


(b) Distribution of the noise measurement differences.

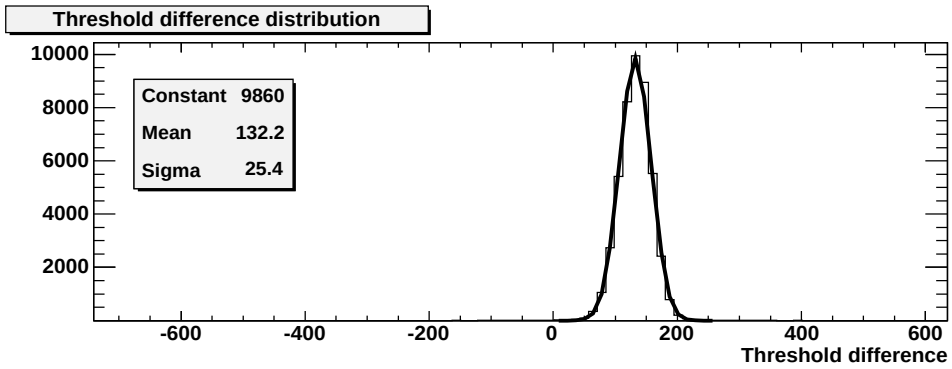


(c) Scatter plot of the noise value differences.

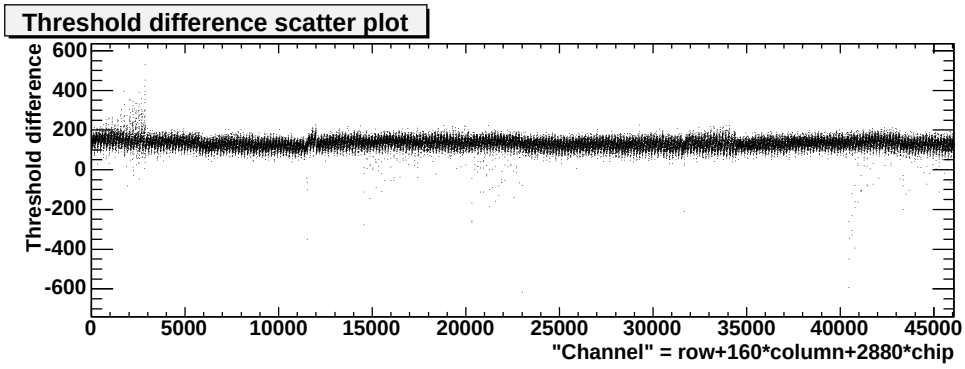
Figure 6.10: The calculated difference of the pixel noise values measured with the TurboDAQ system and the optical system for module 510868 on the test stave is shown.



(a) Pixel threshold difference.



(b) Distribution of the threshold differences.



(c) Scatter plot of the threshold differences.

Figure 6.11: The calculated difference of the pixel threshold measured with the TurboDAQ system and the optical system for module 510868 on the test stave is shown.

6.5 The Interplay of BOC Card Parameters

To guararantee good communication through the optical link, many parameters need to be controlled in order to exclude problems. A listing of all the BOC card parameters is:

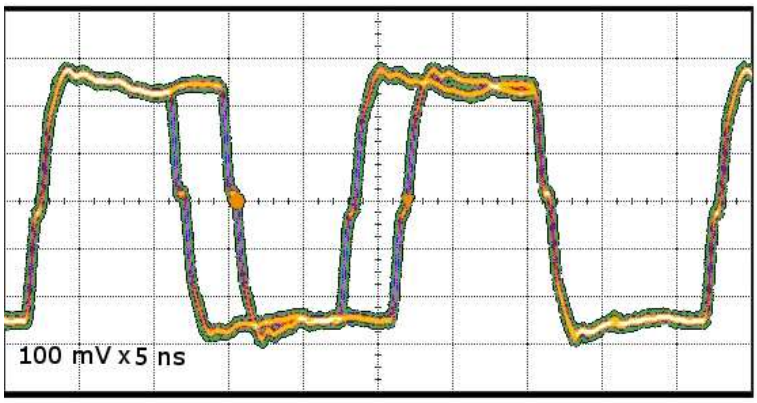
- Phase of B-clock
- Phase of P-clock
- Phase of V-clock
- TX-plugin: Laser Current
- TX-plugin: BPM Mark Space Ratio
- TX-plugin: BPM Fine Delay
- TX-plugin: BPM Coarse Delay
- TX-plugin: BPM Inhibit
- RX-plugin: RX-Threshold
- Data Delay

The BPM delays and the P-clock setting are used to delay the signals going to the modules. With these delays, a correct timing to the bunch crossing in the experiment can be determined for each module individually. This individual timing adoption will be important in the experiment in order to equalise signal propagation delays according to different cable lengths and the location of the module with respect to the interaction point. It has no effect on the system test. A study of this is described in Chapter 7.

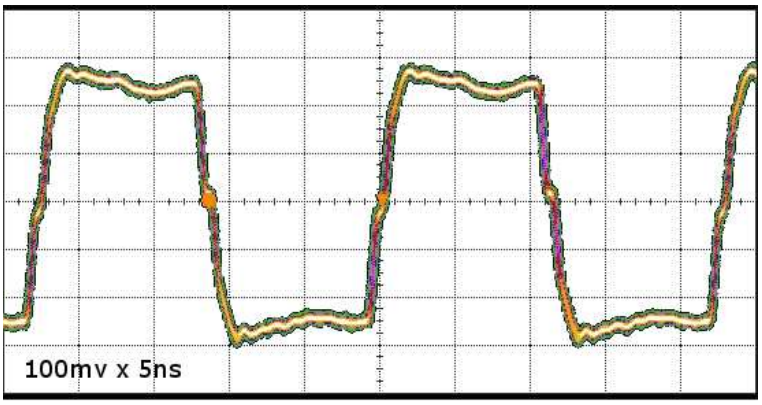
The B-clock is the first parameter to settle in the system, because it determines the phase between the ROD clock and the edges of the data sent by the BOC card to the ROD. The B-clock should be in a 90° phase with respect to the ROD-clock to have a maximal working range here.

For communicating with the modules, the TX-plugin parameters have to be set. The laser current defines the light power of the VCSEL signal. The current has to be well above the laser threshold current to get a stable signal of good shape.

The mark space ratio defines the signal duty cycle. Ideally, it should be 50%. Because the duty cycle of the signal is not only changed by its own register but also by the laser current setting and the BPM fine delay setting, one has to adopt the mark space ratio setting to this. A mistuned mark space ratio has the effect that the clock which is decoded by the DORIC on the optoboard will show a hopping between two states. The clock reconstitution is determined by the signal edges in 25 ns intervals. If these edges are



(a)



(b)

Figure 6.12: DORIC clock edge ”hopping” for different mark space ratio (MSR) settings. a) Mistuned MSR setting. The ”1” alternates a long ($50\% + x$) and a short ($50\% - x$) ”1”, while the ”0” stays at nominal width. b) Optimised MSR setting, where ”1” and ”0” always have the same ratio of 50:50.

not stable in time because of a mistuned mark space ratio, the DORIC will reconstitute a clock which shows a longer ”1” ($50\% + x$) – a nominal ”0” (50%) – and then a shorter ”1” ($50\% - x$) – followed by a nominal ”0” again. So the regenerated clock has two states: a longer state and a shorter state. This is shown in Figure 6.12(a) for a mistuned setting and in Figure 6.12(b) for an optimised mark space ratio setting.

The pulse width difference between the long and the short one has been measured for different mark space ratio settings using one TX-plugin and one optoboard. The measurement shows that it is possible to optimise the mark space ratio setting. The minimal difference is about 0.5 ns, while the maximal difference is around 5 ns. The optimal mark space ratio setting depends on the channel. An optimisation per channel is necessary. Figure 6.13 shows the measurement result. The systematics and the tuning of this parameter

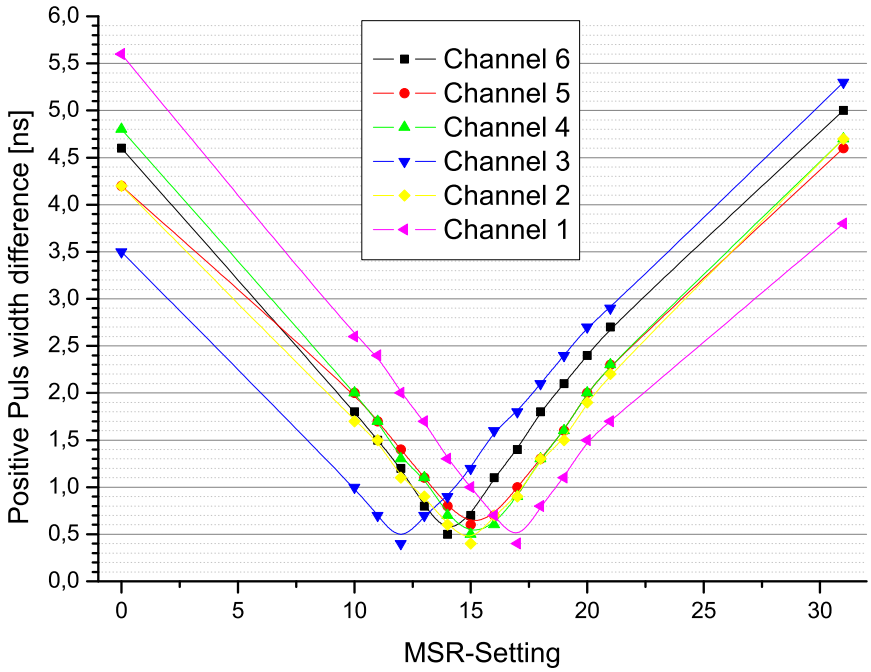
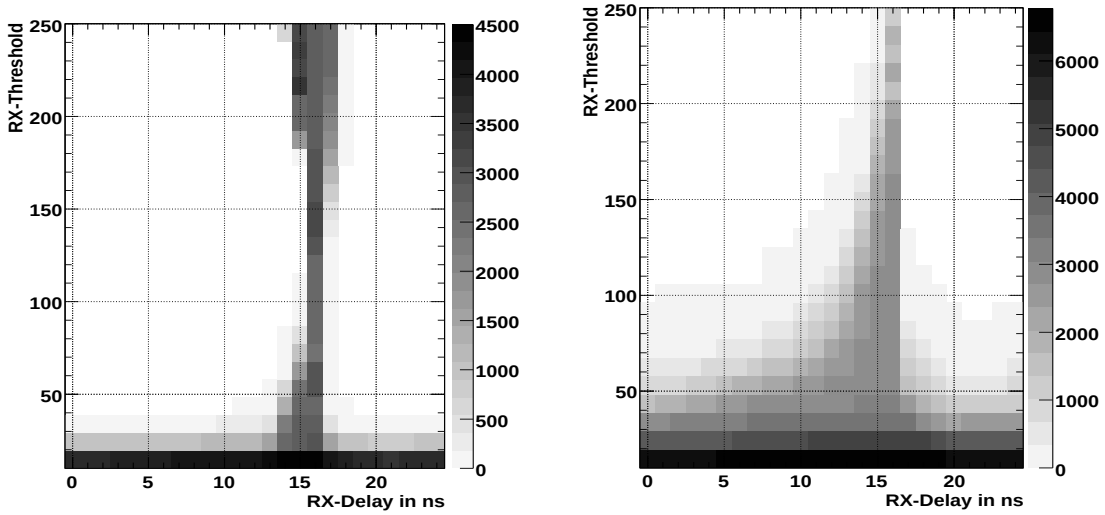


Figure 6.13: Scan of the clock edge ”hopping” in dependence of the mark space ratio (MSR) setting.

is under study [52].

The RX-Threshold setting controls an input signal threshold of the DRX. It is used to mask out noise or a signal offset. The DRX has a dynamic range. If the input current is too high, the amplifiers are driven into saturation and need some time to recover. The output would be an extended ”1”. On the other hand, a threshold too high for low power light signals will mask out the signal partially or completely. To achieve a proper function, the adjustment of the thresholds and of the light power sent from the optoboard – fitting the dynamic range of the DRX – will be necessary.

The data coming from the RX-plugin have to be registered on the BOC card and passed to the ROD. The data is sampled with the B-clock in case of the 40 Mb/s bandwidth, or with the B-clock and the V-clock (set inverted to the B-clock) in case of 80 Mb/s bandwidth. To register the data correctly it has to be guaranteed that sampling is not done at a data edge. For this purpose a delay can be applied to the data streams per channel. The delay has to be set such that a small jitter in either the data or the clocks does not harm the data sampling.



(a) (b)

Figure 6.14: Result of a 2-dimensional scan of the RX threshold versus the RX data delay. The gray scale give the bit errors in the transmission. The different behaviour depends on the light power emitted by the optoboard VCSEL. Plot a) shows the result for an optimised light power. Plot b) shows the scan result for a higher light power. The working range has shrunk.

Using the PixBoc functionalities, the software (STcontrol, in the case of system tests) is able to perform a 2-dimensional scan of the RX-threshold against the data delay. Because of having longer ones in the event of a too-low threshold, the data delay working range is influenced by this. Figure 6.14(a) and Figure 6.14(b) show the result of a data delay versus RX-Thresholds scan for two modules connected to the same optoboard. If the width of the ”high”-pulse is larger than nominal, the RX-delay range within data low pulses can be sampled correctly is shrinked. If this range becomes too narrow jitter and signal form effects will prevent a correct data registration. The measurement performs a bit error counting for the different settings. A known pattern is stored into the MCC on the module which is then read back several times. The regions with squares indicate problematic settings. The darker the square is, the more errors that have been detected. A good setting is within a large empty region. Small changes of the hardware settings should not harm the measurement results, and so a value right in the middle is a good starting point. Taking into account the characteristics of the threshold settings resulting in enlarged ”One’s” in the data pattern, a smaller delay than in the middle of the working range is chosen and a threshold setting closer to the higher limit is taken. The easiest choice of just the middle of the working region already enables a very stable data taking. To prepare the system for radiation damage and lifetime influences, an optimisation of the working points taking into account the characteristics of changes is worth being performed [52, 53].

6.6 Measurements of Data Transmission Bit Errors

For checking the quality of the data transmission, a bit error rate measurement has been performed [54]. The data link from the optoboard to the BOC card was used to transmit known bit patterns. The pattern sent has been compared to the received pattern. The bit error rate is then defined by the ratio of errors over transmitted bits:

$$BER = \frac{\text{Number of Errors}}{\text{Number of Transmitted Bits}} \tag{6.2}$$

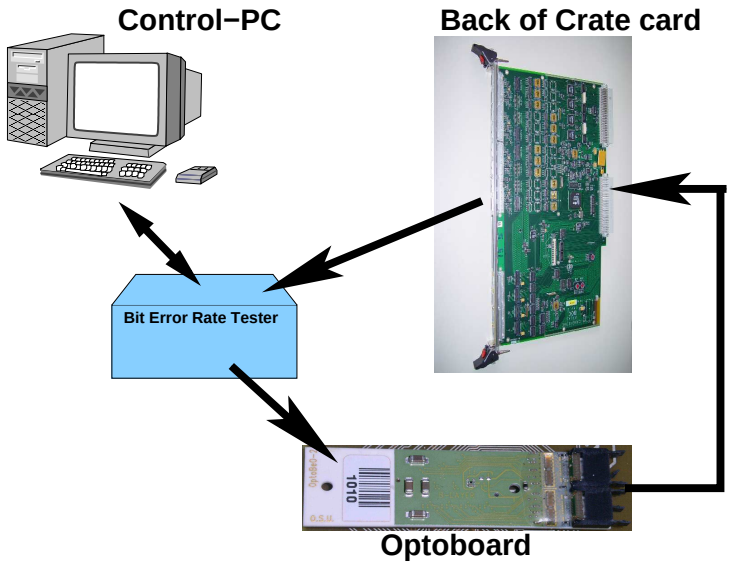
The data pattern was generated by a commercial device, a Bit Error Rate Tester (BERT) by ANRITSU (MB1630). The pattern was given to the optoboard electrically. The pattern used has been a pseudo random bit sequence (PRBS)[f]. The optoboard then transmitted the data optically to the BOC card, where the RX-plugin converted the optical data to electrical LVDS signals. The electrical signals were then fed to the BERT through a ROD-replacement board, the BOCRIG[g]. The BERT compared the pattern sent with the received pattern and calculated the bit error rate.
Because the electrical format of the data sent and received by the BERT (LVTTL format) is different from the electrical format of the signals on the optoboard and the BOC card (LVDS format), two converter boards have been designed and were used to convert between LVTTL and LVDS signals. An overview of the setup is shown in Figures 6.15(a) and 6.15(b).

With this setup, measurements for 40 Mb/s bandwidths have been performed. The measurements have been done with a B-type optoboard. This type of optoboard provides one VCSEL array with 8 connected channels and one VCSEL array with 6 connected channels. On this optoboard the VCSEL array with 8 connected channels was used. In this way it is possible to test a complete RX-plugin on all 8 channels. The results of the measurements are presented in Table 6.4. The four measurements given are separate runs with 8 channels in parallel. The duration of the measurements is given and the number of transferred bits and counted errors. The bit error rate limit is calculated by equation 6.3.

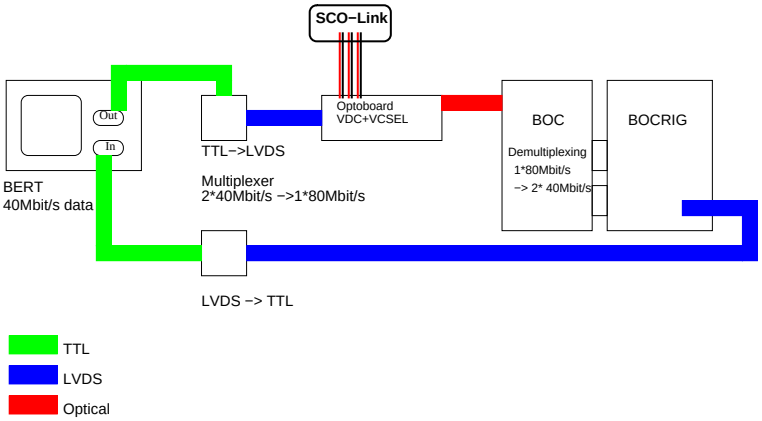
To test the functionality for the 80 Mb/s and 160 Mb/s bandwidths, the same measurement has been repeated with 80 Mb/s data streams. Because the BERT had to run with 40 Mb/s due to the clocking of the system, the 80 Mb/s data streams have been built up by two 40 Mb/s streams. A data multiplexing has been intergrated in front of the optoboard, multiplexing two 40 Mb/s streams to one 80 Mb/s stream for the optoboard. This way four 80 Mb/s data streams have been sent by the optoboard to the RX-plugin on the BOC card. The BOC card then demultiplexes each stream into two 40 Mb/s streams, which are returned to the BERT again. The 4 data streams have been sent in 4 configurations to the BOC card. In 80 Mb/s mode only two RX-plugins are mounted on the BOC card.

[f] PRBS: Pseudo-Random Bit Sequence. A sequence of bits in which all permutations of a given number of bits (0 or 1) are included.

[g] BOCRIG = 9U PCB replacing the ROD. It interfaces the VME bus to the BOC card and vice versa. Additionally, there is a data interface for incoming data and outgoing data.



(a) Components of the bit error rate measurement.



(b) Schematical overview of the setup for the bit error rate measurement.

Figure 6.15: The bit error rate test setup.

The data streams have been sent to either the upper 4 or the lower 4 channels of the RX-plugins for both plugin locations. In total, 4 configurations have been measured, testing each data link available on the BOC card. A schematic of the data routing inside the BOC card is given in Figure 4.10. The results are shown in Table 6.5. Again, the bit error rate limit is calculated by Equation 6.3.

During the measurements a disturbance of the optical transmission due to effects coming from outside the test setup has been recognised. The disturbance affected all measured channels at the same time. It was correlated to the switching of other devices like computer, monitors, or the climate chamber in the laboratory. It acts on the supply line for the lasers, resulting in voltage decreases and a light signal too weak to be registered by the

Measurement	Duration [s]	Number of Errors	Number of Bits sent [10^{12}]	Bit Error Rate Limit (90% CL)
1	13124	0	4.0353	$5.699 \cdot 10^{-13}$
2	146169	0	46.7741	$4.917 \cdot 10^{-14}$
3	244987	0	78.3958	$2.934 \cdot 10^{-14}$
4	90988	0	29.1162	$7.899 \cdot 10^{-14}$
Total	495268	0	158.3214	$1.453 \cdot 10^{-14}$

Table 6.4: Measurement of the bit errors at 40 Mb/s bandwidth.

Measurement	Duration [s]	Number of Errors	Number of Bits sent [10^{13}]	Bit Error Rate Limit (90% CL)
1	62866	0	2.012	$1.14 \cdot 10^{-13}$
2	68797	0	2.202	$1.04 \cdot 10^{-13}$
3	8277	0	0.265	$8.68 \cdot 10^{-13}$
4	80361	0	1.875	$1.23 \cdot 10^{-13}$
Total	220301	0	6.353	$3.62 \cdot 10^{-13}$

Table 6.5: Measurement of the bit errors at 80 Mb/s bandwidth.

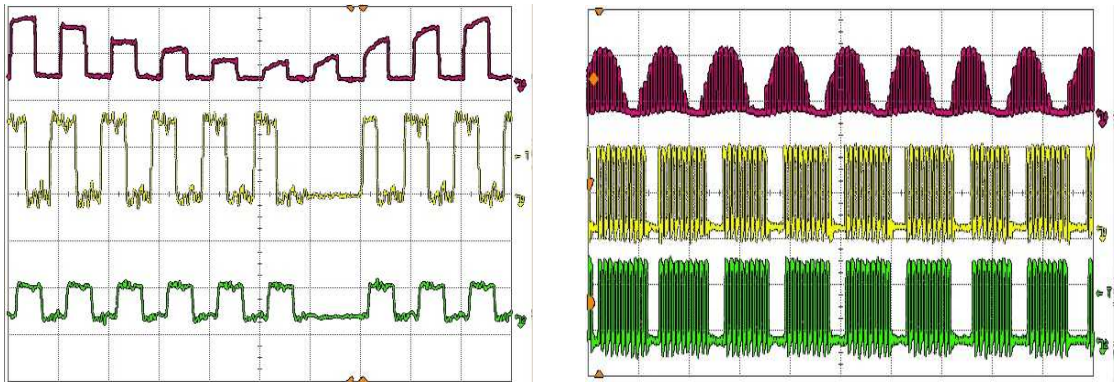
RX-plugin.

In Figures 6.16(a) and 6.16(b) such an error behaviour is shown. In purple the optical signal transmitted on channel 1 of the used optoboard is scoped. In green and yellow the signal on the BOC for channel 2 of the optoboard before (yellow) and after (green) the sampling of the data is shown. The light signal amplitude drops periodically to the light off state, where no signal can be registered on the BOC card.

This kind of effect seems to come through the ground lines of the power network into the system. Some isolation has been tried which decreased the effect, but did not eliminate it. Connecting an oscilloscope to the power lines and the read out signals introduces another ground loop into the setup. This makes a trustable measurement on the supply lines triggered by the observed error behaviour impossible.

Most problematic in the test setup is the electrical connection between the sending and the receiving part of the link inside the BERT. This means that a complete decoupling of the two ends of the optical path is not possible. A solution for this problem has not been found yet. Further studies for this are necessary.

Neglecting these disturbance effects, the results show a very smooth running of the data transmission in either 40 Mb/s or 80 Mb/s bandwith. The performance is very stable over



(a) (b)

Figure 6.16: Signals transmitted by the optoboard in case of induced errors. Scoped are the optical signal (purple) of channel 1 and the received signal (yellow and green) on the BOC for channel 2. The yellow line shows the signal before sampling (RX-plugin output), the green line shows the sampled signal.

Bandwidth	**Number of Error Counts**	**Number of Bits sent**	**Bit Error Rate Upper Limit** (90% CL)
40 Mb/s	0	$15.832 \cdot 10^{13}$	$1.45 \cdot 10^{-14}$
80 Mb/s	0	$6.353 \cdot 10^{13}$	$3.62 \cdot 10^{-14}$

Table 6.6: Results for the bit error rate measurement combining all runs at a certain bandwidth. The limits are calculated by equation 6.3 to a confidence level (CL) of 90%.

long periods of time. On average, the disturbances happened two times a day. The data routing had been tested to work as expected and does not introduce any errors in the data transmission.
The combination of all measurement runs for a certain bandwidth give a limit for the bit error rate with a confidence level of 90% by:

$$BER = \frac{2.3 + (\text{Number of errors})}{\text{Number of bits sent}} \tag{6.3}$$

The results of this calculation are shown in Table 6.6. The limit achieved, on the order of 10^{-14}, is a good result for the operation of the optical link used in the ATLAS pixel detector.

6.7 Conclusion

By introducing the BOC card in different setups useful experience has been gained. The obtained knowledge of controlling and operation of the BOC card will help to introduce and operate the BOC card in the final ATLAS experiment. The three main topics of the system test study have been:

- The introduction of the optical data transmission into the system tests.
- The study of the BOC card parameter interplay.
- The measurement of the bit error rate of the data link using the BOC card.

The development of the steering software for the BOC card to be used in the system tests and, later, in the combined test beam setup (see Chapter 7) was the basis for introducting of the optical link in the readout. The tests which have been performed up to now promise a stable operation of the BOC card in the data transmission. The tests of the module performance show a good operation of the BOC card and the function of the steering software on the one hand, and the necessity of tuning on the other hand. The behaviour of the parameters to control the BOC card and their interaction has been studied in more detail. It has been observed that there are dependencies between the parameters for the control of the transmission section, and that the complete link is sensitive to a mistuning of the control parameters. Important knowledge of this behaviour has been acquired. As a result, further studies concerning the tuning of the BOC card parameters and the long term stability of these settings are under investigation.

The measurement of the bit error rate as a quality check for the data transmission turned out to be very sensitive to any external disturbances. A clean decoupling of the power supply lines for the optoboard is necessary and will be integrated into the supply lines in the ATLAS detector. The measured bit error rate of order of 10^{-14} is a good result compared to the minimal requirements of 10^{-12}. To scale this to the ATLAS data transmission and the consequences for the physics data taking is to be done [55]. This depends strongly on the different bandwidths of the readout, the occupancy in the pixel detector, and the format of the data to be transmitted.

All in all, the optical data transmission system, including the optoboard, the fibre connections, and the BOC card, has been operated successfully and the performance is as good as expected.

Chapter 7

Study of the Pixel Detector Timing at the Combined Test Beam

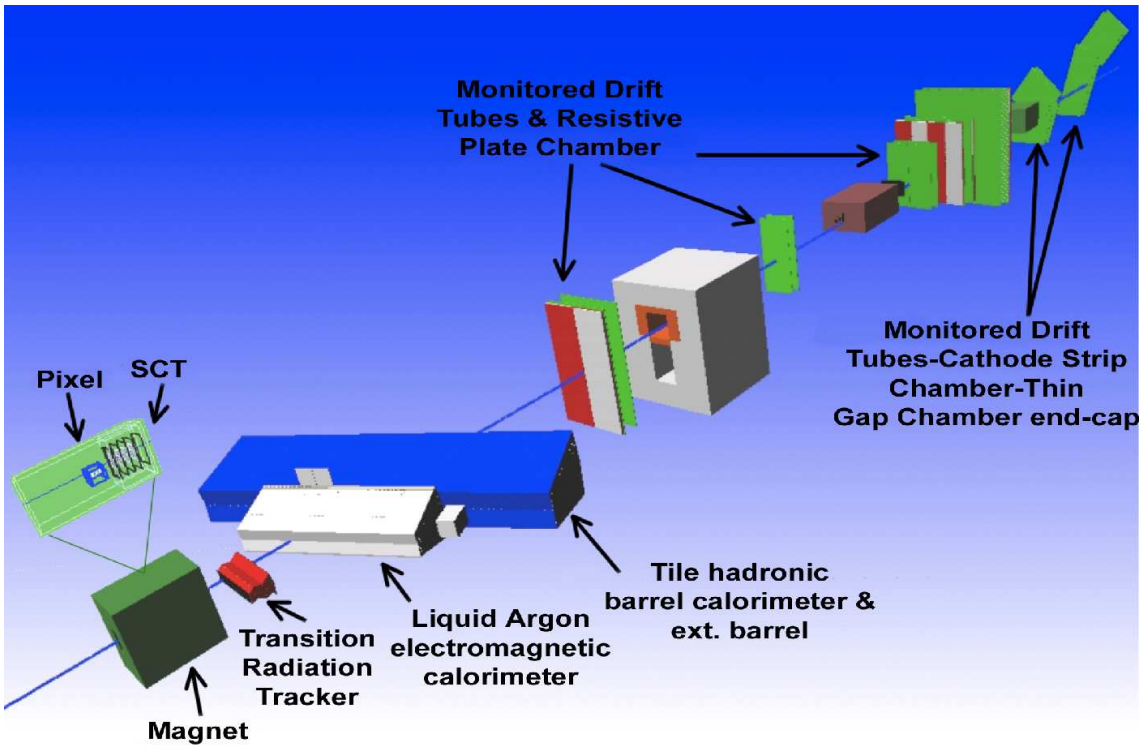


Figure 7.1: Overview of the Combined Test Beam setup.

In 2004 a slice of the ATLAS detector was built up in a test beam environment at the H8[a] line of the CERN SPS[b]. It was operated for several months. All subdetectors were represented. The beam traversed all detectors in the same manner a particle would in the ATLAS experiment. The goal and the setup of the combined test beam is described in the next section. This thesis then concentrates on the pixel detector. During a period of running with beam crossing intervals of 25 ns, a study of the timing behaviour of the pixel detector under a 40 MHz bunch crossing situation was performed.

The timing of the pixel detector is a module-specific property. The clock which the module operates with is transmitted from the BOC card. The clock can be adjusted in time over a wide range. The resolution of the clock setting is 280 ps. As described in Chapter 3, the clock transmission is performed over an optical link from the BOC card to the optoboard. The optoboard converts the optical signal into electrical ones and sends the clock and commands via an aluminium cable to the module. The signal transmission time depends on the cable length. Depending on the position of the module inside the pixel detector, the electrical cable will be between 0.8 m and 1.4 m long. In addition, the position of the module with respect to the interaction point implies a different flight length of the particles to be detected. All in all, the timing of each module has to be adjusted.

The timing adjustment is critical because of the readout technique of the modules. A LV1 trigger signal received by the module marks all hits which have been registered in a certain 25 ns wide window. Due to the timewalk effects of the hit recognition (described in Chapter 3) the read out window has to be optimised to get as many hits read out as possible. How this should work is described later in this chapter.

7.1 The CTB Purpose and Setup

Figure 7.1 gives an overview of the combined test beam setup. The setup was structured like the ATLAS experiment except that the TRT was not in the magnetic field. At the first station the tracking detectors were installed. The pixel detector and the SCT were situated in a magnetic field, with the TRT directly behind it. The distances between the detector parts have been arranged to be as close as possible to those in the ATLAS experiment. The liquid argon electromagnetic calorimeter was placed inside a cryostat followed by the tile hadronic calorimeter. At the end of the queue the muon spectrometer was set up, comprised by all types of muon detectors: monitored drift tubes, thin gap chambers, resistive plate chambers, and cathode strip chambers. The triggering was provided by the muon spectrometer and the calorimeters and was distributed over the central trigger processors. The setup was constructed with the beam direction reflecting the $\eta = 0$ direction in the ATLAS experiment. In ATLAS, this would be at 90° with respect to

[a]Experimental area at an outlet of the SPS at CERN

[b]The Super Proton Synchrotron (SPS) at CERN provides several beam outlets for experiments or test beams. At the outlet areas there are experimental halls where experiments are set up or detector parts can be tested under real beam conditions.

the beam pipe. All in all, a realistic representation of the experiment was obtained as in ATLAS later on, and the test beam setup might be used as a reference system.

The coordinate system in the test beam setup was oriented to have the x-axis parallel to the beam, the y-axis pointing upwards, and the z-direction horizontally. This was to give a coordinate system compatible with ATLAS. The origin was taken as the front of the inner detector magnet. The configuration which was used during the measurements presented in this chapter is named ”InnerDetector-CTB-04” [56]. It is given through:

- Pixel configuration: x=146 mm, y=0 mm, z=8 mm, no rotation.
- SCT configuration: x=512 mm, y=0 mm, z=-9 mm, no rotation.
- TRT configuration: x=1152 mm, y=-8 mm, z=55 mm, rotation around the z-axis by -0.205 rad.

Emulating the ATLAS experimental situation of data taking was the purpose of the combined test beam. The whole detector was studied. The trigger provided by the trigger elements and the acting of all the subdetectors was analysed under beam conditions. The control of the detector had to handle all subdetectors, and the reconstruction received data from all the detector parts. In addition to studies of different parts of the detector, like trigger generated by the calorimeters and the muon chambers, or inner detector studies, 25 ns beam periods, ”all together” runs have been taken.

The main aims of the combined test beam were a precommissioning of the final elements and performance studies in a realistic combined data taking. Over 7 months of running, much experience in the operation of the detector was gained and a large amount of data has been taken. About 2.5 TB of data has been written in around 6200 certified files. This enabled much offline analysis and tests for the reconstruction software. The analysis of combined test beam data will help to understand the detector behaviour. In addition the software can be tested.

7.1.1 Pixel Setup

For the pixel detector six pixel modules were installed. They were arranged in three layers like in the barrel region (see Figure 7.2). Each layer consisted of two modules. The modules were affixed to a carbon-carbon carrier structure which included the cooling system. All 6 modules were housed in a cooling box. The dimensions of the box were

$$\Delta x = 175 \text{ mm}, \qquad \Delta y = 250 \text{ mm}, \qquad \Delta z = 180 \text{ mm}$$

The three layers were arranged at distances of

$$x_1 = 55.5 \text{ mm}, \qquad x_2 = 85.8 \text{ mm}, \qquad x_3 = 122.5 \text{ mm}$$

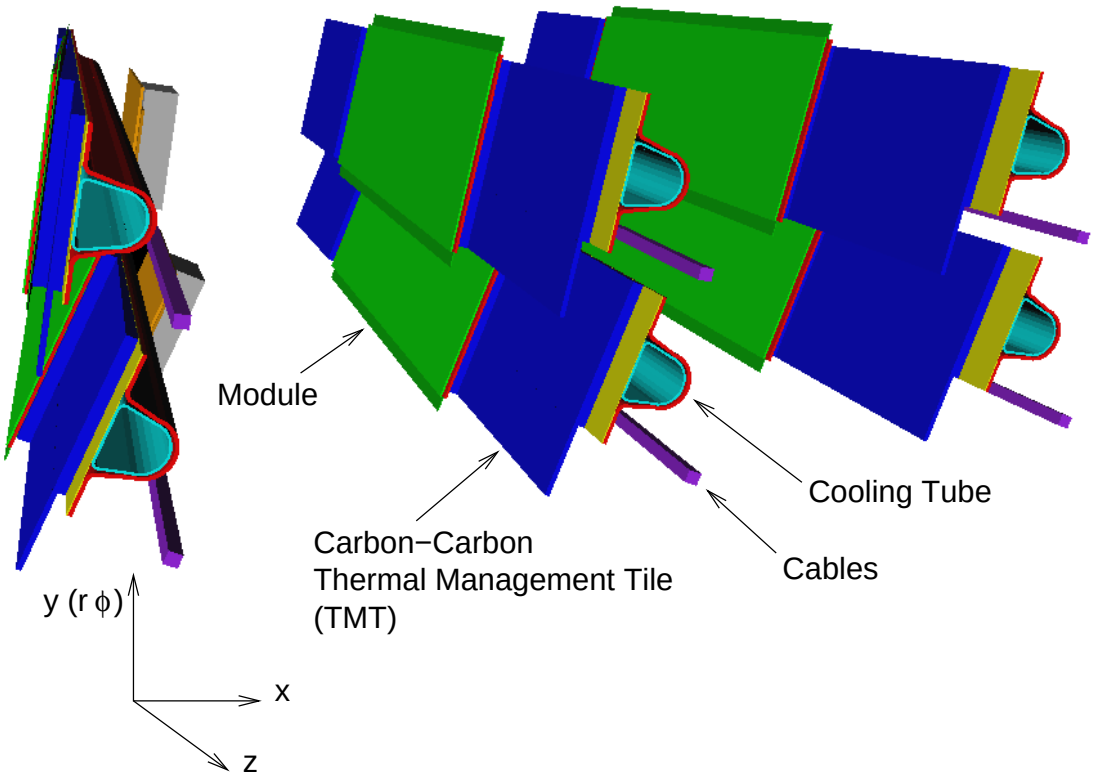


Figure 7.2: GEANT simulation of the pixel detector in the Combined Test Beam setup.

with respect to the front of the pixel box which is compatible with the ATLAS origin. The front of the pixel box is displaced by +146 mm for the CTB origin. The pixel layer configuration is nearly equivalent to the distances of the 3 layers from the beam pipe in the ATLAS experiment. The modules were arranged to have the long pixel side in z-direction and the short side in y-direction. They were mounted to overlap by 0.2 mm on the long side of the modules as it is for two neighboured staves in the ATLAS experiment. The upper module was designated as $\Phi = 1$, and the lower one as $\Phi = 0$. The modules were arranged with an angle with respect to the beam. All the numbers are summarised in Table 7.1.

The cooling of the pixel detector was realized as a chiller using a cooling liquid which was pumped through the cooling tubes of the pixel box. The pixel box was situated inside the magnet, while the chiller had to be outside the magnet for safe operation. Five meter cooling tubes were used to transport the cooling liquid to the pixel box. The heat transport was poor and the normal operation temperature of the modules was between +40° C and +50° C (see Table 7.1). As previously stated, temperature differences induce a change of some module properties like threshold, noise, and threshold dispersion. These parame-

Module Nr: ID	Link Number	Φ	Layer	Angle	Operation Temperature
0 : 510902	1	0	0	28.18°	41.5 ° C
1 : 510953	0	1	0	11.82°	39.5 ° C
2 : 510448	2	0	1	24.73°	40.0 ° C
3 : 510997	42	1	1	15.26°	43.5 ° C
4 : 510909	3	0	2	23.46°	49.5 ° C
5 : 510532	43	1	2	16.54°	48.0 ° C

Table 7.1: Pixel modules in the CTB setup. Positions in Layer and Φ and numbering is given. $\Phi = 1$ is the upper postion, $\Phi = 0$ the lower one. The angle is the deflection of the module plane from the position perpendicular to the beam direction.

ters have been tuned in the laboratory before installing the modules in the combined test beam setup. During the combined test beam a control measurement of these parameters was not possible. The laboratory measurements are taken as a reference for the modules characteristics.

7.2 The Data Runs

During the combined test beam many different data sets were taken. Each subdetector group used the beam to study the performance of its own subdetector with the rest of the detector in place and while getting triggers from the trigger system. Data for electron, pion, or proton beams on an energy scale between 1 GeV and 350 GeV has been recorded.

The data for the analysis presented here was taken during a 25 ns proton beam period. In this period the beam was structured in bunches synchronised to a 40 MHz clock, while in normal mode the beam is unsynchronised. The energy of the beam was around 100 GeV. The combined DAQ was under the control of the muon group during this period. In order to make useful studies during this period the pixel DAQ had to be operated independently form the combined DAQ. Because the pixel detector control was not connected to the combined detector control and storage, only pixel data has been recorded. The pixel readout buffer (a PC) was used to store the data on a computer hard disk. The data was not processed by the combined readout buffer and formatted as a combined event. This implies that the data contained only the pixel ROD information of the event and no further fragment headers and trailers, but the hit information of the pixel modules was kept.

To study the behaviour of the modules for a different readout timing, a scan by shifting the timing (delay) was performed. The BPM decoded clock and command signal (see Chapter 3.2) which was sent to the module from the BOC card was delayed for all modules in parallel. The data runs are listed in Table 7.2.

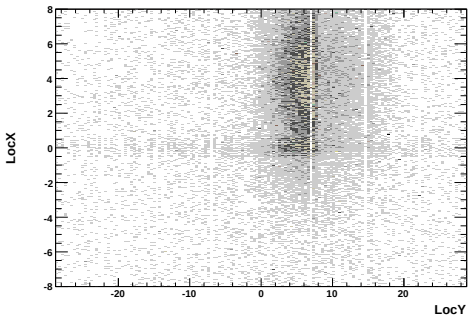
As an example, the hitmaps of the six modules for run 1241 (22 ns delay) are shown in Figures 7.3(a)-7.3(f). The numbering is as in Table 7.1. Modules 0 and 1 were in layer 0, modules 2 and 3 in layer 1, and modules 4 and 5 comprised layer 2. The beam passed layer 0 first. It can be seen from the hitmaps that the beam spot was centred on the bottom modules, covering 1 cm$\times 1$ cm, which is equivalent to ~ 2 chips per module. The dimensions LocX and LocY are the positions of the center of the cells in mm, with (0,0) as the center of the active region. The range in the area of the active region from negative the half length to positive the half length. The two modules of the same layer are mounted to overlap by 0.2 mm in LocX.

Run	Delay	Events	Comment
1230	2 ns	30000	
1231	4 ns	30000	
1233	6 ns	30000	
1235	8 ns	30000	
1248	9 ns	30000	
1245	10 ns	23000	unstable system, ROD errors
1247	11 ns	30000	
1236	12 ns	30000	
1244	14 ns	30000	
1238	16 ns	30000	system seems to be not stable
1243	19 ns	30000	
1239	20 ns	30000	
1241	22 ns	30000	
1240	24 ns	30000	

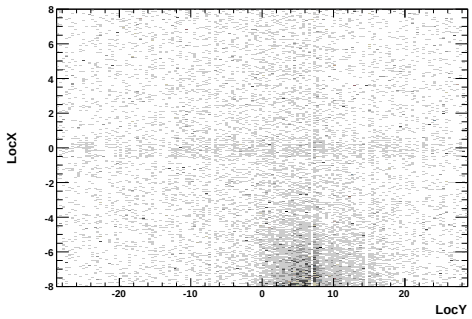
Table 7.2: Listing of the timing study runs at the combined test beam. The delay is the shift of the signal sent to the modules.

7.3 Timing of the Pixel Detector

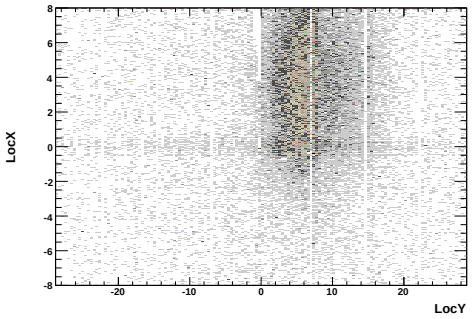
The data acquisition of the pixel detector is described in Chapter 3.1. The important points regarding the timing are summarised here once more. The pixel detector module reads out the signal of its silicon sensor. Depending on the deposited energy, a charge is generated in the sensor and is collected into the pixel cell. This charge loads a capacitor which is cleared by a constant feedback current. A plot of the hit pulse looks like a triangle (see Figure 3.12). Each pixel cell has a threshold. A hit is registered if the pulse goes above the threshold. At this point a timestamp is generated by an internal counter running at 40 MHz. This timestamp is the reference for the incoming time. A higher pulse rises steeply and goes above the threshold earlier than a smaller pulse, which rises more slowly. This effect is named timewalk. It can be measured and determines – together



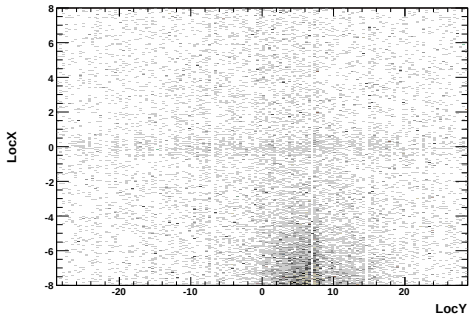
(a) Module 0: lower layer 0



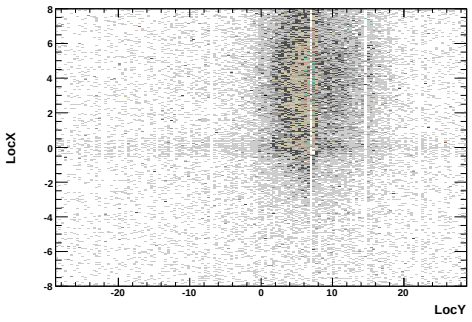
(b) Module 1: upper layer 0



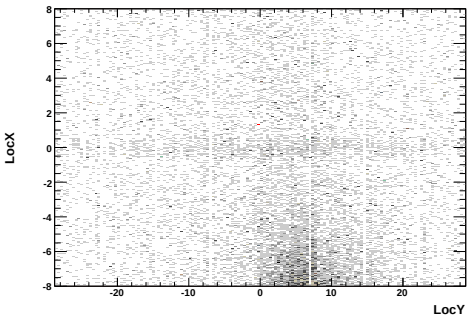
(c) Module 2: lower layer 1



(d) Module 3: upper layer 1



(e) Module 4: lower layer 2



(f) Module 5: upper layer 2

Figure 7.3: Hit maps of the modules using a delay setting of 22 ns. LocX gives the short side of the module in mm and LocY the long side in mm. There was an overlap of 0.2 mm in LocX

with the discriminator threshold – the effective threshold[c]. The capacitor is discharged linearly. The moment when the signal goes below the threshold a second timestamp is

[c]The effective threshold is the minimal amount of charge which can be registered within a 25 ns trigger window

stored, marking the end of the pulse. The difference between the two timestamps is given out as time over threshold, counted in 25 ns steps.

The trigger which is sent to the module for readout gets a timestamp with a programmable offset inside the module, as well. This timestamp is compared to the timestamp of the hits and all matching hits are read out. This means that all hits arriving in the triggered 25 ns bin are read out. To reduce data lost due to the timewalk as much as possible, the detector timing has to be optimised. To study this detector timing in the combined testbeam, the LV1 trigger which the module received was repeated 7 times inside the module. This means not only hits matching the timestamp of the trigger exactly, but all hits which have a timestamp whithin the range $timestamp_{trigger} \leq timestamp_{hit} \leq timestamp_{trigger}+7$ are read out. This way all hits which appear within a 200 ns time interval are recognised. In the readout data the trigger accept (1 of the 8 repeated) in which the hit was recognised is stored, as well.

The timewalk of the hit recognition is shown in Figure 3.13. The time to start the read out has to be chosen correctly to read out all the hits with a high energy deposition and not to lose too many low energy hits. Because most of the particles crossing the pixel detector are minimal ionising particles (MIPs) which generate $20000\ e^-$ in the sensor each, the MIPs are the reference for the timing. The detector timing has to be set such that the MIPs arrive in the beginning of a 25 ns readout window. In the laboratory, the pixel unit cells were tuned to give a TOT of 30 clock cycles for a collected charge of $20\ ke^-$.

The data taken in the timing scan provides the possibility to study the readout behaviour of the modules. The delay is scanned through a complete clock cycle in 12 steps. Because the trigger is repeated 8 times inside the module, each delay step gives 8 measurement points with a temporal separation of 25 ns each. As result a time window of 200 ns was scanned separated into 96 measurement points.

7.4 Data Analysis Methods

In the following section only plots for module 4 are shown. The other modules showed a similar behaviour and the complete set of plots for all modules can be found in Appendix A.

7.4.1 Offline Software - Athena Framework

The offline software includes several components that covers all aspects from processing of raw data to analysis of physics objects. It analyses the raw detector data to reconstruct the particle tracks and the particle properties. The software can be divided into two parts, one part which reconstructs particles and its properties, and another part to analyse the physical processes which create the particles.

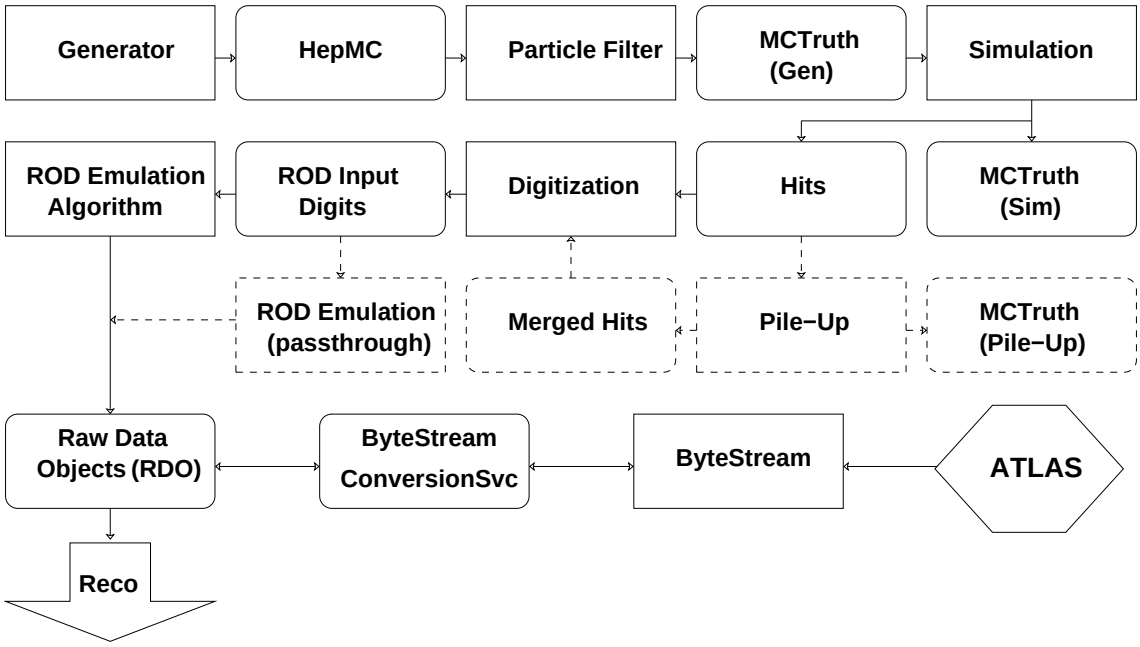


Figure 7.4: Overview of the Athena framework for the offline software development [57]. The upper three lines are showing the Monte Carlo generation being formatted into an RDO. The lower line is representing the detector data being formatted into an RDO.

The ATLAS experiment is to use an offline software framework named Athena [19]. The framework has been developed on the basis of the Gaudi-framework used by the LHCb experiment. The offline software is a collection of algorithms, tools, services (mostly in C++) which are built upon the Athena framework. The collection provides more than 50 external software packages and around 1000 ATLAS specific tools.

Each user can use the Athena packages he needs for his purpose. They can be adopted individually by the user in his own working area. The control of the used software packages is given through a PYTHON script. All the needed parameters can be set here, the environment for running is selectable, and the kind of data to read in and write out is to be set.

Athena software is used for the offline analysis of the detector data but also for running on Monte Carlo samples. For this the starting point of the analysis packages needs a certain data format, named Raw Data Object (RDO). The data coming from the detector are formatted into this by using a *ByteStream Converter*. This ByteStreamer exists for each subdetector and provides the event data in the recommended RDO data format. The Monte Carlo (MC) generated data runs through the detector simulations and is formatted into an RDO by the *Digitisation* process. In this way the same reconstruction algorithms and analysis routines can be used for MC and real data samples, and the results can be

compared. The data flow for the RDO generation is shown in Figure 7.4.

The first stage of the analysis is always the reconstruction of the particles causing the signals in the detector. This is performed by the reconstruction algorithms. Figure 7.5 gives the schematical data flow. The process starts with the RDO being generated by the ByteStreamer. The data is processed by several tools like cluster finding, space point generation, track finding, and vertex finding. The data is processed step to step from the raw information to reconstructed objects.

7.4.2 Data Preparation and Athena Routines

The data produced by the pixel detector system when running in standalone mode is not the standard input for the ByteStream Service which controls the ByteStream Converters for all subdetectors. The service checks the data format to be ATLAS detector data. The data to be analysed for the timing study does not have the ATLAS format, because they were taken by the pixel system only and miss all the headers and trailers and formating of the combined control. To process the data with Athena a modified version of the digitisation routine was used. The raw data was read in event by event. Each event was treated by the digitisation process as a simulated data set and stored into the RDO format. This way it was possible to run Athena on the generated RDO's.

To study the effect of the delay applied to the module clock, it is necessary to read back the information about the time when the hits appeared in the module. As already mentioned, the given LV1 trigger was repeated inside the module, so that 8 continuous triggers have been seen and read out. For each LV1 trigger the module generates 8 LV1 accepts (LV1A) internally and in the readout hit information is read out according to the LV1 accept. This enables an assignment of the hit information to the correct trigger window, which enables a study of the timing behaviour. Due to the fact that in the ATLAS experiment only one LV1 accept for each LV1 trigger is performed, the RDO does not include the LV1 accept information. Hence, it was included manually. The number of the LV1 accept for which

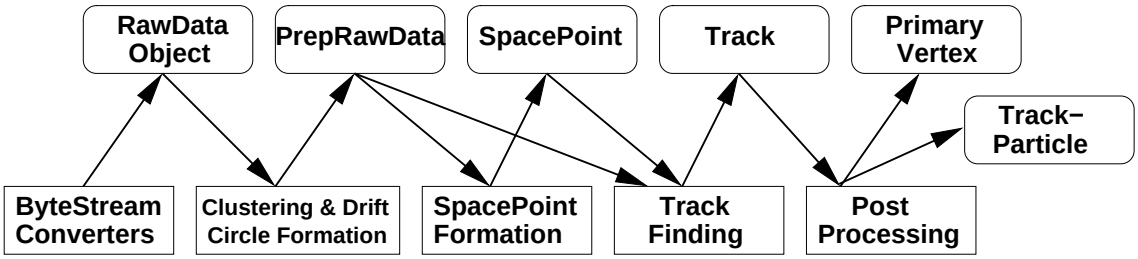


Figure 7.5: Overview of track reconstruction. The data object (top) are processed through algorithms (bottom) [57].

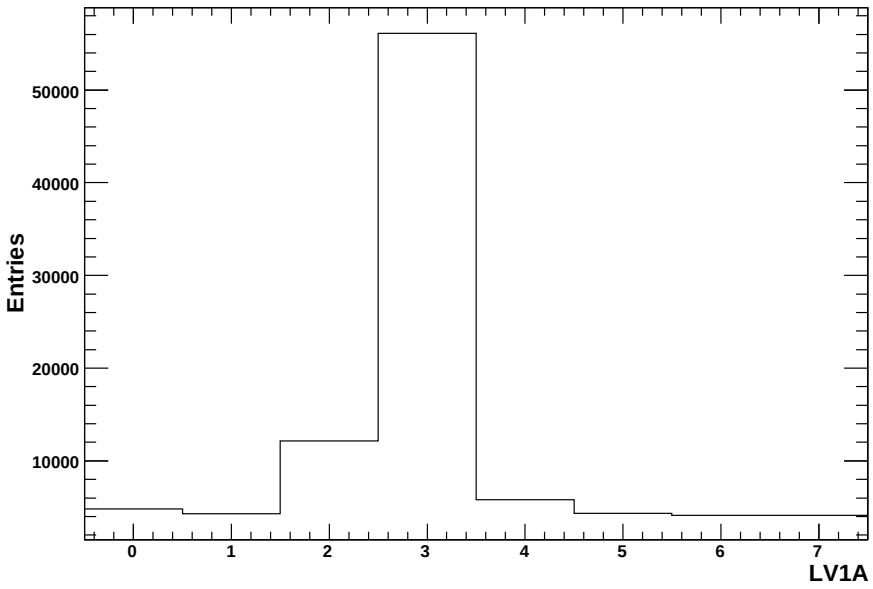


Figure 7.6: LV1 distribution for all TOT values for hits assigned to a track.

the hit was read out was added to be stored into the RDO and was extracted by a special routine inside the Athena analysis package afterwards.

The most interesting parameters of the hit inside the pixel detector are the time over threshold information (TOT) which gives information about the deposited energy, and the timing information included in the LV1 accept number. The information about the position of the hit (row, column, FE-chips) is used to perform a clustering and track finding.

7.4.3 Noise Reduction

Due to the high temperature of the modules, the noise value is expected to be higher than normal. To reduce the noise, two methods have been tried. The first is to use only data which has been assigned to a track (see Figure 7.6). One can clearly see that the floor of hits in all LV1 accept bins remains. Because this is not efficient, another cut on the noise was performed. The distribution of the hit's LV1 accept against the TOT shows a "floor" of hits with low TOT for all LV1 accept values. The region of LV1 accepts for the physical data can be determined by the high TOT hits. Because these hits are registered earliest, all LV1 accept before are obviously "noise". The LV1 accept value marked by the high TOT hits and the next 3 are taken for the data analysis. This covers a region of 100 ns to be sure to collect all the low TOT hits which arrive up to 50 ns later than the high TOT hits. To cut on the noise in these bins the TOT distributions for the other LV1 accept bins have been summed up and averaged. The result is a distribution which

gives the averaged offset. It is then subtracted from the TOT diiiistribution for all the LV1 bins. The noise floor is nearly completely removed after applying this noise correction. Because this method does not flag a single hit as noise, it is not usable for any analysis based on single hits.

In Figure 7.7(a) the LV1 accept against TOT distribution is shown for the raw data. In the region of low TOT values the noise floor can be seen in the uncorrected plot. Figure 7.7(b) shows the plot after the noise correction. The low TOT noise floor is reduced.
The uncorrected LV1 accept distribution shown in Figure 7.8(a) represents the LV1 accepts for all TOT values. The noise corrected plot is shown in Figure 7.8(b). The noise floor is nearly eliminated.

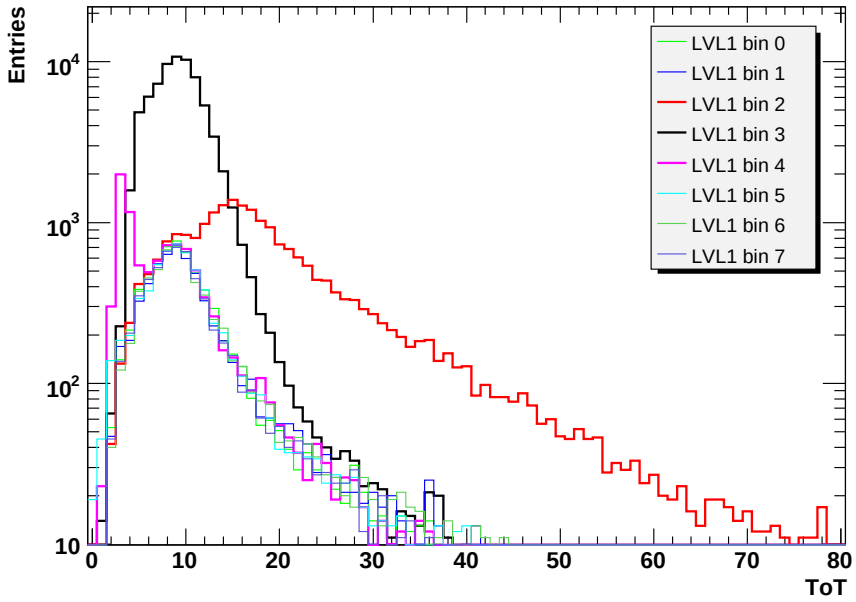
7.4.4 Hit Registering Efficiency

The aim of the study of the timing behaviour is to optimise the efficiency for registering the incoming hits. A measure for this efficiency can be defined by the ratio of the number of hits registered in LV1 accept bin i over all hits:

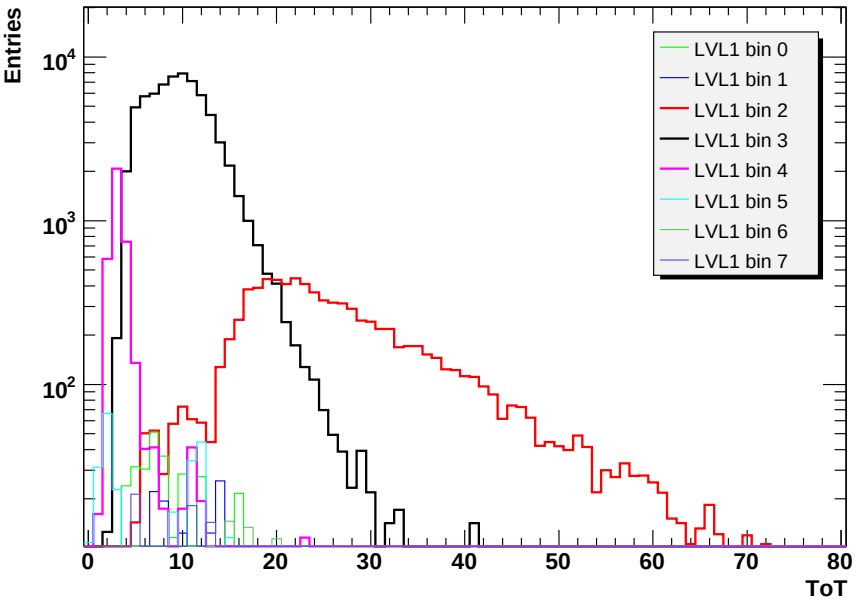
$$\varepsilon_i = \frac{N_i}{N_{total}} \tag{7.1}$$

When shifting the readout window marked by a trigger the efficiency for registering hits becomes maximal for the correct timing window.

Figure 7.9 shows this registering efficiency. The efficiency is plotted as a colour map for the different delay settings and TOT values. The efficiency value was calculated for each delay and TOT separately and filled into the histogram. It can be seen easily that there is a band of high efficiency in the region between the delay settings 20 ns and 45 ns. Due to the noise hits which are registered for all LV1 accept bins, there are entries with very low efficiency in the region beside this band. Because the noise cut is more effective for the low TOT hits (more statistic), the high TOT hits remain after the cut. One can see empty areas in the plot where no data is available. This is due to the fact that these applied delays the operation of the readout system was not stable. To correct this several adoptions in the timing of the readout would be necessary which was not possible in the given measurement period. Unfortunately it turned out in the analysis that these gaps are at the change over from the high to the low efficiency area.
It can be seen also that for low TOT the high efficiency region shifts to larger delay settings. This reflects the fact that hits with low TOT are generated by less charge in the sensor and, therefore, a pulse in the pixel cell which has a slower rise. These hits need a longer time to cross the threshold, so the hits are registered later with respect to hits with higher energy deposition. The shape of the left side (smaller delay) of the high collection efficiency band shows the timewalk. It can be compared to the shape of the timewalk plot (Figure 3.12). The underlying effects are the same and the results are comparable. The

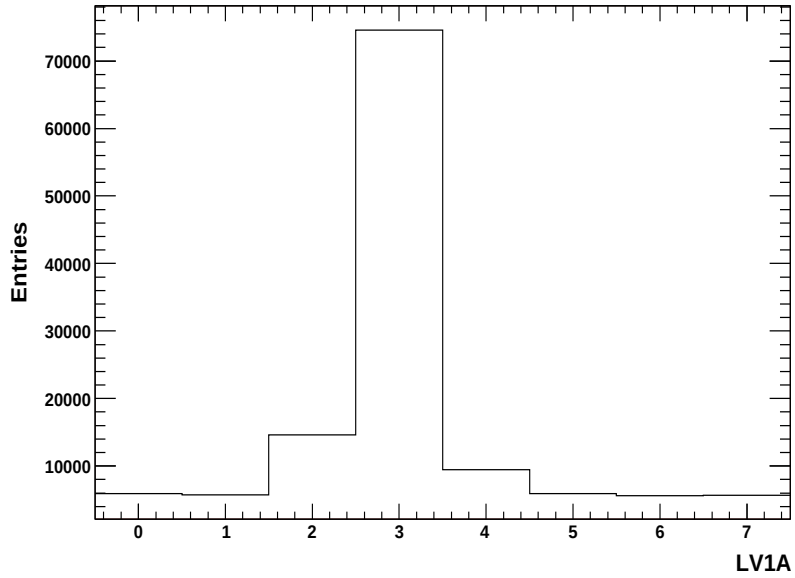


(a) Uncorrected distribution.

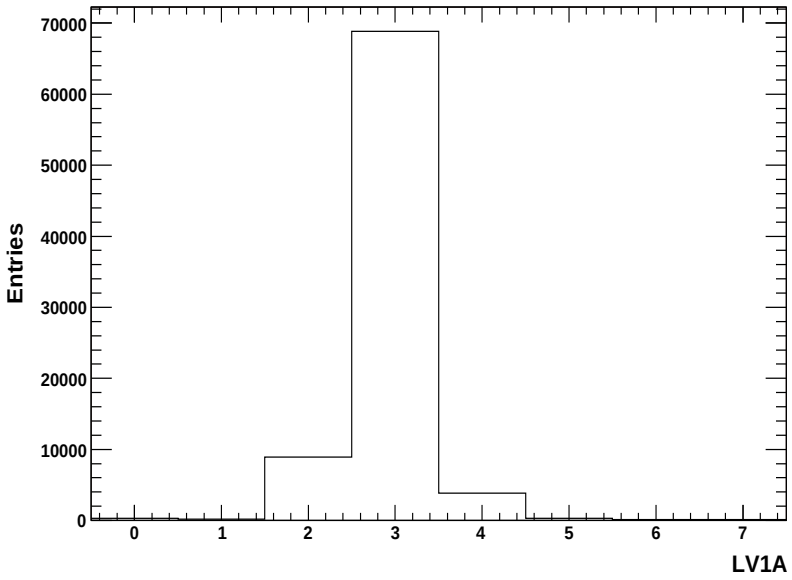


(b) Corrected distribution.

Figure 7.7: The distributions of the TOT values for the different LV1 accepts are shown. For all LV1 accept values there are many hits with low TOT, taken as noise. Hits with high TOT mark the region for registering the data correctly. These are LV1 accept bins 2-5. Data taken with a delay of 19 ns.



(a) Uncorrected distribution.



(b) Corrected distribution.

Figure 7.8: Distribution of the LV1 accepts for all TOT values. The noise level is again visible. The correct data region is between LV1 accept 2 and LV1 accept 5. Data taken in run with a delay of 19 ns.

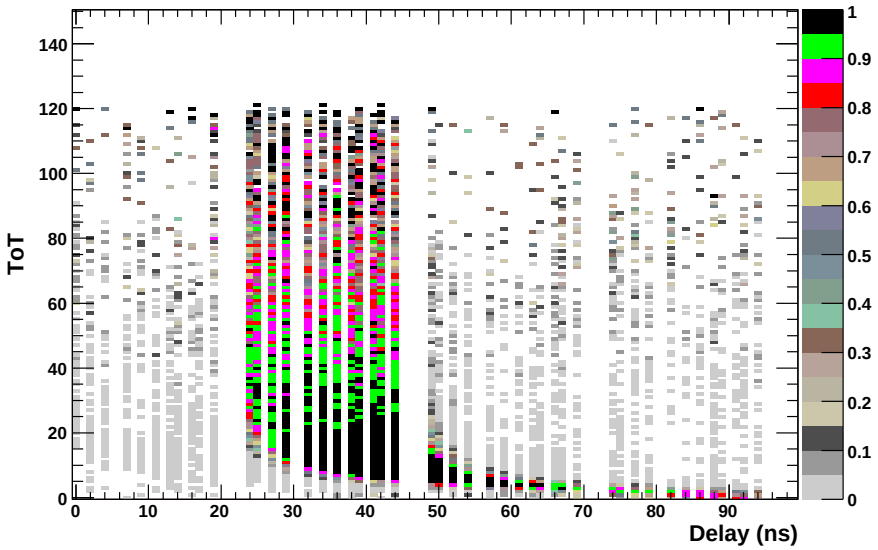


Figure 7.9: Collection efficiency. The colour represents the efficiency for the given TOT - delay setting, 2 dimensional visualisation. The plot shows the 12 delay setting for the 4 LV1 bins of interest, resulting in 48 delay settings in total.

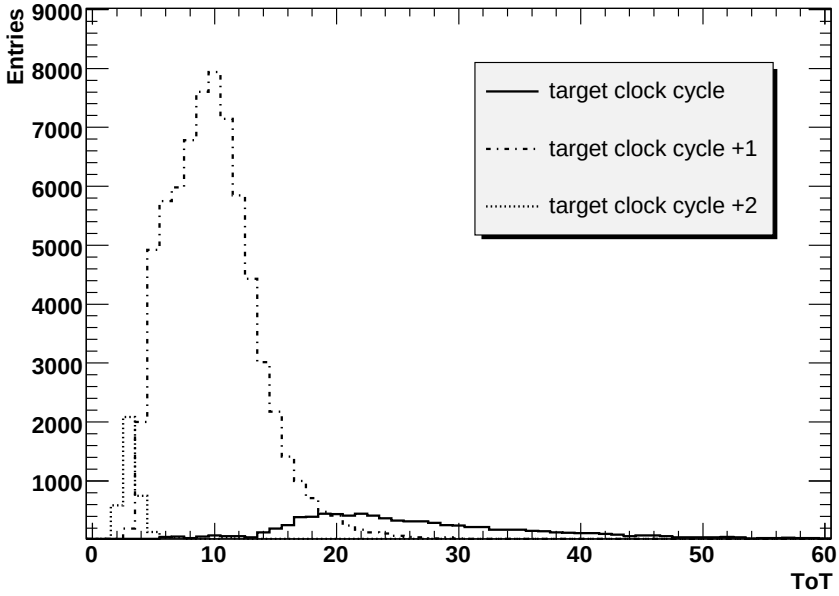
hits with very high TOT values are rare. The statistics in this region are minimal and the efficiency is lower because of the noise hits.

7.5 Adjustment of the Pixel Detector Timing

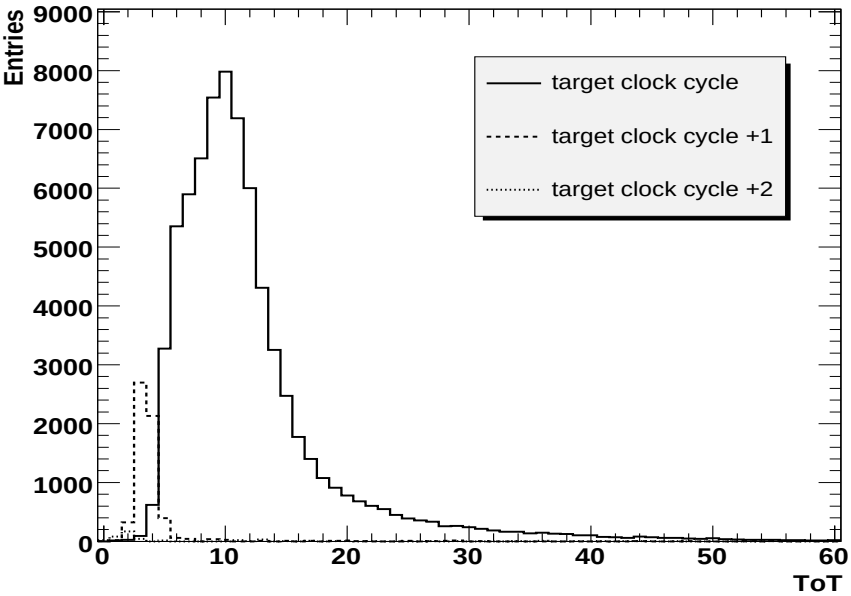
As expected, it is not possible to collect all hits within a 25 ns time window (see Section 3.1.3). Hits with low TOT are registered one clock cycle later. Therefore, it is necessary to optimise the timing of the modules so that most hits are registered in the time window belonging to the trigger. Hits with a TOT value smaller than a limit value are registered one bin later. This TOT limit can be determined from this study as well.

Figures 7.10(a) and 7.10(b) are showing the effect of the delay tuning. While for the untuned case only the high TOT hits are registered in the target time window, in the tuned case the number of hits in the target window is maximised. Anyhow the low TOT hits are registered one or even two clock cycles later.

The strategy for adjusting an optimised timing for the module is based on the fact that most particles registered by the pixel detector are minimal ionising particles (MIPs). These particles are taken as a reference for the timing. Due to the pixel detector geometry the energy deposited by the MIPs in the sensor corresponds to a charge of $20000\ e^-$, on



(a) Untuned distribution.



(b) Tuned distribution.

Figure 7.10: The distribution of the TOT values for the LV1 accept values of interest are shown for an untuned and a tuned delay confiduration. The number of hits in the target time bin are maximised.

average. The pixel modules are tuned to give a TOT of 30 clock cycles for this amount of charge. This means that hits with a TOT of 30 clock cycles are taken as a reference for

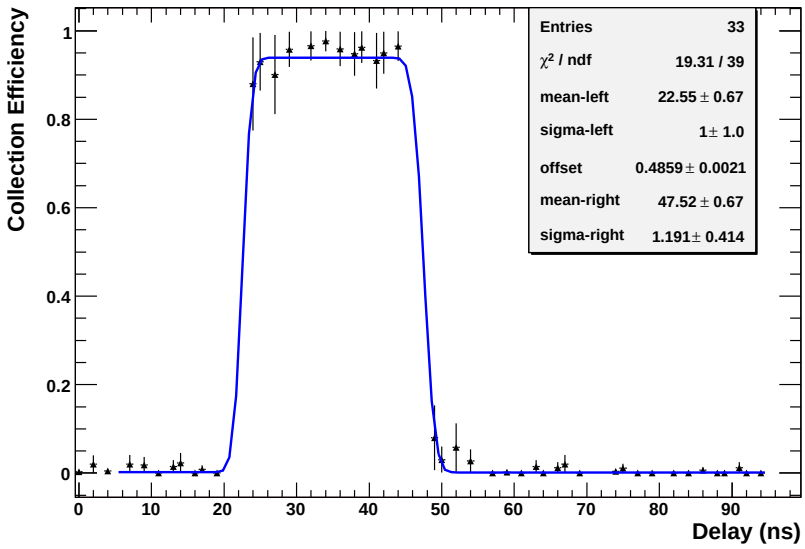


Figure 7.11: Collection efficiency versus the delay for hits with TOT=30.

the timing. The delay is adjusted so that hits with a TOT of 30 clock cycles are registered just in time. The efficency versus delay for these kind of hits is shown in Figures 7.11. The complete set of plots for all modules can be found in Figures A.7(a)-A.7(f).

Ideally the efficiency curve would have a sharp step between $\varepsilon = 0$ to $\varepsilon = 1$ and another sharp step from $\varepsilon = 1$ to $\varepsilon = 0$. The remaining "noise" hits are reducing this number to $\varepsilon = 0.94$. Due to noise and measurement effects this step is not completely sharp, but rather it is smeared out. Therefore an error function (S-curve) has been fitted to each edge. This gives a mean value for the delay settings at the start and the end of the high efficiency region. The mean values are the delay settings for which 50% of the hits are registered correctly, meaning an efficiency of 0.5. The sigma of these fits is taken as the error for the delay settings. The fit has been performed for all modules individually. The fit results are summarised in Table 7.3. The width of the high efficiency region is calculated by the difference between the rising and the falling edge. It can be seen, that the 25 ns width of the read out window is reproduced very well in the width of the region with high efficiency.

The delay setting of the rising edge of the efficiency curve is the delay for which the hits are registered just in time. This delay value has been studied for hits with different TOT values. Due to the timewalk it is expected that the in-time delay setting increases from high to low TOT values. Figure 7.12 shows the in-time delay versus TOT value plot. For low TOT values the in-time delay increases, because the hits are registered later. Additionally, it can be seen that for high TOT values, the in-time delay setting does not change anymore, it propagates asymptotically against the time at which the pulse in the electronics starts. For module 4, shown here, this in-time delay setting is about 22 ns.

Module	In-time Delay [ns]	Off-time Delay [ns]	Width [ns]
0	21 ± 2.6	47.12 ± 0.31	26.12 ± 2.62
1	22.34 ± 0.57	47.4 ± 0.3	25.06 ± 0.64
2	22.47 ± 0.54	47.99 ± 0.77	25.52 ± 0.94
3	21 ± 0.4	45.95 ± 0.97	24.95 ± 1.05
4	22.55 ± 0.67	47.52 ± 0.67	25.07 ± 0.95
5	21.59 ± 1.08	47.48 ± 0.61	25.89 ± 1.24

Table 7.3: Summary of fitted values for the efficiency for hits with a TOT of 30 clock cycles.

The trigger window is 25 ns wide. This means, that all hits being registered within a time window of 25 ns can be read out by one trigger. As can be seen from this plot, there will be hits which are out of this time window. These hits will not be read out and are lost. The goal must be to optimise the read out window to be able to read out as much hits as possible. Inside the front end chips there will be a feature to read out low TOT hits asigned to the next 25 ns cycle as well, which will be discussed later on. Loosing the low TOT hits has two implications. On th one hand if the hit is an isolated hit the complete information is lost. In case of the test beam, the fraction of tracks with isolated low TOT hits of the order 0.2 %. On the other hand, and this is much more likely, the low TOT hit belongs to a cluster of hits. For the test beam this is the case in around 10 % of the tracks. Most likely the charge is not shared equally in this cluster and the hits with higher TOT are read out and give a track information. In case of an equal charge sharing the minimum charge per pixel is 5000 e^- per pixel. Not to lose such hits the module has to be optimised to be able to read out this kind of hits, which means that the effective threshold should be below 5000 e^-.

7.6 The Timewalk

For the measured in-time delay setting of 22 ns it is possible to measure the minimal TOT for which hits can be registered in the correct time window. This TOT can be translated into a charge, the minimal charge which is necessary to register the hit in the correct time window. A typical relation between TOT and charge is shown in Figure 7.13.

The measurement principle is analogous to the laboratory measurement of the timewalk, but instead of pulsing the electronics, the measurement is performed with data of traversing particles. Similarly to the timewalk measurement, the charge, or TOT, of hits being registered in-time for a delay setting of $22\ ns + 20\ ns = 42\ ns$ is measured. The missing 5 ns to complete the clock cycle are a safety margin. Therefore only 20 ns of the trigger window are effectively used for the hit read out. This has influences on the effective threshold, too. In the readout of the ATLAS pixel detector this safety should be

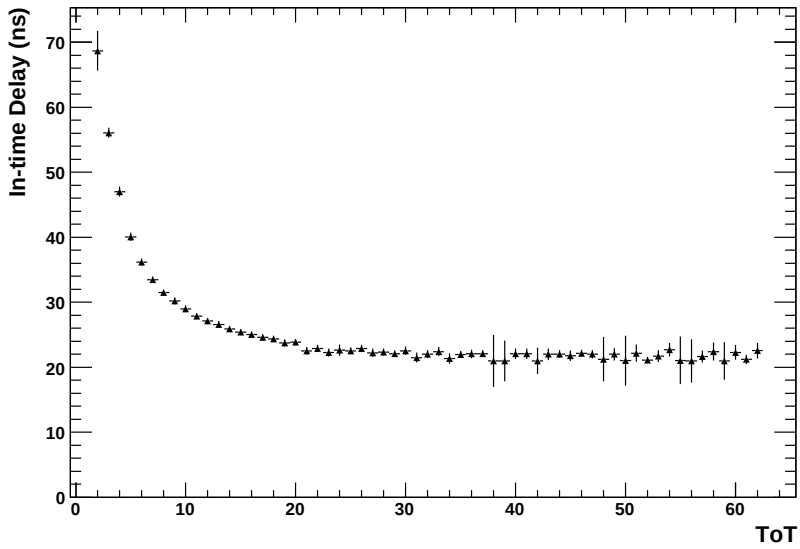


Figure 7.12: Delay setting for in-time registering versus the TOT.

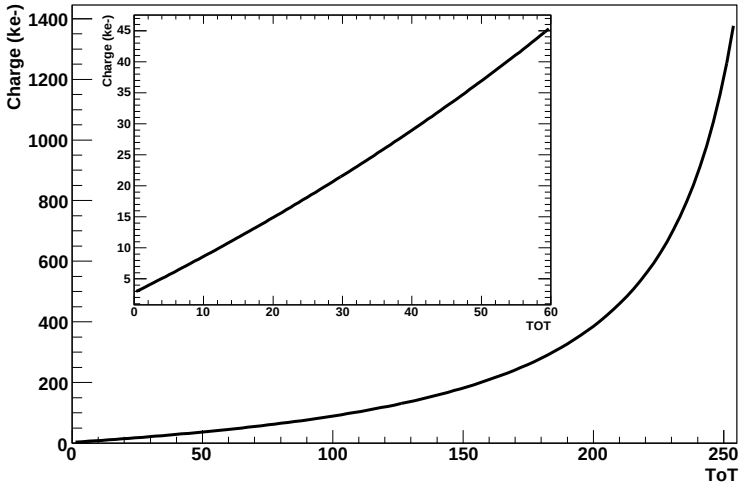


Figure 7.13: A typical relation between the charge and the TOT value.

explored again, to be sure not to influence the data taking too much and therefore reduce the hit readout efficiency. In Figure 7.14 the efficiency versus TOT is shown for the time interval between 22 ns and 42 ns. It can be seen that the TOT thresholds for registering hits is at a TOT of 5 clock cycles. This can be translated into a charge using laboratory measurements of a TOT to charge calibration.

$$TOT = A + \frac{B}{C + Q} \tag{7.2}$$

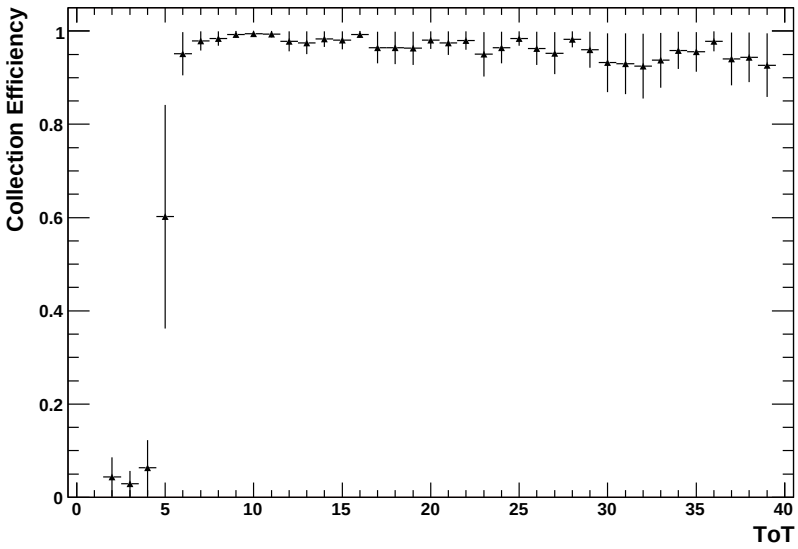


Figure 7.14: Collection efficiency as a function of the TOT for the optimised delay setting of 22 ns. Hits with a TOT lower than 5 clock cycles are not registered in the readout window.

Equation 7.2 describes the dependency between the TOT and the charge Q being collected from the sensor. A, B, and C are fit parameters. The laboratory measurements perform a TOT-charge fit for each pixel separately. This means that an exact analysis would have to use a TOT to charge calibration for each individual pixel. Due to the fact that the operation parameters like threshold, noise value, and TOT calibration at the combined test beam setup are not known exactly, in this analysis an average TOT to charge calibration is used for each module. The parameters used are noted in Table 7.4. With this it is possible to

Module Nr.	**Injection Capacitor**	**A**	**ΔA**	**B [10^7]**	**ΔB [10^3]**	**C**	**ΔC**
510448	low	303.25	0.14	-5.22	47.91	169498.71	89.40
510532	low	306.23	0.12	-5.30	44.57	170681.96	79.04
510902	low	297.75	0.11	-5.11	38.44	169518.30	68.07
510909	low	283.09	0.13	-4.50	45.01	156152.68	87.03
510953	low	312.22	0.12	-5.33	43.08	167538.40	73.33
510997	low	305.44	0.13	-5.39	42.15	174240.04	79.49

Table 7.4: TOT to charge calibration results from the laboratory measurements for the combined test beam pixel modules (Equation 7.2). The errors given are the uncertainties of the fit parameters.

calculate the minimal charge which would be recognised as a hit by the electronic cell. Using Equation 7.2 the corresponding charge Q is extracted. The results are listed in Table 7.5. The aimed effective threshold is 5000 e^-. This reflects a 20000 e^- pulse which is shared equally between four pixel cells. This is a worst case which unlikely due to the geometry of the pixel detector. The measured values are close to the aimed value. Taking into account the circumstances and high operation temperatures of the modules, the result shows the possibility to be sensitive to MIP's sharing the energy to four pixels equally. This means that instead of having one pixel with 20000 e^- there are four pixels with 5000 e^- which have to be read out.

Unfortunately, only 2 of the 6 modules showed a reasonable timewalk result in the laboratory scans performed in Genova before being mounted into the testbeam setup. At a temperature of $-7°$ C module 510909 showed an effective threshold of 4398 e^- and module 510448 showed 4472 e^-. The threshold was tuned to be $3000\ e^-$ for these modules before performing the timewalk measurement. At the combined test beam the threshold was tuned to be $4000\ e^-$. This is why the testbeam results are around 1000 e^- higher. They match the expected value very well.

7.7 Single Hits with Low TOT

To estimate the effect of isolated hits with a very low TOT being registered in a later time bin, the cluster size of the events including a low TOT hit have been studied. A particle traversing the pixel detector may hit between one and four pixels. The deposited energy is shared between the hit pixels. The amount of energy deposited in each pixel depends on the exact location of the traversing particle. In this way, a location correction can be performed due to the energy, or charge / TOT, deposited in the pixels. For the given pixel detector geometry the particles will traverse the detector with a larger angle. This leads to a high probability of having an unbalanced charge sharing between the pixel cells, which is the most probable scenario, there will be pixel cells collecting less charge than 5000 e^-, while the neighboured pixel(s) will collect more charge.

Module Nr.	**Module ID**	**Minimal TOT**	**Effective Threshold [e^-]**
0	510902	5	4882 ± 161
1	510953	5	5982 ± 172
2	510448	5	5568 ± 202
3	510997	5	5305 ± 178
4	510909	5	5510 ± 200
5	510532	5	5142 ± 182

Table 7.5: Results of the effective thresholds from the combined test beam measurements.

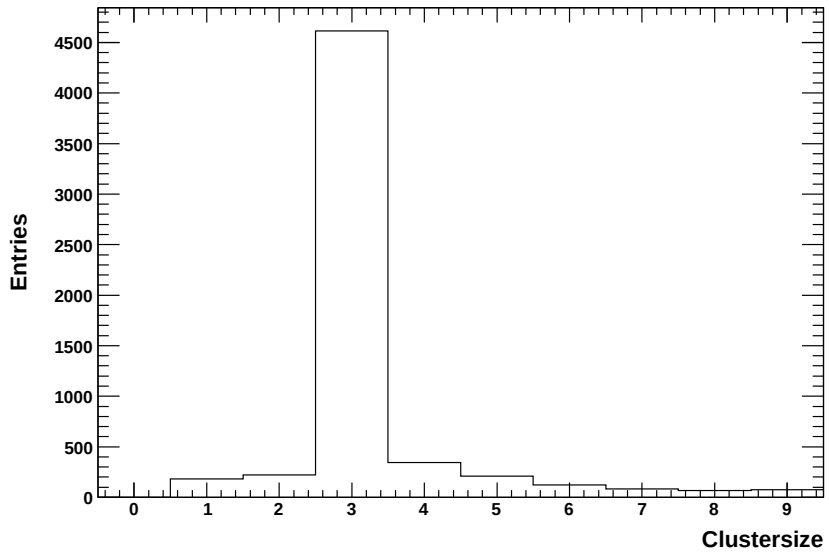


Figure 7.15: Cluster size of the hits with $TOT < 5$ clock cycles.

In this section isolated hits with a very low TOT (4 clock cycles and less) are studied. This translates into a charge below $\sim 5500\ e^-$ in the pixel cell. These hits can be read out for this measurement, because the trigger is repeated within the module to enable the readout of multiple time bins. In case of hits wich are not noise hits, this may only occur if a hit shares the energy over several pixels and only the pixel with the small fraction of energy can be read out, due to defects in the pixel matrix or the other hit pixels are blocked or masked out. A pixel may be blocked, because there is a hit registered for which the readout is ongoing. Figure 7.15 shows the cluster sizes of the events where one hit in the cluster has low TOT. As can be seen low clusters containing a low TOT hit mostly occur when charge is shared between three pixels. This is due to mounting the modules with a certain angular against the beam direction. Therefore the particles hit mostly two or three pixels, but in the third hit pixel only a small energy fraction is deposited leading to a low TOT in the readout. The fraction of single low TOT hits is rather small. Table 7.6 shows the fraction of isolated low TOT hits on the overall number of hits in the modules.

The topology of the hits is shown in the hitmap in Figure 7.16. It can be seen that there are many hits in the region around the middle axis of the module (locX = 0). This is the region of the module with ganged pixels. The ganged pixels fill the region between the chips on the module. As described in Chapter 3.1, in this region 4 electronic cells per row in the front end chips are connected to 8 sensor cells. This leads to an ambiguity in the hit information because it is not known which sensor cell was hit. As can be seen in Figure 3.8 the electronic circuits 159, 157, 155, and 153 of each row have two sensor cells connected. If now a hit crosses two of these additional and neighboured sensor cells the hit information is registered in the two connected electronic circuits. These electronic

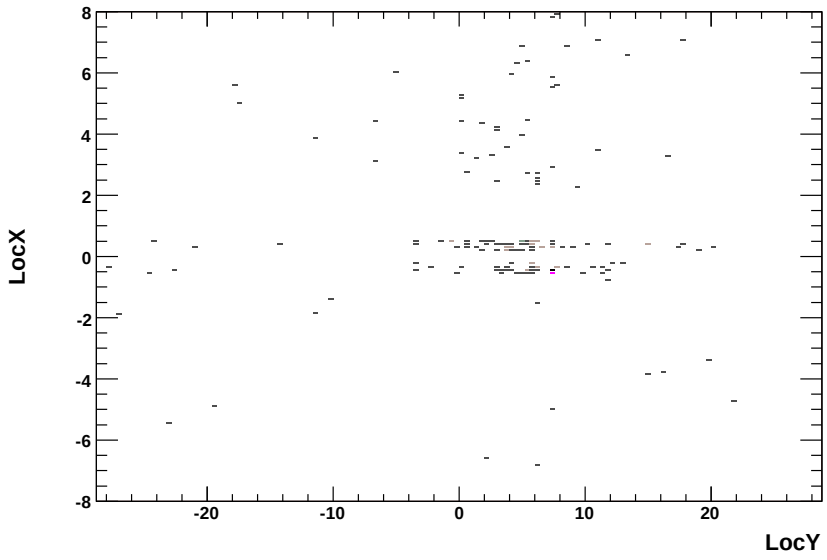


Figure 7.16: Hit map of hits with $TOT < 5$, taken with a delay setting of 22 ns. LocX and LocY are representing the module dimensions in mm.

circuits are not neighboured and therefore the hits are not combined into a cluster. The hit appears as two single hits. Due to the status of the analysis software this ambiguity is not resolved yet. Therefore, the number of isolated hits in the region of the ganged pixels is expected to be higher. This effect can be seen for the three modules which have been centred in the beam spot (Figures A.11(a), A.11(c), and A.11(e)).

The other isolated low TOT hits are spread over the module. The modules centred better in the beam have a higher fraction of single hits with low TOT due to more hits being registered in these modules and due to the different mounting angular. A concrete statement on this effect is not possible because the statistics is minimal.

Module	**Hits Total**	**Low ToT isolated Hits**	**Fraction**
0	88790	178	0.0020
1	24680	40	0.0016
2	84830	217	0.0026
3	25720	51	0.0019
4	82670	183	0.0022
5	27850	52	0.0019

Table 7.6: Isolated hits with low TOT in the complete sample of run 1241 (22 ns delay).

7.7.1 Hit Doubling

The FE-chips have a function, named hit doubling, to copy hits with a low TOT information to a bunch crossing earlier by storing the hit information twice with different timestamps. The hit is stored with the timestamp t of hit recognition and with timestamp $t-1$.

The hit doubling leads to a readout of the low TOT hits. They will not be lost for the offline analysis. They can be used for correcting the track prosition or, in case of single low TOT hits, to make a track point for the reconstruction.

On the other hand there are some disadvantages. The readout of the copied hits slightly increases the amount of transferred data. And more noise hits which normally have a low TOT are read out.

Although this feature is nearly untested it is worth to to be studied. Because the hit doubling feature of the FE-chips copying the low TOT hits to the bunch crossing earlier is needed to recognise these hits. This is the only way to register even the low TOT hits with the correct trigger and fewer hits would be lost due to small energy deposition.

There are some consequences for the offline algorithms. The clustering should take into account if the pixel that is the neighbouring of a low TOT cluster is dead or not. If it is dead the cluster position should reflect this, maybe in a correction for the dead pixel, maybe in an larger error.

It would be interesting to study things like this, even if they might be a fine tuning of the existing algorithms.

7.8 Conclusion

In the ATLAS experiment each LV1 trigger for the pixel detector forces the readout of all hits that appeared in one clock cycle (25 ns). This fits to the bunch crossing rate of 40 MHz. Ideally all hits belonging to the triggered bunch crossing should be read out. The studied behaviour of the pixel detector shows that the timing of the modules have to be optimised to read out the maximal number of hits. In order not to lose hits the phase of the module timing has to be set correctly with respect to the bunch crossing. This can be realized by shifting the delay of the clock being sent to the module through the BOC card. This clock can be delayed in steps of approximately 0.3 ns.

With the correct timing 100% of the hits with $TOT \geq 5$ clock cycles can be read out. This is not taking into account facts which influence the readout efficiency like noise, blocked pixels, dead pixels, transmission errors, and others. The hits with lower TOT values are registered a clock cycle later. The hit doubling feature of the front end chips enables a copying of low TOT hits to one clock cycle earlier. This way no hit is lost for the readout.

The case of having only a low TOT single hit in a cluster is very unlikely. It is of order 0.2%. But including the hit doubling feature these hits can be read out and are usable for the offline analysis.

All in all the performance of the detector modules in terms of timing and readout capabilities has shown to be good. The timing behaviour is as expected and the interplay between the readout electronics – BOC card and ROD – and the data taking electronics – the modules – performs fine. Finally it has been shown that the tuning of the modules in terms of thresholds, timewalk, and timing, is essential to achieve good results for the operation in the ATLAS detector.

Summary and Outlook

The LHC and its experiments will open new possibilities to study the properties of known and unknown particles in the next 10 years. The readout of the detectors is a very important task for being able to analyse the data. A careful examination of the components for the readout systems is necessary.

The control and the readout of the ATLAS pixel detector is performed through an optical transmission line. The studies on the Back of Crate card, the optical interface in the counting room, are presented in this thesis. The BOC card has been tested in various setups, starting with the production, standalone tests, introduction into system tests, and operating the card in a test beam setup.

For qualifying the BOC cards during the production, tests have been developed and realised. These tests ensure a complete functionality of the BOC card and prove its operation within given limits.

To test the interaction of the BOC card within the complete readout chain of the ATLAS pixel detector, the BOC card has been introduced into several system test setups. In these setups a study of the optical readout of the detector modules using the optical link – optoboard, BOC card, and ROD – has been performed. For this thesis the main focus in these studies has been given to the operation of the BOC card and its influence on the detector performance. It has been observed that an optimal function of the detector readout needs a tuning of the parameters of the optical link. Both the control settings on the BOC card and the settings for the optoboard must be optimised to guarantee an optimal performance of the optical readout. Two factors are critical: the light power of the optoboard and the timing of the complete chain. The light power of the optoboard must be tuned to fit the working range of the DRX. The timing is critical for registering the module data correctly. This is even more critical the higher the bandwidth and, therefore, the narrower the time window for data registering is. The system tests showed the expected behaviour of the BOC card. With the correct tuned parameters a stable readout of the pixel detector module is achieved.

A main task to be performed by the BOC card is the timing adoption of the pixel detector modules and its readout system. This capability has been studied during a combined test beam period. For this combined test beam a slice of the ATLAS detector was installed and the performance of hardware and software was studied. Through this it was possible to

test the timing for the pixel detector during a 25 ns beam period using triggers generated by the central trigger processors and distributed through the TTC chain as it will be in the ATLAS experiment. The analysis of the recorded data proved the timing capabilities of the BOC card to be as expected. An optimisation of the timing for the pixel detector modules is possible and maximises the readout efficiency for hits assigned to the triggered bunch crossing. Furthermore the timewalk and the effective threshold of the detector modules has been reproduced to be in the expected range of around $5500\ e^-$.

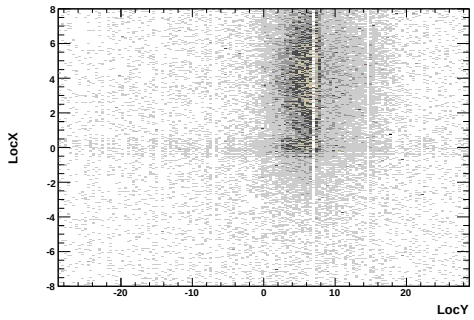
The production of the BOC cards, its testing, and optical assembly will be finished this year. In addition, the study of the BOC card, its tuning, and the long term stability is continued in Wuppertal. A tuning algorithm to optimise the BOC card parameters automatically is under investigation and testing.

Until the LHC machine will start operation in 2007 the testing and commissioning of the pixel detector and its readout will be extended and continued. At CERN a system test including 10% of the final pixel detector and the readout system is under preparation. It will test the operation of a larger system to be scaled to the final size. The test of multiple ROD/BOC card operation and furthermore multiple crate operation is the central topic concerning the readout system. The hardware installation and software adaption is under investigation.

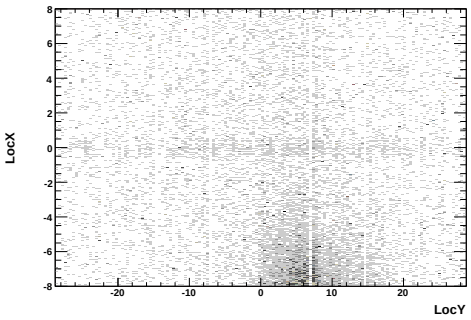
The installation of the ATLAS pixel detector and its readout into the cavern will start end of this year and has to be completed by mid of 2007 to be ready for data taking at the beginning of the LHC operation.

Appendix A

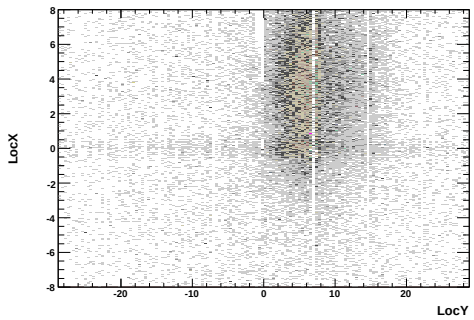
Plots for all Modules of the Combined Test Beam



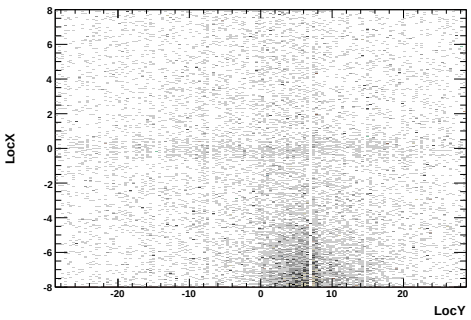
(a) Module 0: lower layer 0



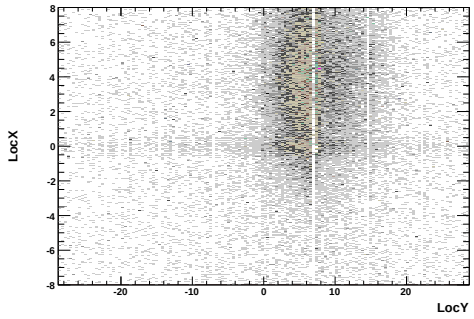
(b) Module 1: upper layer 0



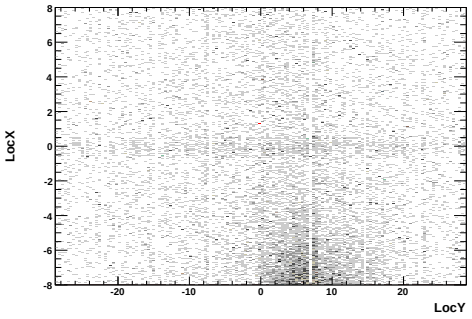
(c) Module 2: lower layer 1



(d) Module 3: upper layer 1

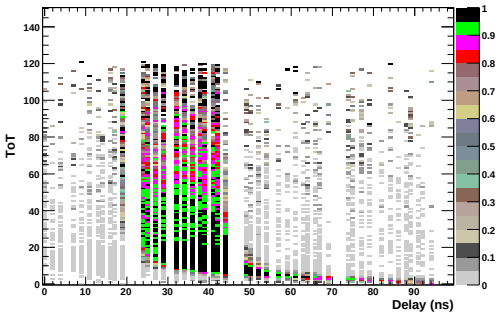


(e) Module 4: lower layer 2

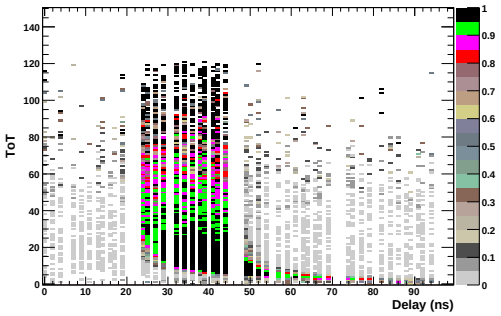


(f) Module 5: upper layer 2

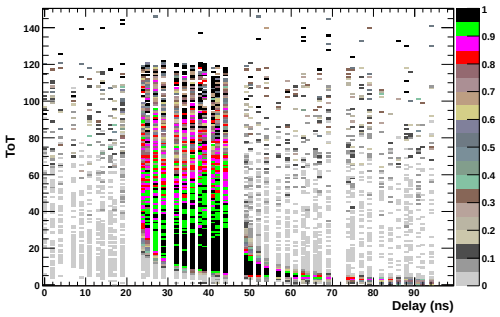
Figure A.1: Hit maps of the modules using a delay setting of 22 ns.



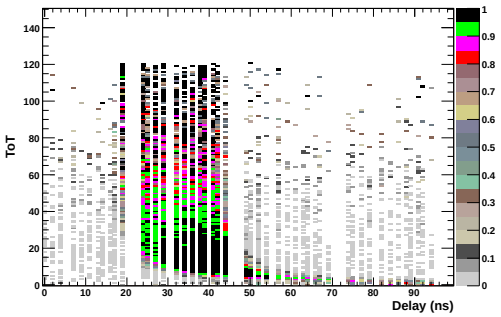
(a) Module 0: lower layer 0



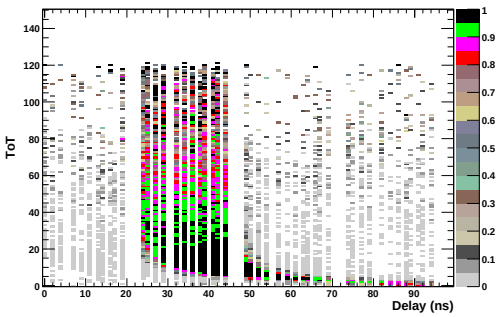
(b) Module 1: upper layer 0



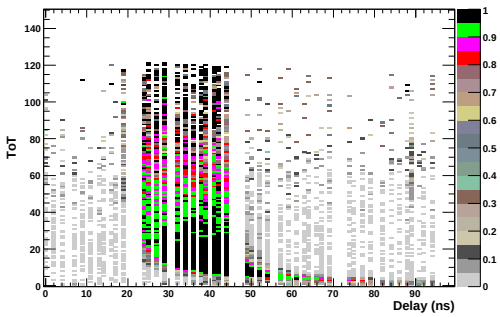
(c) Module 2: lower layer 1



(d) Module 3: upper layer 1

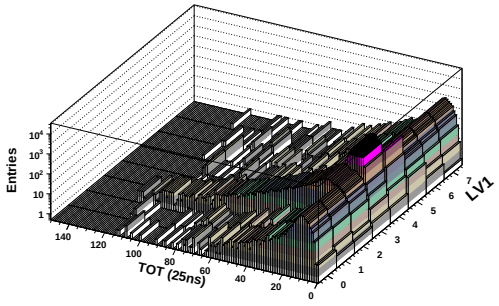


(e) Module 4: lower layer 2

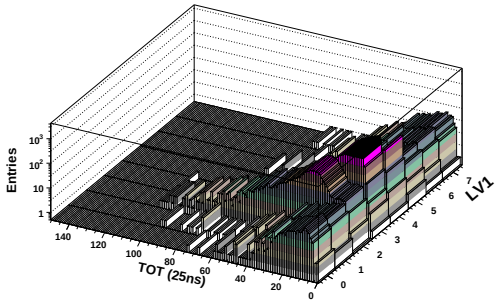


(f) Module 5: upper layer 2

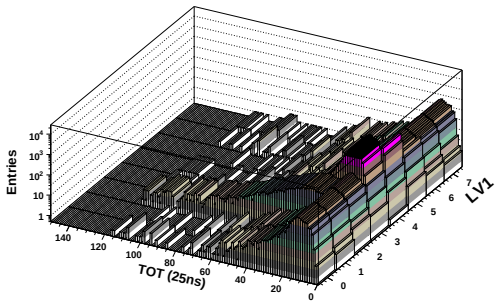
Figure A.2: Collection efficiency. The colour is representing the efficiency for the given TOT - delay setting, 2 dimensional visualisation.



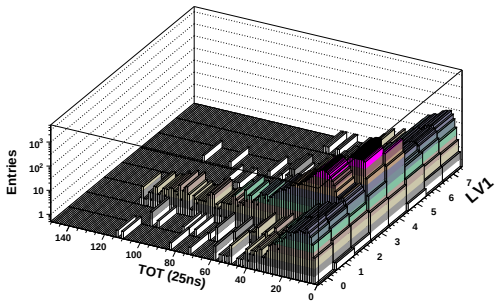
(a) Module 0: lower layer 0



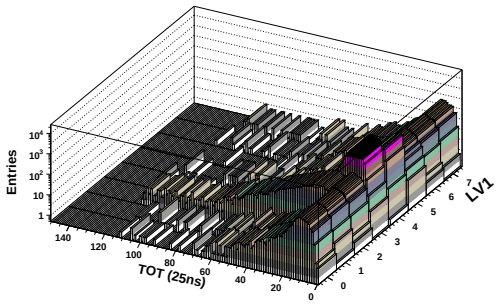
(b) Module 1: upper layer 0



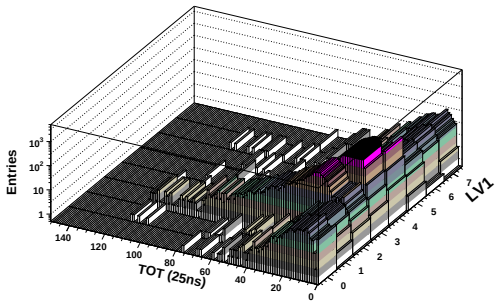
(c) Module 2: lower layer 1



(d) Module 3: upper layer 1

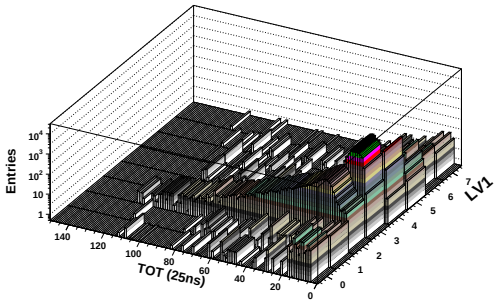


(e) Module 4: lower layer 2

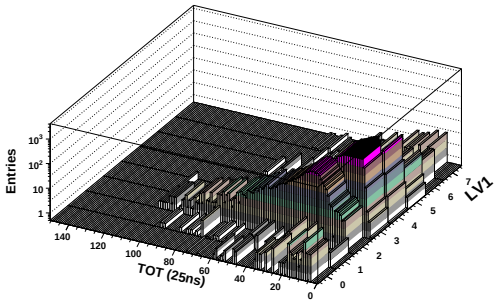


(f) Module 5: upper layer 2

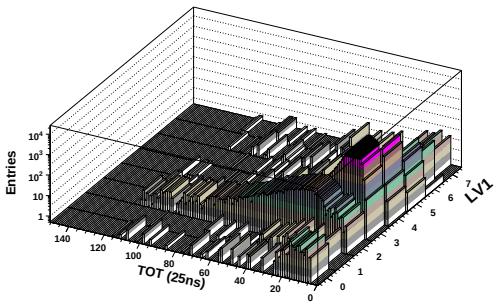
Figure A.3: Distribution of the LV1 accept against the TOT. For all LV1 accept values there are many hits with low TOT, taken as noise. Hits with high TOT are marking the region for registering the data correctly. These are LV1 accept bins 2-5. Data of the run with 19 ns.



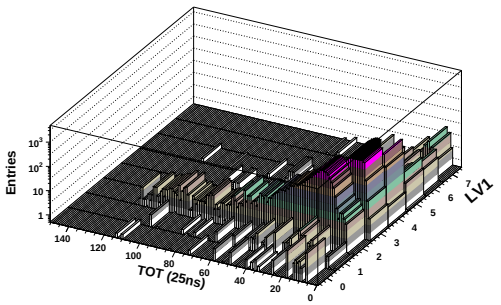
(a) Module 0: lower layer 0



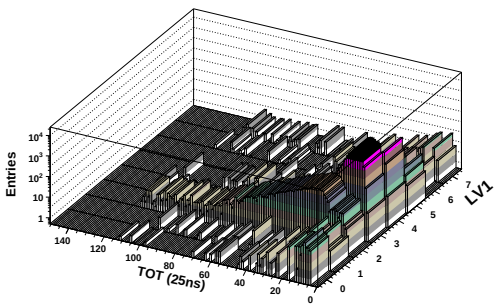
(b) Module 1: upper layer 0



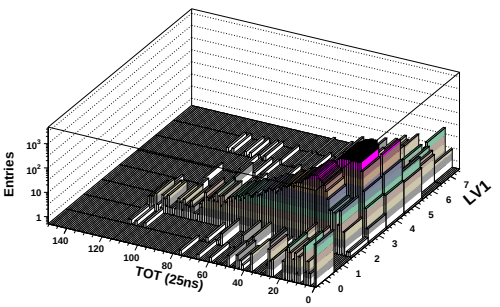
(c) Module 2: lower layer 1



(d) Module 3: upper layer 1

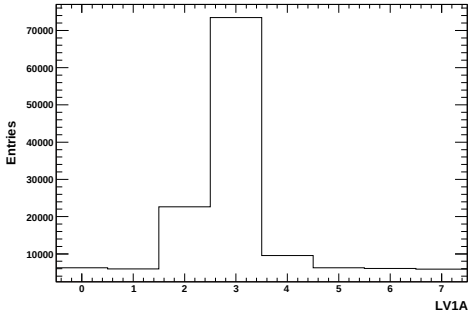


(e) Module 4: lower layer 2

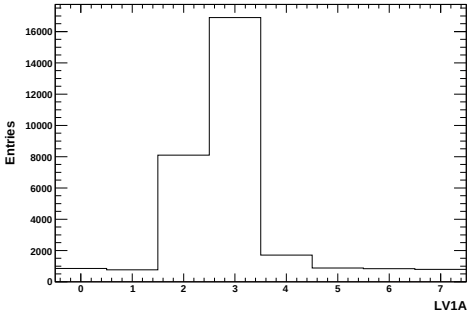


(f) Module 5: upper layer 2

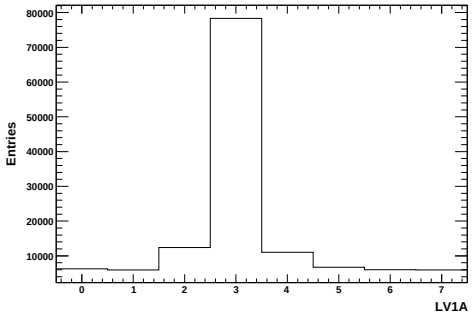
Figure A.4: The LV1 accept - TOT distribution after applying the noise correction. The data set for a delay setting of 19 ns is shown.



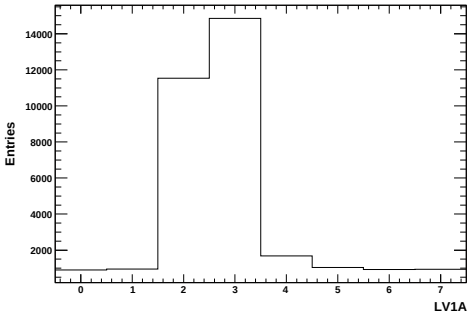
(a) Module 0: lower layer 0



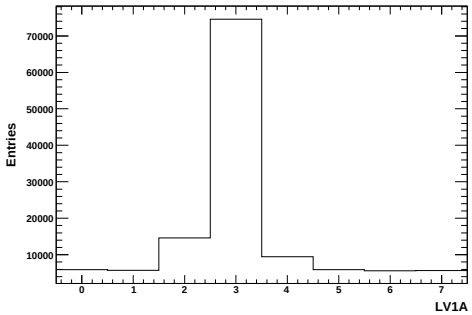
(b) Module 1: upper layer 0



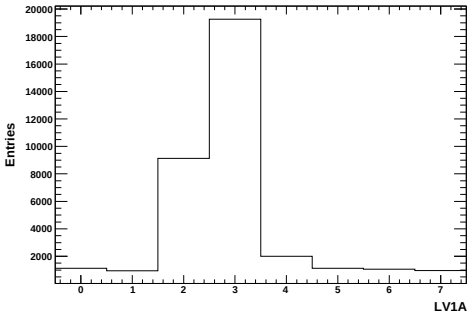
(c) Module 2: lower layer 1



(d) Module 3: upper layer 1

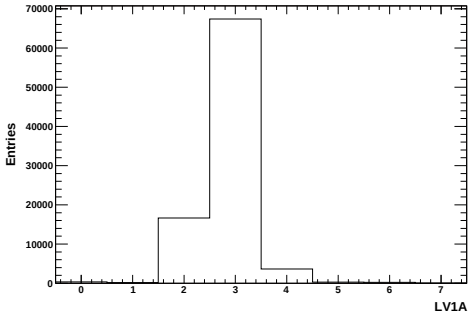


(e) Module 4: lower layer 2

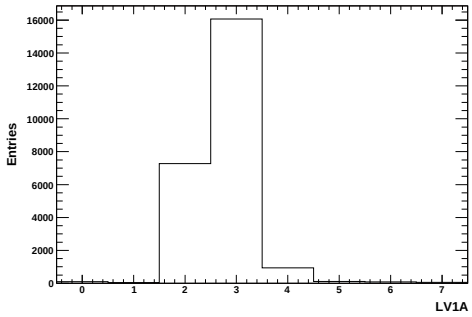


(f) Module 5: upper layer 2

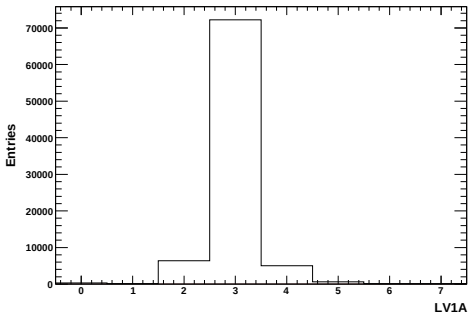
Figure A.5: Distribution of the LV1 accepts. The noise level is visible. The correct data region is for LV1 accept bins 2-5. The data is taken with a delay of 19 ns.



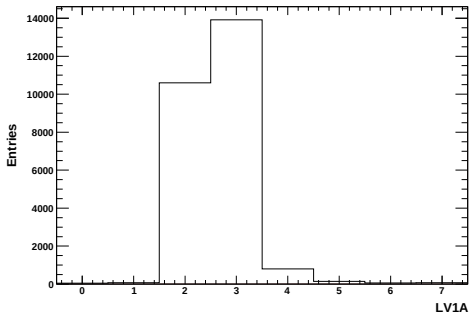
(a) Module 0: lower layer 0



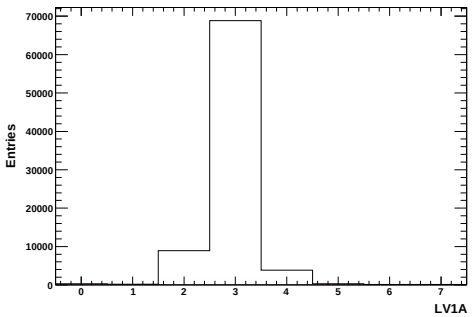
(b) Module 1: upper layer 0



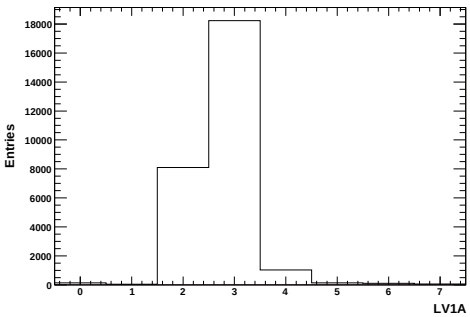
(c) Module 2: lower layer 1



(d) Module 3: upper layer 1

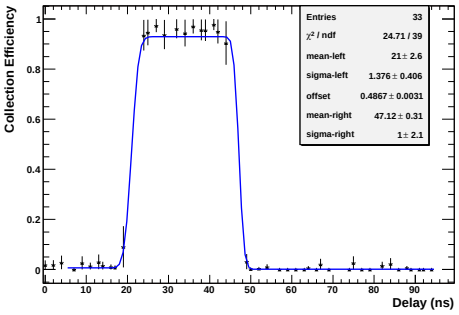


(e) Module 4: lower layer 2

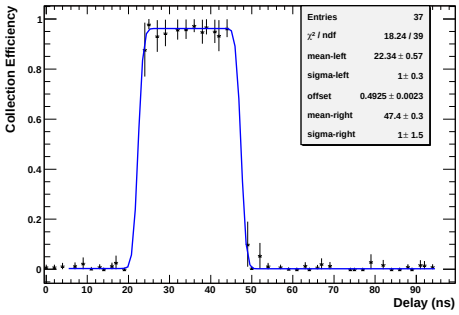


(f) Module 5: upper layer 2

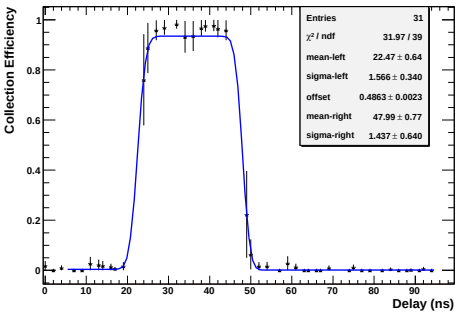
Figure A.6: Noise corrected LV1 accept distribution.



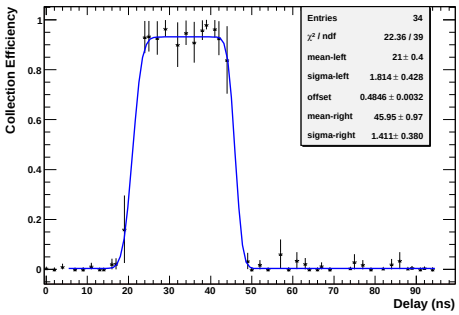
(a) Module 0: lower layer 0



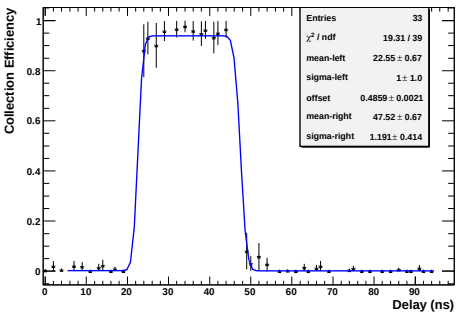
(b) Module 1: upper layer 0



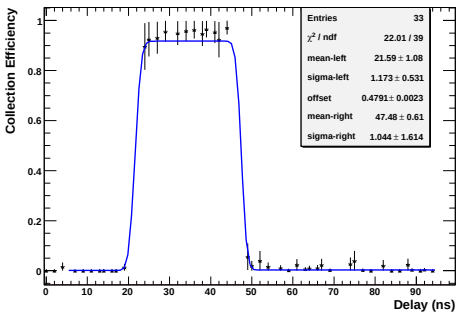
(c) Module 2: lower layer 1



(d) Module 3: upper layer 1

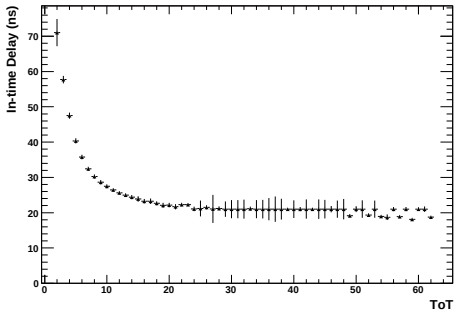


(e) Module 4: lower layer 2



(f) Module 5: upper layer 2

Figure A.7: Collection efficiency versus the delay for a hits with TOT=30.



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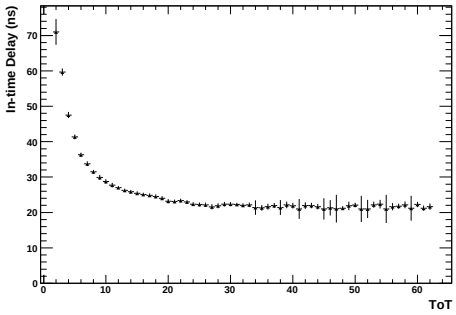
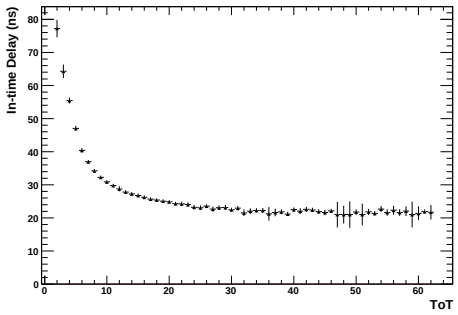
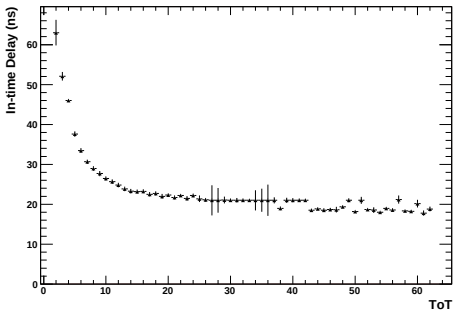


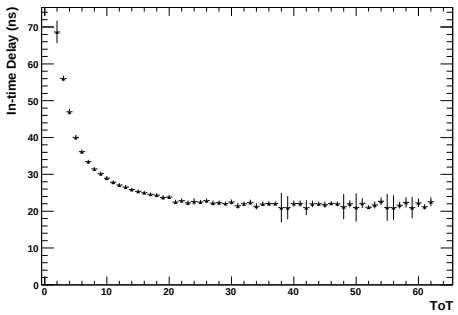
(b) Module 1: upper layer 0



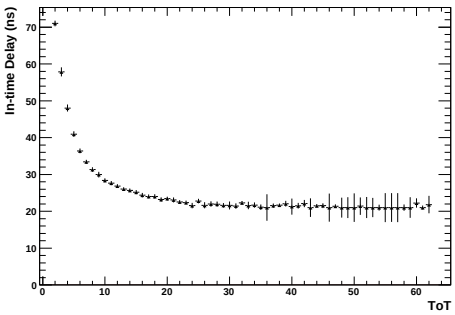
(c) Module 2: lower layer 1



(d) Module 3: upper layer 1

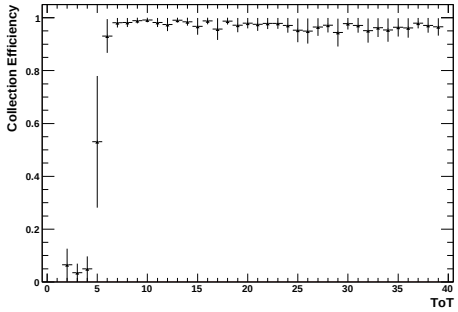


(e) Module 4: lower layer 2



(f) Module 5: upper layer 2

Figure A.8: Delay setting for in-time registering versus the TOT.



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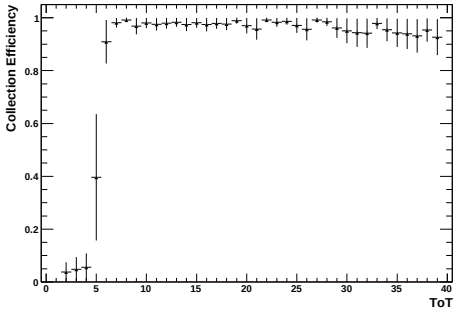

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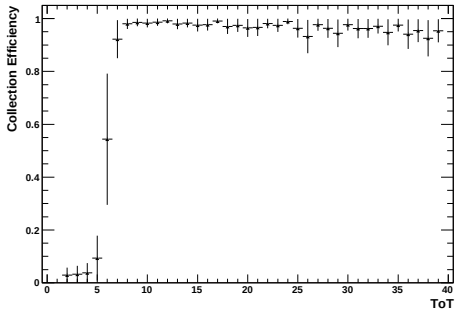

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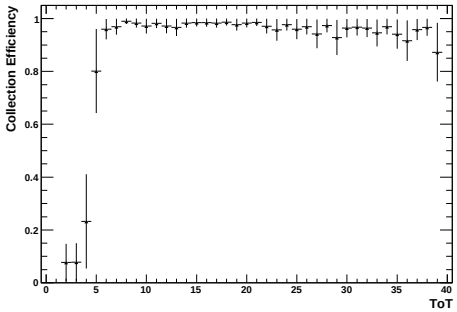

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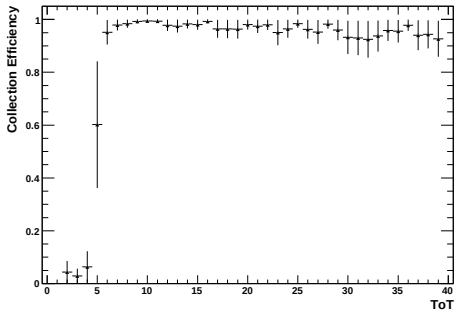

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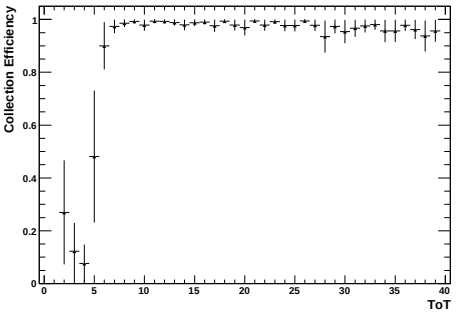
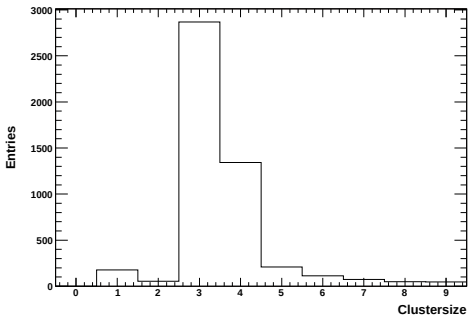


(f) Module 5: upper layer 2

Figure A.9: Collection efficiency as a function of the TOT for the optimised delay setting of 22 ns.



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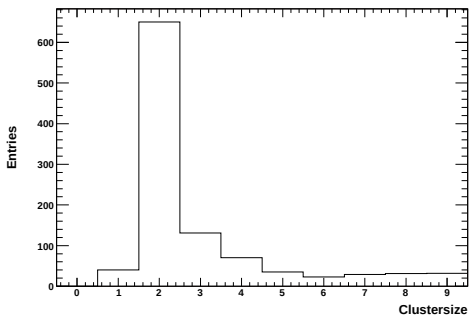

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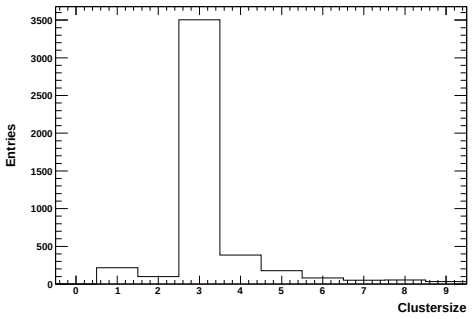

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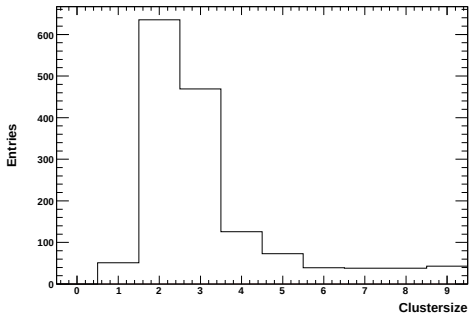

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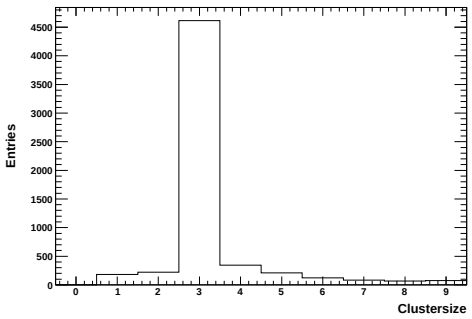

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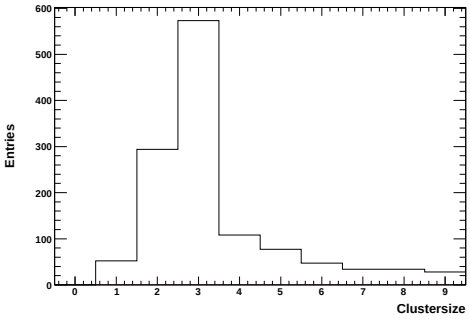
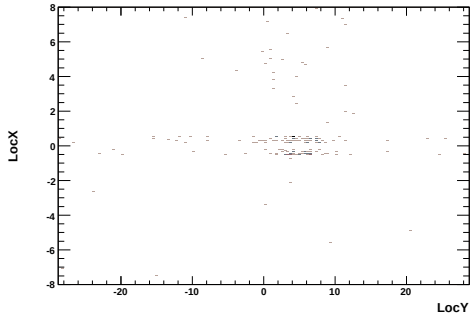


(f) Module 5: upper layer 2

Figure A.10: Clustersize of the hits with $TOT < 5$ clock cycles.



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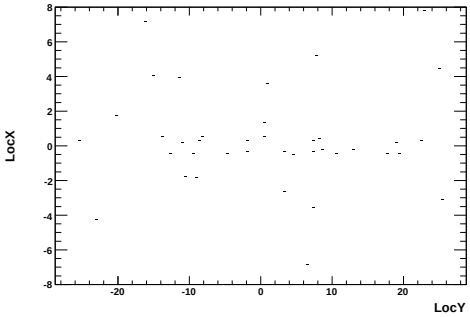

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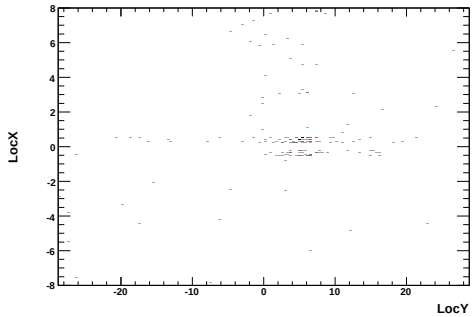

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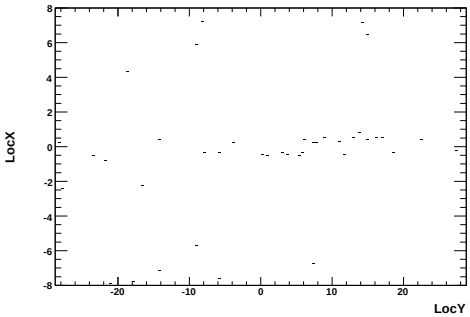

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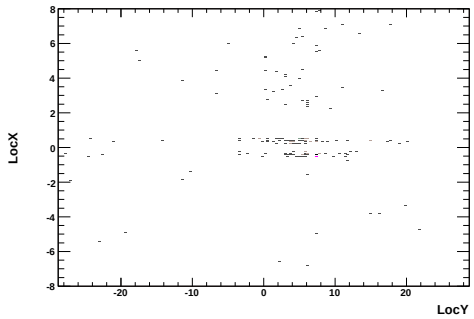

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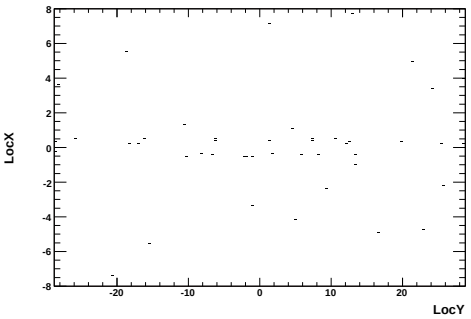

(f) Module 5: upper layer 2

Figure A.11: Hit map of hits with $TOT < 5$, taken with a delay setting of 22 ns.

Acknowledgements

Many people contributed to this thesis and I want to express my gratitude to all of them. I can only mention some of them explicitly here, but my acknowledgement includes all those, who are not mentioned here explicitly.

First I want to thank my 'Doktorvater' Prof. Dr. P. Mättig who made this research project possible and carried it with his support.
Dr. P. Gerlach and Dr. K. Reeves I want to thank for supporting my work with their ideas and the useful discussions of my ideas.
I am indebted to Dr. G. Gorfine, I had a large benefit from his knowledge concerning the data handling and analysis for the combined test beam study.

To all the other colleagues at the high energy physics group in Wuppertal I want to express my gratitude for the very good work atmosphere, their support and the fruitful discussions amongst us.

The support of the ATLAS pixel group was a useful part of our investigations. Especially the support during the combined test beam, namely by Dr. G. Gagliardi, was very useful to be able to record the data which was needed for the timing study. I hope that I contributed positively to the pixel project during this past time, as well.

A special thank is for all who read this thesis in advance to help me to set up the wording correctly.

And I would like to thank my family for their support and their willingness to accept my staying at CERN even for longer periods. Their backing has always given me strength.

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Glossary

A

ASIC Application Specific Integrated Circuit, p. 31.

B

BOC Back of Crate Card, p. 57.

BPM Bi Phase Mark encoded signal or the chip to encode the signals, p. 50.

C

CERN European Centre for Nuclear Research. The French name gave the abbreviation: Conseil Européen pour la Recherche Nucléaire, p. 18.

CPLD Complex Programable Logic Device, p. 60.

CSC Cathode Strip Chambers. Detector type used in the muon spectrometer of the ATLAS Experiment., p. 21.

CTP Central Trigger Processor of the ATLAS experiment., p. 27.

D

DAC Digital Analog Converter, p. 41.

DCS Detector Control System. System for controlling and monitoring the temperatures, voltages and currents of detector components, p. 82.

DDC DAQ to DCS Communication, p. 83.

E

EF Event Filter of the trigger in the ATLAS experiment., p. 28.

F

FE Front End chips of the ATLAS pixel detector module., p. 31.

G

GDAC Global DAC to control the threshold inside an ATLAS pixel module., p. 41.

H

HLT High Level Trigger. Second and third trigger stage of the ATLAS experiment., p. 26.

HOLA High Speed Optical Link for ATLAS, p. 69.

L

LEP Large Electron Positron Collider, operated between 1988 and 2000 at CERN, p. 18.

LHC Large Hadron Collider, Collider Ring at CERN for accelerating protons or heavy ions., p. 13.

M

MC Monte Carlo simulation, p. 113.

MCC Module Controller Chip, part of the ATLAS pixel module., p. 46.

MDT Monitored Drift Tubes. Detector type used in the muon spectrometer of the ATLAS Experiment., p. 21.

MIP Minimal Ionising Particle, p. 34.

N

NTC Negative Temperature Coefficient. A resistor with a negative temperature coefficient., p. 69.

O

optoboard The optoelectrical interface on the on-detector side, p. 50.

P

PP0 Patch Panel 0, connection place nearest to the pixel detector. Location of the optoboards., p. 50.

PP1 Patch Panel 1, p. 53.

PP2 Patch Panel 2, p. 83.

PRBS Pseudo Random Bit Sequence, p. 100.

PS Proton Synchrotron at CERN, p. 18.

Q

QCD Quantum Chromo Dynamics, p. 8.

QED Quantum Electro Dynamics, p. 6.

R

ROB Read out Buffer, storage system for the data taken in the physics runs of ATLAS, p. 50.

ROD Read out Driver, p. 54.

RoI Region of Interest, p. 27.

RoIB Region of Interest Builder. Part of the LVL2 trigger of the ATLAS experiment., p. 27.

RPC Resistive Plate Chambers. Detector type used in the muon spectrometer of the ATLAS Experiment., p. 21.

S

SCT Silicon Tracker, Tracking subdetector in the ATLAS experiment, p. 25.

SPS Super Proton Synchrotron at CERN, p. 18.

SUSY SUper SYmmetry, p. 20.

T

TDAC Trimming DAC, to tune the threshold dispersion of a ATLAS pixel detector module., p. 41.

TGC Thin Gap Chambers. Detector type used in the muon spectrometer of the ATLAS Experiment., p. 21.

TIM TTC Interface Module, p. 50.

TOT Time Over Threshold. A measure for the energy a hit deposited in the sensor of a ATLAS pixel detector module., p. 41.

TRT Transition Radiation Tracker in the ATLAS experiment, p. 24.

TTC Timing Trigger and Control signal coming from the LHC machine., p. 27.

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Erklärung

Hiermit versichere ich, dass ich diese Arbeit selbstständig verfasst
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sowie Zitate kenntlich gemacht habe.