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Development of the MCM–D Technique for Pixel Detector Modules

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for Ariane
you are my light

Contents

Übersicht

Diese Dissertation behandelt eine Kupfer–Polymer basierte Dünnfilmtechnologie, die MCM–D Technik, und Ihre Anwendung zum Aufbau von hybriden Pixeldetektor Modulen. Die Anforderungen an ein solches System für den Einsatz in zukünftigen Hadronkolliderexperimenten, wie das ATLAS Experiment sind hoch.

Das ATLAS Experiment am LHC wird über ein Pixeldetektorsystem verfügen. Die kleinste mechanische Einheit des Pixeldetektors sind Multichipmodule. Die wichtigsten Komponenten dieser Module sind 16 Elektronikchips, ein Kontrollchip und ein grosser Sensor, der über mehr als 46 000 Pixelzellen verfügt. MCM–D ist eine überlegene Technologie um das notwendigen Signalbussystem und das Stromversorgungssystem direkt auf den Sensor aufzubauen.

In Zusammenarbeit mit dem Fraunhofer Institut für Zuverlässigkeit und Mikrointegration, IZM, wurde der Dünnfilmprozess überprüft und weiterentwickelt. Das Vielschichtsystem wurde entworfen und sowohl für das Verbindungssystem als auch für die mehr als 46 000 Pixelkontakte optimiert. Prototypaufbauten wie Einzelchiphybride und vollständige Module wurden gebaut und getestet. Labormessungen haben gezeigt, dass ein komplexes Verbindungsschema für geometrieoptimierte Einzelchips durchführbar ist und vernachlässigbaren Einfluss auf die Leistungsfähigkeit der Auslesechips hat. Ein vollständiges Modul wurde gebaut; und so konnte nachgewiesen werden, dass sich die Technologie eignet um Pixeldetektormodule zu bauen. Weitere Tests beinhalten u.a. die Untersuchung des Einflusses von hadronischer Bestrahlung auf die Dünnfilmlagen. Einzelchipaufbauten wurden auch in einer Teststrahlumgebung betrieben und die Umsetzbarkeit der Sensoroptimierung konnte gezeigt werden. Es wird ein Überblick über das Potential und die Perspektive der MCM–D Technologie in zukünftigen Experimenten gegeben.

Abstract

This thesis treats a copper–polymer based thin film technology, the MCM–D technique and its application when building hybrid pixel detector modules. The demands on such a system for the usage in upcoming hadron collider experiments, such as the ATLAS experiment, are high.

The ATLAS experiment at the LHC will be equipped with a pixel detector system. The basic mechanical units of the pixel detector are multi chip modules. The main components of these modules are: 16 electronic chips, a controller chip and a large sensor tile, featuring more than 46 000 sensor cells. MCM–D is a superior technique to build the necessary signal bus system and the power distribution system directly on the active sensor tile.

In collaboration with the Fraunhofer Institute for Reliability and Microintegration, IZM, the thin film process is reviewed and enhanced. The multi layer system was designed and optimized for the interconnection system as well as for the 46 000 pixel contacts. Prototype assemblies like single chips and full size modules have been built and tested. Laboratory measurements prove that complex routing schemes for geometrically optimized single chips are suitable and have negligible influence on the front–end chips performance. A full scale MCM–D module has been built and it is shown that the technology is suitable to build pixel detector modules. Further tests include the investigation of the impact of hadronic irradiation on the thin film layers. Single chip assemblies have been operated in a test beam environment and the feasibility of the optimization of the sensors could be shown. A review on the potential as well as the perspective for the MCM–D technique in future experiments is given.

Chapter 1

Introduction

Particle physics studies and describes the forces of nature and the constituents of matter. Large accelerators like the Lʜᴄ[1] at the European Organization for Nuclear Research, Cᴇʀɴ[2], allows particle physics to create energy densities, that existed a few instants after the Big Bang. The observation of particles that are created during the collisions and the determination of their properties is a technological and intellectual challenge.

The Aᴛʟᴀs[3] experiment is one out of four experiments at the Lʜᴄ and will begin to operate in 2007. Like most modern detector concepts in high energy physics, the Aᴛʟᴀs detector comprises of several subsystems. The smallest and innermost detector system of Aᴛʟᴀs is also one of the most technologically advanced systems: the Pixel detector. The Pixel detector is one of the three tracking devices and provides at least three measured space points for particle track reconstruction. The precise determination of the primary collision points and of secondary vertices are the major tasks of the detector. For that purpose the Pixel detector will be built out of 1744 individual modules, which are the basic mechanical unit. A module features a large segmented silicon sensor tile with over 46 000 sensor cells, which are read out by 16 radiation hard electronic chips and an additional controller chip. These multi chip modules also require a highly integrated interconnection system. This interconnection system has to supply both, the readout chips and the controller chip with power. Furthermore, it provides a data bus system for the intramodular signals and the module's communication to the outer world.

The *Multi Chip Module Deposited* technique, MCM–D, is studied in this thesis in order to build a multi chip system like the modules for the Aᴛʟᴀs pixel detector. The level of integration poses a challenge. The MCM–D technique uses a copper–benzocyclobutene deposition process that builds the interconnection system directly on the 250 µm thin silicon sensor. Solder bump bonding is used as the only contact technology to join the 17 electronic chips and the sensor. It is the goal to manufacture a robust, manageable module with a high performance signal bus system. The 46 000 individual sensor cells have to be contacted through the thin film system. However this offers the opportunity to adapt geometries of the individual parts. This allows the optimization of the sensor geometry

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[1] Lʜᴄ: **L**arge **H**adron **C**ollider
[2] Cᴇʀɴ: **C**onseil **E**uropeénne Pour la **R**echerche **N**ucleaire
[3] Aᴛʟᴀs: **A** **T**oroidal LHC **A**pparatus

to enhance the resolution. It will be critically examined whether the performance of the electronics chips is not harmed by this kind of routing.

The MCM–D technique utilizes technologies of the semiconductor industry. Particularly in the area of high density interconnect (HDI) and wafer level packaging, the application of thin dielectric films and conductive layers with thicknesses of the order of µm become more common. These kind of interconnection systems are mostly used in a one or two layer scheme. For the Atlas pixel detector multi chip modules an advanced system of four electroplated copper layers and five dielectric layers of spin–on BCB is required in order to build the necessary interconnections. This exceeds available industrial processes by far. A small series production of MCM–D modules is anticipated to establish a reliable set of process parameters and to spot critical issues during the manufacturing.

Chapter 2

The ATLAS Experiment at the LHC

Over the last decades the Standard Model of High Energy Physics has been tested by numerous extraordinarily precise measurements and has proven to be the most valuable theory that particle physics has developed so far. Successful prediction of particles like the ν_τ–lepton, the most recently discovered fundamental fermion, has also been a strength of the model. Despite its successes there are still open questions concerning the origin of mass and the discrepancy between matter and antimatter. Resolving these questions and opening the future for physics beyond the Standard Model is the main goal of the next generation of colliders and detectors, like LHC and ATLAS.

This chapter will shortly cover the basics of the Standard Model and summarize the physics goals of ATLAS. A description of the overall design of the detector will be given, whereas the concept and layout of the innermost part of the detector, the Pixel Detector, will be covered in the next chapter.

2.1 The Standard Model of High Energy Physics

The Standard Model of particle physics describes the fundamental structure of matter and its interactions. It is based on gauge theories. According to the model our universe is built out of fermionic (spin = $\frac{1}{2}$) particles, quarks and leptons. Bosonic (spin = 1) mediator particles, like the photon, carry the four fundamental forces. In Table 2.1 an overview of the fundamental fermions and some of their properties is given.

The four fundamental forces are:

- **The strong force**, which is the force between quarks. Leptons do not interact via the strong force. The mediators of the strong force are the gluons, g. Three colors, red R, green G, and blue B, were introduced as the charge of the strong force. Any particle built of quarks, baryons and mesons, has to be free of color. That is accomplished by the principle that in baryons only combinations of three quarks with different color RGB (or the anticolors $\bar{R}\bar{G}\bar{B}$) are allowed, while mesons are combined of two quarks with color and anticolor ($R\bar{R}$, $G\bar{G}$ or $B\bar{B}$). The coupling constant of the strong force is $\alpha_s \simeq 0.1\ldots1$ and its range is $\leq 10^{-15}$m.

Family	Leptons			Quarks		
	Flavor	Charge [e]	Mass [MeV]	Flavor	Charge [e]	Mass [MeV]
1st	ν_e	0	$< 3 \cdot 10^{-6}$	u	2/3	$1.5 \ldots 4.0$
	e	$-$ 1	$0.510998918 \pm 4.4 \cdot 10^{-8}$	d	$-$ 1/3	$4 \ldots 8$
2nd	ν_μ	0	< 0.19	c	2/3	$(1.15 \ldots 1.35) \cdot 10^3$
	μ	$-$ 1	$105.6583692 \pm 9.4 \cdot 10^{-6}$	s	$-$ 1/3	$80 \ldots 130$
3rd	ν_τ	0	< 18.2	t	2/3	$(174.3 \pm 5.1) \cdot 10^3$
	τ	$-$ 1	$1776.99^{+0.29}_{-0.26}$	b	$-$ 1/3	$(4.1 \ldots 4.9) \cdot 10^3$

Table 2.1: The elementary fermions, charge and mass from [1].

Measurements of deep inelastic scattering of electrons and protons show that this picture has to be corrected. The proton consists of three *valence quarks*, accompanied by many quark–antiquark pairs, the *sea quarks*.

This part of the Standard Model is known as Quantum Chromodynamics, QCD.

- **The Electromagnetic force** is the force between electrically charged particles. The stability of the nucleus, crystalline structures, chemical processes and generally most of the phenomena we are faced with, are driven by the Electromagnetic force. Its mediator boson is the photon, γ. The coupling constant of the electromagnetic force $\alpha_{em} = e^2/4\pi\hbar c \approx \frac{1}{137}$. Unlike the gluon that carries color, a photon does not carry electric charge and is therefore not able to interact with itself. The photon is massless and thus the range of the electromagnetic force is infinite.

- **The Weak force** is the force in the beta decay of nuclei. All particles interact with the weak force. Neutrinos, for example, only interact via the weak force, as they are uncharged leptons. In contrast to the other forces the mediator bosons of the weak force have masses, the $W^{\pm}$ with $m_{W\pm} = 80.425 \pm 0.038$ GeV and the Z^0 with $m_{Z^0} = 91.1876 \pm 0.0021$ GeV. The range of the weak force is of the order of 10^{-18} m and its coupling constant $\alpha_W \cong 10^{-5}$.

Combining the electromagnetic and the weak force in the electroweak theory was honored with a nobel prize in physics for Glashow, Salam and Weinberg in 1979.

- **Gravity**. Although gravity determines the course of planets; its influence in elementary particle physics is negligible, due to its coupling being proportional to the squared mass thus leading to a coupling of the order of 10^{-40} for protons. The so far unobserved boson of gravity is called the graviton. The range of gravity is endless. The reason why gravity is of such importance to our life is that there are no negative masses. Unlike the electric charge, being cancelled in a neutral atom, the potential effecting one proton is equal to the sum of all potentials of all particles. The general theory of relativity describes gravity and thus the physics at astronomic scales.

2.2 LHC – Physics at the TeV Scale

Starting in 2007 the LHC will accelerate protons up to the energy of 7 TeV. At four points of the underground collider ring, two beams of protons will be focused and proton–proton collisions will take place at a center-of-mass energy of 14 TeV. LHC will be the last part of a chain of accelerators. Starting with linear acceleration to 50 MeV, the PS Booster followed by two synchrotrons, the PS and the SPS[1], accelerate the protons for injection into the LHC to energies of 450 GeV. Liquid Helium cooled superconducting dipole magnets will force the protons on the circular path of about 26.7 km length, n.b. this will be the world's largest cryogenic system. The protons will be organized in packets, called bunches.

The rate of interactions R for a given process of cross section σ is given by:

$$R = \sigma \times \mathcal{L}$$

where $\mathcal{L}$ is the luminosity, the main parameter of colliders. $\mathcal{L}$ is proportional to the circulation frequency, the number of bunches, the number of particles inside both colliding bunches and reciprocal to the cross sectional area of the bunches.

The phase of low luminosity ($\mathcal{L}_{low} = 1 \times 10^{33}$ cm^{-2}s^{-1}) is scheduled for the first three years of operation. Increasing the luminosity to $\mathcal{L}_{high} = 1 \times 10^{34}$ cm^{-2}s^{-1} by increasing the number of protons per bunch will yield a rate of proton–proton collisions of $R_{pp} = \sigma_{pp} \times \mathcal{L}_{high} \simeq 70$ mb $\times 10^{34}$ cm^{-2}s^{-1} = 7×10^{8}s^{-1}.

2.2.1 The Higgs Search

The search for the Higgs boson is the most prominent part of the physics program at the LHC.

The Higgs boson is the only particle of the Standard Modell, which has not been observed so far. The Higgs mechanism was named after its inventor P. Higgs [2] and explains the masses of the gauge bosons W$^{\pm}$ and Z^{0} by the existence of a scalar field called the Higgs–field. The mass of the Higgs boson is not predicted by theory, but ATLAS offers a wide range of possible search channels. Figure 2.1 shows the discovery potential of ATLAS over a wide possible Higgs mass range from 80 GeV to 1 TeV in units of standard deviations, corresponding to the significance of the signal after an integrated luminosity of 30 fb^{-1}.

Data from the LEP[2] experiments indicate a light Higgs and have established a lower bound for the Standard Modell Higgs boson mass of 114.4 GeV at the 95% confidence level [4]. A theoretical upper limit of 1 TeV can also be set.

2.2.2 B–Physics and CP Violation

The production rate of B–hadrons at the LHC is very high, even in the low luminosity phase. The rate of b–quarks is of the order of 0.01 Hz. It is expected to collect about 2.3×10^{10}

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[1] PS/SPS: The **P**roton **S**ynchrotron and the **S**uper **P**roton **S**ynchrotron at CERN
[2] LEP: the **L**arge **E**lectron-**P**ositron storage ring at CERN
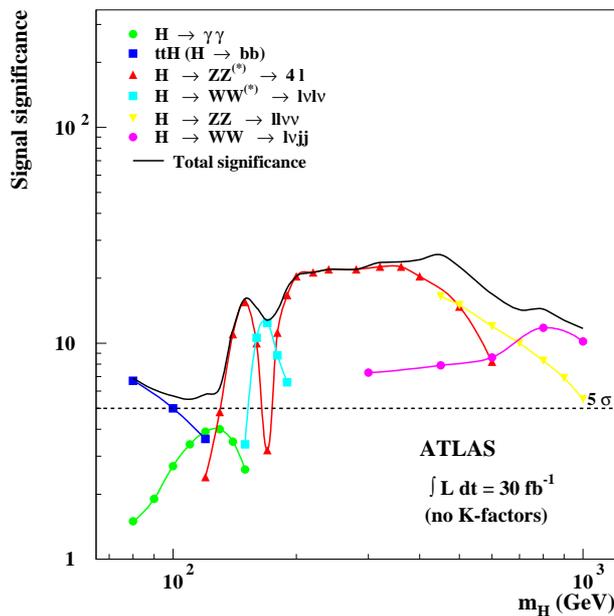
Figure 2.1: Dicovery potential of the Higgs boson at the LHC after $30\,\text{fb}^{-1}$ [3].

b–quark events in the first year of operation, which is higher than in any actually operating accelerator.

This high event rate allows a wide range of studies in the b–physics field. Major focus lies in the overestimation of the unitarity triangle. In the Standard Modell the CP violation in weak decays is introduced by the phase of the CKM[3] quark mixing matrix. The unitarity of the matrix can be used to determine triangle relations between the matrix elements.

As an example, one can measure the time–dependant CP violating asymmetry in the $B_d^0 \rightarrow J/\Psi K_s^0$ decay, which is given by:

$$A(t) = \sin 2\beta \sin(\Delta m_d t)$$

Where the angle β is an angle of the unitarity triangle and Δm_d is the mass difference in the B_d^0–$\overline{B_d^0}$ system. It is an important part of the B–physics program to test the Standard Modell and possibly give evidence for new physics beyond the Standard Modell.

2.2.3   Searches in Supersymmetry

Supersymmetry, SUSY, is an extension of the Standard Modell and introduces super-symmetric partners to all particles. The transformation between these particles includes changing the spin of the particle by $\pm\frac{1}{2}$, thus a fermion has a bosonic supersymmetric partner, while a boson has a fermion as a partner.

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[3] CKM: **C**abibbo **K**obayashi **M**askawa

One of the properties of supersymmetry is that it includes the unification of the coupling constants of the gauge interactions at high energy. This is part of the Grand Unified Theories (GUT). Supersymmetry predicts the existence of a stable neutral Weakly Interacting Massive Particle, referred to as WIMP. WIMPs can possibly explain the dark matter in the universe. WIMPs would manifest themselves as a signal of missing energy in the ATLAS experiment. Details on the physics program of ATLAS can be found in [5].

2.3 The ATLAS Detector

ATLAS will be a general purpose 4π proton-proton collision detector, designed to exploit the full discovery potential of LHC [6]. Figure 2.2 shows a schematic overview of the subsystems.
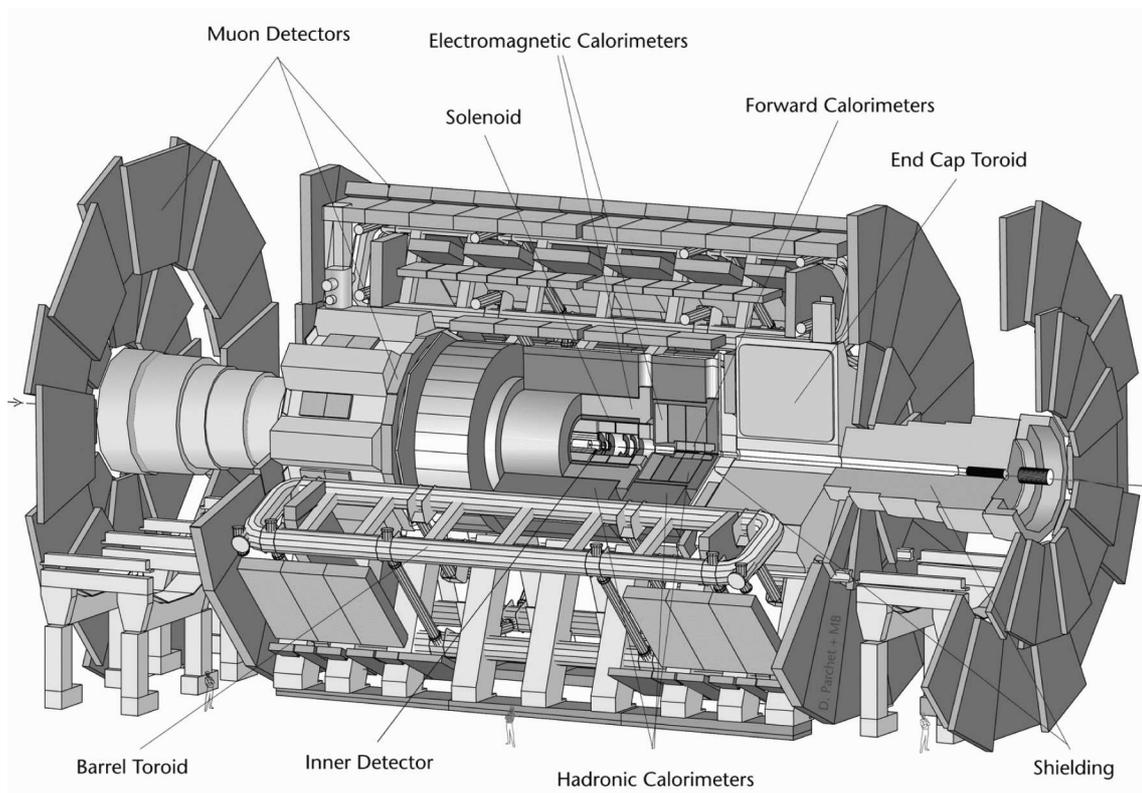
Figure 2.2: Schematic view of the ATLAS–Experiment.

2.3.1 Muon Spectrometer

The Muon spectrometer of ATLAS is the outermost part of the detector system and occupies the largest fraction of the volume of ATLAS ($\sim 16\,000$ m^3). It serves mainly for the precise momentum measurement of heavy charged leptons with high p_T and is furthermore an important part of the ATLAS Level–1 trigger system. The system can therefore be divided

into one part of slow, but precise detectors for track reconstruction and a second part with fast, but less precise detectors. The latter will allow the identification of processes with a high p_T–lepton in the final state within the correct 25 ns window of the LHC bunch crossing clock cycle [7].

For the determination of the momentum, a magnetic field of 0.5 to 2.0 T is provided by eight superconducting coils in the barrel region of the system ($|\eta| < 1$). The End Cap Toroids generate the magnetic field in the region of $1.4 < |\eta| < 2.7$ and the intermediate pseudorapidity range is covered by a superposition of both toroid's fields.

Three barrel layers and four disks of Monitor Drift Tube Chambers (MDT) comprise the main part of the muon spectrometer's volume dedicated to momentum measurement. This is completed by Cathode Strip Chambers in the very forward region where highest particle fluxes result in stronger requirements in terms of radiation hardness. The MDTs feature a total of $\sim 370\,000$ individual tubes with an average single tube resolution of $80\,\mu m$. Simulation predicts a momentum resolution of the muon spectrometer of $\sim 10\,\%$ at $p_T = 1\,\mathrm{TeV}$ and $\sim 2\,\%$ at $p_T = 100\,\mathrm{GeV}$.

The fast detectors are built of Resistive Plate Chambers in the barrel region and Thin Gap Chambers for the end–caps. The acceptance region of the Trigger part is $|\eta| \leq 2.4$. The signals are generated with a time resolution of a few nanoseconds and are then directly used for the hardware trigger generating system of the ATLAS readout system. The requirements in terms of spatial resolution are rather low. A resolution of 5-20 mm is sufficient for this part. An efficiency of $> 90\,\%$ is required for the acceptance of muons with a p_T–threshold in the range of 6-35 GeV. The rate of fake triggers due to cosmic rays or hadronic shower leakage must be kept low.

2.3.2   Calorimeter System

The Calorimeter System of the ATLAS detector plays an important role in achieving the physics goals. The discovery of the Higgs–boson, for instance, will be strongly dependant on the performance of the calorimeter system, e.g. promising channels in the low mass region of up to ~ 180 GeV are $H \to \gamma\gamma$ or $H \to 4l$ rely on the performance of this system. One distinguishes two parts of the calorimeter:

The Electromagnetic Calorimeter   is a Lead–Liquid Argon sampling calorimeter in an accordion–shaped geometry. The barrel region of the detector covers the pseudorapidity range of $|\eta| < 1.475$. It is completed by two end–cap calorimeters, both featuring two coaxial wheels, that cover the regions of $1.375 < |\eta| < 2.5$ and $2.5 < |\eta| < 3.2$. The accordion–like shape of the detector in the barrel part gives a complete 2π coverage in ϕ. The thickness of the lead absorber plates vary between 1.1 mm and 2.2 mm as a function of $|\eta|$. In the region of precision physics ($|\eta| < 2.5$), the system has a longitudinal segmentation in three parts and a transverse segmentation of 0.025×0.025 in $\Delta\eta \times \Delta\phi$. The overall energy resolution will be better than $10\%/\sqrt{E/GeV} \oplus 0.7\%$. A total of $\sim 190\,000$ channels is provided by the EM calorimeter.

The Hadronic Calorimeter of ATLAS uses iron absorbers with plastic scintillating plates (tiles) and a scintillating tile–calorimeter in the barrel region of $|\eta| < 1.7$. The segmentation in this part is 0.1×0.1 in $\Delta\eta \times \Delta\phi$. At larger pseudorapidities, a Liquid Argon sampling calorimeter with copper absorbers will be used due to the intrinsic radiation hardness of this technology. These hadronic end–cap calorimeters will cover the range of $1.5 < |\eta| < 3.2$. In the very forward region of $3.1 < |\eta| < 4.9$, the dense forward calorimeter will be installed in three longitudinal segments, the first one using copper as the absorber material and tungsten in the last two segments. These forward calorimeters play a crucial part in the determination of missing transverse energy E_T^{miss} and in forward jet tagging. The energy resolution of the hadronic calorimeter is better than $50\%/\sqrt{E/GeV} \oplus 3\%$ for $|\eta| < 3$ and $100\%/\sqrt{E/GeV} \oplus 10\%$ for $3 < |\eta| < 5$.

2.3.3 The Inner Detector

The Inner Detector is a system composed of three different tracking detectors and is closest to the interaction point. Two high granularity systems at inner radii, the Semiconductor Tracker (SCT) and the Pixel Detector, as well as a system of continuous tracking elements, the Transition Radiation Tracker, at outer radii are all placed inside a solenoid. The solenoid provides a magnetic field of 2 T running axially to the beam axis, necessary for the precise reconstruction of the momentum of charged particles. The length of the Inner Detector is 6.8 m, its radius is 1.15 m [8]. Figure 2.3 shows an overview of a quarter of the Inner Detector's layout.

The Transition Radiation Tracker is comprised of 4 mm diameter straw tube detectors. The TRT uses a gas mixture of 70 % Xe, 20 % CF_4 and 10 % CO_2. Polypropylene/Polyethylene acts as the radiator material between the straws generating transition–radiation photons. Combined with a two–threshold readout system, this yields a high efficiency electron–pion differentiation in the TRT. In the barrel region (radius 56 to 107 cm) more than 52 000 straws of 2×74 cm length coaxial to the beam direction are able to provide a resolution of ~ 170 µm. Improvements in terms of spatial resolution are accomplished by readout at both ends of the tubes and a drift time measurement. In the end–cap regions of the TRT $\sim 320\,000$ straws in radial orientation cover the radii of 64 to 103 cm. In average the TRT provides 35 hits per track giving the possibility of a sophisticated pattern recognition. Another advantage is the intrinsic radiation hardness of such a system, the drawback being the occupancy. During the phase of high luminosity the occupancy is expected to be up to 40 % of the $\sim 420\,000$ readout channels.

The Semiconductor Tracker is the outer one of the two precision tracking detectors of ATLAS. The basic building blocks of the detector are silicon strip detector modules built as high resistivity reverse biased diodes. Four single–sided strip detectors build such a module. Two detectors are daisy–chained together, while the backside pair is identical but rotated by 40 mrad to provide z–measurement capability. Small stereo angles like this one have the advantage of reducing the number of ghost hits (ambiguities) in events of high multiplicity. The four–layer barrel part consists of 2112 modules, providing a total area of around 34 m^2. Nine disks on each end–cap side feature 1976 modules and 27 m^2.
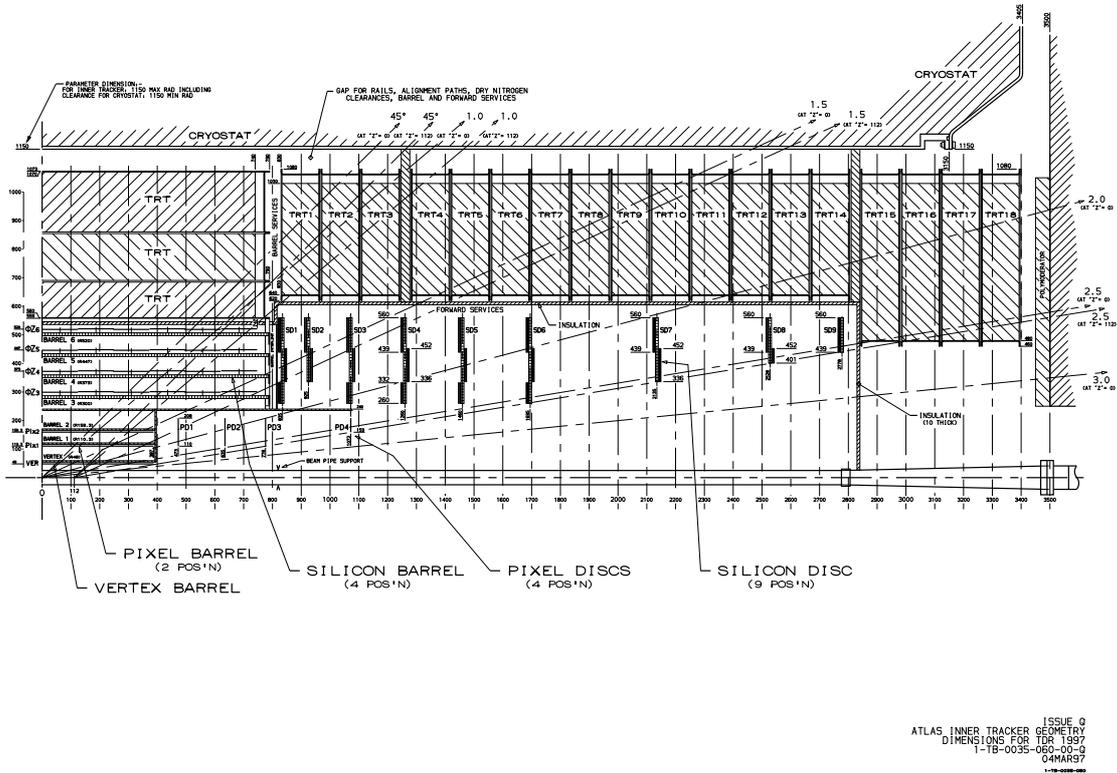
Figure 2.3: Schematic cross section view of the Inner Detector showing the three subsystems TRT, SCT and Pixel [8].

The resolution in a detector plane is 20 µm while the double hit resolution is 200 µm. The pseudorapidity coverage of the SCT is $|\eta| < 2.5$. The SCT provides a total of $\sim 6.3 \cdot 10^6$ channels with binary readout. Four space points in the barrel region and a minimum of three space points in the disk section are delivered by the SCT.

The Pixel Detector is the innermost system of the Atlas detector and closest to the interaction point [9]. Reconstruction of primary and secondary vertices is of highest importance, being the main task of the Pixel detector. The latter is essential for the reconstruction and tagging of B–hadrons by the distance they travel before they decay ($c\tau \simeq 500$ µm for B$^\pm$).

Figure 2.4 clearly shows the improvement in the resolution of the impact parameter by the additional installation of a vertex layer at minimum radius, the *B–layer*. The next chapter will describe the Pixel Detector System of Atlas in more detail.

2.3.4 The Data Acquisition and Trigger System of Atlas

The average number of events per bunch crossing at the Lhc in its high luminosity phase is around 23, while the bunch crossing frequency is 40 MHz. Bearing in mind that the total number of channels is $\sim 10^8$, it becomes immediately obvious that the amount of data is
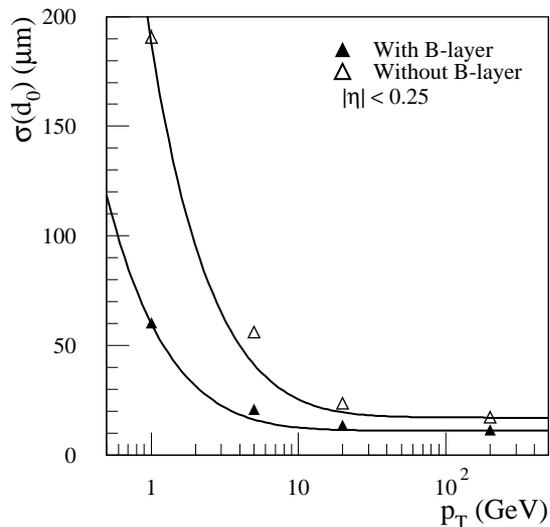
Figure 2.4: Improvement of impact parameter resolution by the B–layer [8].

far too high to be stored completely. Selecting only relevant events and reducing the data rate to acceptable levels is a challenge [10]. Three layers of processing are necessary for this purpose:

- The Level–1 trigger (LVL1) accepts data from parts of the muon spectrometer and the calorimeter at the full bunch crossing rate of 40 MHz. Dedicated hardware aims at a decision within $< 2\,\mu s$ and reduces the event rate to 75 kHz (up to a maximum of 100 kHz). During this time the information has to be stored in on–detector pipeline memories. If interesting signatures are found, for instance a high p_T muon signature in the resistive plate chambers of the muon spectrometer, the LVL1 trigger signal is globally distributed to the on–detector electronics and the detector data are send to the readout drivers and get stored in the readout buffers (RODs and RODs).

- The Level–2 trigger further reduces the event rate to ~ 1 kHz and makes use of the information of the "regions–of–interest" (RoI) in the detector that are passed from the LVL1 trigger. These include position and p_T range of objects like high–p_T muons, electrons/photons, hadrons, taus and jets. In a mean time of 10 ms the trigger has to come to the decision based on the full detector granularity including the tracking system. The data is then passed to the event builders.

- The Level–3 trigger or event filter for complete event reconstruction, uses sophisticated algorithms running on dedicated PC–clusters with a computing performance of $\sim 10^6$ MIPS[4]. After about 1 s the event is either selected and send to permanent storage or discarded. With an approximate event size of 1.5 MB the rate has to be reduced to 10 to 100 Hz. One year of operation of ATLAS produces ~ 1 PB of data.

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[4] Million Instructions Per Second.

Chapter 3

Pixel Detectors for High Energy Physics Applications

Pixel detectors are among the most advanced detector systems in the field of high energy physics, because they provide the highest granularity and resolution. An additional advantage is the avoidance of ambiguities, which are an intrinsic problem of strip detectors. Pixel detectors can therefore be used at very close distances from the collision point, where track densities are highest. Due to the high number of events, this is exceedingly true for hadron collider experiments. In this chapter the basics of semiconductor detectors with special focus on pixel detectors are covered and a description of the ATLAS pixel detector's components will be given. Sensors, readout electronics and the overall system design of the ATLAS pixel detector have also been used for the development of modules in MCM–D technology.

3.1   Basics of Semiconductor Detectors

Semiconductor detectors are mostly based on silicon or germanium as the crystalline semiconductor material. A charged particle of high energy passing through a semiconductor loses energy to the crystal generating electron–hole pairs along its path. The semiconductor acts like a solid–state ionization chamber. For silicon the mean energy required to generate an electron–hole pair is 3.62 eV. For ionization to occur one has to overcome the energy gap in the energy band structure of 1.12 eV for silicon; but also the generation of phonons - in the end thermal energy - has also to be accounted for.

Generally the energy transfer of a charged particle in matter is described by the Bethe–Bloch equation formula.

$$-\frac{dE}{dx} = 2\pi N_a r_e^2 m_e c^2 \rho \frac{Z}{A} \frac{z^2}{\beta^2} \cdot \left[\ln\left(\frac{2 m_e \gamma^2 v^2 W_{max}}{I^2} - 2\beta^2 - \delta - 2\frac{C}{Z} \right) \right] \qquad (3.1)$$

with (values for silicon given in brackets):

dE/dx:	mean energy loss per track length
N_a:	Avogadro's number $= 6.022 \times 10^{23} \text{ mol}^{-1}$
r_e:	classical electron radius $= 2.817 \times 10^{-13}$ cm
m_e:	electron mass $= 511 \text{ keV}$
ρ:	density of absorbing material (2.33 gcm^{-3})
I:	average effective ionization potential ($\approx 173 \text{ eV}$)
Z:	atomic number of absorbing material (14)
A:	atomic weight of absorbing material (28)
z:	charge of incident particle in units of e
M:	mass of the incident particle
β:	v/c speed of the incident particle in terms of c
γ:	$1/\sqrt{1 - \beta^2}$
δ:	density correction
C:	shell correction
W_{max}:	$\simeq 2m_e c^2 \beta^2 \gamma^2$, if $M \gg m_e$
	maximum energy transfer in a single head on head collision.

Formula 3.1 includes the density effect correction δ and the shell correction C and is valid down to $\beta \simeq 0.1$ [11].

The energy loss of a traversing particle is decreased by the density effect at high energies. The presence of the electric field leads to the polarization of atoms along the path of the particle and thus electrons far from the path are shielded from the full electric field. The density effect depends on the density of the absorbing material.

The effect of the shell correction, reducing the energy loss at low energies, is small. This accounts for the wrong assumption of a stationary electron in the absorber.

At around $v \simeq 0.96\,c$ or $\beta\gamma \simeq 3.5$ a minimum in the Bethe–Bloch formula is reached. Particles at that point are called *minimum ionizing particles* (MIP). For instance, the mean energy loss of a minimum ionizing pion ($m_\pi = 139.57 \text{ MeV}$) in 250 μm silicon is $\simeq 97.5 \text{ keV}$ generating $\simeq 27\,000$ electron–hole pairs (see Figure 3.1). The spectra of the deposited energy was first calculated by Landau [12] and in depth by Bichsel [13]. In the case of thin absorbers the energy loss probability density functions, the *straggling functions*, are non gaussian but have a tail to high energies due to possible interactions with high energy transfer. The straggling function is parametrized by its most probable value and width. The difference between the mean value calculated by integration of the Bethe–Bloch formula and the most probable energy loss is significant, e.g. $\simeq 19\,300$ electron–hole pairs corresponding to $\simeq 70\,\%$, in our case of a 250 μm silicon detector.

A charged particle of high energy will traverse a thin semiconductor detector almost undisturbed, losing only a small fraction of its energy. The density of charge carriers is nearly constant along the particle's path, almost independent from the energy and proportional to the square of its electric charge.

Semiconductor detectors have to separate the electrons and holes to avoid direct recombination and thus loss of the signal. One approach is to use a *pn–junction* and apply a reversed bias. The charge carrier free area at the *pn–junction* can be increased over almost the whole semiconductor thickness. Electrons and holes are then directly separated by the

dE/dx in Silicon (Bethe Bloch formula)
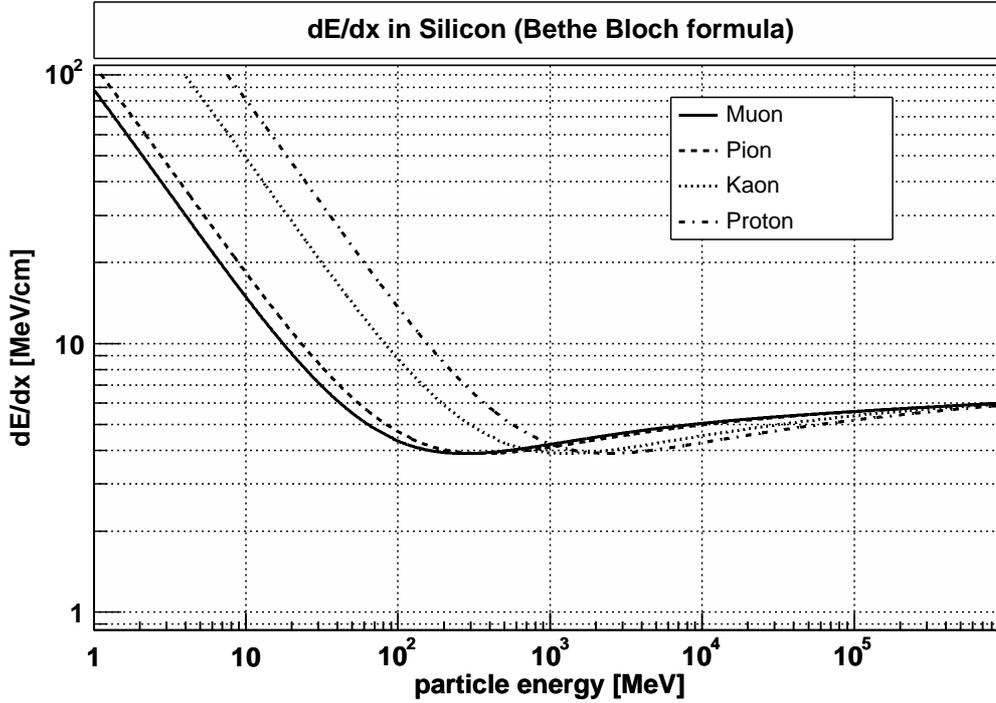
Figure 3.1: Energy loss of different particles in silicon in dependance of the particle's energy.

bias voltage and charge carriers are generated along the complete particle path through the detector. The movement of the charge carriers induces a signal at the electrodes that is detectable by sensitive electronic channels. Thermally generated charge carriers and other free charge carriers, for instance released from trapping centers of crystal defects, contribute to the leakage current of the sensor. This current has to be kept as low as possible to get a good signal to noise ratio in the system. A segmentation of the diode in the shape of strips or single elements allows a position measurement.

Due to the statistic nature of a position measurement by the discrete information of a single strip or a single element the variance $\langle \Delta x^2 \rangle$ of the position measurement is given by:

$$\langle \Delta x^2 \rangle = \frac{1}{p} \int_{-p/2}^{p/2} x^2 dx = \frac{p^2}{12} \tag{3.2}$$

Where p is the *pitch*, the distance between the center of two strips or elements. Note that this does not account for weighting the position by pulse height measurements, when more than one element is responding.

When measuring the energy deposition of a well known energy E the achievable energy resolution is limited. Due to the statistical fluctuations in the number of ionizations and excitations a sharp delta–function energy peak like in an ideal case is never reached. The finite width of the peaks limits the energy difference down to which two different energies can be resolved as being individual peaks. This is illustrated in Figure 3.2.

Figure 3.2: Energy resolution [11].

The relative energy resolution R is usually given in terms of the *full width at half maximum*(FWHM) [11]. The assumption of a Poisson–like statistics in the number of ionizations $J = E/w$, w being the average electron–hole pair creation energy for a specific material, would lead to:

$$R = \Delta E/E = 2.35\frac{\sqrt{J}}{J} = 2.35\sqrt{\frac{w}{E}} \qquad (3.3)$$

This is true for a dE/dx measurement like in the case of a particle passing a thin silicon detector. If the full energy of the radiation is deposited in the detecting material, e.g. by the photo effect, the naive assumption of the independent ionizations is wrong. In this case, the energy resolution is enhanced:

$$R = \Delta E/E = 2.35\frac{\sqrt{FJ}}{J} = 2.35\sqrt{\frac{Fw}{E}} \qquad (3.4)$$

In Equation 3.4 the *Fano factor* F corrects the variance of the mean number of ionizations J by a material and dependant number significantly below unity ($F = 0.115$ for Si [14]).

3.2 Pixel Detectors

The term pixel originates in *picture* and *element*. A two–dimensional array of diodes with element size of less than $1\,\mathrm{mm}^2$ combined with its dedicated readout electronic is called a pixel detector. The segmentation of one electrode side of the sensor and its underlying structures is sufficient for building the array. In contrast to pixel detectors, strip detectors feature only a one–dimensional segmentation. Only one coordinate of a plane space point can be measured by a single strip detector. Combining two layers of strip detectors rotated

Figure 3.3: Inherent problem of ambiguities in the reconstruction of true particle hits when using strip detectors.

against each other allows measuring both coordinates, but the intrinsic disadvantage of ambiguities in the case of multiple hits cannot be avoided. Figure 3.3 illustrates this topic.

Pixel detectors provide a true 2D position information and are therefore suited for the usage close to the interaction point, where track densities are highest. One of the challenges in building pixel detectors is the enormous number of channels. Typical channel numbers of pixel detectors in the LHC experiments are of the order of 10^8. The higher signal to noise ratio of a pixel detector compared to a strip detector due to the lower leakage current per channel is an additional advantage.

3.2.1 Hybrid Pixel Detector

The approach of hybrid pixel detectors takes advantage of sensors and electronic chips built in separate technologies. In this way, both components can be optimized on their special requirements. The need for an interconnection technique arises. Pixel detectors make high demands on the interconnection technology where each sensor cell has to be contacted with the corresponding electronic cell. Technologies are bump bonding and flip chip. In Chapter 4.4 a more detailed description will be given. The ATLAS pixel detector uses this technique for hybridization.

3.2.2   Examples of Pixel Detectors

The Charge Coupled Device (CCD) is by far the most frequently used pixel detector. Despite its usage in commercial cameras, CCDs are also quite common in research. The X–ray Multi Mirrow satellite, the world's most powerful X–ray telescope, features a pn–CCD used for high efficient X–ray spectroscopy in space. Due to their serial readout and relatively low readout speed, CCDs are not suited for the application in ATLAS.

Monolithic and semi–monolithic pixel detectors where both parts of the system can be merged into one entity are in development.

Another interesting new approach for the use of silicon as detector material is the 3D silicon detector approach, especially within conjunction with active edges [15]. The basic principle of the sensor is shown in Figure 3.4. Vertical holes are plasma etched into the un-doped silicon bulk and filled with p^+ and n^+ doped electrodes. The depleted area then starts to grow in the direction parallel to the detectors surface resulting in very low depletion voltages. The edges of the device can also be formed as being doped reducing the inactive zone of the sensor border to a few μm. This development is very promising resulting in

Figure 3.4: Cartoon of 3D pixel detector with active edges [15].

radiation hard, fast and homogeneous sensors.

The use of DEPFET[1] sensors, where a first amplifying stage is directly integrated in a pixel cell, in future pixel detector has been studied in [16]. The usage of diamond detectors as tracking devices is also a field of research, due to their intrinsic radiation hardness [17].

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[1] DEPFET: **DEP**leted **F**ield **E**ffect **T**ransistor

3.3   The ATLAS Pixel Detector

The overall layout of the ATLAS pixel detector is shown in Figure 3.5. Three barrel shaped layers and three disks in the forward and backward region cover a pseudorapidity range of $|\eta| < 2.5$. With a minimal end of lifetime efficiency of at least 95 % the pixel detector has to provide three space points.

6 disks

~ 1.3 m

3 barrel layers

modules (1744 in total)
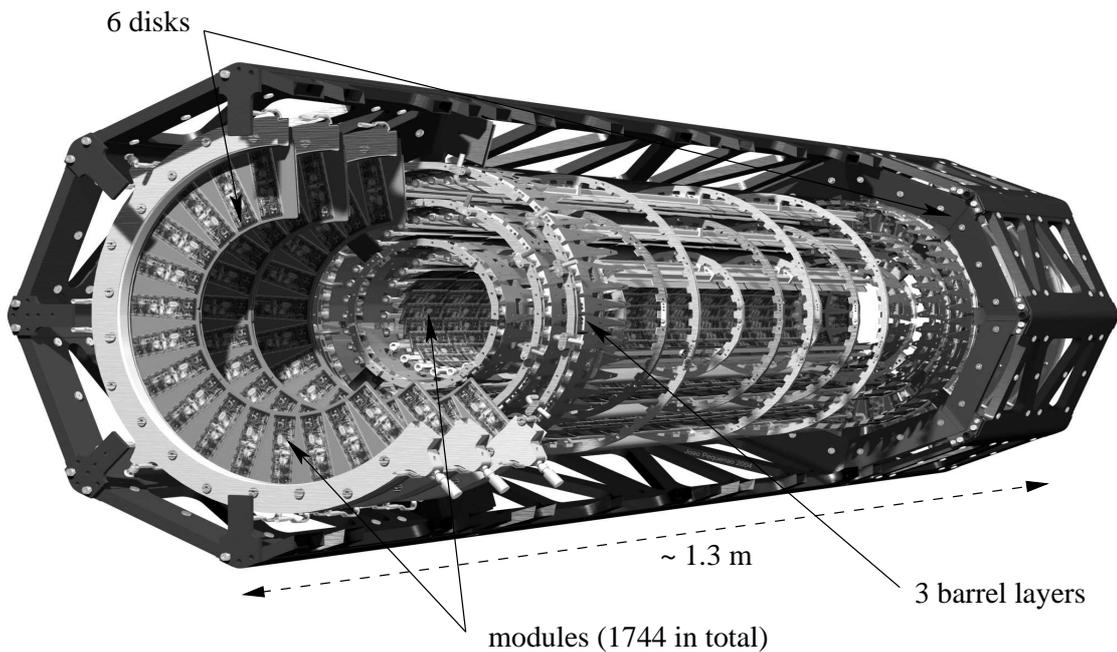
Figure 3.5: Drawing of the ATLAS pixel detector.

Furthermore all detector components have to fulfill the ATLAS requirements of radiation hardness. A total fluence of $10^{15}\, n_{eq}/cm^2$ is expected in the innermost barrel layer, the B–layer, corresponding to ~ 50 Mrad in silicon.

The basic building blocks of the pixel detector will be the modules. A total of 1744 modules are positioned on carbon structures in the barrel respective disk sections. Table 3.1 gives an overview of some global parameters of the Pixel Detector.

The total number of channels of the pixel detector will be about $\simeq 0.8 \times 10^8$, serving a total area of $\simeq 1.74\,\mathrm{m}^2$. The pixel cell size is $50 \times 400\,\mathrm{\mu m}^2$ and a module features a total area of $\simeq 10\,\mathrm{cm}^2$ ($6.08 \times 1.64\,\mathrm{cm}^2$).

3.3.1   Sensors for the ATLAS Pixel Detector

The main, although hardest to meet requirement of sensors for the ATLAS pixel detector, is the radiation hardness in the very harsh radiation environment close to the interaction

Detector-part	Nom. radius mm	No. of staves	No. of modules
B–layer	50.5	22	286
Layer 1	88.5	38	494
Layer 2	122.5	52	676
	Nom. z–position	No. of sectors	No. of modules
Disk 1	± 495	8	48
Disk 2	± 580	8	48
Disk 3	± 650	8	48

Table 3.1: Parameters of barrel layers and disks of the ATLAS pixel detector [18].

point.

The development of sensors for the ATLAS pixel detector has been carried out on a two trace strategy, that is described in detail in [19]. The ATLAS collaboration itself investigated design related aspects with a detailed prototyping program. The technology of choice is a n^+–pixel on n–bulk technology with the p-implantation on the backside of the sensor [20]. This has the following implications:

- the sensor bias voltage is applied to the backside of the sensor shielded by a guard ring structure and therefore the danger of sparking between sensor and electronic chip is avoided. The gap between the sensor and the electronic chip is only $\simeq 10\,\mu m$ and thus this side of the sensor including the edges has be at ground level.

- In the unirradiated case the depleted area of the sensor grows from the backside of the sensor. It is necessary to reach full depletion of the bulk in order to isolate the pixel from each other. After a fluence of around $10^{13}\,n_{eq}/cm^2$ the *type inversion* will occur, where the n–type bulk of the sensor will convert to p–like behavior. The depleted area then grows from the front side and a partially depleted operation of the sensor is possible. A disadvantage of this technique is the required double sided processing of the sensor during production.

- Due to the low resistive contact between the n^+–implantations of the sensor cells a p–isolation is required for isolation between the sensor cells. A p-implantation of medium dose covers the complete n–side for that purpose. This technology, known as p–spray isolation technique, has proven to be superior in terms of charge collection after irradiation. It offers the additional advantage of a simple design and the possibility of small structure sizes.

The second trace of the sensor development has been carried out by the ROSE[2] collaboration in a worldwide effort. Its aim is to increase the radiation hardness of the silicon itself. Technology of choice is DOFZ (Diffusion Oxygenated Float Zone) silicon, where selective impurities of oxygen are placed in the silicon crystal by diffusion. This oxygen

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[2] Research and development On Silicon for future Experiments (CERN – RD48).

enrichment has shown to significantly reduce radiation damages in silicon, allowing even a full lifetime operation of the sensors for the B–layer [21].

Among other, significant features of the sensor for this thesis are: a sensor will be equipped with a total of 16 readout chips. A certain gap between these chips has to be kept, for safe and reliable mounting of the electronic chips. The design gap between the chips is 200 µm. Together with the unavoidable dead border area of the chips of 100 µm, one has to cover an interchip region of 400 µm, to guarantee full coverage of a sensor.
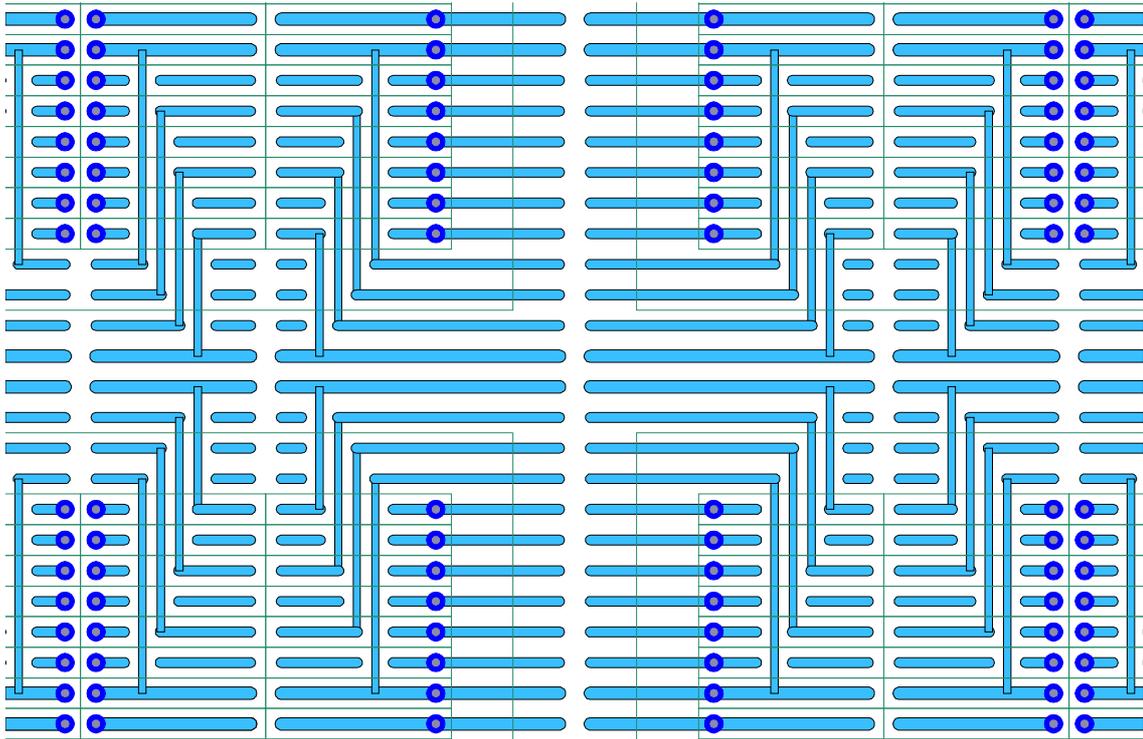
Figure 3.6: Sensor coverage of interchip region. Sensor metallization and readout contact position is shown as well as the geometry of the readout chip

The solution in the ATLAS pixel sensor design is shown in Figure 3.6. In the short direction of the pixel four additional sensor pixel structures are routed in the sensor metallization layer to one of the top eight contacted sensor cells. In the long direction of the pixel cells, the outer column of sensor pixel are elongated by 200 µm. This leads to a quite large fraction of 13.3 % of pixel cells with a non standard size (and different behavior in terms of performance). These pixel are referred to as "ganged", "long" and "long–ganged" pixel cells.

Full testability of a sensor is guaranteed by the implementation of the *bias–grid*. This structure is made possible through the p–spray technique to isolate the pixel implants [22]. A mesh of metallization gives the opportunity to contact all pixel cells via one contact by the *punch–through effect* [23].

3.3.2   Readout Electronics – the Front–end Chip

The main requirements of the pixel detector for the readout electronics, or front–end chips, are [24]:

- small pixel size to achieve high resolution,

- high signal to noise ratio of the electronics (ENC $\leq 400\,e^-$),

- threshold tuning capability, to achieve a low threshold variation over the chip (dispersion $\leq 300\,e^-$),

- simultaneous readout and sensitivity to avoid dead time of the detector,

- low power consumption ($< 50\,\mu W$ per pixel),

- digital readout with zero suppression in every pixel,

- on chip hit information buffering until the Level–1 trigger signal arrives or else discarding

- unique assignment of a hit to the correct bunch crossing time window of 25 ns.

Electronic chips for hybrid pixel detectors need readout architectures that amplify and digitize signals at the contact to the sensor for each individual pixel. This requirement limits the size to which the actual pixel cell size can be reduced on the electronic side. The individual pixel circuit of the ATLAS pixel detector readout electronic chips fits into a rectangle of $50 \times 400\,\mu m^2$. The circuits are organized in 160 rows and 18 columns and thus each readout chip serves a total of 2880 pixel cells. Each pixel unit of the chip houses a charge sensitive preamplifier with DC–feedback and leakage current compensation. The constant current return to baseline of the amplifiers output signal allows an energy measurement in terms of the signal's *time over threshold* in units of 25 ns, the ToT. This is useful for increasing resolution in the case of multiple hits in neighboring pixels, by calculating the energy weighted center of the hits. The analog part of the pixel unit cell (only a simplified description is given here) is followed by a discriminator with a global threshold setting. If the signal rises above the threshold a grey–coded digital information of the hits timing information (leading and trailing edge) is stored and transferred to the *end of column* logic. The hit information: row, column and ToT waits for the readout in the case of a time matching Level–1 trigger decision or else is discarded. The option of casting up to sixteen Level–1 trigger in series enforces the additional trigger identification information.

Test signals can be injected via capacitors directly into the preamplifiers of selectable pixels on each chip, allowing detailed studies of the chips' analog performance. The front–end offers the possibility of performing a pixel wise tuning of the preamplifier's feedback current and the tuning of the discriminator's threshold settings. Each pixel can be selected for the mentioned charge injection but also masking for readout is possible, which is useful in case of noisy pixels.

History of Prototypes

A short summary of the evolution of the front–end chip through the different prototype stage is given here:

- Front–end A, B and C were the first front–end prototypes with ATLAS geometry. These were all non radiation hard designs. They were produced in 0.8 µm CMOS[3)] processes [25–28].

- Front–end D and D2 were the first attempt to produce radiation hard readout chips for ATLAS in a world wide effort, combining experience and manpower of the involved institutes. Nevertheless the DMILL[4)] process turned out to be unsatisfactory in terms of performance and yield. A second submission achieved only marginally better results.

- Front–end I: The FE-I1 was the first attempt of a newly developed technique in a commercial *Deep SubMicron technology*, DSM. The strong advantage of DSM is its adaptation to the current industrial processes, therefore offering a larger range of possible industrial partners and well known processes [29, 30]. The FE-I1 and the following DSM prototypes are fabricated in a 0.25 µm CMOS process. The FE-I1 was available in two different flavors, "A" and "B", with the only difference in the size of the analog blocks feedback capacity. This generation of front–end chips turned out to be very successful, especially in terms of radiation hardness.

- Front–end I3 now is the actual production chip of ATLAS. It is noteworthy that the FE-I3 features an autotune capability that allows a very fast threshold tuning of the chip.

In Chapter 9 laboratory measurements on DSM prototype hybrids will be presented.

3.3.3   Correlated Systems apart from Modules

Mechanics and Support Structures

To guarantee the requirements of the ATLAS pixel detector in terms of radiation length and cooling, a low mass space frame of carbon–carbon is built. This system has to be produced in very high precision [31].

Optical Link

At both ends of the pixel detector patch panels are located, where a conversion between the electrical signal from the detector to optical signal lines to the readout side is performed. This guarantees electrical decoupling and the minimization of cable cross section in the detector. The optical link is described in detail in [32].

[3)]Complementary Metal Oxide Silicon.
[4)]Durcie Mixte sur Isolant Logico-Lineaire.

Detector Control System

The Detector Control System, DCS, of the pixel detector manages the power supply and monitoring of the detector. This includes a temperature monitoring via NTC thermistors[5] located directly on the modules. For monitoring purposes their signal is connected to the DCS system but as well to a dedicated hardware interlock system, the I–Box, developed by the University of Wuppertal [33].

3.3.4   Pixel Detector Modules

As mentioned before the basic building blocks of the Pixel detector are modules. They are comprised of 16 readout chips and the controller chip, MCC. The base support of such a module is the sensor itself. Passive components like decoupling capacitors, termination resistors and the temperature sensor have to fit on such a module, too. Building a module is referred to as the hybridization process.
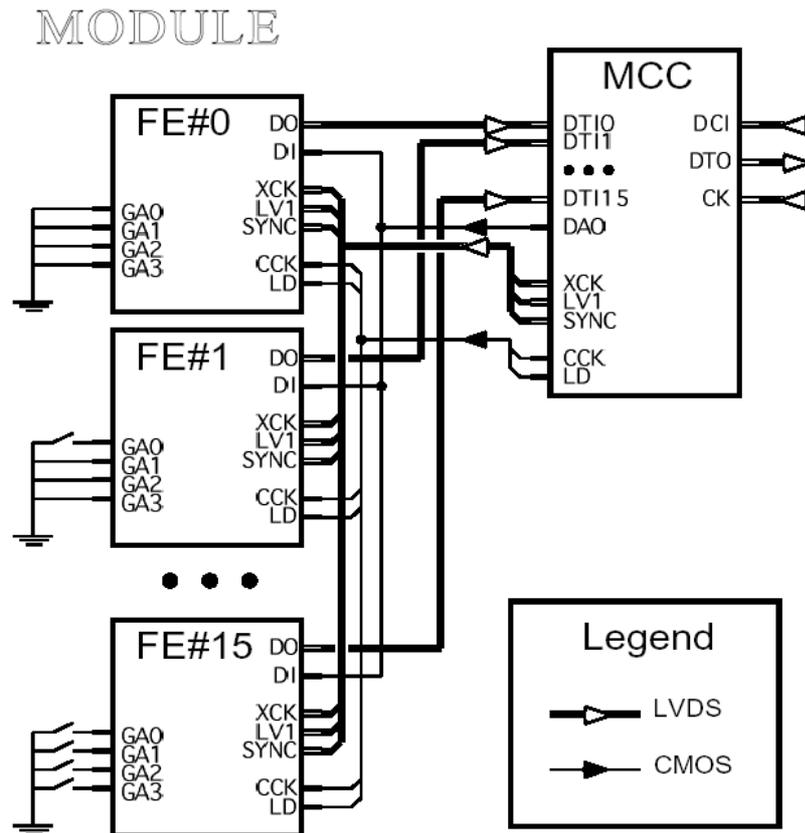
Figure 3.7: Block diagram of the intramodular signals of an ATLAS pixel detector module [34].

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[5] NTC: **N**egative **T**emperature **C**oefficient

(a) Low voltage CMOS (LV–CMOS), used for slow control commands and configuration.

(b) Multi drop LVDS, used for fast control commands, e.g. LV1 trigger.

(c) Point to point LVDS, used for data transmission from FE to MCC.
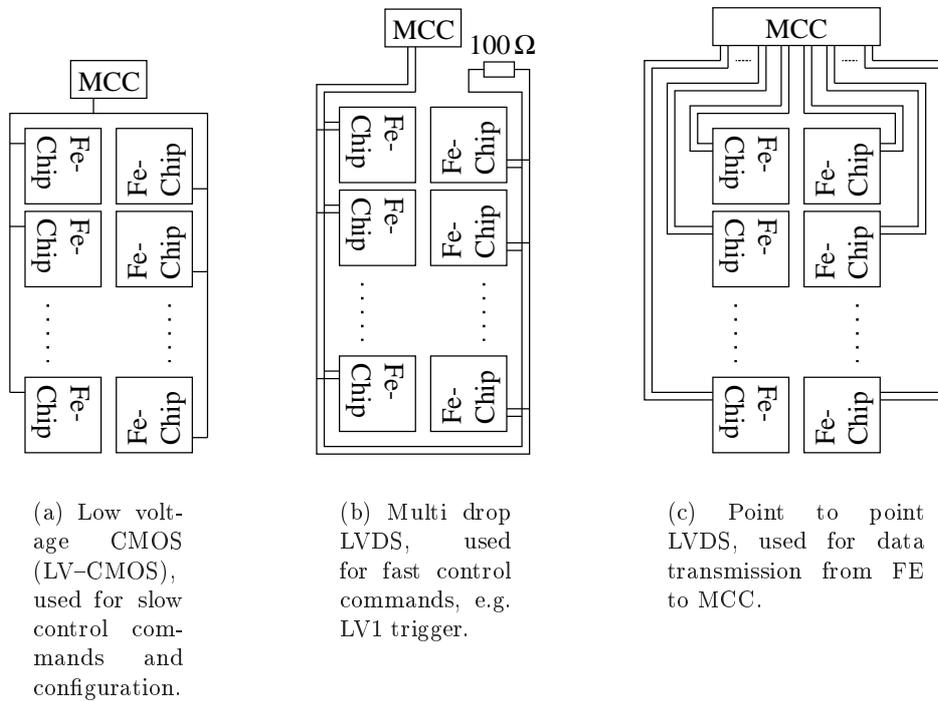
Figure 3.8: Schematic view of the three different signal type connections between MCC and FE chips [35].

Figure 3.7 shows the intramodular signals between the controller chip and the front–end chips. These intramodular signals are sent via signal lines of three different ways (compare to Figures 3.8(a), 3.8(b) and 3.8(c)), combined in the signal bus system of a module. Furthermore a power distribution system is necessary to supply all ASICs[6] on a module as well as temperature monitoring and the supply with the sensor's bias, the depletion voltage. Figure 3.9 gives a schematic overview of the system's architecture and connections to the readout system of the detector. The different technologies for building the modules' power distribution and signal bus system, the MCM–D approach and the ATLAS Flex–Hybrid solution will be described thoroughly in the next chapter.

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[6] ASIC: **A**pplication **S**pecific **I**ntegrated **C**ircuit
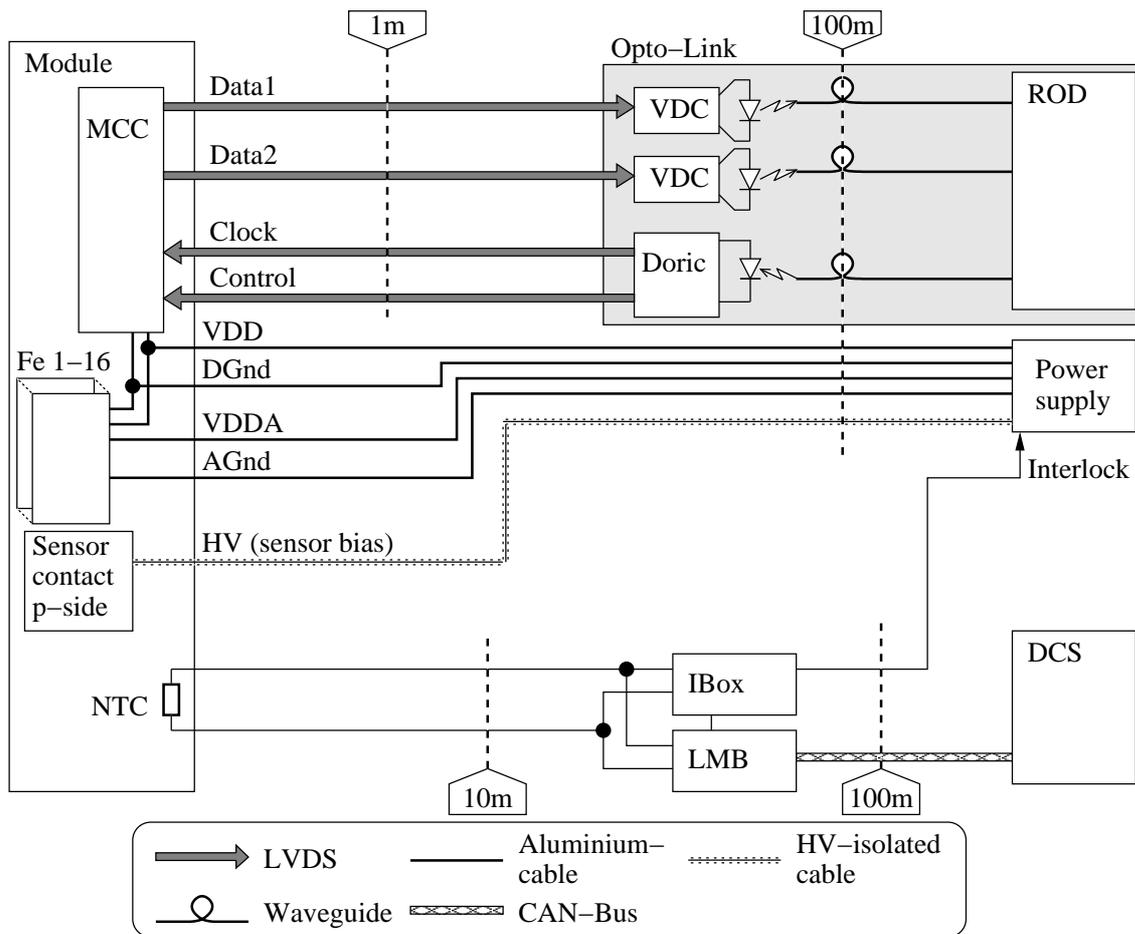
Figure 3.9: Readout and control connection between modules and off detector electronics [35].

Chapter 4

MCM–D Technique

width = 24,2 mm

lenght = 69,8 mm
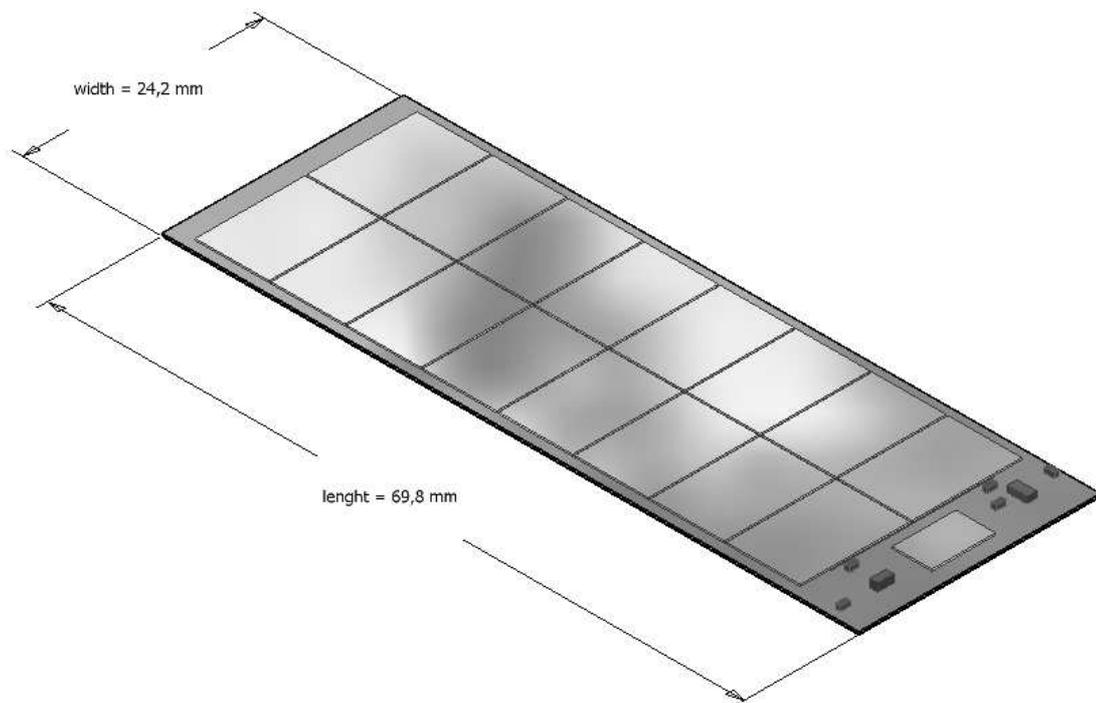
Figure 4.1: Drawing of a complete ATLAS pixel detector module in Multi Chip Module Deposited technique (MCM–D).

The need for a highly integrated technology for interconnecting and supplying electronic chips on a pixel detector module has already been shown. For the last years, the technology of choice was the gluing of a flexible kapton foil with integrated metal layers onto a module. Hundreds of thin wires contacting the electronic chips, numerous assem-

bly steps and dedicated tooling are the major drawbacks of this technology. In the last two decades a market for solutions for miniaturization has been growing rapidly mostly driven by communication and automotive applications. Using new technologies and adapting them to the needs of high energy physics applications has lead to the development of MCM–D modules. Such Multi Chip Modules (MCMs) are built by on wafer deposition of dielectrics and conductors. In this chapter the basics of the MCM–D technology are described and a comparison to the standard technology is given.

4.1   Standard Solution: Flex–Hybrid Approach

The solution of using an additional thin flexible print circuit is the baseline choice of the ATLAS experiment. This printed circuit is a two metal layer system of copper on a Kapton® or Upilex® layer. The controller chip MCC and the passive components for decoupling and termination are located on this flexible printed circuit, usually referred to as *the flex*. The MCC is glued and afterwards connected by redundant wire bonding with 22 µm Al wires (see section 4.4 on page 36 for a short summary on the mentioned interconnection techniques). The passive components are soldered to the flex. These necessary assembly steps are done before mounting it onto a module.

In parallel assembly steps the readout chips are contacted by bump bonding and flip chip to the sensor. At this stage the module is called a *bare module*. The fine–print is then glued to the backside, the p–side of the sensor. About 560 wire bonds perform the necessary connection between the frontend chips and the printed circuit. In Figure 4.2(a) the principle of the final buildup is shown. For details on the fine–print see [36].

In Figure 4.2(b) a full operational module, mounted on a PCB[1] for test purpose, can be seen. As full encapsulation of the wirebond connection is not foreseen, due to minimization of radiation length and CTE[2]-mismatch between silicon and the kapton circuit, this type of module is highly fragile. The wirebond connections are done by 25 µm thin Al–wires [37]. The mixture of interconnection technologies is one of drawbacks of this technique.

This scenario of a ATLAS Flex module is a chip–down one, where the unstructured backside of the frontend chips is directly glued to the carbon–carbon support structure. This guarantees a good thermal exchange, as the support structure features the integrated cooling pipe.

4.2   The Multi Chip Module–Deposited Technique

From the experience made with the building of the pixel detector modules for the vertex detector of the DELPHI[3] experiment [38], the approach of the MCM–D technique evolved. There bump bonding is used as the only interconnection technique. The idea and evaluation of the MCM–D technology was pursued mainly by the University of Wuppertal in collaboration with the Fraunhofer Institute for Reliability and Microintegration (IZM)

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[1] PCB: **P**rinted **C**ircuit **B**oard
[2] CTE: **C**oefficient of **T**hermal **E**xpansion
[3] Detector with Large Parton and Hadron Identification.
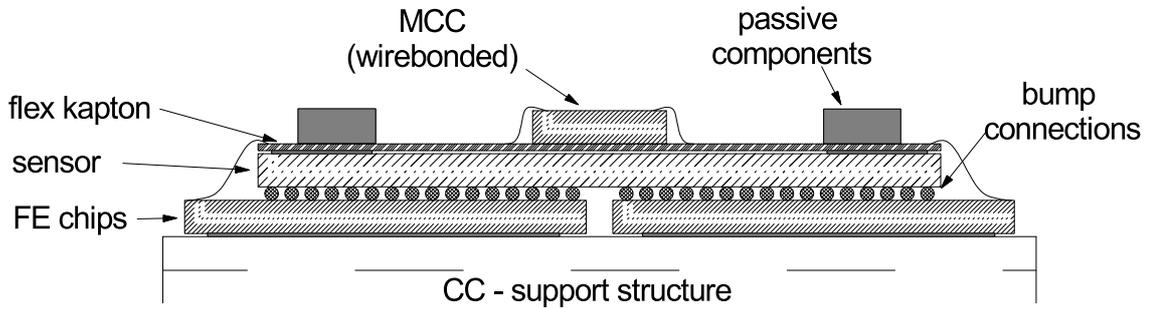
(a) Schematic cross section of an Atlas Flex module
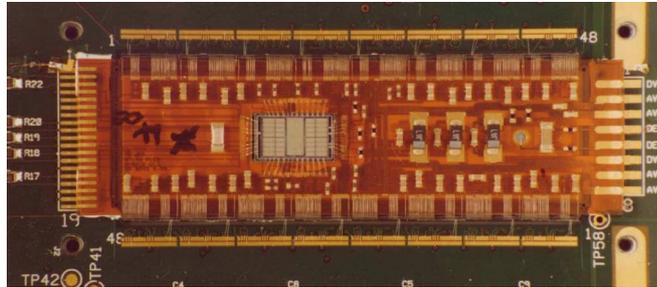
(b) Photograph of an Atlas Flex module

Figure 4.2: The concept of a Flex Hybrid.

in Berlin. First developments were also done in collaboration with the Interuniversity Microelectronics Center (IMEC) in Leuven, Belgium [39].

In this approach a system of conducting layers of metal and isolating layers of a dielectric material is built directly on the sensor wafer. Industrial techniques of wafer treatment like sputtering, electroplating and spin coating are used. Details of the processing will be discussed in Chapter 7. The technologies of wafer treatment promise small achievable structure sizes and well defined electrical properties [40, 41].

It has been shown elsewhere [35], that a system of four copper layers isolated by polymer layers of Cyclotene® is suitable for the demands of Atlas. Cyclotene® is a benzocyclobutene (BCB) based photosensitive polymer. The choice of four copper layers is determined by the powering requirements of Atlas modules (summarized in Table 4.1). It is required, that the on module voltage drop should not exceed 100 mV on VDD or VDDA.

Figure 4.3 shows the principle cross section of such a module. The sensor substrate also acts as the base carrier of the complete module. It has to be slightly larger compared to the Flex module. The readout chips are contacted exclusively by bump bonding. For the purpose of MCM–D the IO contacts of the frontend chips also feature bump bond pads (four per IO for reasons of redundancy). These bump contacts are directly connected to the MCM–D structures. The complete data bus system and power distribution could in

Potential	nom. voltage V	nom. current mA	nom. power mW	max. voltage V	max. current mA	max. power mW
VDDA	1.6	1100	1760	2.1	1300	2725
VDD	2.0	750	1500	2.5	1000	2500
HV	600	1	600	600	2	1200
Total power			3860			6425

Table 4.1: Supply voltages and current for a ATLAS pixel detector module as requirements on the power supply system [18].
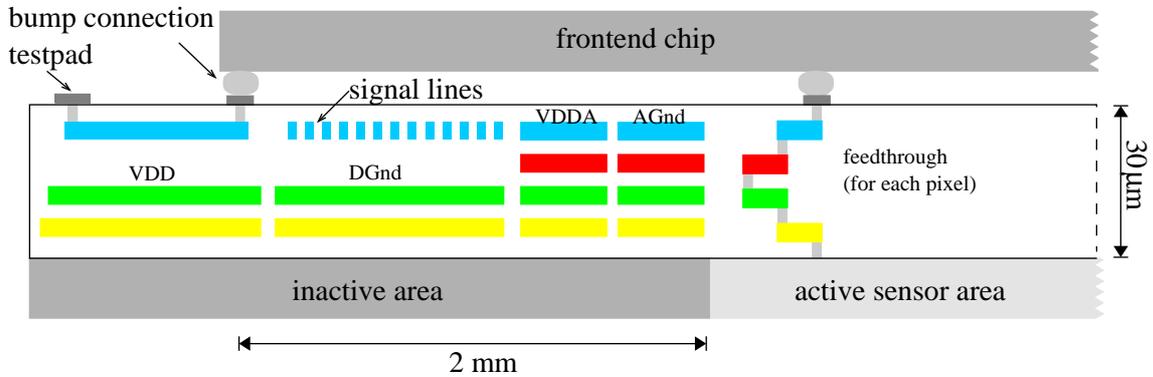
Figure 4.3: Schematic cross section of a MCM–D module.

principle be built underneath the inactive area of the frontend chips. It has been proven very useful to realize the module slightly larger, so that by building additional test pads each IO of the frontend could be contacted by probes after final assembly. Loading passive components on top of the module is not possible with MCM–D and one has to provide additional space for these as well as for the controller chip.

In the area of the pixel cells, one has to connect each of the sensor cells with the corresponding electronic cell through the MCM–D layers. Figure 4.4 shows a microscope image of a feed–through in cross section, including the PbSn–sphere for the bump connection, whereas Figure 6.11 on page 61 shows the basic design of such a feed–through.

4.3   Comparison of the Solutions

During the early phase of the development of the pixel detector both concepts, the Flex–Hybrid and the MCM–D technique were followed in parallel. MCM–D is a promising solution but lacks the large experience that has been achieved in other experiments with the Flex–Hybrid technique. A comparison of the systematic properties of both techniques is the topic of this section.
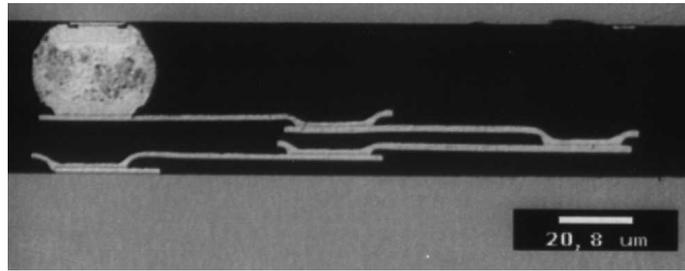
Figure 4.4: Photo of a cross section of a feed–through structure in MCM–D [IzM].

4.3.1 Disadvantages of the MCM-D Technique

It should not be neglected, that even the MCM–D technique has some disadvantages compared to the conservative solution:

- Increased size of a module. MCM–D modules are larger than flex–modules due to the need for space in order to place the controller chip MCC and the passive components.

- Reduced access to the interconnection system. Once the frontend chips are bonded to a MCM–D module, the module offers only reduced probing and debugging possibilities. The realization of probe pads for each frontend chip has proven to be very helpful, but it has to be considered carefully if the increase in size is affordable.

- Yield dependance. Defects in the thin film layer system of an MCM–D module lead most probably to the loss of the complete module. The possibility of realizing MCM–D is therefore dependant on a high yield.

4.3.2 Advantages of the MCM–D Technique

The main advantages of the Multi Chip Module Deposited technology compared to the Flex–Hybrid approach are:

- Bump bonding as the only interconnection technique is one of the major advantages the MCM–D technique offers, avoiding the delicate wire bond connections.

- High performance signal bus system. The properties of the data bus system realized in MCM–D are a very low crosstalk and well defined impedance (see Chapter 6) [42].

- Geometrical optimization of the sensor becomes possible. The investigation of the possibility to use feed–throughs to adapt between different sensor and electronic chip geometries is one of the major topics in this thesis. Chapter 6 describes this in more detail.

- Drastically increased manageability. As encapsulation of wirebonds is unwanted, a module with ~ 700 Al–wires of ~ 25 µm thickness is very fragile. A MCM–D module is very well manageable.

- Rework of chips after final assembly may be possible. This option was investigated (see Section 9.4 for details). It promises the option of a simple technique for chip replacement on a full module. With the Flex–Hybrid technology a replacement is possible during the phase of a bare module, before mounting the loaded flex kapton on the module.

- Reduction of assembly steps. Although a large number of processing steps are added by MCM–D, this refers to industrial processing techniques, that could be automated to a high degree. Assembly steps in the laboratories of the contributing institutes are eliminated to a large part.

4.4   Interconnection Technologies

Interconnection techniques like wire bonding and bump bonding are very broad topics; therefore only the basics will be summarized here.

4.4.1   Wire Bond Technology

Wire bonding is the widespread technique to contact a chip by welding a thin wire (10 to 100 µm Al or Au wire) ultrasonically to contact pads. The chip is usually glued onto the substrate with its structured side facing upwards. Reliability of the fragile connection is achieved by potting (encapsulating) the wire connection with epoxy or similar products and a distance in the range of a millimeter can be bridged with these technique. The Atlas flex–hybrid approach uses about 700 wire bond connections between the integrated circuits including the MCC and the flexible kapton circuit typically of 150 µm pitch. The position of contact pads is restricted to the border of a chip, eventually in two rows displaced by half of the pitch to each other.

4.4.2   Flip Chip Technology

In general Flip Chip technology refers to techniques where the chip is contacted with its structured side facing to the substrate. In comparison to wire bond techniques this offers the advantage of the possibility to equally distribute the chips' contacts over the complete chip surface, a must for the concept of a hybrid pixel detector, and the achievable contact density of this technology is superior. A variety of techniques is established to perform the necessary connection between contacts of the IC and the substrate. Bump bonding is one of these techniques, others are using anisotropic adhesives or tape–automated bonding. Bump bonding establishes the contact by a metal sphere between the contacts of chip and substrate. Different metal alloys are in use, e.g. PbSn or SnAgCu. Recent investigations were driven by the environmental requirement for a lead free technique. Based on the IBM C4 technology[4] [43], this technique has become a widespread application in consumer electronics. Ball grid arrays are an example of this technology.

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[4]IBM C4: **C**ontrolled **C**ollapse **C**hip **C**onnection

The ATLAS pixel collaboration anticipated a bump size of $\simeq 25\,\mu$m and a pitch of $50\,\mu$m. These requirements make high demands on the technology of choice. Two bump bonding techniques have been investigated and will be used in the experiment.

PbSn Bumping

With this technique lead–tin (solder) is deposited on dedicated pads of the integrated circuit. Mask printing is commonly used for that or electroplating in conjunction with photolithographic patterning, as in the case of the ATLAS Pixel project. A dedicated metallization has to be deposited first on the corresponding pads, the *Under Bump Metallization* (UBM). In the case of the ATLAS pixel detector, the UBM consists of a thin Ti:W layer serving as adhesion layer and diffusion barrier. Cu (sensor side) or Cu-Ni (chip side) of some micrometer thickness is the main interface material of the UBM. Furthermore a thin Au layer is deposited on the sensor side to prevent oxidation. The UBM serves as adhesion interface, avoids diffusion and guarantees long term stability of the metallurgical interface. The deposition of the UBM is followed by the galvanic deposition of PbSn on the integrated circuit side of the interface (Figure 4.5(a)). By melting the PbSn cylinders, the *reflow*, the bumps get spherical shape (Figure 4.5(b)).
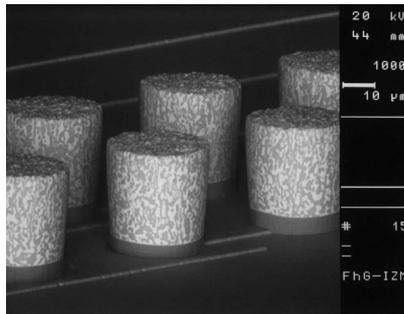
(a) PbSn Bumps after deposition.
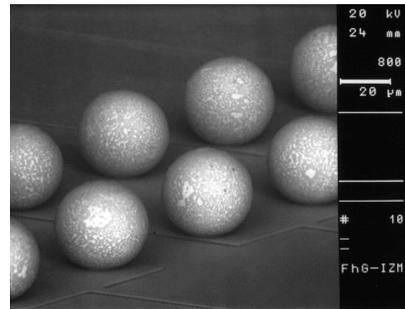
(b) PbSn Bumps after reflow.

Figure 4.5: PbSn Bumps before and after reflow [IzM].

Joining chip and substrate can be done in automated flip chip bonders, where aligning and placing takes place with subsequent transport to a nitrogen purged oven, where the second reflow is done, to bond chip and substrate. The surface tension of the fluid PbSn makes sure that the chip and the substrate are perfectly aligned, the *self alignment* of the PbSn process. In the case of the ATLAS pixel detector modules, all chips are placed on the substrate and bonded during the same thermic cycle.

Indium Bumping

Indium Bumping uses a Chromium layer as adhesion layer and diffusion barrier under an Indium layer of some micron thickness. The Indium is usually deposited by a sputtering

technique on a structured photoresist layer. By using a lift–off technique, the photoresist and excess Indium is removed, leaving cylindrical Indium remnants at the desired locations on a chip or a substrate wafer. The parts are later aligned, placed and bonded at 20 to 100 °C with dedicated pressure in the range of some gram per bump. The technology of Indium Bumping for ATLAS has been developed by AMS[5] and INFN[6], Genova [44].

[5] Alenia Marconi Systems, Italy.
[6] Instituto Nazionale di Fisica Nucleare, Italy.

Chapter 5

Experience with the MCM–D Technique

Together with IzM and IMEC, the University of Wuppertal has developed the first MCM–D module for the ATLAS pixel detector. MCM–D has long been an alternative for the production of the detector, although the technology suffered from the early stage of development.

After the baseline decision of the ATLAS pixel community to concentrate their worldwide effort on the more conservative solution of the ATLAS Flex–Hybrid option, it is the topic of this work to evaluate the opportunities the MCM–D technology can offer to future experiments.

In this chapter a summary of the experiences and results, that have been achieved so far, will be given.

5.1 Achievements in Developing MCM–D Modules for HEP Applications

The evaluation process of the MCM–D technology lead to the design of a high performance signal bus system in a micro strip configuration. Figure 5.1 shows a measurement of the transmissions–parameter S_{21} of early test structures. For our application the low frequency region of the plot ($\simeq 1$ GHz) is of interest, where crosstalk to neighboring lines is below -17 dB and the attenuation on such a 70 mm long line is -4 dB. A more detailed description is given in [35] and [45].

Other important aspects of the development of MCM–D technology for HEP application, that have been shown before, are:

- High reliability of via structuring in BCB and building the necessary interconnection structures in the pixel matrix, the feed–throughs. Measurements presented in [35] result in a failure rate of 8.13×10^{-6} for feed–through vias. A rate of 1.5 unconnected pixels per module is expected from that.
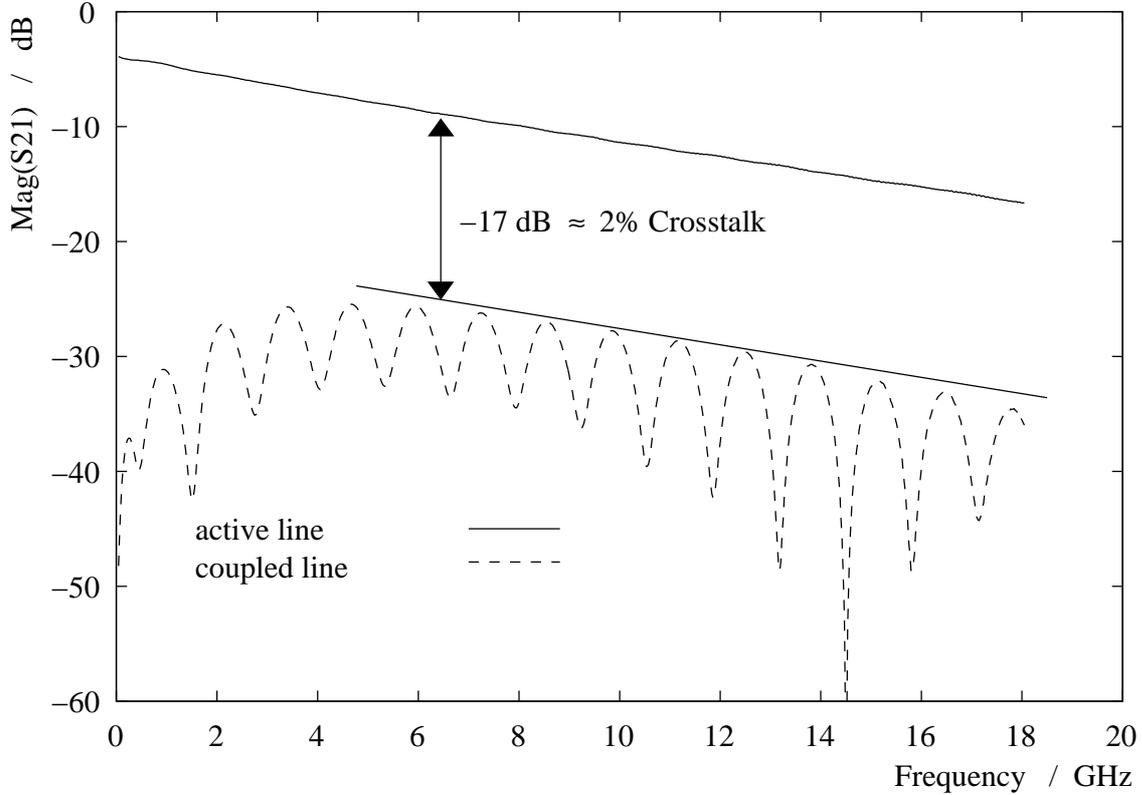
Figure 5.1: Attenuation and crosstalk of a 70 mm long pair of signal lines [45].

- Superior properties of BCB as dielectric layer. With an effective dielectric constant of $\epsilon_{r\,\text{eff}} = 2.65$ (1 kHz-20 GHz) BCB is a low–k dielectric [46]. The low moisture absorption of < 0.25 mass percent leads to high stability of the $\epsilon_{r\,\text{eff}}$.

- Radiation hardness of BCB to electron and proton radiation. Measurements presented in [35] show that after irradiation with $10^{15} \frac{electrons}{cm^2}$ at 40 keV energy and $5 \cdot 10^{15} \frac{protons}{cm^2}$ at 24 GeV the total change of $\Delta\epsilon_{r\,\text{eff}}$ was 3%. This effect is compatible with the expected effect of moisture absorption in the range of 0.25 mass percent.

5.2 First Prototypes using MCM–D Technique

Single chip hybrids with different MCM–D feed–through structures were built with front–end chip prototypes of the FE-B and FE-C generation [35,47–49]. These prototypes proved that feed–through structures do not significantly influence the front–end chip's performance.

A first MCM–D module[1] showed encouraging results presented in [50] and proved its suitability.

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[1] This generation could only be built with FE-B type front–end chips

5.3 Integrated Resistors in Thin Film Layers

An interesting possibility, when following the MCM–D approach, is the integration of passive components into the thin film layer system. This development is driven by the ongoing efforts of further miniaturization of systems in the industry.

The integration of NiCr resistors into a thin film layer system in a similar setup to the application of ATLAS modules was performed at IZM (BCB-NiCr-BCB-Cu) [51]. With courtesy of IZM samples of these resistors were cut from a wafer and irradiated at CERN (with 24 GeV protons to a total fluence of $1.12 \cdot 10^{15} \frac{protons}{cm^2}$). During the tests at IZM the 4 samples of 160 resistors each have been aged for 100 h at 125 °C. The value of resistance is between 10 Ω and 450 Ω with a resistor line width between 50 to 100 µm.
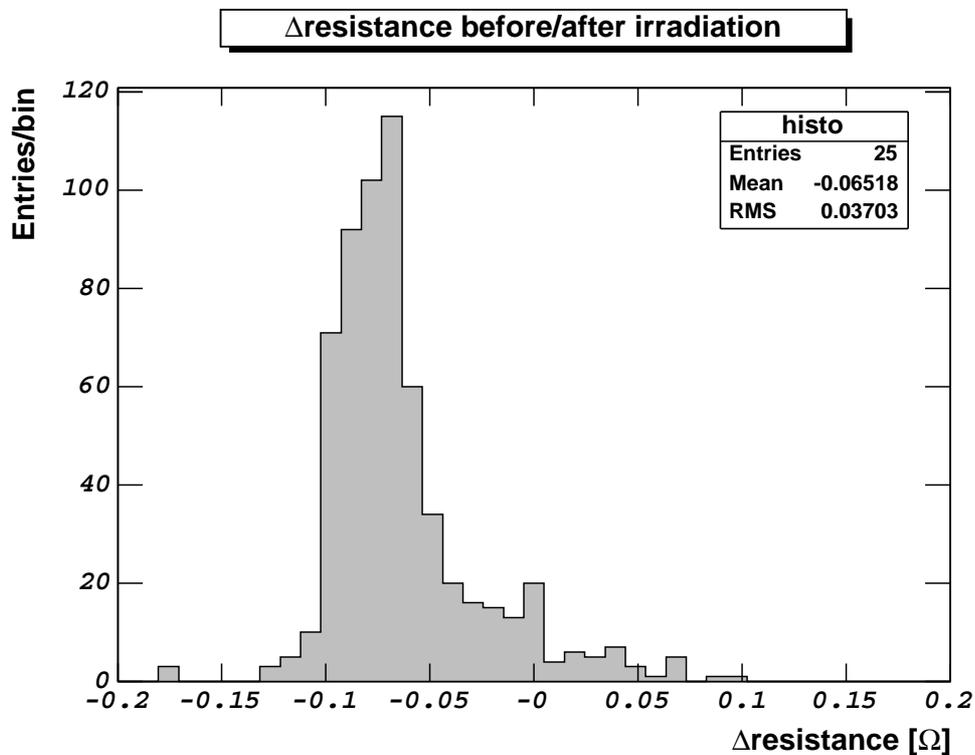
Figure 5.2: Difference of integrated resistors, before and after proton irradiation [52].

The difference in resistance before and after irradiation was measured by 4–wire measurements. The result is shown in Figure 5.2. The mean difference is below 0.1 Ω and is compatible to the uncertainty of the measurement.

5.4   Estimation of Yield Expectation

A major problem for failures during early MCM–D production runs, were impurities on
sensor wafers and other sources of defects leading to shortcuts in the power bus system
between Cu layers on top of each other. Figure 5.3 shows a layout which was designed at
Wuppertal and processed at IzM to get an estimation of the yield which one could expect
during a production of MCM–D modules.

This 2 metal layer design features two main areas on 4–inch wafers:

- 5 large structures for the investigation of breakdown voltage of BCB, the High Voltage
  Test (described in Section 5.5).

- The area for defect density estimation (close up in Figure 5.3(b)). This area is
  subdivided into 102 individual structures of 4 different shapes and sizes. These
  structures can be contacted by an automatic wafer–prober and the two metal layers
  of the structure are tested whether they are shortened or not.

(a) Design overview.

(b) Test structure for defect density estima-
tion.
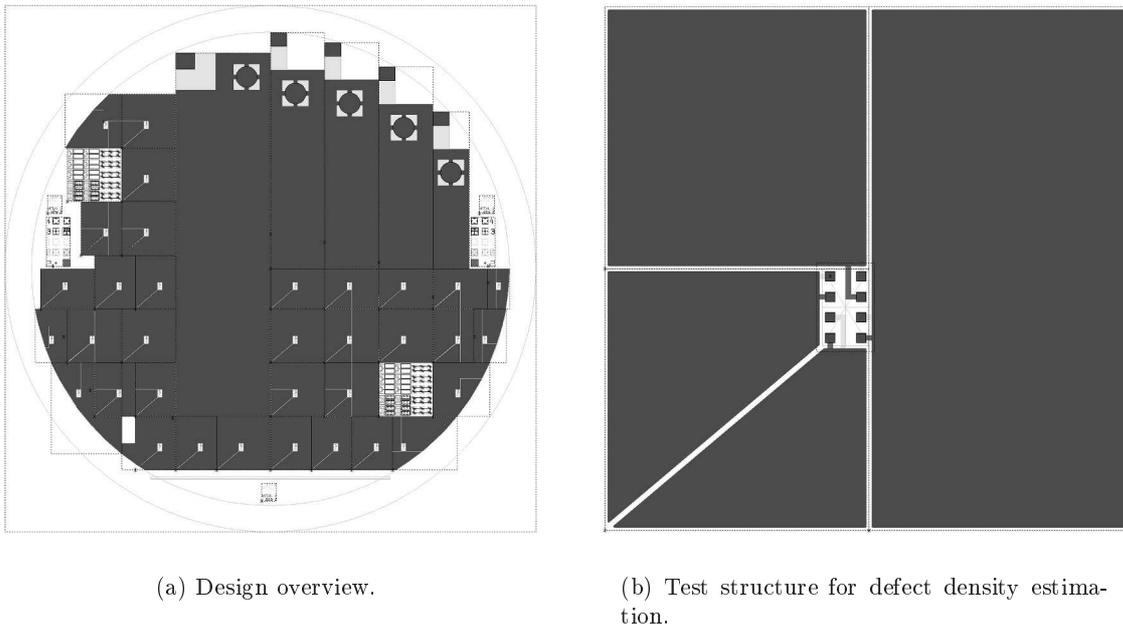
Figure 5.3: Layout of test wafer for high voltage and yield test.

A total of 16 wafers were processed in an ATLAS comparable layer configuration of a
unstructured 3 µm layer of BCB, 3 µm electroplated Cu layer, covered by 5 µm of BCB
and finally a Cu cover layer of again 3 µm. The results are summarized in Table 5.1.

The aim is to get a correlation between yield, Y, and the critical area A_{crit} of a module.
A_{crit} is defined to be the area where different potentials are organized in metal layers on top

of each other. Following the Poisson equation the expected yield in a simplified scenario is then [53]:

$$Y = e^{-\delta_{dens} \times A_{crit}} \qquad\qquad (5.1)$$

with:

Y: expected yield
δ_{dens}: defect density in defects/cm^2
A_{crit}: critical area of structure

Considering Table 5.1 on the following page one has to distinguish between structures dedicated to the High Voltage Test, labeled BT1 to BT5, and the structures covering the rest of the wafer in higher segmentation, which are labeled according to their geometrical shape and size. With the assumption of a single defect per structure when proving a shortcut, even in the case of BT–structures, one can calculate the number of mean defects per area D_i ($i = 1$ considering all structures, $i = 2$ considering only the Yield Test dedicated structures). D_i can serve as approximation of δ_{dens}. Another approach is shown in Figure 5.4. The measured occurrences of defective structures are used to calculate an estimation of the yield in dependance of A_{crit} and functions as shown in Equation 5.1 are fitted to the data points by minimization of χ^2. This was done for the complete set of data points leading to a defect density of $\delta_{dens,2} = 0.0805 \pm 0.0126 \frac{defects}{\text{cm}^2}$. The large statistical deviation of the BT–structures lead to a very low probability of the fit of below 5 %. With a probability of 70.1 % the defect density has been determined from a fit to the small area structures' data points to:

$$\delta_{dens} = 0.1013 \pm 0.0173 \frac{defects}{\text{cm}^2}$$

The more pessimistic results was chosen. One expects then a yield of 54.5 %, when assuming a critical area of 6 cm^2, like it was used in the very first process runs for MCM–D. The design presented in Chapter 6 thus aims to avoid critical area as much as possible. A pre design guideline was 0.5 cm^2, which seemed achievable, leading to a yield expectation of 95.1 % (see Fig. 5.4).

Note that the yield estimation uses several simplifications. It does not account for reworking localized defects and does not include any other defect source than shortcuts between metal layers on top of each other. The investigation of the exact nature of the defect was not possible, except the fact that systematic defects (e.g. at the borders of the metal structures) were ruled out. Nevertheless the yield test showed that the design target of the first production runs, where decoupling between the supplying potentials is achieved by *maximizing* the critical area, is not feasible.

Label	Area [cm^2]	Number	Total area [cm^2]	No. of defect	Yield [%]
BT1	11.71	16	187.36	6	62.5 ± 12.1
BT2	3.81	16	60.96	8	50 ± 12.5
BT3	3.61	16	57.76	2	87.5 ± 8.27
BT4	3.15	16	50.4	3	81.25 ± 9.76
BT5	1.52	16	24.32	5	68.75 ± 11.59
Rectangle 1	0.503	192	96.58	8	95.83 ± 1.44
Rectangle 2	0.249	400	99.6	13	96.75 ± 0.89
Rectangle 3	0.246	240	59.04	7	97.08 ± 1.09
Triangle	0.115	800	92	8	99 ± 0.35
$\sum_1$			728.02	60	
$\sum_2$			347.22	36	
D_1 [Defects/cm^2]				0.824	
D_2 [Defects/cm^2]				0.104	

Table 5.1: Investigation of Yield Expectation. D_2, quotient of totalized number of defects and totalized, can be used as estimation for the defect density. D_1 the same, but including the BT–structures.

5.5   High Voltage Isolation Test

The material property of the dielectric breakdown voltage of Photo–BCB is given to 300 V/µm by the manufacturer of Photo–BCB, the Dow Chemical Company [46]. Therefore the material is also suitable as an isolation layer against the sensor's bias voltage of up to 600 V, which is applied to the backside of the sensor wafer (referred to as the High Voltage). In the case of the ATLAS–Flex hybrid approach the High Voltage is underneath the flex kapton circuit, which features an isolation layer for that purpose. In the case of the MCM–D approach the High Voltage side will be glued onto the conducting carbon–carbon support structure.

Naturally the determination of the BCB breakdown voltage at Dow was based on small area investigations [54]. The High Voltage isolation test aims to examine the possibility of using BCB as isolation layer on a large area scale of several cm^2.

The design shown in Fig. 5.3(a) features 5 large structures (referred to as BT1 to 5) with one even of the approximate size of a full module. All these structures are designated to the High Voltage test. The layout foresees a similar layer configuration like it was described in the last section of the defect density estimation, with the following differences:

- the underlying metal layer is supposed to be as flat as possible, thus only being a sputtered metal layer.

- the thickness of BCB was varied to 5 µm and 8 µm.

A very first run suffered from a mask defect, which lead to an unexpected opening in the isolation layer.
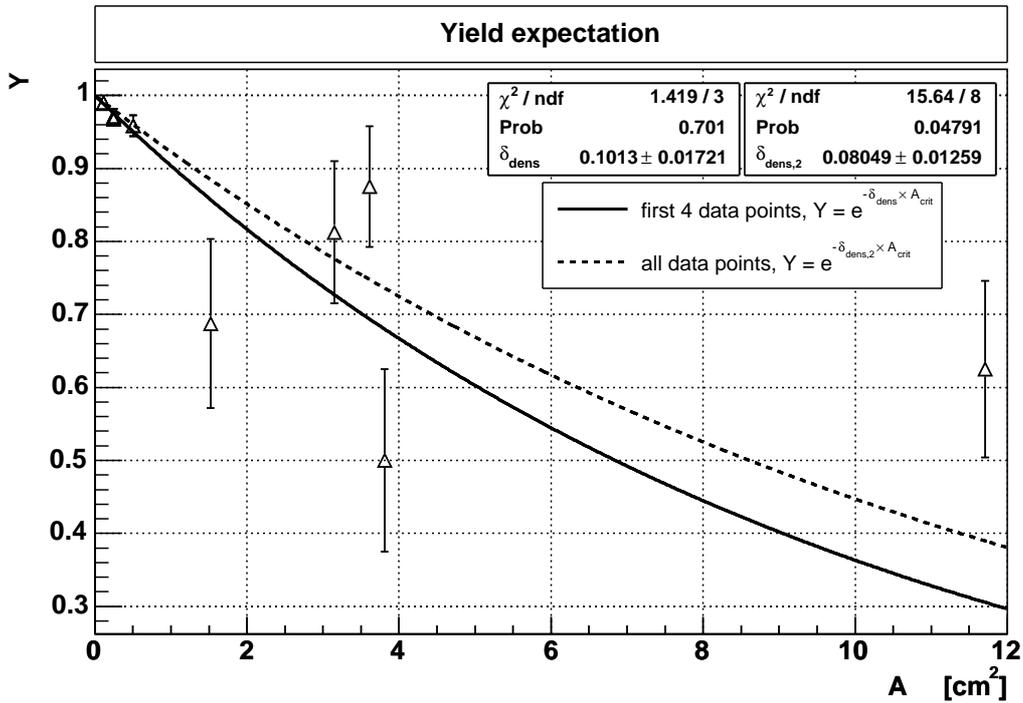
Figure 5.4: Yield expectation based on estimation of defect density between electroplated Cu layers.

The measurement of the breakdown or the isolation property itself was performed by applying a voltage (DC) to the buried Cu layer and by grounding the Cu layer on top. The voltage was raised until either a dielectric breakthrough or reaching 1 kV. Further defect investigation was not possible, due to the destructive nature of the test.

The results are summarized in Table 5.2.

The requirement for the ATLAS pixel detector is a reliable isolation against up to 700 V. While on the one hand the results of the tests indicate the high breakdown property of BCB, the reliability of the isolation is yet unsatisfactory. Not accounting the shortcuts to neighboring structures under 700 V, which were introduced by a design error leading to electric flashover to neighboring structures, a total of 56 % of the structures do hold the 700 V and more. A dependance on the thickness of the isolating BCB can not be determined. The thinner layer of 5 µm shows an even higher reliability (72 %) than the 8 µm BCB layer (43 %). This indicates that not the isolation property of BCB itself is the source of the large fraction of breakthroughs. Other sources can be: particle contaminations or scratches on the wafer reducing the effective isolation thickness and particle contaminations during processing or during exposure, which would lead to unintended openings in the BCB layer. The planarity and cleanliness of the sensor wafer's backside is expected to be superior compared to the underlying layer of the High Voltage test wafers.

These studies have given reason for expecting the MCM–D technology to be able to

Wafer	BT1 11.71 cm^2	BT2 3.81 cm^2	BT3 3.61 cm^2	BT4 3.15 cm^2	BT5 1.52 cm^2
Run 2001-26, BCB=5 µm					
w47183	short	> 1 kV	> 1 kV	700 V	630 V (x)
w47184	260 V	> 1 kV	950 V	850 V	730 V (x)
w47185	850 V	850 V	1 kV	600 V	600 V (x)
w47186	310 V	700 V	1 kV	1 kV	550 V
Run 2001-53, BCB=8 µm					
w47064	short	short	390 V	short	550 V (x)
w47065	420 V	> 1 kV	short	1 kV	550 V (x)
w47066	240 V	250 V	295 V	960 V (x)	720 V (x)
w47068	short	870 V	short	short	830 V (x)
w47069	290 V	> 1 kV	> 1 kV	840 V	730 V (x)

Table 5.2: Breakthrough voltages (x: breakthrough to neighboring structure)

build Pixel Detector Modules for High Energy Physics, when design and production process are further enhanced.

Chapter 6

The MCM–D Design for ATLAS

The design of the MCM–D thin film interconnection layers is based on the geometries of the sensor, serving also as the basis of the thin film build up, the front–end chips and the controller chip MCC [55]. Passive components are commonly available and can be chosen out of a great variety.

The optimization of the basic components for the ATLAS pixel detector application implicated several drawbacks for the development of MCM–D modules in parallel. But it should also be pointed out that without the support of the ATLAS pixel collaboration this work would have been impossible. For example, the additional IO bump connection of the front–end chips and of the MCC (all DSM designs) were especially dedicated for the MCM–D application.

During the technology transfer of the ATLAS readout chips from the first non–radiation hard prototypes (FE–A,FE–C and FE–B) to a radiation hard process, the design of the next generation of MCM–D modules, the second MCM–D design, took place. This anticipated second design of thin film structures was dedicated to the DMILL[1] processed FE–D (and FE-D2) prototypes, but the necessary mask production was halted until these readout chips were tested.

With the delivery of the chips it soon became clear that their performance could not meet the requirements of ATLAS. A redesign from FE–D to FE–D2 could not improve the performance adequately. The change to deep submicron technology inflicted serious time efforts for the collaboration and through massive changes in pinout and the powering scheme a complete new design became also necessary for MCM–D. In that way the actual MCM–D design directly became generation three, while design 2 has never been realized. This MCM–D design fits the pinout of FE–I and the following generations FE-I2 and FE-I3.

6.1 Elements of the Prototype 2.0 Sensor Wafers

Figure 6.1 shows an overview of the ATLAS Prototype 2.0 sensor wafer. These 4 inch sensor wafers were designed with special focus on the MCM–D option.

Main elements are:

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[1] Durcie Mixte sur Isolant Logico-Lineaire.
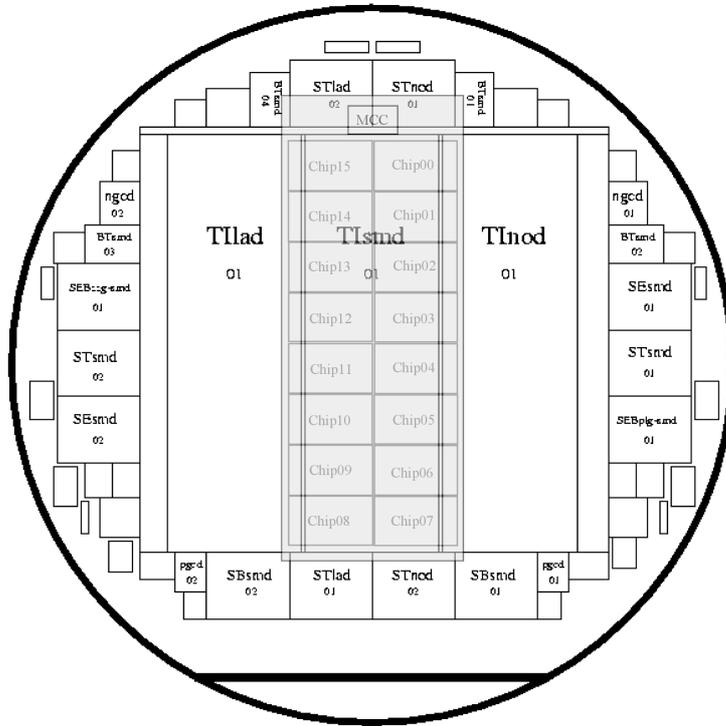
Figure 6.1: Elements an the ATLAS prototype 2.0 sensor wafer.

- the large sensor tiles for building of modules, labeled "TIlad","TIsmd" and "TInod", featuring different implementations of the technique to contact all pixel cells via the bias grid. The pixel cell implementation itself follows the concept of a "small gap" design (SSG–design), the baseline choice for the ATLAS pixel detector.

- Single chip sensors in different designs, labeling starting with "S". These will be explained below in more detail.

- Structures labeled "BTsmd", which are designed for the special geometry of 63×12 pixel cells of the B&P chip.

- Alignment marks and test structures. Alignment marks for bump bonding are also used for the alignment of the MCM–D masks.

It is noteworthy that the production sensor wafer of ATLAS is identical to the Prototype 2 wafer in two major points: the alignment mark position for bump bonding and the passivation openings for the central tile structure. This gives the theoretical possibility of MCM–D module production with the final production sensor wafers of ATLAS.

6.1.1 The Module's Sensor

As a MCM–D module is slightly larger than a standard ATLAS module, only the centered tile labeled "TIsmd" can be used for MCM–D module production. The outline of the MCM–D module is also sketched out in Figure 6.1. This implicates one of the difficulties inherent to the compromise solution of not using dedicated wafers for MCM–D: the prepared dicing streets for singulating the three tiles of the wafer will be right underneath the critical bus system area of the MCM–D module. The dicing street represents a grid of non–isolated Al traces covering the complete sensor.

The design of the centered tile is identical to the baseline choice for the pixel detector of ATLAS.

6.1.2 Single Chip Sensors

A total of 6 single chip sensors can also be used for MCM–D applications. These sensors provide an active area of 8.2 mm × 7.6 mm, corresponding to 1/16 of a module and read out by one front–end chip. Single chip sensor structures above and below the tiles (Fig. 6.1) will be partly overlapped by the MCM–D module and thus cannot be used. Although the module tiles could not especially be adapted to the MCM–D needs, four of the remaining single chip sensors are. These single chips feature three different designs: an "equal–sized" and two "equal–sized–bricked" designs with different implementations of the bias grid. Figures 6.2(a) and 6.2(b) show the design metallization layer (black) and passivation openings (grey) of the two bricked designs (see also in [49]).
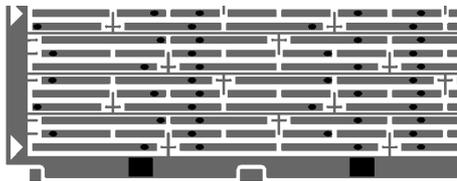
(a) Parallel bias grid implementation.
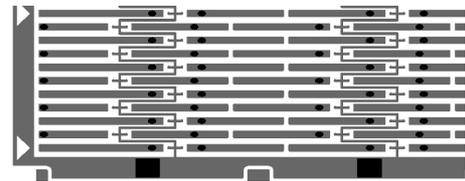
(b) Zigzag bias grid implementation.

Figure 6.2: Equal–sized–bricked single chip sensor designs on ATLAS Prototype 2 wafers (rows $0 - 10$, column 17 at left).

A summary of all single chip sensors, which can be used for MCM–D applications is given here:

- two standard ATLAS pixel sensors (STsmd 01 and STsmd 02). These feature a total of 2880 sensor cell contacts and follow the geometry described in Section 3.3.1, including the additional region necessary to cover the interchip regions on a module. Categories of different pixel are (see Fig. 3.6 on page 25):

  - $156 \times 16 = 2496$ pixel with standard size of $50 \times 400\ \mu m^2$ (row 0-152/154/156/158 and column 1-16).

- $156 \times 2 = 312$ elongated pixel cells (referred to as *long* pixels) of $50 \times 600\,\mathrm{\mu m}^2$ size (row 0-152/154/156/158 and column 0/17).

- $4 \times 16 = 64$ pixel cells with two standard sensor cells connected together in the sensor metallization layer (referred to as *ganged* pixels) of $2 \times 50 \times 400\,\mathrm{\mu m}^2$ size (row 153/155/157/159 and column 1-16).

- $4 \times 2 = 8$ pixel cells with two long sensor cells connected together in the sensor metallization layer (referred to as *long–ganged* pixels) of $2 \times 50 \times 600\,\mathrm{\mu m}^2$ size (row 153/155/157/159 and column 1/17).

Just a total of $86.67\,\%$ of all electronic channels of the pixel detector are of standard size, corresponding to a fraction of $82.16\,\%$of the geometrical area.

- The equal–sized design option, realized in structures SEsmd 01 and SEsmd 02, features 2880 pixel cells of $51.25 \times 422.22\,\mathrm{\mu m}^2$. Due to the deviating geometry, compared to the electronic chip, a routing between the contact to the sensor (the passivation opening) and the readout chip's contact (the bump position) becomes necessary.

  This solution promises a very homogeneous detector performance and advantages in track reconstruction.

- The equal–sized–bricked design with parallel bias grid is realized in the structure labeled SEBplg–smd 01. In comparison to the equal–sized design, the sensor cells are shifted in the long direction of the sensor cell by $\pm 1/4$ cell size ($-1/4$ for even row numbers, $+1/4$ for odd row numbers). Shifting the sensor cells increases the resolution of the sensor in the case of double hits, when a particle causes two pixels to fire, which are in neighboring rows. The drawback of reintroducing different cell sizes in the first and last column (3/4 resp. 5/4 standard cell size) of the sensor would be relevant only for the first and last column of a full module and not for each front–end chip area as in the standard approach.

  The bias grid needs to reach close to each pixel cell, so that by applying a small voltage to it, a punch–through contact to the sensor cell metallization can be achieved. A metal trace runs parallel to the long direction of the pixel cells between every third row.

- The equal–sized–bricked design with zigzag bias grid is realized in the structure labeled SEBzzg–smd 01. It is very much the same than SEBplg–smd 01, except that the bias grid follows almost the same way than a standard chip. It has to follow the brick wall structure of the pixel cells and therefore runs in a zigzag pattern through the pixel array.

6.2   Design Layer Description

Table 6.1 gives a detailed overview of all layers that have been used during the design of the MCM–D thin film layers. A total of 14 layers were used for the layout. Corresponding masks have been produced by Image Technology[2] as 5 inch clear or dark field masks. Three

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[2] Image Technology Inc., Palo Alto, USA

different top metallization layers were used for the different purposes of mounting passive components by soldering, bump bonding the electronics chips and realizing additional rigid testing pads for the front–end chips' IOs with the backup option of wire bonding. The latter has also been realized as individual mask, while the former two were merged into the same physical mask for the reason of process simplification. Each additional processing step, which are several for the processing of each layer, leads to increased processing time, costs and risk (see next chapter for details on this topic esp Section 8.2 on page 80) and thus should be avoided.

6.3   Design Rules

Design rules for MCM–D have been developed over several years of collaboration between the University of Wuppertal, IMEC and IzM. In most of the following points the currently available technology has been driven to the actual maximum:

- Line width and gap. 15 µm minimal width of metal lines and 15 µm minimal gap between metal lines where used during the design phase. This requirement originated in the very dense routing scheme in the Equal–sized(–bricked) single chip design.

- Minimum via spacing has been reduced to 17.5 µm between adjacent layers and kept to 20 µm between vias in the same layer.

- Via diameter. Mostly elliptic vias are used with $25 \times 30 \ \mu m^2$ diameters. One exception is the topmost BCB layer, the passivation or isolation layer. In this layer, one is governed by the size of the bump pads. These should be kept as close as possible to the standard ATLAS solution to rule out technological process differences. A diameter of 22 µm is used for these openings to guarantee some security overlap with the bump pad of 27 µm diameter. As the topmost layer should be realized thinly, this size reduction seems appropriate.

- Staggered edges. As has been shown in [52] the metallization thickness tends to grow towards the edges of an area. To avoid superposition of this effect the borders of metal shapes are not placed directly on top of each other. As a drawback this leads to reduced available cross sections in higher metal layers.

- No pointed edges. During the electroplating process (described in chapter 7) an electric potential is applied to a thin metal layer serving as the *plating base*. To avoid discontinuities and extreme values it is avoided to use sharp *pointed* edges. Wherever possible a minimal corner radius is applied to edges during the design.

- The power bus cross section has to be outlined as large as possible. The gap between this relative massive copper structures was put as low as 30 µm to reduce the dead area.

- Minimization of decoupling. It has been shown [47] that a crossing of copper lines in adjacent metal layers should be avoided in the area of the pixel matrix to reduce signal losses due to cross coupling.

#	Name	Mask	Type	Function	Description
1	PN_M			reference	sensor metallization
2	PN_P			reference	sensor passivation openings
10	BCBA	BCB1	-	design	cover of sensor, openings to contact the sensor
12	META	MET1	+	design	main power supply layer 1 and contact layer to sensor
14	BCBB	BCB2	-	design	intermediate dielectric layer, connections between META and METB
16	METB	MET2	+	design	main power supply layer 2 and mirror GND plane for the signal bus
18	BCBC	BCB3	-	design	intermediate dielectric layer, connects METB and METC
20	METC	MET3	+	design	interconnection layer to power and signal bus
22	BCBD	BCB5	-	design	intermediate dielectric layer, connects METC and METD
24	METD	MET4	+	design	signal bus layer and via lands to contact layers
26	PASSIV	PAS	-	design	cover layer of thin film layers, openings to contact layers
28	WB_PAD	WIRE	+	design	contact layer 1, pads for wire bonding
30	BB_PAD	UBM	+	design	contact layer 2, pads for bump bonding
32	S_PAD	UBM	+	design	contact layer 3, pads for soldering passive components
34	NICR	NiCr	+	design	experimental layer for integrated resistors
36	BCBBACK	Backside	-	design	backside protection of the sensor, contact openings for bias voltage
50	FE_PAS			reference	front–end chip/MCC passivation openings
62	TEXTA			sketch & text	sketch and text layer
63				sketch & text	sketch and text layer front–end chips/MCC
64	TEXTB			sketch & text	additional sketch and text layer (never used)

Table 6.1: The definition of layers for the MCM–D design.
"+": structures are drawn — clear field mask;
"-": openings are drawn — dark field mask.

- Minimization of critical area. As shown in chapter 5 the critical area on a module has to be as low as possible to reduce sensitivity to the incorporation of defects during the process.

This variety of design rules, partly in competition with one another, has lead to the very sophisticated design presented in this work.

6.4 MCM–D Single Chips

Of the three types of single chips, the standard single chips (STsmd) are designed easiest, as they are a repetition of the module's standard feed–throughs and the front–end chips will directly fit onto the sensor, even without MCM–D structures in between. The geometrically optimized devices of equal–sized and equal–sized–bricked are a greater challenge, from the design point of view.

(a) Geometries of standard single chip sensor and front–end chip.

(b) After flip chip. Note the enlarged interchip region of 200 μm

(c) Geometries of equal–sized single chip sensor and front–end chip

(d) After flip chip. Note the distance between bump and sensor contact.
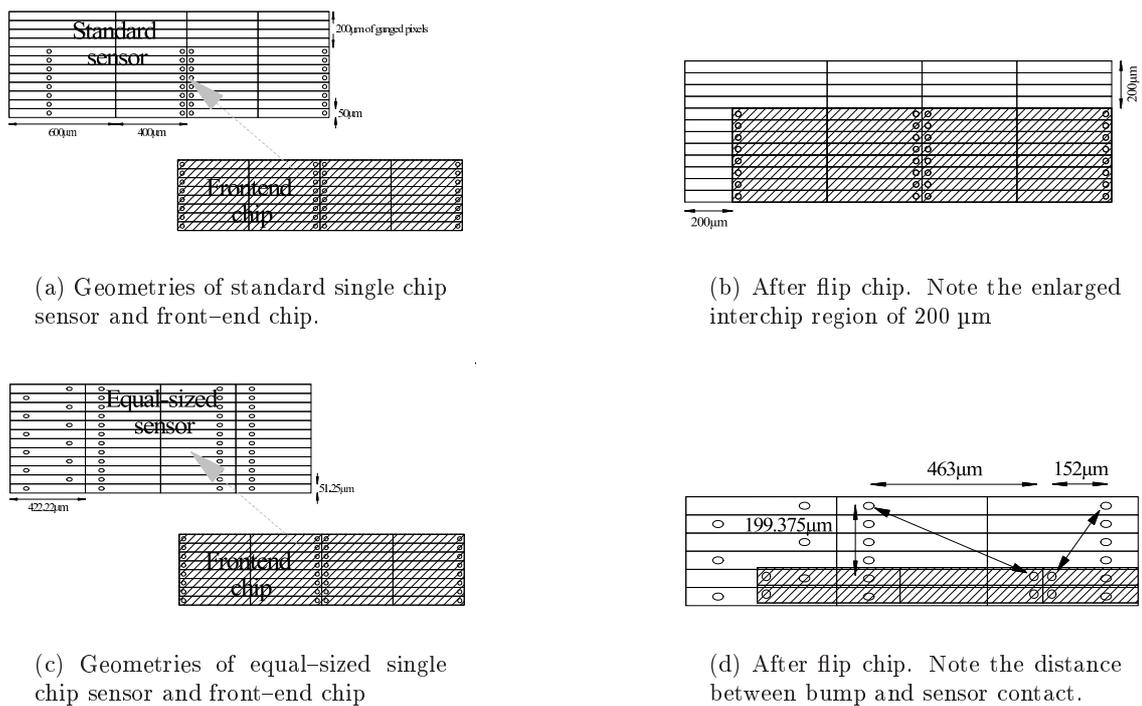
Figure 6.3: Geometries of different single chip sensors in comparison to the front–end chip. Detail view of upper left corner (front–end chip rows 142–159 and columns 17–14).

As shown in [47] crossing of Cu–lines should be avoided especially in metal layers directly on top of each other. An additional difficulty is to minimize the overlap of routing structures over the bias grid metallization to minimize signal loss due to coupling to the sensor structures. This has led to the attempt of realizing the main routing in one metal plane only (METD).

6.4.1   Equal–sized Single Chips

Each contact between readout chip and sensor has to cover a distance x_i, which is dependant on the column number and a distance y_i, which is dependant on the row number of the pixel cell. The maximum angle α_{max} that a routing structure can be designed to have is defined by the line width and gap restriction of 15 µm and 15 µm (see Fig. 6.4). With a contact pitch of 50 µm one calculates:

$$\alpha_{max} = \arccos(d_{min}/50\,\mu m = \arccos(30\,\mu m/50\,\mu m) = \arccos(0.6)$$
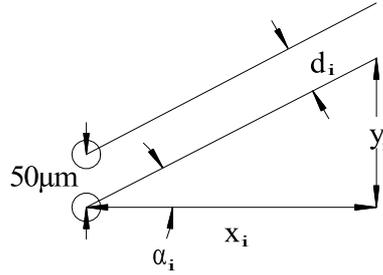
Figure 6.4: Routing scheme explanation for equal–sized(–bricked) single chip sensors.

The distance $y_i = (i + 0.5) \times 1.25$ µm ($i = row = 0 \ldots 159$) is covered by the routing in METD, so that the distance in x can be covered by a staggered structure through the lower metal planes, similar to Figure 6.11. This gives a maximum distance of 199.375 µm, for the topmost routing of pixel 159 and together with the maximum angle defines also the maximum distance in x.

$$x_{max} = 0.6 \times (y_{max}/\sin(\arccos(0.6))) \simeq 149.5\,\mu m$$

These considerations are valid for both designs: the equal–sized and the equal–sized–bricked single chip sensors. For the equal–sized option it was decided for reasons of a simpler design to keep the routing's end point at x_{max}, while changing the angle of the routing structure along a column.

$$\alpha_i = \tan(y_i/x_{max}) = \tan((i + 0.5) \times 1.25/149.5)$$

with:

i:	index along a column = row number $= 0 \ldots 159$
α_i:	angle of the routing structure in METD of row i
x_i:	covered x–distance of the routing structure in METD of row i
y_i:	covered y–distance of the routing structure in METD of row i
d_i:	distance between routing structures of row i and i + 1 (approx.)

A gap/width change of the structures from the "safe" 20 µm/20 µm to 15 µm/15 µm can be done at row number 90. The equal–sized single chips' design is symmetric to the axis between column 8 and 9.

6.4.2 Equal–sized–bricked Single Chips

The equal–sized–bricked single chip sensor design has to be adapted for the alternating x–position of the sensor contacts due to the bricking. Following the basic description of the equal–sized design considerations, the choice for the bricked designs was to keep the angle constant at its maximum value and decrease the length of the pixel's routing in METD to cope with the sensor contact position in y.

$$x_i = 0.6 \times \frac{y_i}{\sin(\arccos(0.6))} = 0.6 \times \frac{(i + 0.5)1.25\mu m}{\sin(\arccos(0.6))}$$

The gap/width of 15 µm/15 µm becomes necessary over the complete column, as well as an individual adaption of each pixel for the further routing to the sensor contact. In Chapter 7 some pictures of the finished structures underline the complexity and density of these designs. Figures 6.5(a) and 6.5(a) illustrate the two routing schemes. Where crossing of lines is visible it has been done in non adjacent metal layers.

6.5 MCM–D Module

The module itself can be divided into four parts: the pixel matrix with 46080 feed–through structures in the standard configuration (see Fig. 4.4 on page 35), the area under the front–end chips' End of Column logic (EoC), where the bus system is situated and the two balconies. Figure 6.6 shows a sketch of an MCM–D module without front–end chips. Dimensions of the pixel matrix and the surrounding inactive areas are also given in the sketch. Compared to MCM–D modules of former generations, these prototypes are significantly reduced in size, mostly thanks to the smaller layout of the MCC.

A short description of the main areas of the MCM–D module from the design point of view will be given here. Figure 6.7 shows the complete design of the module.

6.5.1 Main Balcony

The main balcony is dominated by the MCC and passive components, like capacitors and resistors. The complete list of parts to be contacted in the region of the main balcony is:

- the Module Controller Chip, MCC. This design is done for the first Deep Sub-Micron generation of the MCC, the MCC–DSM. This chip has a design size of $6.38 \times 3.98 \, \text{mm}^2$ and features a total of 93 IO pads. During the evolution from the former generations of the MCC, the design was changed in a way that the IO pads were concentrated on three side of the die, in a "U"–type manner. Pads on the fourth side remained only due to compatibility reasons to former designs and are thus called the *AMS–compatibility* pads. These pads were used for MCM–D, to keep a more uniform contact distribution during the flipchip process.

(a) Routing structure over a column of equal–sized single chip sensor.

(b) Routing structure over a column of equal–sized–bricked single chip sensor.
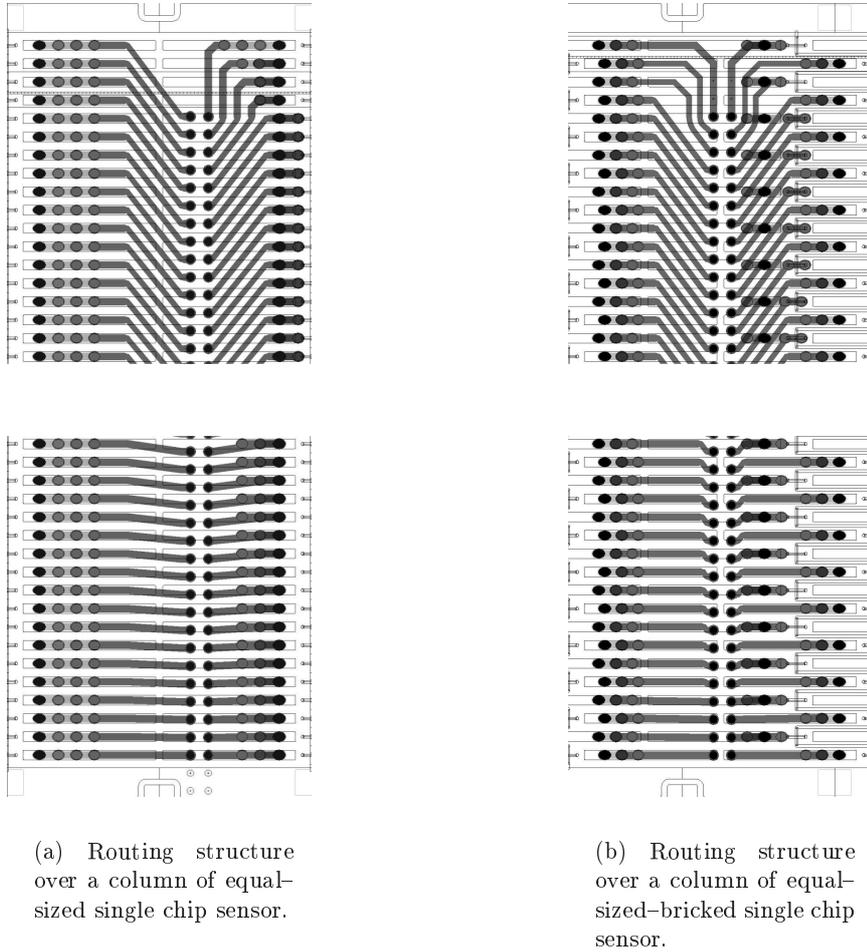
Figure 6.5: Comparison of equal–sized and equal–sized–bricked designs.

- A resistor array of 4× 100 Ω in a 0408 case size of $\simeq 2 \times 1\,\mathrm{mm}^2$ size. This array is used as the termination of the four multi drop LVDS signal lines of the signal bus system (SYNC, XCK, STRO, LV1), which is used for fast signal transmission between MCC and the front–end chips.

- Decoupling capacitors. A total of 5 decoupling capacitors of 100 nF in 0402 case size is foreseen on the balcony. One per potential per module side and one additional for the additional MCC supply voltage.

- The NTC thermistor, responsible for monitoring the module's temperature. The NTC is a 10 kΩ precise thermistor in a 0603 case. These NTC thermistors were qualified for the ATLAS experiment and these shall also be used on MCM–D prototypes.

- The contact area of the module's pigtail. With this generation of MCM–D modules an ambitious step of development shall be done in contacting the module. As former module prototypes have been contacted to a PCB by wire bonding, it is desirable to
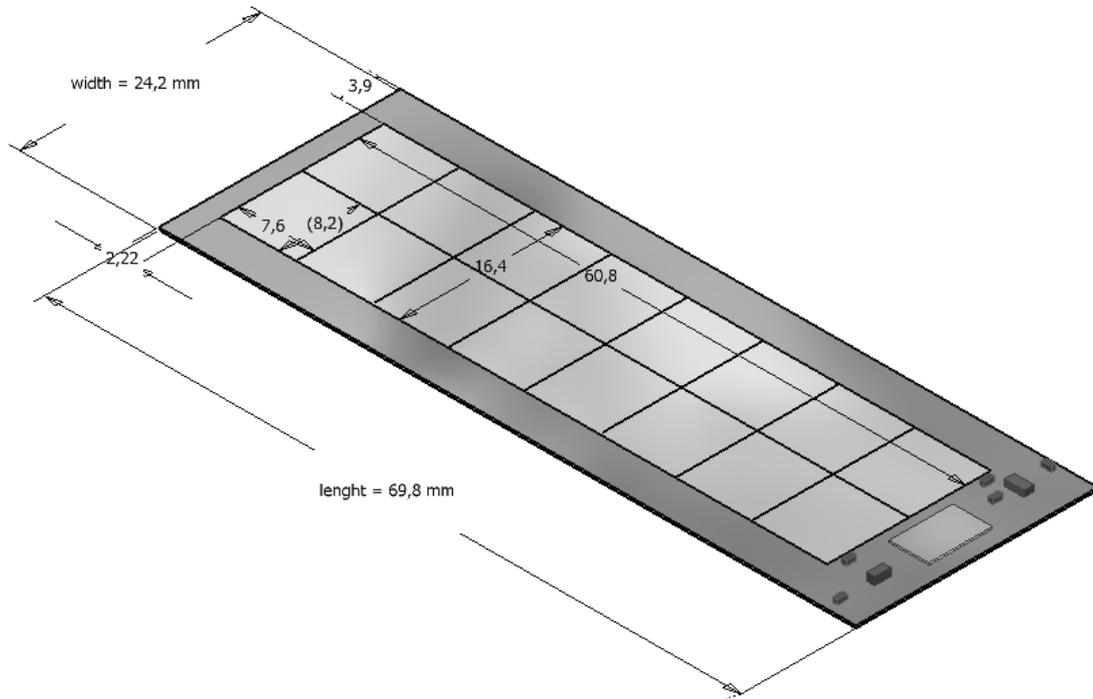
Figure 6.6: Drawing of a MCM-D module. Front–end chips are hidden. Dimensions of active and inactive areas of a MCM–D module are given.

achieve an advanced solution. All data lines, clock, supply voltages and monitoring should be connected via the main balcony to a dedicated flexible circuit, the *pigtail* (see section 7.6 on page 76 for details).

6.5.2 Signal and Supply Bus Design

As described in Section 4 the main purpose of the MCM–D thin film layers is building the signal and power distribution bus system. DGnd will be distributed below the signal bus system, acting as the mirror plane, and all potentials will be designed side by side following the results of Chapter 5. The width of the signal bus system is given by the necessary signals (29 in total), each in a 20 µm/30 µm line width/gap configuration. An approximation of a step compensating contact design has been chose to adapt steps in the width of all signal lines [56]. While the DGnd plane is also limited by the bump connection pads of the front–end chips, only a very limited space between the DGnd plane and the pixel matrix is available for the analog supply with AGnd and VDDA (750 µm in total).
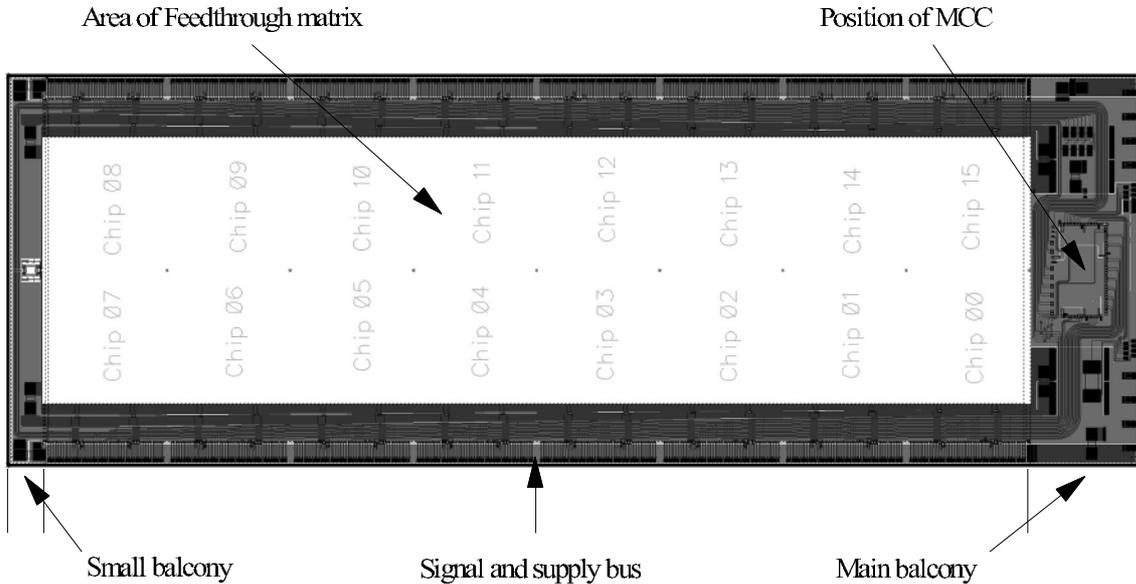
Figure 6.7: Design of the MCM-D module, (3rd generation/design).

Although all 4 metal layers can be used for the analog supply. Figure 6.9 shows that part of the module design.

Including the necessary gaps between the power distribution planes, which have been reduced to 30 µm at the MCC side of the module, and a distance of 20 µm to the bias grid, a total of 335 µm is available for the two analog supply lines. The available space increases along the long side of the module as each front–end chip's point–to–point LVDS signal to the MCC reduces the signal busses width by 100 µm, when reaching the corresponding IO. However the gap between the power lines is increased to 50 µm along the module's side.

6.5.3   Feed–throughs

The module's feed–through structures are designed to connect sensor and electronic cells in the most simple way, as described in Section 4.2. Figure 4.4 shows a feed–through of earlier versions in the cross section. These are used in the new design almost identically. Figure 6.11 shows the layout of the new generation in a schematic cross section and a top view.

6.5.4   Small Balcony

At the main balcony's opposite small end of the module, the small balcony (see Fig. 6.12) gives room for the additional placement of decoupling capacitors for the supply voltages. This is a backup solution if additional decoupling seems necessary. This side of the module serves mainly two other purposes: the routing of the four multi drop LVDS–signals to the left side (chips 8–15) of the module and contacting the power bus system during the processing to check for shortcuts between the power traces. This is usually done by
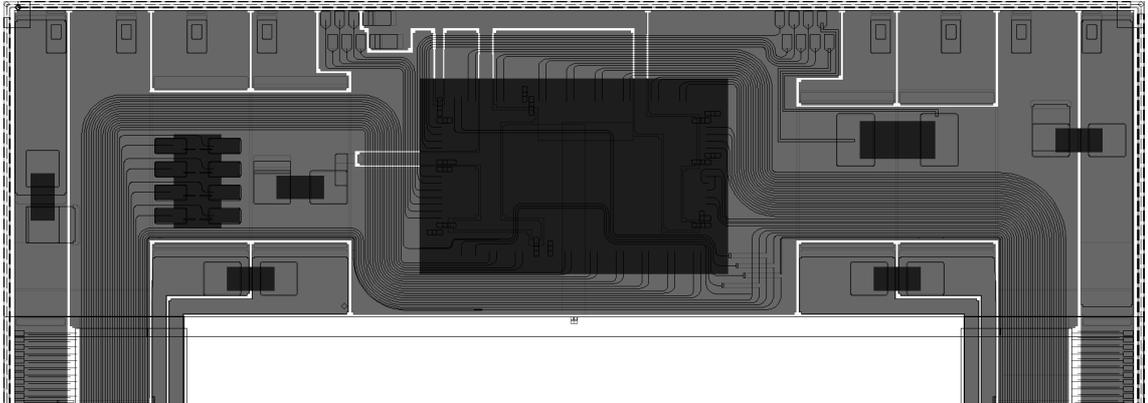
Figure 6.8: Main balcony of the MCM–D module.

probecard after the deposition of a metal layer. In our case sixteen contacts are provided, which allow redundant probing of each supply line of each module side. Note that the left and right side potentials of the module are divided. DGnd as an exception is connected between the left and right side on the main balcony for the reason of MCC stability. Although the possible potential difference at the small balcony between the left and right side of the module might lead to unsteadiness in the DGnd mirror plane, a second connection between both sides could build a ground loop and lead to resonances. As the concerned range of frequency is quite low 40 MHz system clock, the latter could lead to more serious problems and therefore the potentials are kept divided here.
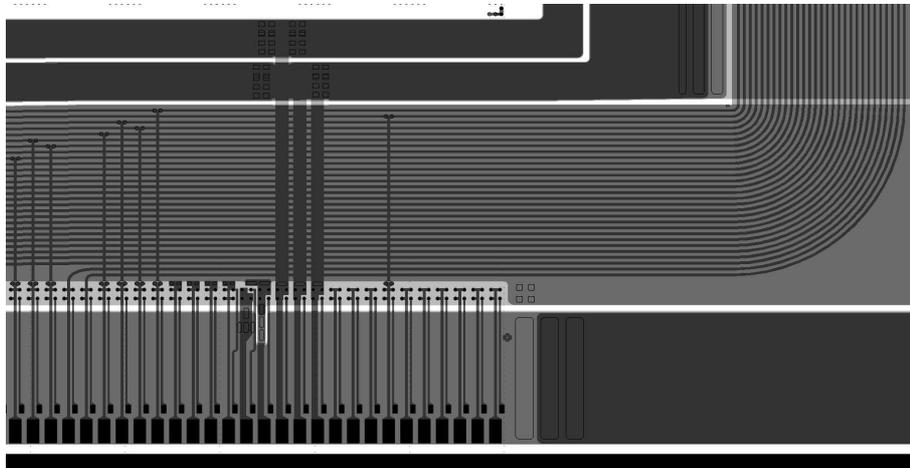
Figure 6.9: Design picture of the bus system. On top a part of the pixel matrix is visible, on the right side the signals are coming from the MCC. Note the direct MCC - FE–chip LVDS connection visible on the left side.
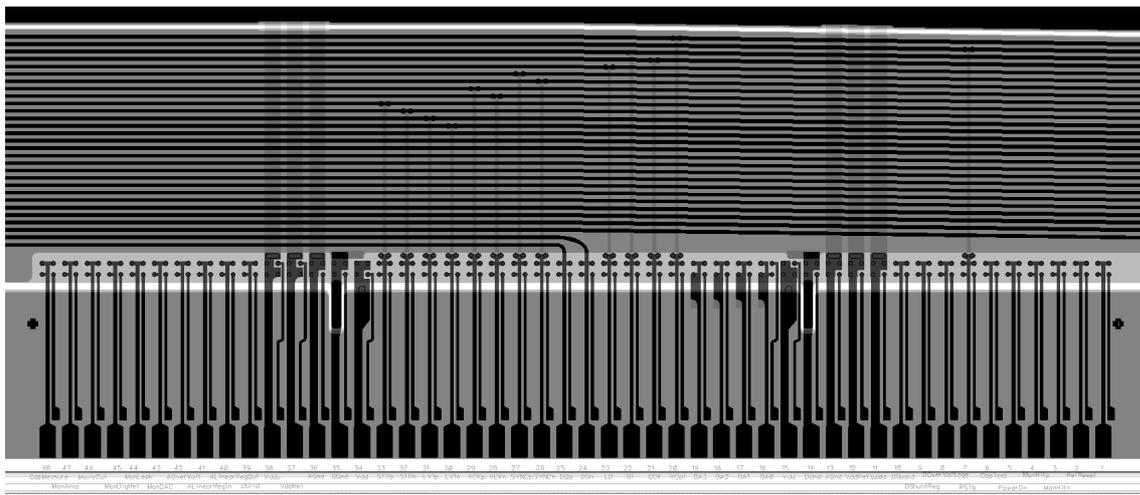
Figure 6.10: Design picture of a front–end chip's IO area in MCM–D.
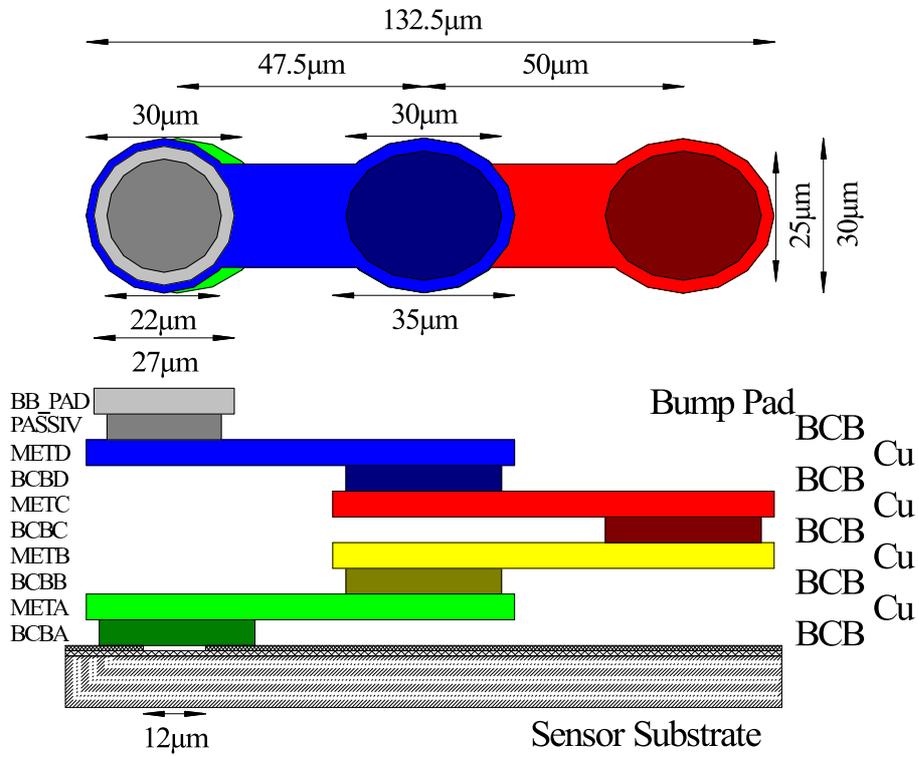
Figure 6.11: Layout of standard feed–through for MCM–D modules, 3rd design.
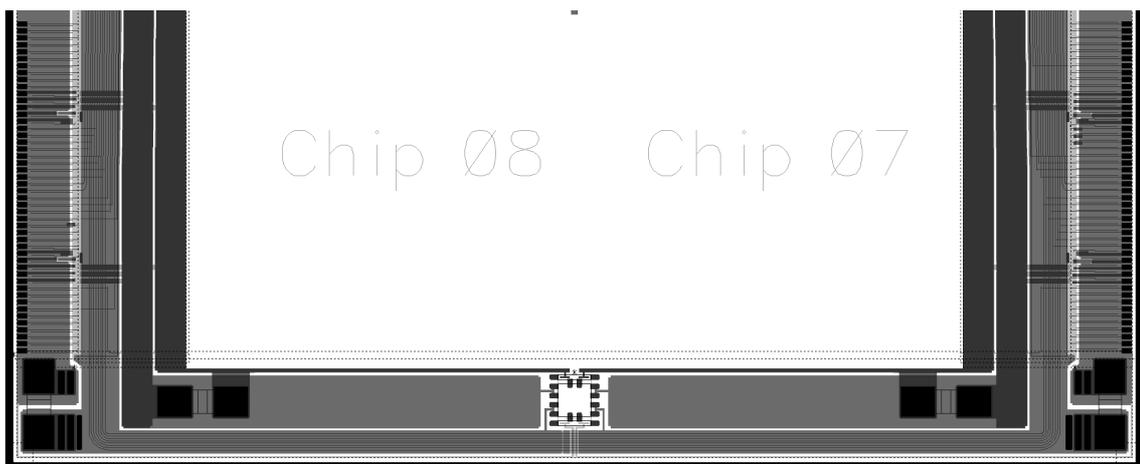
Figure 6.12: Layout of the small balcony of the MCM–D module.

6.6   Process Monitoring

Besides the probecard pattern dedicated to testing the module's power distribution functionality during the creation of the thin film layer system, especially designed Process Monitoring structures are included at three different locations on each wafer. These are designed in order to allow the investigation of several parameters of the thin film layer system during the process. By using the same dedicated probecard and wafer–prober system for the module surveillance during processing one can check (compare to Fig. 6.13):

- the sheet resistance of two metal layers. This is determined by a 4–wire resistance measurement of 4 different line widths (upper and middle left structure in Fig. 6.13).

- The isolation between these metal layers by checking for shortcuts between the metal structures.

- The reliable opening of the intermediate BCB layer (upper and middle right structure in Fig. 6.13) by measuring the resistance of daisy chained vias by a 4–wire measurement.

- The precise resistance of BCB vias with different diameters (bottom row of structure in Fig. 6.13), also by a 4–wire resistance measurement.

Table 6.2 on the next page gives an overview of the possible measurements.

Test	Line width/gap µm	Via diameter µm	Units per test
Metal 1 (buried)			
$R_{sheet}1$ [$\Omega/\square$]	15/15	-	1876.1
$R_{sheet}2$ [$\Omega/\square$]	20/30	-	1068.4
$R_{sheet}3$ [$\Omega/\square$]	30/30	-	1025
$R_{sheet}4$ [$\Omega/\square$]	100/50	-	106.6
Metal 2 (on top)			
$R_{sheet}1$ [$\Omega/\square$]	15/15	-	1870.6
$R_{sheet}2$ [$\Omega/\square$]	20/30	-	1061.4
$R_{sheet}3$ [$\Omega/\square$]	30/30	-	1015.5
$R_{sheet}4$ [$\Omega/\square$]	100/50	-	106.9
BCB layer			
$R_{viachain}1$ [Ω]	-	20	2×270
$R_{viachain}2$ [Ω]	-	25×30	3×270
$R_{viachain}3$ [Ω]	-	40	2×136
$R_{viachain}4$ [Ω]	-	80	1×80
$R_{via}1$ [Ω]	-	20	2×4
$R_{via}2$ [Ω]	-	25×30	2×4
$R_{via}3$ [Ω]	-	40	2×4
$R_{via}4$ [Ω]	-	80	2×4

Table 6.2: Overview of process monitoring structures.
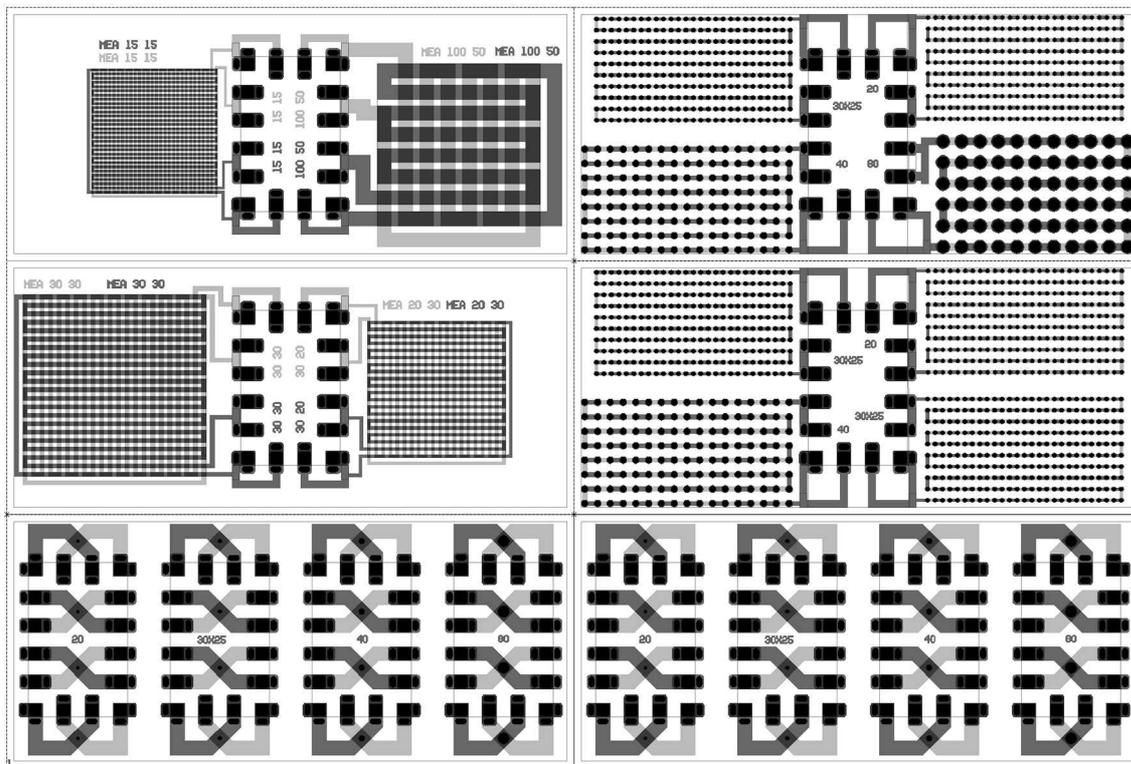
Figure 6.13: Process monitoring structure of the MCM–D3 design generation, $5.4 \times 8 \, \text{mm}^2$. Structure dedicated for testing MetA, dark grey, MetB, light grey and BCBB, openings in black.

Chapter 7

The MCM–D Process

In the beginning of the year 2001 the collaboration between Izm and the University of Wuppertal was extended and a joint effort was made to achieve an improvement in yield and stability in the production of a small series of MCM–D modules. Besides the definition of several design rules and design aspects, also the MCM–D process itself was reviewed. The MCM–D process, as it has been used for the latest MCM–D prototypes is described in detail in this chapter. The term process is used for all steps until the wafer is diced; thereafter further steps are referred to as assembly steps.

7.1 Process Flow

Figure 7.1 shows an overview of the complete process flow of MCM–D wafers at Izm.

The first process step is an optical inspection of the sensor wafers at Izm. The wafers have been tested electrically in different institutes of the Atlas Pixel collaboration, therefore it is necessary to inspect them for transport damages, scratches and the level of particle contamination of the wafers. The following bow and warp measurement also includes a measurement of the wafers' thickness. After the following cleaning procedure the run collection of wafers is transferred to a dedicated wafer box. This step includes the cleaning of the wafer box itself immediately before the wafers are transferred to it.

One of the major problems in former runs of MCM–D were impurities on the sensor wafer. The dicing streets of the sensors were especially attractive for the deposition of particles causing a high risk of module short cuts in the power bus system right above the dicing street. The usage of a high pressure water cleaning system, usually used for cleaning the glass masks for photolithography, was incorporated and lead to clear improvements.

Another improvement of this design and this process generation is the use of a backside protection by a BCB layer of thickness of $\simeq 7.5\,\mu m$ (maximum for this BCB formulation). This layer serves as a protection against scratches during the following process steps and also as isolation layer against the bias voltage contacted at the sensor's backside, thus this layer is patterned at the very end of the process. The drawback of this step is the fact that the wafer may incorporate particles on the front side again during these steps. Therefore

the sensor is cleaned again by the high pressure water cleaning procedure after the backside BCB spin coating procedure.

After the second cleaning, the wafer is ready to enter the thin film layer buildup of the process. The following steps build these thin film layers by alternating the procedure of: deposition and structuring a BCB layer, deposition of a structured copper layer and an electrical test of the metal plane. The individual steps will be described below in more depth. After the final metallization of the UBM (BB_PAD), including the module's IO pads and the pads for soldering passive components, and the remaining test pads (WB_PAD); the module is diced and cleaned. The further assembly of passive components and the 17 IC's is done by flip chip technology. The very last stage of assembly is the attachment of the flexible printed circuit MCM–D pigtail, on which most of the passive components have been soldered before.

Process flow, total time estimate under optimal prerequisites: ~ 12 weeks

| Inspection |
| Measure Bow & Warp |
| Cleaning |
| BCB backside |
| Cleaning |
| BCB layer 1 (BCBA) |
| Cu layer 1 (META) |
| Measurement |
| BCB layer 2 (BCBB) |
| Cu layer 2 (METB) |
| Measurement |
| BCB layer 3 (BCBC) |
| Cu layer 3 (METC) |
| Measurement |
| BCB layer 4 (BCBD) |
| Cu layer 4 (METD) |
| Measurement |
| BCB layer 5 (PASSIV) |
| Top metal 1 (BB_PAD) |
| Top metal 2 (WB_PAD) |
| Measurement |
| BCB Backside patterning |
| Wafer sawing & cleaning |
| Flip chip and soldering of passive components |
| Attachment of (loaded) MCM-D pigtail |

Legend:
- BCB processing
- Metal processing
- Clean/Tests/Assembly

Figure 7.1: MCM-D - Process overview.

7.2 BCB Processing

7.2.1 Basic Properties of BCB

The polymer of choice for our application is distributed under the trademark Cyclotene® by the Dow Chemical Company. It is based on the monomer Divinylsiloxan–bis–Benzocyclobutan (DVS–bis–BCB)[1], whose structural formula is shown in Figure 7.2.

By a 2+4 Diels–Alder–Cycloaddition the monomer reacts and forms a 3–dimensionally linked duroplast. This polymer is called BCB throughout this thesis. Figure 7.3 shows a part of the polymer BCB.

BCB is available as a precursor solved in Mesitylen (1,3,5–Trimethylbenzol) with additives to prevent oxidation. The further addition of two photosensitive components make it possible to structure the BCB by photolithographic exposure and developing. This type

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[1] 1,3–bis(2–bicyclo[4.2.0.]octa–1,3,5–trien–3–ylethenyl)-1,1,3,3–tetramethyldisiloxan is the full name of the monomer
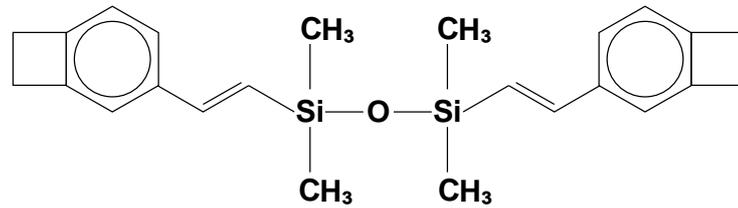
Figure 7.2: Structural formula of DVS–bis–BCB
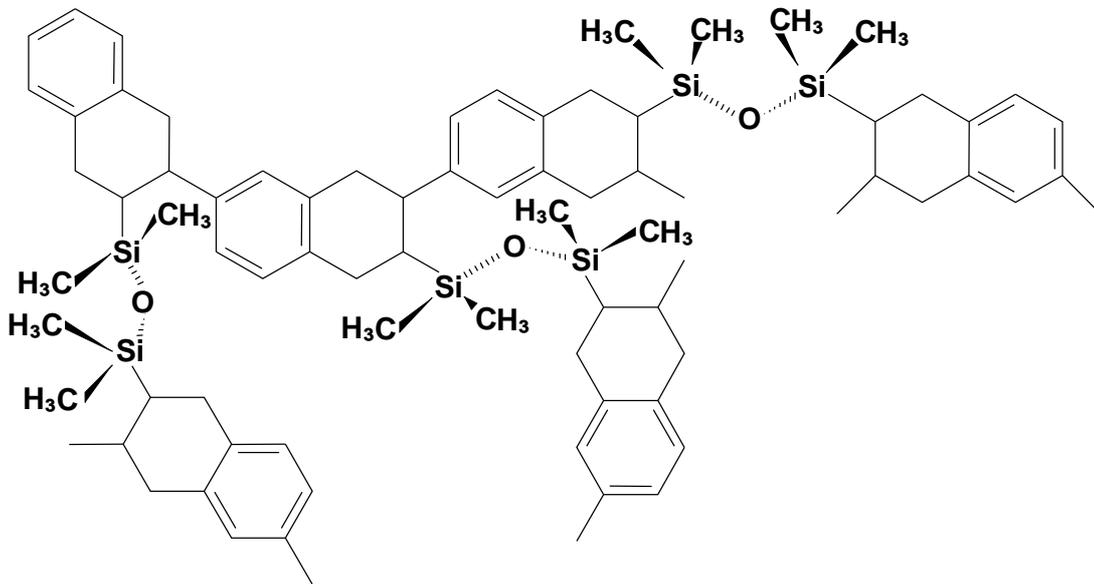
Figure 7.3: Part of the structural formula of the BCB polymer

of BCB formulation is referred to as Photo–BCB and features simplified processing and application. The Photo–BCB series of Dow is the 4000 series, which offers mainly three different formulations of BCB with different mass fractions of the solvent. The different viscosities of the products allow different ranges of thicknesses from 2.5 up to 14 µm. The formulation of choice for the application of MCM–D modules is Cyclotene® 4024 with a recommended film thickness between 3.5 and 7.5 µm.

Table 7.1 gives an overview of the relevant electrical and mechanical properties of BCB.

7.2.2   BCB Deposition and Structuring

The process of structuring Cyclotene® 4000 series is described in Figure 7.4.

Step 1 of the processing procedure is the cleaning of the substrates to remove any organic residues and other contamination. This is done by oxygen plasma clean in the case of the unprocessed sensor wafer and by Reactive Ion Etching in the case of an underlying BCB film as part of the metal deposition process. In the next step the adhesion

Property	Value	Unit
CTE	52	ppm/$^{\circ}C$
T$_g$	> 350	$^{\circ}C$
Tensile Modulus	$2.1 - 2.9$	GPa
Residual stress on Si at room temperature	28	MPa
Thermal conductivity	0.29	W/mK
Breakdown voltage	300	V/μm
Dissipation factor, tanδ (100 Hz - 1 MHz)	0.0008 - 0.0009	-
Volume resistivity	10^{19}	Ωcm
Dielectric constant ϵ_r (100 Hz - 20 GHz)	2.65	-

Table 7.1: Mechanical and electrical properties of Photo–BCB [46,57]

promoter AP3000 is applied during rotation. The adhesion promoter is not only used on the unprocessed sensor, but also between all BCB layers of the complete buildup for the avoidance of layer delamination. The next step (Step 4) is to spin coat the Photo–BCB on the wafer. This is done in four steps, described in Figures 7.5(a) to 7.5(d). Directly after the application of the adhesion promoter the polymer is dispensed on the wafer and distributed over the complete surface at very low spin speed of about 50 rpm[2]. A short increase to about 500 rpm spreads the polymer over the complete wafer surface building a polymer film. The thickness of the resulting film is determined by the next spin step. The spin speed is increased to up to 6000 rpm (Fig. 7.5(c)), followed by the edge bead removal step at about 1000 rpm, where a solvent (usually Mesitylen) is dispensed on the wafer edge to remove the BCB from the outmost radii.

The thickness of the polymer before exposure is determined by the fastest rotation during these steps and is mainly dependent on the viscosity of the polymer, which is in turn dependent on the temperature and the mass fraction of the solvent. Note that the spin speed of 6000 rpm is a maximum value. The typical speed to achieve a final film thickness of about 5 - 6 µm is between 2500 and 3000 rpm. The influence of the spin duration is negligible after about 25 s, due to the vaporization of solvent and the resulting increase in viscosity [57].

Before exposure, the Photo–BCB has to be dried by a bake (Step 4 in Figure 7.4). Residual solvent is evaporated, during this step, to prevent contamination of equipment and to guarantee adequate mechanical stability of the film. This can be done either in the oven or on a hot plate, as it was done at IzM. The latter offers the advantage of a higher degree of automation, as automated coating systems are mostly equipped with hot plates. To prevent contamination or damages to the backside, the sensor wafers are not in direct contact to the hot plate but are laid on pins to keep a distance of some millimeters. Baking at 85 $^{\circ}$C for 80 s yields good results.

The process of structuring Photo–BCB is similar to the standard processing of photoresists for lithography in thin film applications. Note that Photo–BCB is negative acting in contrast to standard photoresists, thus the exposed region are crosslinked and form the

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[2]rounds per minute
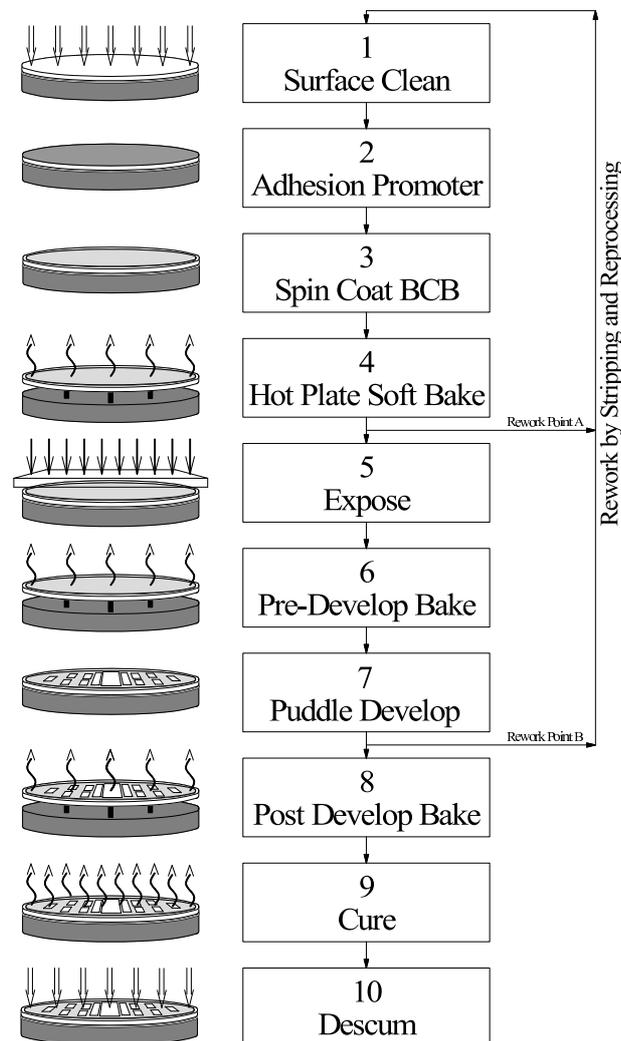
Figure 7.4: Process Description for Cyclotene®, partly from [46].

Duroplast. These regions will remain after development and the unexposed areas will be removed.

After cooling down to room temperature the BCB coated wafers are exposed to the G–line and I–line of Hg (medium range UV light with wavelength of 436 nm resp. 365 nm). 5–inch masks are used for the 4–inch wafers to perform a full field exposure in contact or proximity mode. Especially the glass mask for BCB structuring should be checked very carefully to avoid unintended openings in the dielectric layers and it has to be cleaned regularly, as BCB coverage by contaminations leads also to openings in the layer.

Before development of the Photo–BCB an additional bake step, the Pre–Develop Bake is recommended. The aim of the Pre–Develop Bake is to equalize possible differences in the end point of the development time, especially after a delay between exposure and development.

(a) Application of Photo BCB at very low spin speed

(b)   Distribution   over wafer surface at low spin speed

(c) Determination of polymer film thickness at highest spin speed

(d) Removal of Edge bead at medium spin speed
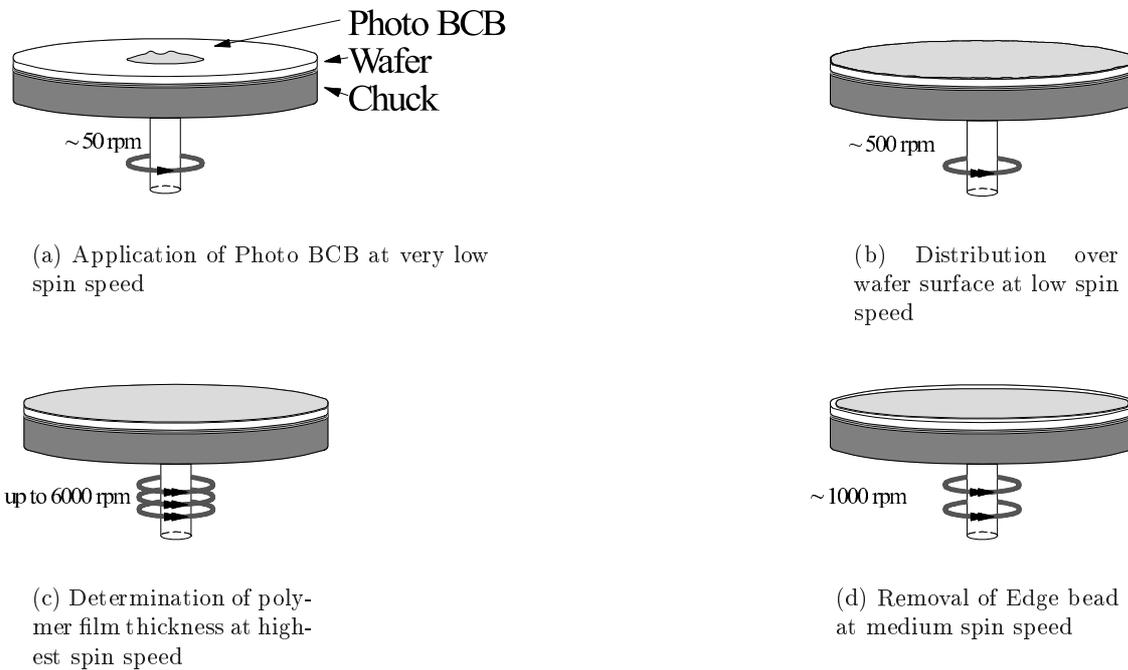
Figure 7.5: Spin Coating of Photo BCB.

The development of the exposed Photo–BCB can be done in different processes. The *immersion develop* has been used so far. This technique uses an immersion tank with heated developer DS3000. The change to the *puddle develop* process offers the advantage of a further automation of the procedure as this can be done in the automated coating system. The developer (DS2100) is applied to the wafer, so that the full wafer surface is covered by the puddle. About 10 s before reaching the predetermined developing time the wafer is rinsed by a stream of DS2100 at a medium rotation of 500 rpm. The wafer is then dried at 3000-4000 rpm. During these steps the unexposed areas of the BCB layer are dissolved and removed.

The Post–Develop Bake follows immediately to the development process and is used to dry the wafer and to stabilize the polymer layer. Like all other baking procedures, this is done on a hot plate in the automatic coating system.

The cure of BCB is either a soft cure for an intermediate layer of the thin film system or a hard cure for the last layer. The cure procedures differ in the applied temperature profile (a convection oven is used at this stage) and the resulting fraction of polymerization in the layer. A typical soft cure is performed at 210 °C for 40 min resulting in $\leq$ 75% polymerization. Hard cure is typically at 250 °C for 60 min resulting in a degree of polymerization of $\leq$ 95%. The adhesion between the intermediate layers is strengthened by this procedure. The resulting temperature profile is determined by the maximum speed at which the oven can reach cure temperature while purging oxygen, as the BCB oxidizes at temperatures > 150 °C.

The *Descum* is a plasma cleaning step, necessary to remove remnants of BCB in the via openings of the BCB layer. A parallel plate etcher in reactive ion etch mode is used to remove these residues of some thousand Å[3] thickness. A gas mixture of oxygen and SF_6 (or other silicon etching gas) is necessary, as there is silicon in the polymer layer. Note that when the structuring of the backside layer is done, the plasma etching step is extended and can be used to structure the cured polymer layer. A photoresist of $\leq 10\,\mu m$ has first to be deposited and structured for that purpose. A 2×11 min plasma etching step slowly removes the photoresist and the open lying polymer, so that the backside layer can be structured. The photoresist is stripped afterwards by NMP[4] and spin drying. This scenario offers the advantage that contaminations during exposure do not lead to unexpected openings. This also should improve the reliability of the backside isolation compared to the High Voltage test presented in 5.5 on page 44.

After the Descum step a short dip in acetic acid to prevent corrosion and discoloration of copper as well as a cleaning step in a standard Spin Rinser Dryer finalize the BCB deposition procedure and the wafers can proceed to the processing of the metallization.

7.2.3   Repair Options during BCB Processing

After the curing the BCB layers are highly rigid. The described dry etching process is a possibility to structure a complete layer. A local rework by laser can be done, too, but this could not be tested during this thesis. The first rework point in Figure 7.4 is before exposure. The BCB is not yet crosslinked and can be removed with an appropriate solvent, e.g. Mesytilen. Removal of the BCB layer after exposure and development is much more difficult. [46] offers information on how to perform this procedure, although in the case of an intermediate layer of a multi layer system, one takes the risk of problems with decreased adhesion, which may lead to delamination of the layers.

The Descum process step itself can be extended to open vias in the case when there is a small remaining remnant due to e.g. over exposure, where the BCB partially gets crosslinked below covering photo mask structures. A remnant thickness of some hundred nanometer of BCB can be removed, but this reduces also the BCB thickness over the complete wafer. This can lead to uncovered copper structures.

7.2.4   Comment on BCB Processing

The manufacturer information of Dow [46] offers detailed process information and recommendations. The provided information have to be adapted to a complex multi layer system like the MCM–D modules. Exposure times and development times do vary with increasing layer number. The incorporation of the Pre–Develop Bake at Izm showed good results. A system as complex as the one presented here, relies on a large fraction of automated process steps. This has been significantly improved compared to earlier studies. The higher degree of automation also directly leads to improved cleanliness conditions. Keeping the number of process steps with human involvement as low as possible is highly recommended, but

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[3] $1\,\text{Å} = 10^{-10}$ m
[4] NMP: **N**–**M**ethyl 2 **P**yrrolidone (C_5H_9NO)

on the other hand optical inspections during BCB processing are necessary for early error detection and possible rework. It should also be pointed out that parameter fluctuations from wafer to wafer have been recorded in higher layers. [57] gives profound insight into the procedure of BCB deposition and material properties of the polymer.

7.3   Cu Electroplating

The intermediate metallic layers of the MCM–D system are formed in an additive electro-plating process. Figure 7.6 describes the basics of the procedure.
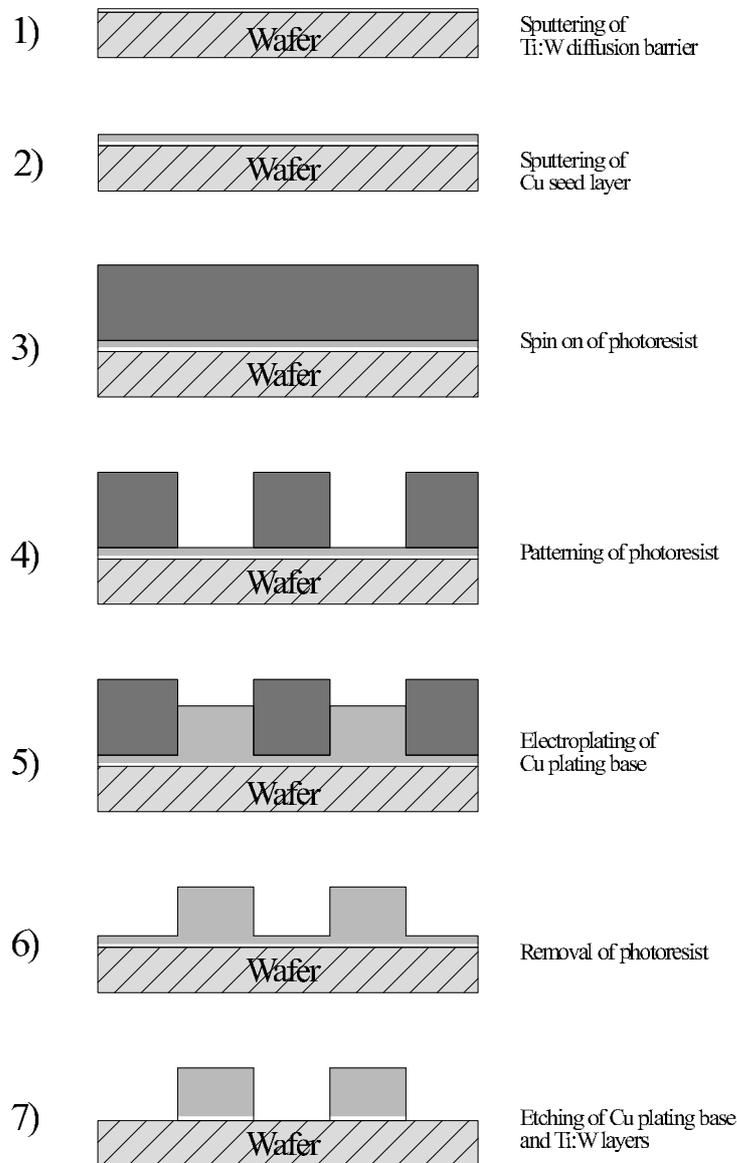
Figure 7.6: Electroplating of Cu layers

The first step of the process is to deposit a thin layer of Titanium and Tungsten (Ti:W) of $\simeq$ 100 nm. The layer improves adhesion between the Cu metal layers and acts as a diffusion barrier. It is deposited over the complete wafer surface by electro sputtering to the sensor's Aluminium pads. The second step is the deposition of a thin Cu layer by sputtering, which acts as the seed layer for the electroplating procedure. Before entering the galvanic bath a photoresist is spun on the wafer and structured by exposure and development (Step 3 and 4 of Fig. 7.6). The desired structures are patterned as openings in the photoresist layer. A typical thickness between 3 µm and 3.5 µm of Cu is then built in these openings by electroplating (Step 5). The next step is stripping the photoresist layer by an organic solvent, such as Aceton. At last the Cu seed layer and the underlying Ti:W layer are removed in a two fold etching procedure.
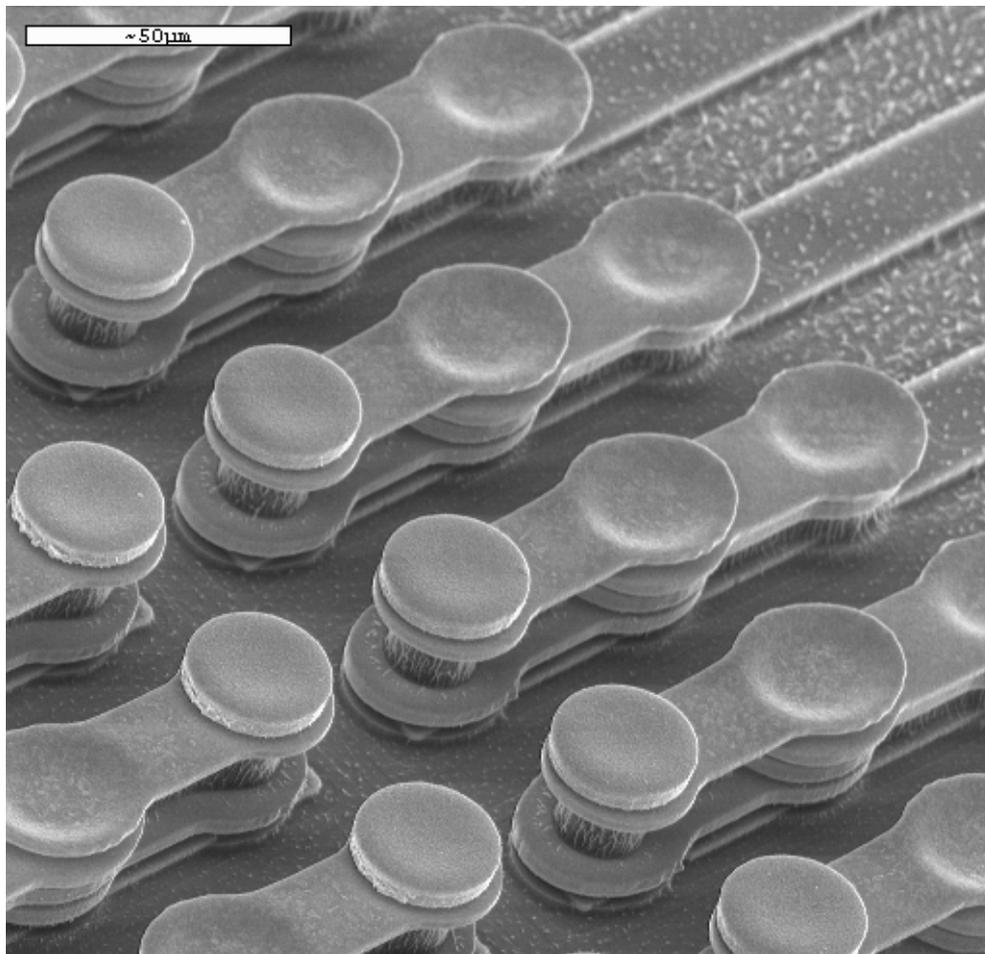
Figure 7.7: Electroplated feed–through structures (BCB has been etched for visualization, some remnants are visible as pillars between the metal layers, acting as stabilization for the structures) [Photo: IzM].

Figure 7.7 shows an electron microscope image of a feed–through MCM–D structure to visualize the very high quality of the galvanic process. The four plated copper layers and the bump metallization pad are visible on a standard Atlas sensor.

7.4   Test Measurements on Wafer Level

After each buildup of a metal layer the test measurements described in Chapter 6 are performed with an automatic wafer–prober and a dedicated 16 needle probecard. These measurements can be divided into two groups:

- Process quality assurance. The Process Monitoring structures give the possibility to measure the via resistance and reliability, as well as the sheet resistance of the plated Cu layer. No rework option for the intermediate BCB layer is available.

- Module functionality. A contact pattern to the module's power bus system allows to check for shortcuts between different potentials and perform an eventual metal rework.

7.4.1   Repair Options after Metal Deposition

Theoretically, there are two options to repair the metal structures if errors are found during the test measurements.

1. Rework by removal of the complete metal layer and reprocessing of the layer. This step is hypothetically possible, but has not been tested during this thesis. The removal of a complete metal layer by etching causes two problems: the control of the etching process has to be very accurate to stop the etching exactly after the removal of the target metal layer. Otherwise the underlying layer of metal will also be etched and damaged unintentionally through via openings in the BCB. Stopping the etching process too early introduces uncontrollable metal thickness after replating the layer and furthermore the possibility remains that the defect is not removed.

2. Rework of local etching of the defect area. This is by far the superior method of reworking although it requires the exact localization of the defect. The complete wafer is then covered by a photoresist, which is exposed manually, e.g. using a microscope lamp, and developed. Afterwards the wafer can be etched with almost no risk. Eventual over etching in via openings directly under the defect area might occur but a damage stays local.

7.5   Assembly Steps

The following sections describe the necessary assembly steps to build a complete MCM–D module.

7.5.1 Flip Chip

After singulating the module, single chips and test structures from the wafer a last inspection and cleaning is done manually, so that the parts are prepared for the further assembly steps. The main step is the flip chip bonding, which has been presented briefly from the technological point of view in Section 4.4. The MCM–D specific aspects of this step are described here.

One of the major fields, where the MCM–D project has been supported by the ATLAS pixel community, is the supply with front–end chips. When building a Multi Chip Module it is of highest importance to assure functionality of the assembled parts. When building a Multi Chip Module of N chips the risk of mounting defect chips drastically decreases the module's yield:

$$Y_{MCM} = Y_{IC}^{N} \tag{7.1}$$

with:

Y_{MCM}:	yield of the Multi Chip Module
Y_{IC}:	yield of the mounted ICs
N:	no. of chips mounted

This is well known as Known–Good—Die problem (KgD). In the case of the MCM–D module these parts are:

- the Module Controller Chip, MCC-DSM. This generation of MCCs was produced together with the front–end chips FE-I1 on the same wafers. Twelve MCCs per wafer featured IO pads with bumps (4 per IO for reason of redundancy) for the MCM–D application.

- 16 front–end chips, FE-I1 or later generation. The MCM–D dedicated chips (20 per wafer) featured additional bumps on the IO pads, too.

The Pixel collaboration follows a two fold strategy to deal with the KGD problem. This guarantees the functionality of the ICs before flip chip bonding with highest probability and MCM–D benefitted from these efforts, too:

- Test on wafer level: after the delivery of the IC wafer from the manufacturer a detailed test of functionality and calibration is performed. In the case of the front–end chip wafers this is done either at the University of Bonn or at the Lawrence Berkeley National Laboratory (LBNL). The MCC wafers are tested at DELTA[5]. This test are performed for all wafers during the production of modules for the Pixel Detector.

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[5] Delta: **D**anish **E**lectronics, **L**ight & **A**coustics, Hørsholm

- Test of single front–end ICs: after the bump deposition and dicing of the front–end chips the ICs are sent in dedicated carriers from the bumping vendors back to institutes of the collaboration (Bonn and LBNL) and tested again. This step incorporates a lot of effort and is very time consuming compared to wafer level tests. The latter can be automatized to a much higher degree. If the fraction of chips that pass both tests will be close enough to 100 % during production, the single front–end IC test can be skipped.

- Bare module probing: After the successful bonding of the sixteen front–end chips to a sensor tile and successive X–ray inspection to detect bonding errors like displacement or large scale bump shortage (very seldom), a electrical test is performed before further assembly. By contacting each front–end chip individually with a probecard a recharacterization can be done at this stage. Unconnected or shortened pixels can be detected reliably, by measuring noise and crosstalk (see chapter 9 for more detailed information. Individual chips can be replaced by desoldering and repeating the flip chip process.

- Test of mounted Flex kapton: when the MCC is glued and wire bonded to the Flex, a full functionality test is done by connecting it to the dedicated PCB, where the Flex is laminated to. The University of Bonn temporarily ran a test setup where single MCC probing and testing was done during preproduction. The MCCs, which were used for building MCM–D modules were kindly tested on this setup.

The option of replacing a defect chip of a module improves the situation. MCM–D modules offer the advantage of being able to rework (to replace) individual chips even after the full assembly of the module, while a standard Flex–module can only be reworked on a bare module level. Once the loaded kapton is glued to the bare module, a replacement of chips is impossible.

The procedure of the flip chip process is very similar to that of a standard ATLAS Flex–module, with two minor modifications:

- The MCC-DSM is flipped and bonded in the same procedure, using the same tooling.

- After the manual application of solder paste, the passive components are placed on the main balcony of the module and bonded during the same temperature cycle.

The standard ATLAS temperature profile is then run in a nitrogen atmosphere reflow oven, with a maximum temperature of 250 °C.

7.6   Attachment of a Flexible Printed Circuit to MCM–D Modules

The attachment of a flexible kapton circuit, the MCM–D pigtail, to the MCM–D module allows a very simple and reliable connection to the module, offering greatest flexibility in handling the module, as there are no additional PCBs involved. Earlier versions of MCM–D

modules relied on being contacted by wire bonding to a dedicated readout PCB [35]. This mixture of contact technologies should be avoided and furthermore the MCM–D approach should take advantage of the progress of the Pixel community in building the readout chain of the Pixel detector. To achieve an "as close to reality as possible" status has been the aim of this thesis. The choice of using a pigtail attached to the module, where a plugin for the *Type0* cable[6] is mounted, is driven by that consideration.

Figure 7.8 shows an overview of the MCM–D pigtail's components, signal and power routing, as it has been realized. These circuits have been produced by ANDUS[7].
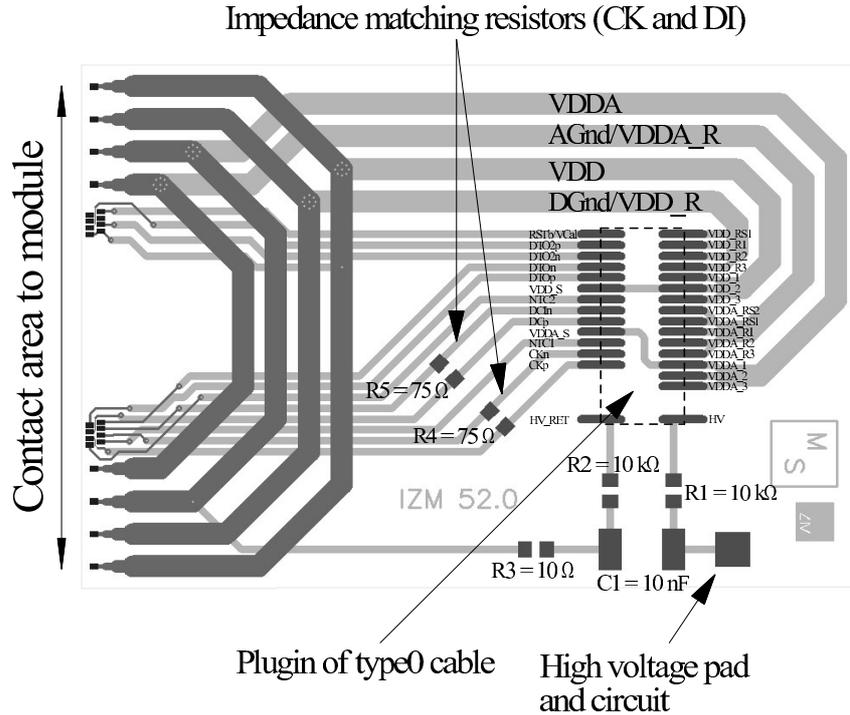
Figure 7.8: MCM–D kapton printed circuit layout: MCM–D pigtail

The critical point in the connection is the module - pigtail interface. The outmost contacts (top and bottom in Figure 7.8) are responsible for the power supply of the module. The signal contacts are located at the modules edge left and right of the MCC, in two groups of contacts. On the module side all pads are designed with a size of 300 µm × 200 µm. The corresponding pads on the pigtail are 300 µm × 200 µm in the case of power contacts and 300 µm × 150 µm in the case of signal contacts (these had to be reduced in size, due to design rule restrictions of the pigtail).

While first aiming for a solution using soldered connections, first attempts with test structures revealed several problems. The application and reflow of solder on the pads were difficult and in the end not homogeneous. The pigtails themselves became rippled after being heated to reflow temperature and in conjunction with non dedicated tooling (which

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[6] Type0: connection cable between the ATLAS pixel detector modules and the first patch panel.
[7] ANDUS Electronic GmbH, Berlin

made a two step bond procedure necessary) the results of the tests were unsatisfactory and
showed:

- weak mechanical stability,

- shortcuts due to solder over application,

- delamination of MCM–D layers.

As a result the technique of choice became Au–stud bumping under thermocompres-
sion using anisotropic conductive adhesive to strengthen the mechanical interface. This
technique ultrasonically welds an Au wire to the pigtail's contact pads, cutting the wire
off after some microns. The *Au–stud* remains on the pad. In our specific case as much
Au–studs as possible are welded on the pad. The MCM–D pigtail is then attached to
the vacuum holder of a Flip Chip bonder, which is used for the alignment, pressure, and
heat application, to the interface. Before the procedure the pigtail is mounted with its
components by applying solder paste and reflow in a convection oven with nitrogen purge.
The Type0 cable connector will be attached later, as it is too tall in height to be used with
the existing tooling.

The anisotropic conductive adhesive[8] is carefully applied with a syringe, the alignment
of the two parts - module and pigtail - is done by the bonder. The vacuum tool is then
lowered until there is contact after which predefined pressure and heat is applied to cure
the adhesive and to mechanically stabilize the connection. Figure 7.9(a) and 7.9(a) show
microscope images of a cross section of assembled MCM–D test pieces.
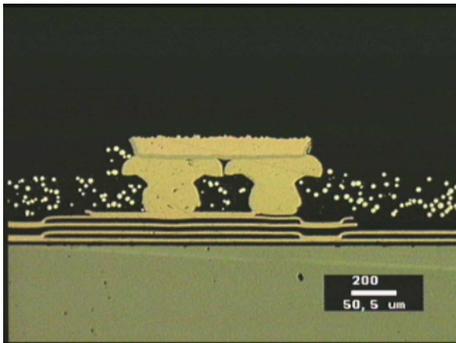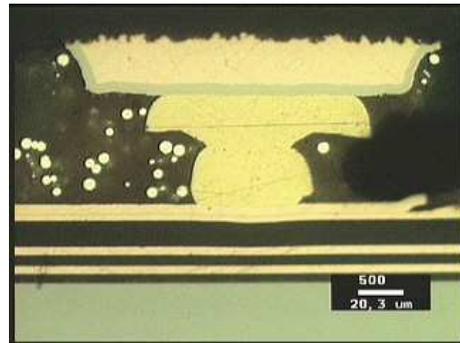
(a) Power supply pad.   (b) Signal pad.

Figure 7.9: Cross sections of Au stud connection [IzM].

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[8] ThreeBond 3372C: a microencapsulated, anisotropically–conductive adhesive for bare–chip mounting

Chapter 8

Production and Optimization of MCM–D Prototypes

In May 2002 the first run to produce MCM–D modules for the Deep Submicron generation of readout electronics and controller chip was started at the Fraunhofer Institute Izm in Berlin. A total of 11 Prototype 2.0 sensor wafers were available and it was decided to split these wafers into 3 different runs. See Appendix A for a detailed wafer overview of each individual run.

Challenges in the production of MCM–D modules were the relaunch of the process after a two year gap and the parallel struggle to improve the process.

8.1 Run Overview

An overview of the processed runs featuring the third MCM–D design is given here:

- Run 2002-058[1]: MCMD3 Daisy Chain Run 1

  The runs that produced the first generation of MCM–D prototypes presented in Chapter 5 were mainly processed in the Year 1999 and the first MCMD3 Run 1 started in May 2002. To close this gap, that is unavoidably connected with partial loss of knowhow on the operator level and exchange of equipment and personal, the MCMD3 Run1 consisted only of one Prototype 2 sensor wafer and several sensor replacement wafers. This minimized the risk for the rare remaining sensor wafers and established a reasonable process flow for the next runs. The included sensor wafer delivered the MCM–D single chip hybrids described in Chapters 9 and 10.

- Run 2002-096: MCMD3 Sensor Run 2

  After the first successful production the remaining 10 sensor wafers were equally split among Run 2 and Run 3. A fatal handling error lead to curing the first BCB layer despite massive damages of the layer. This run was further used as experimental run, on which process parameters could be optimized on real sensor wafers.

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[1] This is the corresponding run number used internally at Izm

- Run 2002-147: MCMD3 Sensor Run 3

  Finally Run 3 was dedicated to incorporate all optimizations with the target of producing the highest possible number of modules.

Figure 8.1 shows a photograph of one of the Prototype 2 sensor wafers, which successfully finished the MCM–D processing at IzM.

8.2   Variations of Top Metallization

Another option for improvements in processing sensor wafers for MCM–D is the simplification of the top metallization processing. Until now the technology of choice has been the electroplating of two different metallizations with different purpose:
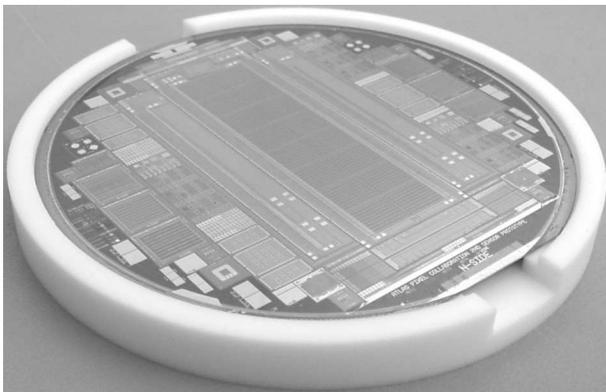
Figure 8.1: Finished MCM-D wafer [IzM].

- Cu - Au metallization serving as the Under Bump Metallization, as it has been used during the very first runs for MCM–D and for the standard Atlas bumping procedure. This technique has been thoroughly investigated for the Atlas pixel detector [58]. The thin Au layer serves as prevention of oxidation.

- Cu–Ni - Flash Au serving as the pad metallization for eventual wire bonding. This has proven useful in the past, but is not expected to be of further need for this generation of MCM–D modules.

The combination of the two different metallizations introduces increased complexity of the MCM–D process at a very late stage of the production. The photoresist spin on, exposure and developing as well as the electroplating procedure itself has to be done twice. Therefor a part of the Runs 2002-096 and 2002-147 was used to evaluate the possibility to reduce the complexity and the number of handling steps. Using the well known technique for all the main part of the wafers should minimize risk. Two different metallization configurations were successfully processed, assembled and investigated by cross sectional cuts and X–ray microscopy:

- Cu–Ni - Au. This variation uses a Cu–Ni metallization for all pads including the bump pads of the sensor.

- Cu - PbSn. This approach is completely different. A thin layer of PbSn of $\simeq 2\,\mu m$ is galvanically deposited on the sensor side and reflowed, similar to the process, that is done on the electronic side.

Figure 8.2 shows the cross sectional views of the two different metallization schemes described above. These cross sections were cut and polished from daisy chain assemblies with electrically non functional electronic chips. For instance in Figure 8.2(b) the buried Cu layer is visible on top. The BCB layer forms the opening to the Underbump Metallization, which is separated by a thin Ti:W layer (bright strip) and build out of the Cu and the Ni layers. Note the complete coverage of the PbSn sphere across both UBM metallizations. The slight void inclusion in the bump is uncritical. Figure 8.2(c) shows an example of a PbSn – PbSn connection with a buried copper socket. The intermetallic phase around the copper socket is slightly more developed compared to Figure 8.2(b). Both metallization schemes yielded sufficient results, but based on low statistics. It should be taken into consideration that first tests with the PbSn scheme (see Figure 8.3) resulted in a high amount of shortened bump connections, which were observed during X–ray inspection. The reduction of the plating thickness to the $\simeq 2\,\mu m$ avoided these difficulties. Another approach could be to reduce the thickness of the bump sphere on the chip side of the assembly, but this could not be tested in our case due to the usage of standard ATLAS pixel front–end chips.

The PbSn cover on all pads excludes the possibility of wire bonding but yield superior results when mounting passive components. The variation of a Cu–Ni UBM on the sensor side was processed without difficulties and yielded very good results. Both techniques significantly simplified the final processing steps.
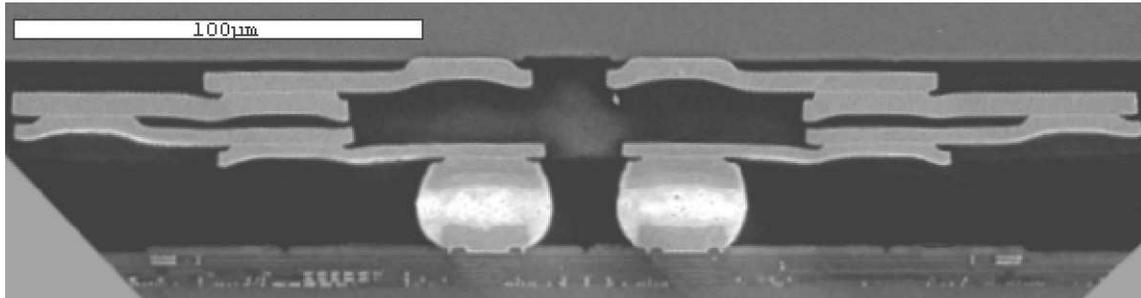
(a) Cross section of a double feed–through structure (Cu–Ni - Au)
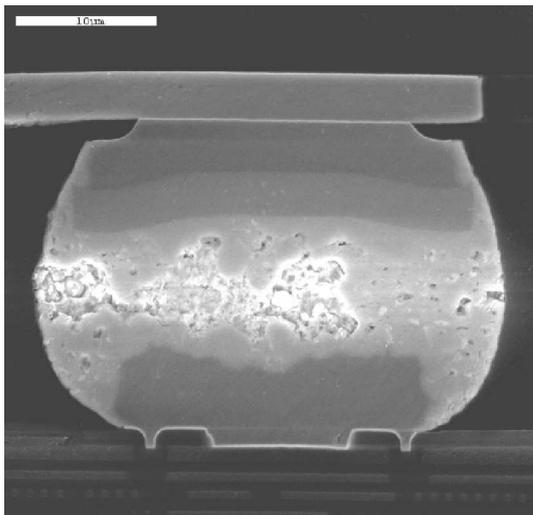
(b) Cross section of a bump (enlargement of 8.2(a))
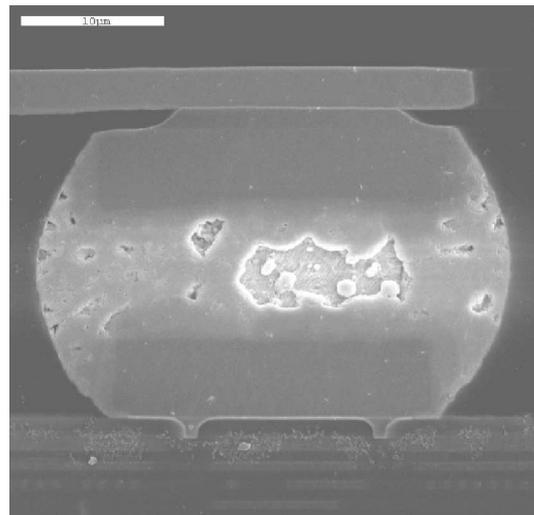
(c) Cross section of a bump with Cu - PbSn metallization scheme

Figure 8.2: Cross sectional view of two different Top metallizations [Izm]
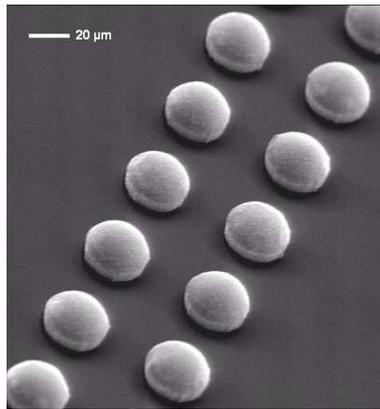
Figure 8.3: Additional PbSn deposition on sensor UBM (test run) [Izm].

Chapter 9

Performance of Pixel Detector Prototypes in MCM–D Technique

A variety of characterizing measurements on ATLAS pixel detector prototypes can be done in laboratory. The ATLAS pixel detector front–end chips, used for the assembly of MCM–D prototypes, offer the feature of injecting a known test charge into the preamplifier of *selected* pixel cells for that purpose. In this chapter an overview of the produced prototypes is given and selected measurements on single chip assemblies as well as module size prototypes are presented.

9.1 Overview of MCM–D Prototype Production

The production of the new MCM–D design prototypes was a milestone for the MCM–D project. In July 2002 the first run of wafers for the radiation hard front–end chip generation was finished. Prototypes from the two subsequent runs were finished in December 2003 and during the year 2004.

9.1.1 MCM–D Single Chip Assemblies

Single chip assemblies are built using one front–end chip and a sensor diode, that fit to each other in size and geometry. 2880 electronic channels are provided for readout. The dedicated sensor features corresponding contact positions for bump bonding. As described in Section 6.1.2 on page 49 there are different types of available single tiles with dedicated geometries for MCM–D (see Section 6.4). These sensors are labelled *equal–sized* and *equal–sized–bricked* and can only be used after building routing structures in MCM–D. In Figure 9.1 a SEM[1] picture of a part of the completed structure on a equal–sized–bricked device with zigzag bias grid configuration is shown.

Table 9.1 summarizes the production of MCM–D type single chip assemblies. These prototypes cover the different geometrically optimized devices as well as the devices with

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[1]SEM: **S**canning **E**lectron **M**icroscopy
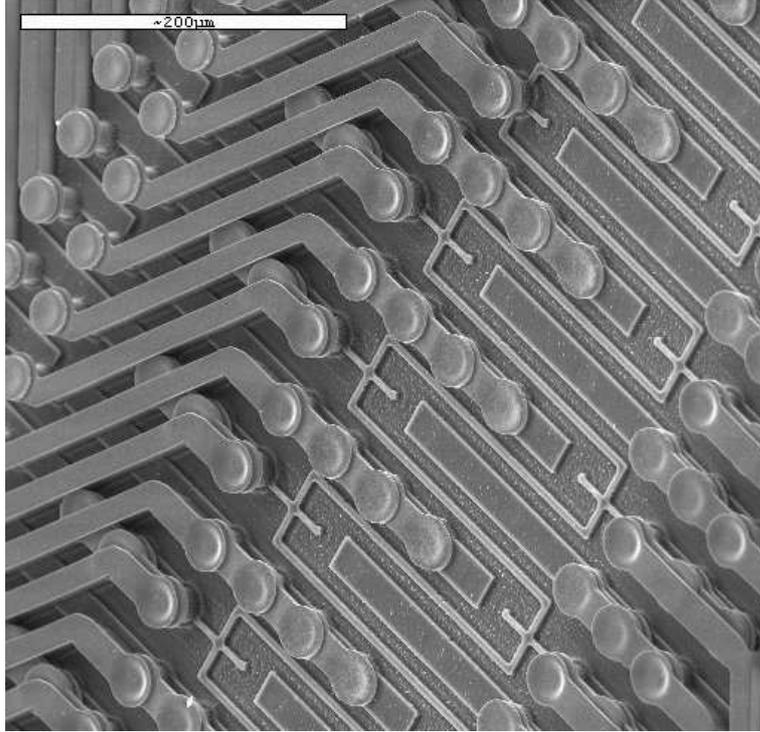
Figure 9.1: Routing structures on equal sized bricked device with zig zig bias grid configuration (BCB etched) [Izm].

standard Atlas pixel detector layout. After completion of the flip chip process the prototypes are glued to a dedicated PCB with components for signal recovery and all IO pads are directly wire bonded to this PCB.

9.1.2   MCM–D Modules

A total of 6 MCM–D type pixel detectors was built using the radiation hard generation of front–end chips, FE–I1A/B and FE–I3. All these modules used a controller chip (MCC) of the first DSM generation. Table 9.2 summarizes the production.

During the measurement of the process monitoring structures of Module 1 (wafer 3695–03) partly closed vias in the topmost BCB layer became evident after the final control measurement. As described in Chapter 7 a repair at this stage was not feasible. This module has then been used to qualify the further assembly steps and finally showed a perfectly working communication link to the MCC. Unfortunately a great part of the front–end chips' IO pads were unconnected to the signal bus system. A design feature offered the possibility of checking this connection. This structure is shown in Figure 9.2. An additional pad is connected to one of the four redundant IO bump pads of a front–end chip's IO. If the IO is successfully contacted, an electrical connection can be measured by probing this pad as well as the standard large test pad. At least two of the bumps are then in contact to the chips IO pad, one of the two being the one at the additional pad. When

Name	Type	Front–end	Wafer
Wu–1–B	Equal sized bricked zig zig grid	FE-I1B	3695–03
Wu–2–B	Standard	FE-I1B	3695–03
Wu–3–A	Equal sized	FE-I1A	3695–03
Wu–4–A	Standard	FE-I1A	3695–03
Wu–5–A	Equal sized bricked parallel grid	FE-I1A	3695–03
Wu–6	Standard	FE-I2	3695–03

Table 9.1: Overview of MCM–D single chip prototypes (Design 3).

Name	Type	Front–end	Wafer	Top metal	condition
Module 1	Standard	FE–I1B	3695–03	Cu	IOs (vias)
Module 2	Standard	FE–I1A	3695–13	Cu	ok
Module 3	Standard	FE–I3	3696–12	Cu	IOs (bumping)
Module 4	Standard	FE–I3	3696–02	Cu/Ni	Flex
Module 5	Standard	FE–I3	3696–14	Cu/PbSn	Flex
Module 6	Standard	FE–I3	IRST 38	Cu/Au	pending

Table 9.2: Overview of MCM–D module prototypes (Design 3).

measuring an open connection one can state that at least this bump is not connected. One usually expects a very low failure rate of $< 1\,\%$ of missing bump connections or shortcuts between bumps.

This type of measurement confirmed the origin of the failure of Module 1. Nevertheless the communication link to the controller chip was running perfectly in the 2×80 Mbit mode utilizing both data channels of the controller. Two of the front–end chips responded digitally but showed bad analog performance, due to their partly unconnected IO pads. Furthermore measuring the current–voltage characteristics of the sensor tile revealed no major influence of the MCM–D processing on the sensor properties. Figure 9.3 shows the results of this measurements.

Through the measurement of the IO contact test structures an issue of only six responding front–end chips with Module 3 was traced back also to a small number of IO contacts ($22\,\%$ showing contact). This was caused by an accidental series of very thin front–end chips ($< 150\,\mu$m), which where also the reason for low contact yield in standard ATLAS devices. Due to their reduced thickness these chips get a stronger bow during the heating up of the flip chip process, preventing the IO pad bumps from being in mechanical contact to the corresponding IO pad during phase transition of the solder.

Module 4 and 5 revealed another unexpected issue related to the contact of the MCM–D pigtail. These two modules showed no communication link to the MCC. Due to space limitations on the module's balcony the additional IO test pads are not available for the MCC. So the MCC was removed at IZM to get access to the pads and investigate the failure. Vital signal lines (e.g. CLKn and CLKp) between the MCC IO pads and the corresponding contact of the Type0 cable were without connection. It was thus proven, that the electrical contact at the pigtail interface was missing. At the time of writing
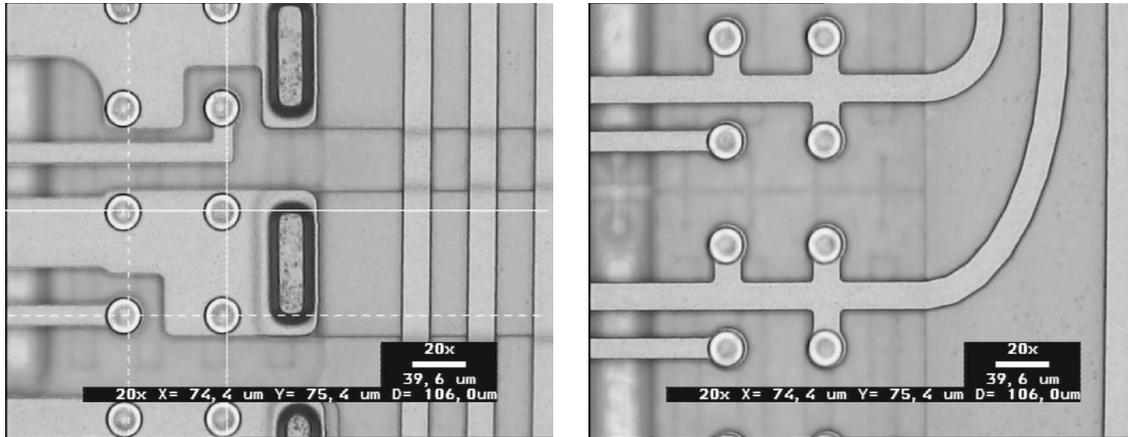
(a) Connectivity test structure at power bus contact.

(b) Connectivity test structure at data bus contact.

Figure 9.2: Test structure for checking the front–end chips' connection to the MCM–D system.

this thesis, a solution for safe reworking the cured epoxy adhesive without damaging the underlying MCM–D structures is under investigation. The pigtail attachment of Module 6 has been delayed. Tests of the module could be done by a dedicated probing setup.

Module 2 is equipped with front–end chips of FE–I1A type and has been successfully operated and tested. Details on this module and the results of characterizing test measurements will be presented in Section 9.4 on page 100.

9.2   Single Chip Hybrids

Measurements on single chip assemblies determine the analog performance of the front–end chips' pixel cells. The focus of attention during these tests in the case of MCM–D type prototypes is the influence of the necessary feed–through structures. Despite these, a variety of digital tests can be performed that are capable of testing all internal registers and DACs[2]. All digital tests have been passed by the front–end chips, which is a requirement for the following analog tests. The setup that has been used for these measurements is sketched out in Appendix B.

The major analog test procedure is the determination of the threshold and noise performance of each pixel cell. This is done by injecting a number n of test pulses of known charge into the preamplifiers of selected pixel cells. This can be done by either switching an internally generated voltage, using a dedicated internal DAC of the chip (internal calibration) or by using an external switching device e.g. a pulse generator. These voltage pulses are fed to one of the two internal injection capacitances ($C_{high} \simeq 37.5\,\mathrm{fF}$ and $C_{low} \simeq 5\,\mathrm{fF}$,

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[2]DAC: **D**igital to **A**nalog **C**onverter
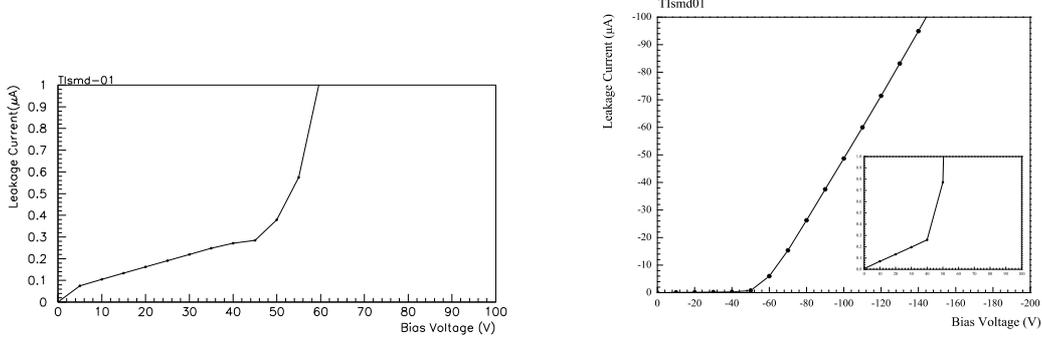
(a) Initially measured IV curve of TIsmd01 of wafer 3695–03 from [59].

(b) IV curve of MCM–D Module 1.

Figure 9.3: IV curve of MCM–D Module 1 before (on wafer level) and after MCM–D processing. *Note the different scales between Fig. 9.3(a) and 9.3(b).*

more precisely measured on each chip individually) to cover a large range in charge. The amount of charge is determined by:

$$q[e^-] = \frac{U_{inj}[V] \times C[F]}{1.6022 \times 10^{-19}[C]} \tag{9.1}$$

Subsequently increasing the charge, the ratio of pulses, which are reported by the front–end chip, is recorded. Ideally one would expect, that this response function $r(q)$ follows a step function, yielding no reported hits below an adjustable threshold $q_{threhold}$ and n hits above this threshold. In reality the response function is smeared by the electronics noise σ_{noise}, following the error function:

$$r(\frac{q - q_{threshold}}{\sigma_{noise}}) = erf(x) = \frac{1}{\sqrt{2\pi}} \int_0^x e^{-\frac{t^2}{2}} dt + \frac{1}{2} \tag{9.2}$$

The threshold is then determined by fitting the error function to the measured response function. The point of 50 % response is equal the threshold and the noise is equal to σ_{noise} being a measure of the steepness of the function. The electronics noise is also referred to as the *equivalent noise charge*, ENC. More details on laboratory measurements can be found in [60].

Keeping the threshold low and uniform as well as a low noise is of great importance for the detector. The target is to allow stable operation at a threshold of $\simeq 3000\,e^-$ to keep a large enough margin for the detection of signal sizes of down to $10000\,e^-$ expected for partially depleted, irradiated sensors at the end of their lifetime. The threshold dispersion and the noise determine the rate of noise or fake hits in the detector.

9.2.1   Geometrically Optimized Devices in Laboratory

Figure 9.4(a) to 9.4(d) show the results of noise measurements on the specified prototypes. All measurements were done by using on external injection using injection circuit of the readout system situated on the TPLL card, the *Turbo Pixel Low Level* card.
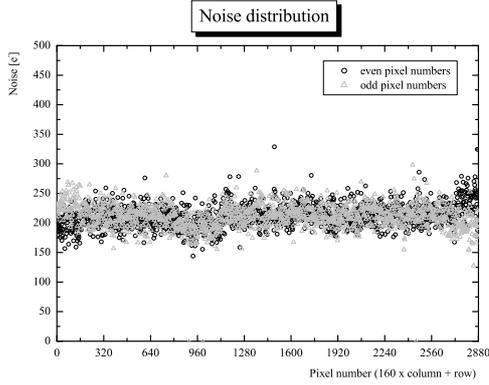
(a) Wu–1–B (EQBZZG)
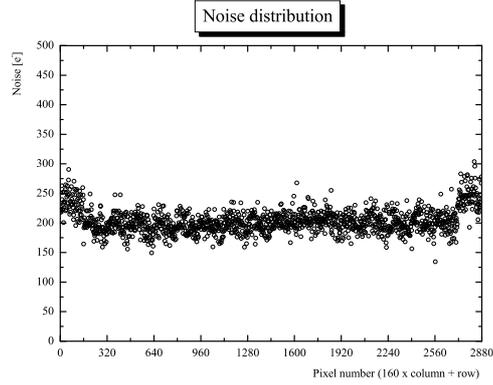
(b) Wu–2–B (STD)
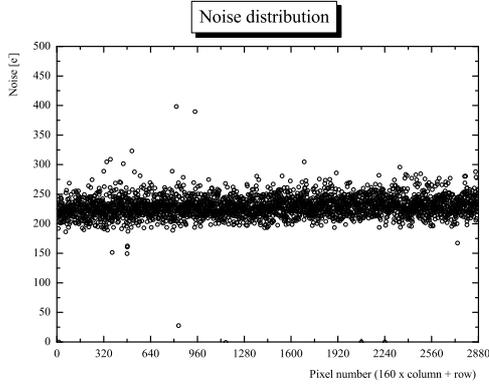
(c) Wu–3–A(EQ)
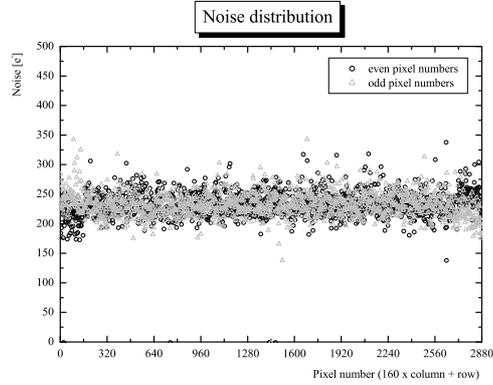
(d) Wu–5–A (EQBPG)

Figure 9.4: Noise distributions of different MCM–D single chips assemblies.

In Figure 9.4(a) the noise distribution shows a uniform behavior in the center of the pixel matrix (columns 1 to 16). The noise is distributed with gaussian shape around a mean value of $\mu_{wu1b} = 212\,\mathrm{e}^-$ and a width of the distribution of $\sigma_{wu1b,1} = 17\,\mathrm{e}^-$. As the capacity of the sensor contributes linear to the electronics noise, the different sizes of adjacent rows in column 0 and 17 increases the noise (for sensor cell size of $5/4\times$ standard size) and down (for sensor cell size of $3/4\times$ standard size).This increases the width of the

	A/A$_{total}$	Wu–1–B		Wu–2–B		Wu–3–A		Wu–5–A	
		μ	σ	μ	σ	μ	σ	μ	σ
EQB std	89 %	212	17					233	18
EQB col 0/17	11 %	215	28					230	26
std	80 %			199	16				
std (long)	15 %			239	17				
std (ganged)	5 %			307	32				
EQ	100 %					202	19		

Table 9.3: Noise measurements on MCM–D single chips (values in electrons).

noise distribution in these two columns to $\sigma_{wu1b,2} = 28\,\mathrm{e}^-$. This effect is expected and could be limited to the border columns of a module in a geometrically optimized layout. This is emphasized by the distinction in grey shade between data points of even and odd row numbers.

In Figure 9.4(b) the noise distribution of an MCM–D prototype with standard sensor geometry is shown. While the noise behavior in the center of the pixel matrix is again uniform, one notices the significant increase of noise in the region of the long sensor cells (column 0 and 17). This corresponds to an increase from $\mu_{wu2b,1} = 199\,\mathrm{e}^-$ to $\mu_{wu2b,2} = 239\,\mathrm{e}^-$ and even $\mu_{wu2b,1} = 307\,\mathrm{e}^-$ for ganged pixel cells.

The most uniform noise behavior is measured - as expected - with the equal–sized prototype (see Figure 9.4(c)). The slightly increased mean value of $\mu_{wu3a} = 229\,\mathrm{e}^-$ ($\sigma_{wu3a} = 15\,\mathrm{e}^-$ compared to the FE–I1B type prototypes is due to the preamplifier difference between these chips. FE–I1A type chips are known to be slightly noisier due to their increased gain in the preamplifier stage. This can also be seen in Figure 9.4(d) ($\mu_{wu5a} = 233\,\mathrm{e}^-/\sigma_{wu5a,1} = 18\,\mathrm{e}^-$) with an increased dispersion of $\sigma_{wu5a,2} = 26\,\mathrm{e}^-$ in the first and last column. Table 9.3 summarizes these numbers and gives the fraction of the concerned sensor area over the total sensor area.

The noise measurements of the geometrically optimized devices prove the feasibility of the advanced routing structure layout in MCM–D. A very uniform noise behavior can be achieved by using equal sized pixel cells. In the case of bricking an enlargement of the width of the noise distribution in the border region of a single chip or a module has to be expected.

Figure 9.5 shows a typical threshold distribution after tuning. Particularly this shows the distribution after fine tuning the threshold to a value of $\simeq 3000\,\mathrm{e}^-$, as preparation for the test beam measurements presented in the next chapter. The threshold distribution shows a sharp mean value of $\mu = 3003\,\mathrm{e}^-$ with $\sigma = 77\,\mathrm{e}^-$. All other chips show similar behavior and can be tuned with comparable quality. Front–end chips of type FE–I1A are usually tuned to values of $5000\,\mathrm{e}^-$ due to the higher gain of their preamplifier's input. The effect of the fine tuning is also pointed out in the next section. No decrease of performance due to the MCM–D routing schemes can be seen in any of the single chip assemblies.

Another lab measurement has been done by investigating the crosstalk between the pixel cells. The crosstalk of a pixel N with a known threshold Q_{thres} (N corresponding to the pixel's row number) is measured by injecting a large charge Q into two pixels $N-1$ and
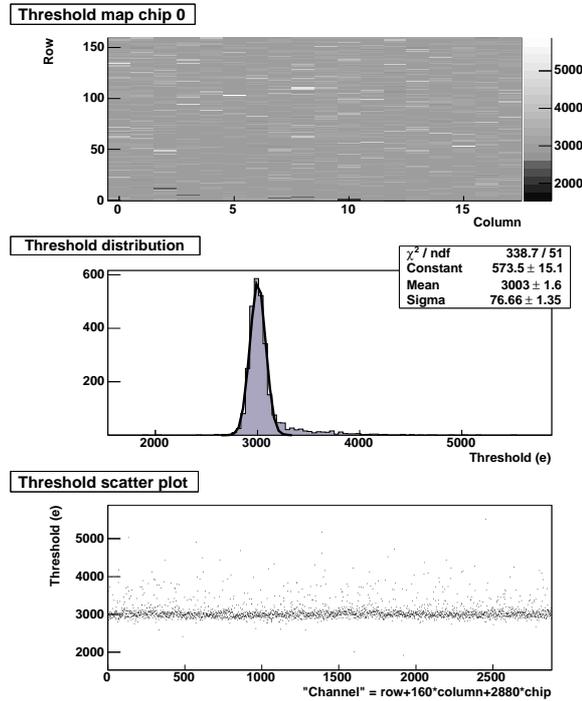
Figure 9.5: Threshold distribution after tuning of Wu–1–B.

$N+1$, which are masked to readout. The response function of pixel N is recorded by the identical procedure as for the determination of the threshold. The point of 50% response, corresponds to a charge of Q_{thres} that has been coupled into pixel N from its neighbors. The crosstalk is then defined as being the fraction of the charge being coupled into pixel N by one of its neighboring pixel cells. This crosscoupling is mainly determined by the inter pixel cell capacitance, dominated by the length of the contact between the two sensor cells. The crosstalk should be kept low (≤ 5–10%) to avoid unintended response from pixel cells, that are not directly hit. The crosstalk does also reduce the signal amplitude, which of course should be avoided. In Figure 9.6 the crosstalk of two prototypes is shown (compare also to Figure 9.14(a) on page 99).

The equal–sized–bricked device delivers a lower crosstalk signal, due to the shorter contact length between pixel cells (shifted by pitch/2). The mean value of crosstalk in column 1–16 is $\mu = 2.42\%$ with $\sigma = 0.13\%$. For the equal–sized device the crosstalk is measured to $\mu = 3.48\%$ with $\sigma = 0.17\%$. Summarizing, the crosstalk of both devices is low and well within the specifications for the ATLAS pixel detector. No major structural dependance, that could originate in the routing structures, is detectable.

9.2.2   MCM–D Hybrid with Front–end I2

One of the MCM–D single chip assemblies has been build, using a front–end chip of the generation FE–I2. In Figure 9.7(a) and 9.7(b) the effect of fine tuning the threshold indi-

(a) Wu–1–B (EQBZZG) (b) Wu–3–A (std)
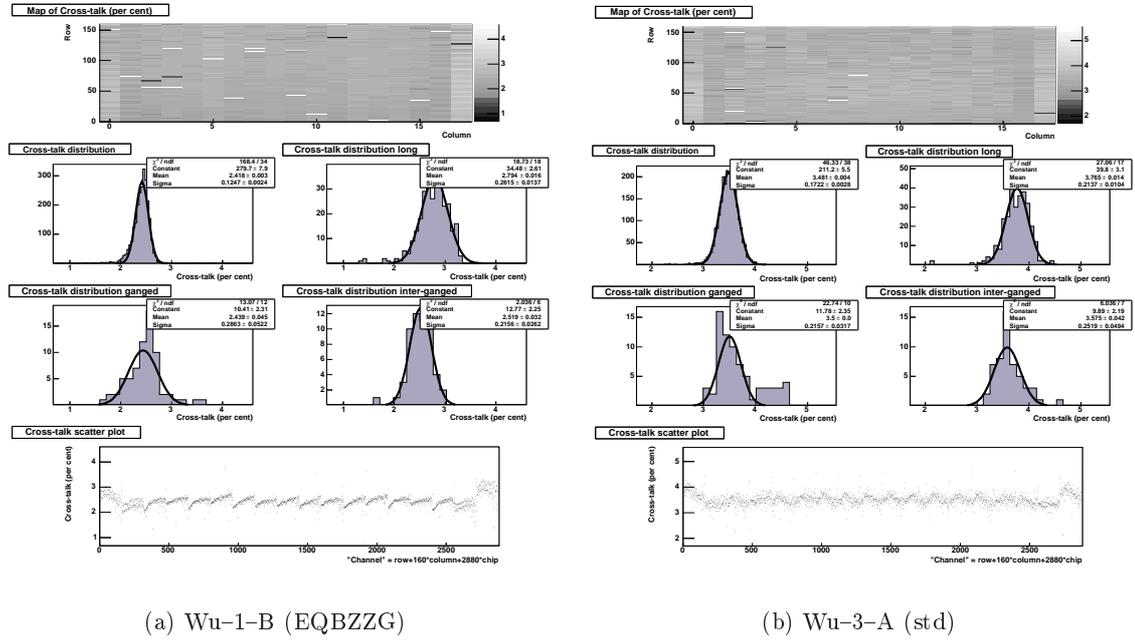
Figure 9.6: Crosstalk of geometrically optimized devices.

vidually for each pixel cell is shown. A reduction of the width of the threshold distribution from $\sigma_1 = 747\,\mathrm{e}^-$ to $\sigma_1 = 64\,\mathrm{e}^-$ after tuning, shows the facility of this adjustment.

Measuring the noise distribution of the prototype to $\mu = 212\,\mathrm{e}^-$ with a width of $\sigma = 13\,\mathrm{e}^-$ as shown in Figure 9.8 reveals no performance degrading influence of the feed–through structures. A small area of unconnected pixel cells in column 4/row 36-41 is detectable by the smaller noise as well as two not responding pixel cells in column 1/row 1 and 2. The missing connection is detectable due to the missing detector capacitance at the input of the pixel cells' preamplifiers. These effects are uncorrelated with MCM–D processing.

Figure 9.9 shows an image of a radioactive source ($^{241}_{95}\mathrm{Am}$) placed on the sensor. In such a measurement the discriminators outputs of all non masked pixel cells are used to generate a trigger signal. A total of 100 000 hits has been recorded with the assembly. Again the small areas of unconnected and dead pixel cells are visible. The very homogeneous response to the radiation of the source is a feature of the equal sized prototypes .
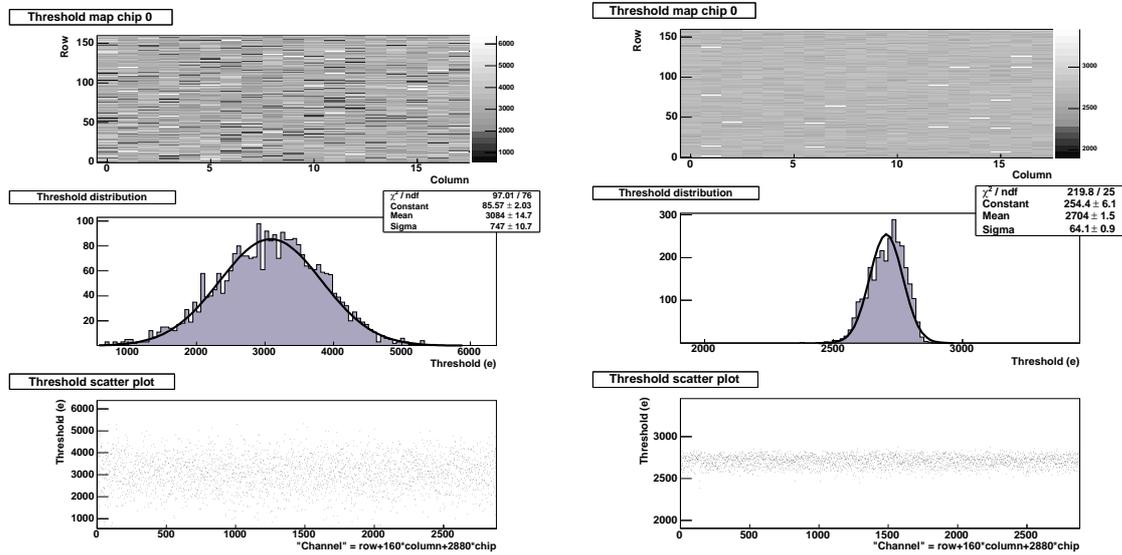
(a) Untuned threshold distribution

(b) Tuned threshold distribution

Figure 9.7: Threshold distribution of MCM–D Wu–6 before and after tuning.
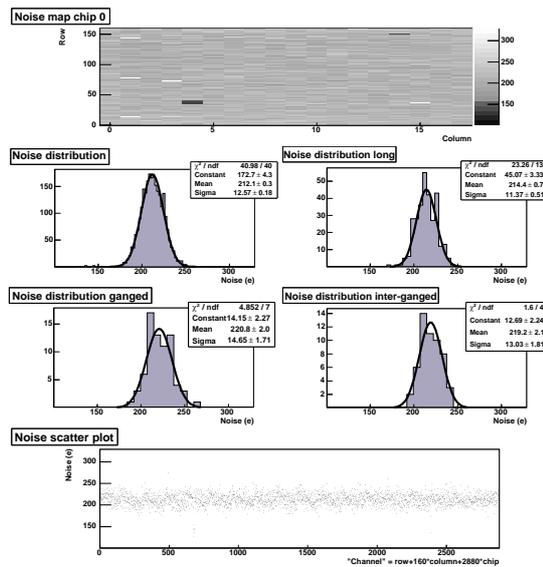
Figure 9.8: Noise distribution of MCM–D Wu6.
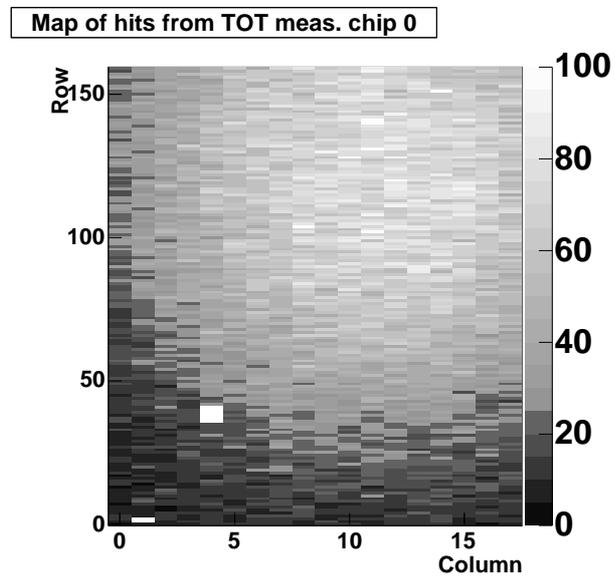
Figure 9.9: Hitmap of MCM–D Wu–6 from source measurement ($^{241}_{95}$Am).

9.3   Irradiation of a MCM–D Single Chip

One of the FE–I1B MCM–D devices (Wu–2–B) has been irradiated at CERN in the period of August 20th–25th in 2003. In the T7 test beam facility a 24 GeV/c proton beam from the PS accelerator is regularly used to irradiate parts of the pixel detector system or other systems. The MCM–D assembly could not be operated during the irradiation. The dose rate was approximately $1.4^{13} \frac{p}{cm^2 h}$ and the irradiation was done in a moderated cooled environment of 15 °C. The total accumulated dose was 50–55 Mrad = 500–550 kGy [61]. This corresponds to layer 1 lifetime dose of the ATLAS pixel detector. After irradiation the assembly was stored at -18 °C until the level of activation was low enough to send it to the University of Dortmund, where the measurements after irradiation were done.

9.3.1   Sensor Leakage

The measurement of the sensors current voltage characteristics before and after the irradiation is shown in Figure 9.10(a) and 9.10(b). A high increase in the current due to the irradiation is visible. This will lead to an expected decrease in performance by the massive irradiation damage in the sensor. Note that this sensor is not oxygen enriched and does therefore not belong to the radiation hardest type of sensors, that are available for the ATLAS pixel detector. All following tests have to be done in a climate chamber at-10 °C to keep the leakage at a reasonable level and to prevent thermal runaway of the sensor, where the high current would lead to an increase in temperature of the device, leading to even higher current and so on.

In Figure 9.11 a measurement of the leakage current per pixel is shown. This is possible due to a new feature of this type of front–end chip. An internal ADC[3] is used to measure the sum of the leakage current and the feedback current in the preamplifier in each pixel. The result of such kind of measurement shows clearly the position of the highest irradiation, where the beam spot during irradiation has been situated. In the lower left corner the maximum dose has been accumulated. Note that this type of measurement can only be done for an irradiated sensor, as in the unirradiated case the feedback current of the pixel cells preamplifier stage is dominant (for FE-I2). In [62] details on tests after irradiation of standard ATLAS pixel sensor prototypes can be found.

9.3.2   Threshold, Noise and Crosstalk

When comparing threshold and noise before and after irradiation (Figure 9.12(a), 9.12(b) and Figure 9.13(a), 9.13(b)) one notices that the threshold dispersion can be tuned to as low as about $\sigma = 100 \, e^-$ even after irradiation. The noise distribution is increased by around $100 \, e^-$ to $\mu = 307 \, e^-$ with a width of $\sigma = 28 \, e^-$ and reveals in its structure also the irradiation level dependance on the position of the pixel cell.

The crosstalk distribution of Wu–2–B in the unirradiated case (Figure 9.14(a)) is centered at a mean value of $\mu_1 = 3.1 \, \%$ with a width of $\sigma_1 = 0.2 \, \%$. The highest crosstalk is measured in row 0 and 17, where the 600 µm long pixel cells are situated. The crosstalk

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[3] ADC: **A**nalog to **D**igital **C**onverter

(a) Before irradiation.

(b) After irradiation.
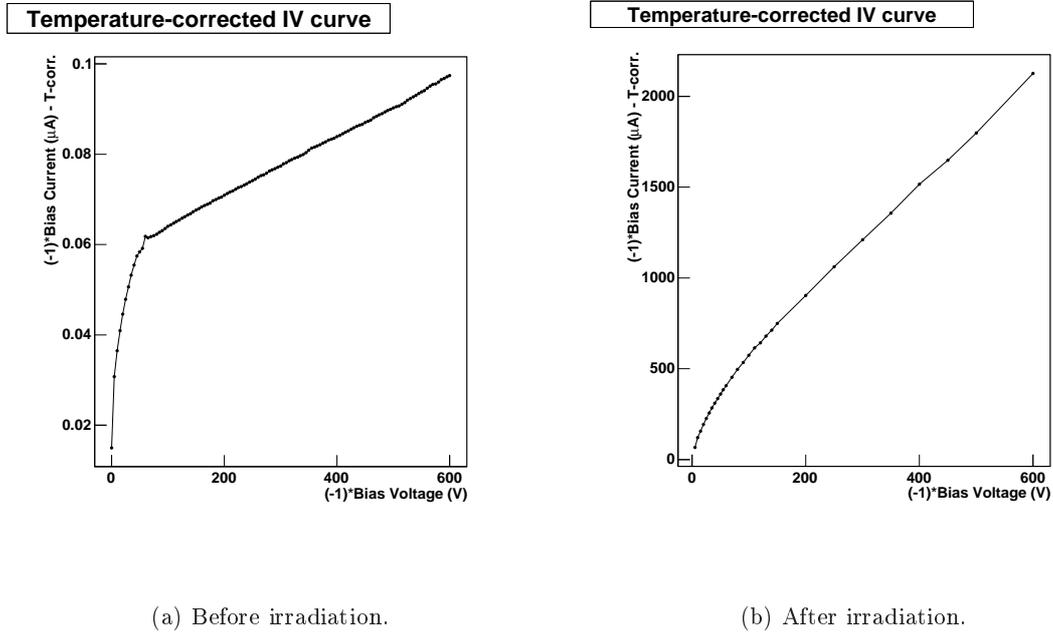
Figure 9.10: Sensor IV curve of MCM–D Wu–2–B (temperature corrected to 20 °C).

is measured here to $\mu_2 = 4.6\,\%$ with a width of $\sigma_2 = 0.3\,\%$. After irradiation the crosstalk is increased by $\Delta\mu_1 = 1.3\,\%$ for standard and by $\Delta\mu_2 = 1.5\,\%$ for the 600 µm long pixel cells.

After a total accumulated dose of 500–550 kGy the assembly Wu–2–B (standard ATLAS pixel geometry) is operational with its mean noise increased by $\simeq 100\,\mathrm{e}^-$ and a slightly increased crosstalk by $\Delta\mu = 1.3\,\%$ for standard pixel cells. Irradiation induced defects in the thin film layers cannot be concluded from the measurements.
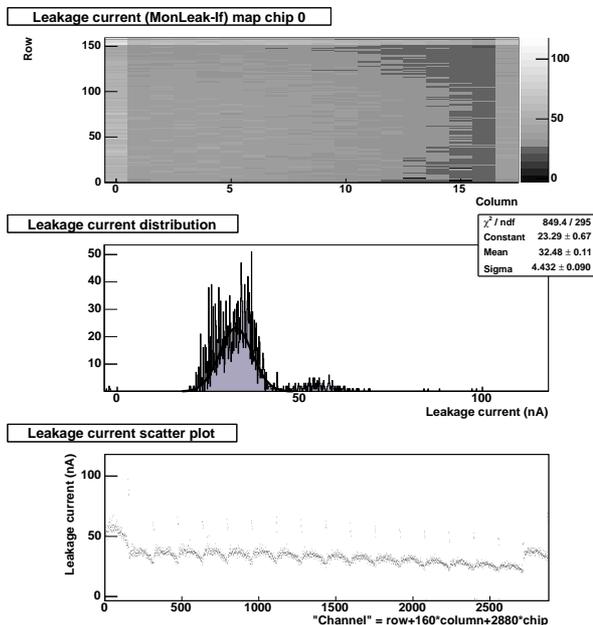
Figure 9.11: Leakage current measurement of MCM–D Wu–2–B after irradiation.
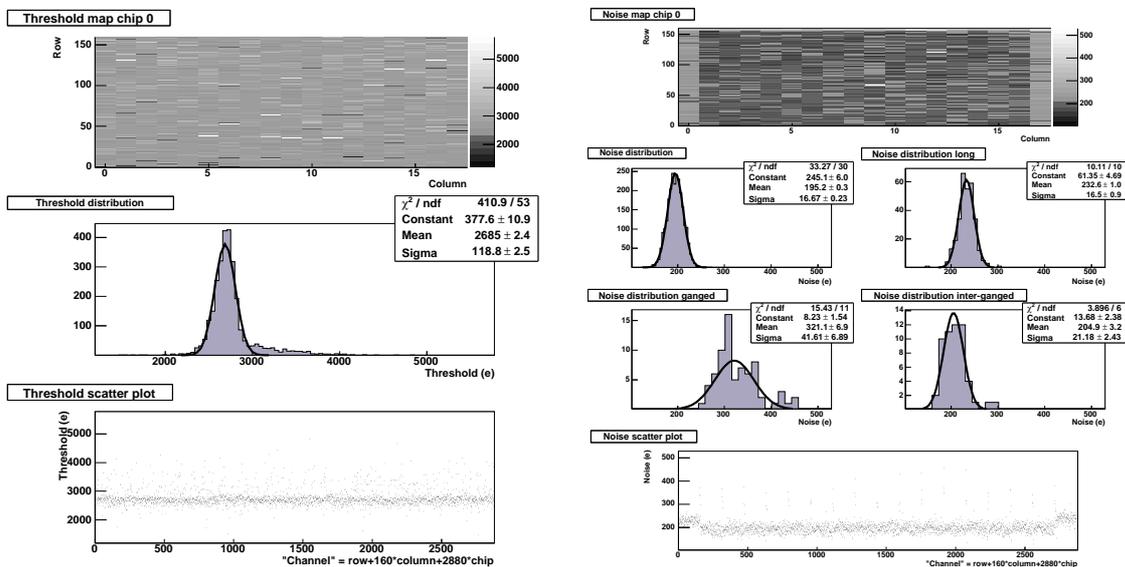
(a) Threshold distribution after tuning.

(b) Noise distribution.

Figure 9.12: Threshold and noise behaviour of MCM–D Wu–2–B before irradiation.

(a) Threshold distribution after tuning.

(b) Noise distribution.
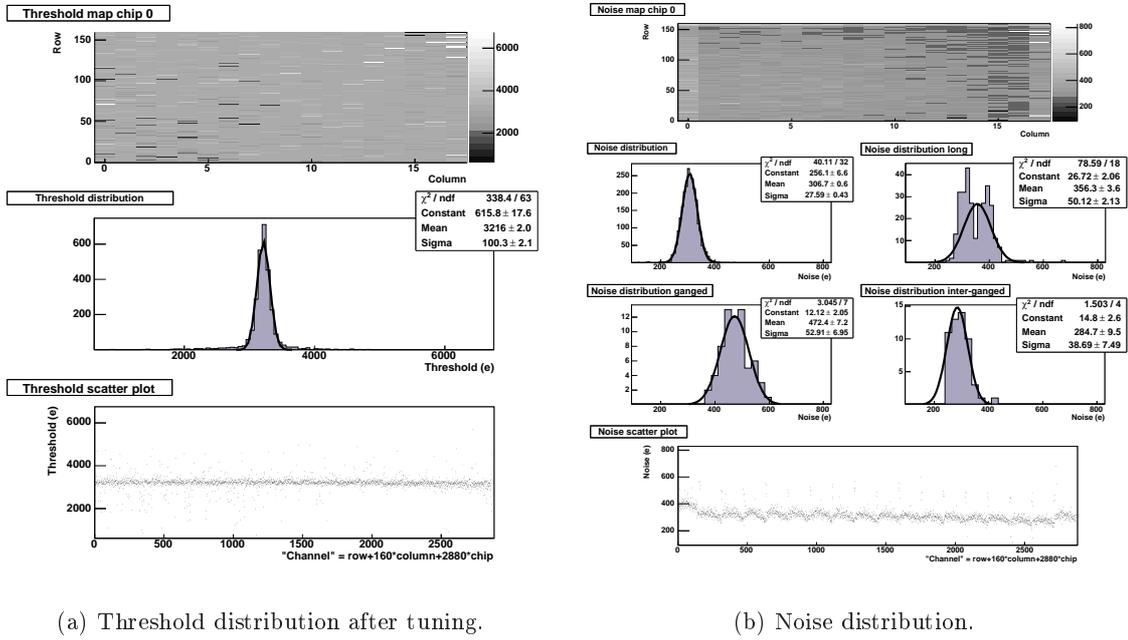
Figure 9.13: Threshold and noise behaviour of MCM–D Wu–2–B after irradiation.

(a) Before irradiation.

(b) After irradiation.
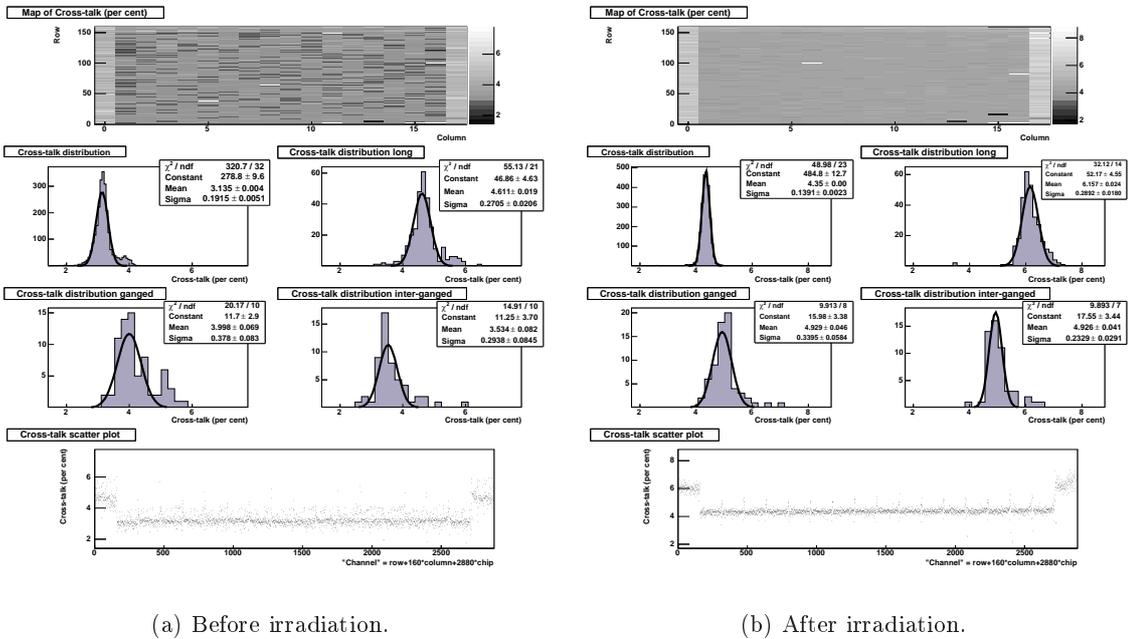
Figure 9.14: Crosstalk behaviour of MCM–D Wu–2–B.

9.4   MCM–D Module
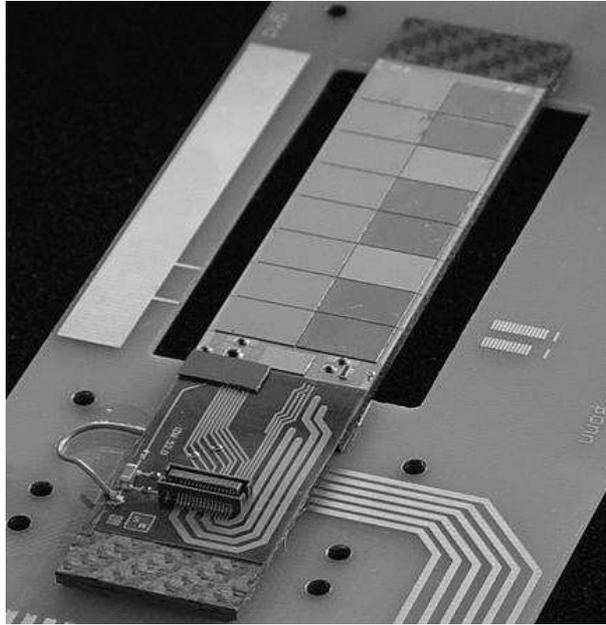
Figure 9.15: Photograph of MCM–D Module 2.

Measurements on the performance of the MCM–D Module 2 are presented in this section. Figure 9.15 shows a photograph of the module. To keep mechanical compatibility to the existing test setups for ATLAS pixel detector modules, the MCM–D module was glued to a custom carbon–carbon support structure. The procedure was done mainly manually using the standard glue for the ATLAS module gluing procedure SE4445 from Dow Corning. SE4445 is a non conducting silicon based two component gel with good thermal conductivity. Prior to this assembly step, the carbon–carbon support structure was glued to a PCB frame holder for ATLAS pixel detector modules. On the MCM–D flexible pigtail the necessary connection to the backside sensor bias voltage contact is visible (compare to 7.8 on page 77).

Module 2 is fully operational and can be read out at highest data rates, which corresponds to the 2×80 Mbit/s configuration. Both data output channels of the MCC (DTO and DTO2) are used in this mode. Typical power consumptions of the prototype in the idle state with configured front–end chips are (voltages sensed on the pigtail):

- $I_{DD} = 750$ mA at $V_{DD} = 2.0$ V

- $I_{DDA} = 825$ mA at $V_{DDA} = 1.7$ V

Figure 9.16 shows an image of the infrared spectrum of Module 2 running at these supply voltages. The cooling is done by using a heat conductive sheet between the carbon support and a underlaying massive aluminum frame, which is in thermal contact to a

cooling system (10 °C). To adapt a height difference an additional thin (1 mm) Al sheet is placed between the carbon and the Al frame. The system therefore cannot be regarded as optimal. Nonetheless the infrared image shows only a moderate temperature gradient along the module. The cooling is sufficient and a spot temperature measurement at the hottest position (MCC) shows a temperature of 22.2 °C. This is in agreement with measurements done with the NTC resistor.
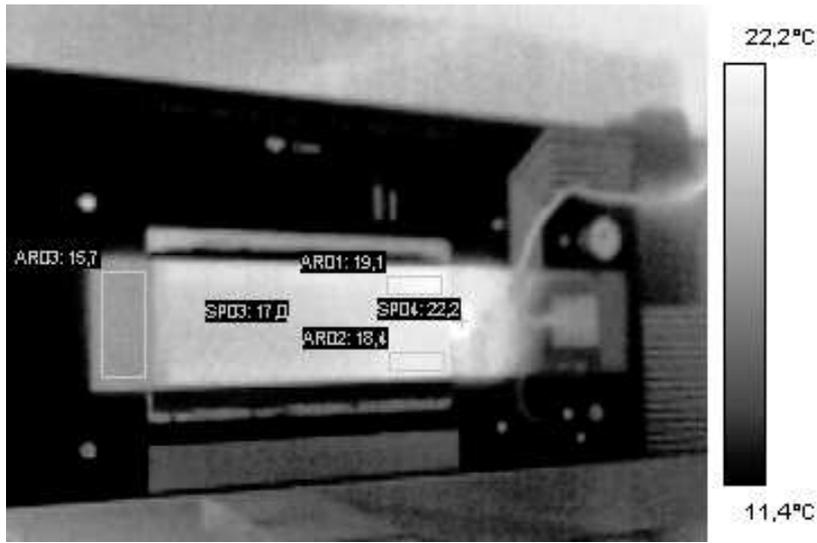
Figure 9.16: Picture from infrared camera of running MCM–D Module 2.

9.4.1   Measurement of Voltage Drop

One of the major requirements of the multi chip module's interconnection system is to keep all supply voltages within the limitation of 100 mV. This guarantees optimal working conditions for all chips on a module. The voltage drop along the sides of the module has been measured under operation using a probe station. The voltages were measured twice per chip on the additional test pads and at the capacitors placed on the main balcony as well as on the redundancy pads on the small balcony.

Figure 9.17 shows the result of the measurement. The voltage were supplied by a Agilent E3631 triple output power supply using sense lines. These sense lines are looped back to the power supplies from the MCM–D pigtail. A voltage drop of 80 mV along the interface between pigtail and the main balcony is clearly visible. This additional voltage drop is due to the suboptimal solution of using Au stud bumping and could be improved by using e.g. soldered connections.

Due to the non homogenous current consumption of the front–end chips the voltage drop is not symmetric between both sides of the module. Nevertheless it does not exceed 100 mV between first and last chip on one side. The power bus system is thus able to supply the module within the voltage drop specifications.
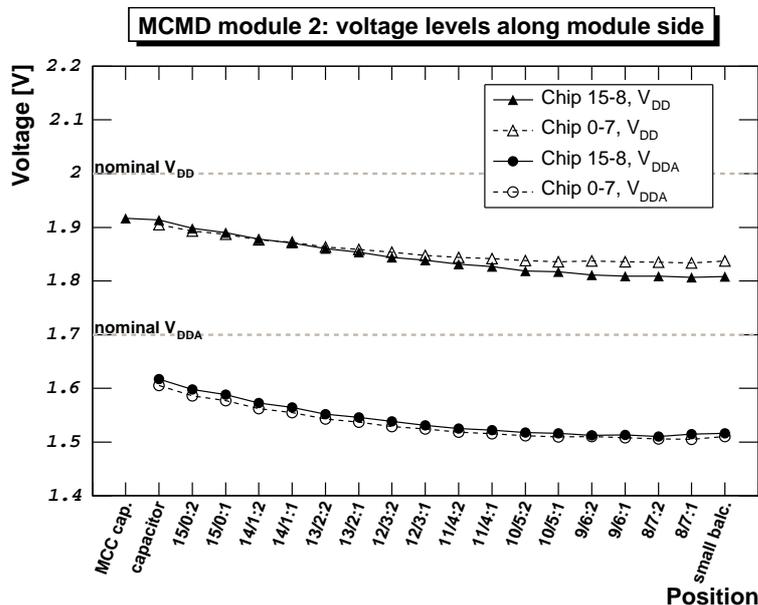
Figure 9.17: Voltage drop measurement of MCM–D Module 2.

9.4.2 Threshold and Noise Performance of MCM–D Module 2

Important properties of a pixel detector module are the threshold distribution and noise performance, similar to a single chip assembly. But the achievable uniformity is more difficult to realize compared to a single chip device, as all 16 chips have to be tuned individually at different supply voltages and due to voltage drop in the module's power distribution system. The same arguments for low noise and good threshold agreement like for the single chip assemblies are valid.

After tuning the threshold to the typical value of $5000\,e^-$ for the FE-I1A front–end prototype a threshold distribution with a mean value $\mu_{thres} = 4958\,e^-$ and a dispersion of $\sigma_{thres} = 169\,e^-$ has been measured. This is shown in Figure 9.18(a). Chips 0, 1, 14 and 15 (compare to 6.7 on page 58) show a slight gradient in their threshold distribution. These areas correspond to the left and right border of the scatter plot shown in Figure 9.18(a). Physically these are the areas closest to the controller chip MCC. There the highest supply currents are flowing under the chips' logic parts and the number of data transmission lines is the highest. The total dispersion of $\sigma_{thres} = 169\,e^-$ is nevertheless very low.

The distribution of the noise values as shown in Figure 9.18(b) reveals much more structure. The mean value of the noise distribution is $\mu_{enc} = 257\,e^-$ with a width of $\mu_{enc} = 23\,e^-$. The areas between the chips, where the noise peaks up, are caused by the longer pixel cell size ($\mu_{enc,long} = 318\,e^-$) and the ganged pixel cells ($\mu_{enc,ganged} = 456\,e^-$, $\sigma_{enc,ganged} = 66\,e^-$). Two areas of small noise ≤ 200 in chip 4 as well as chip 10 and 11 are due to an issue when opening the vias of BCB layer 3. About 1000 pixel cells are affected. This has been regarded as a minor problem as the functionality of the module is not influenced. The efficiency is decreased to $\simeq 98\,\%$. The front–end chip 12 shows
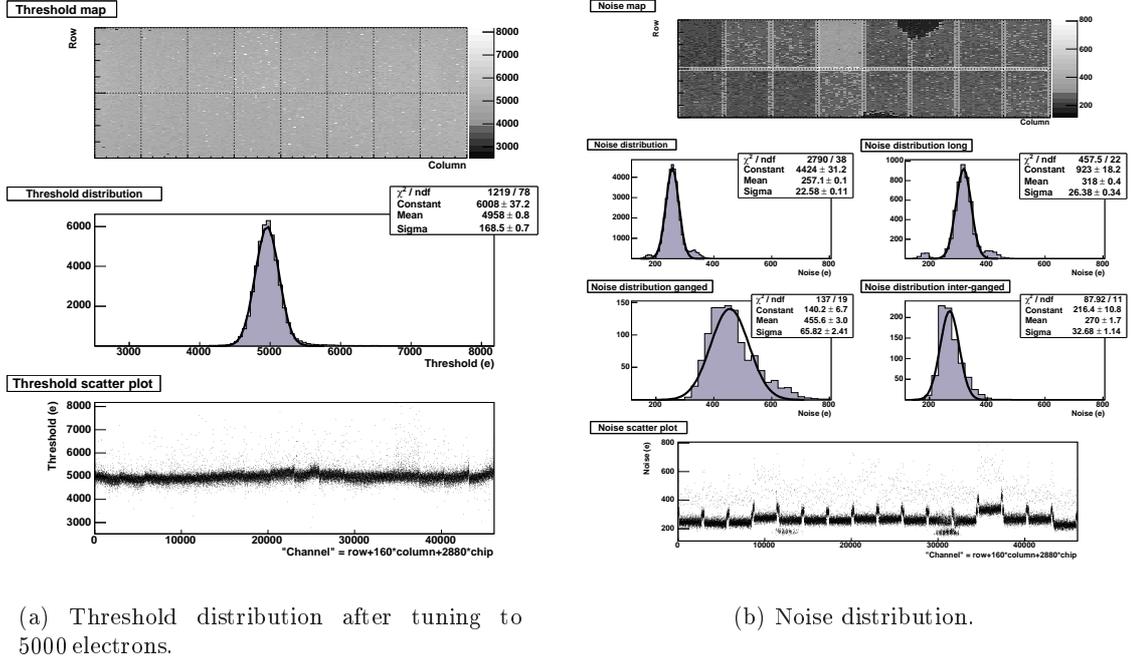
(a) Threshold distribution after tuning to 5000 electrons.

(b) Noise distribution.

Figure 9.18: Analog performance of MCM–D Module 2 (chip by chip test mode).

increased noise. This is due to the lower quality of this front–end chip, as the selection criteria for MCM–D had to be lowered to assemble a full module with FE-I1A chips.

Summarizing the threshold and noise measurement of Module 2, the overall performance is good. The loss of two small areas of pixel cells due to unconnected sensor cells is of minor importance at this stage of prototyping. The contact efficiency is still at $\simeq$ 98 %. The noise is measured to $\mu_{enc} = 257\,e^-$. This is a bit higher compared to standard pixel detector modules, where values around $\mu_{enc} = 200\,e^-$ are expected. In conjunction with the shape of the threshold distribution of the chips closest to the MCC, it is apparent that the decoupling scheme of the module could be improved. Furthermore an optical reinspection under a microscope of the passive components on the modules balcony showed a defect capacitor. The mechanical damage was most probably due to a micro crack in the capacitor and lead to a macroscopic damage during the reflow procedure. The total of 5 capacitors of 0402 size and 100 nF is therefore further reduced by one and the analog supply voltage of chips 15 to chip 8 is not decoupled at all.

This suboptimal decoupling becomes even more apparent when running the module in concurrent mode. In this mode all chips are pulsed and read out simultaneously. The results of a threshold and noise scan in concurrent mode are shown in Figure 9.19(a) and 9.19(b). The increase in the threshold dispersion ($\mu_{thres} = 5056\,e^-$, $\sigma_{thres} = 209\,e^-$), especially for chips close to the MCC is obvious. Now also the noise distribution is affected by the effect ($\mu_{enc} = 282\,e^-$, $\sigma_{enc} = 35\,e^-$). This proves the assumption of a non optimal decoupling, but the good functionality of the module would have been impossible without a high quality interconnection system like the MCM–D system.
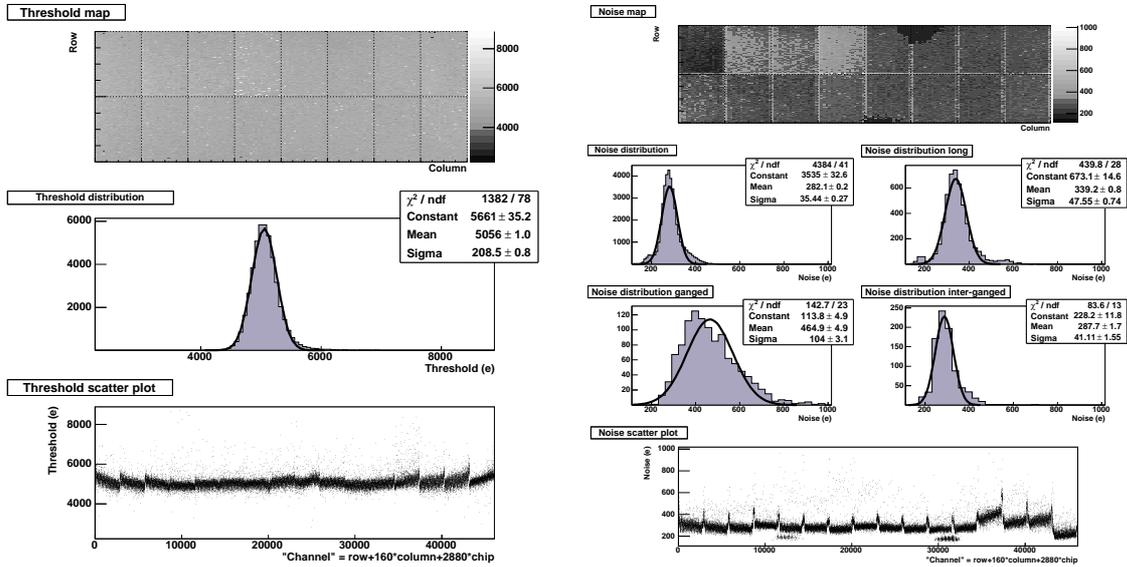
(a) Threshold distribution after tuning to
5000 electrons.

(b) Noise distribution.

Figure 9.19: Analog performance of MCM–D Module 2 (concurrent mode).

9.4.3   Measurements with a Radioactive Source

In Figure 9.20 a measurement of γs from a radioactive source $\left(^{109}_{48}\text{Cd}\right)$ is shown. This has been done by placing the source four times in the middle of each four chip cluster, reading out a total of 500 000 measured hits. One can therefore see four spots of higher count rate, where the source has been placed for each individual irradiation period. As expected the areas of long and ganged pixel cells show a significantly increased count rate due to the larger area they cover. What is a bit surprising is the detection of hits in the two areas of unconnected pixel cells. But Figure 9.21 shows that the mean ToT measured from the hits - as a measure of the mean pulse height - is decreased. The signal from the γ–hit is coupled into the pixel cell, as the isolation BCB layer is only of $\simeq$ 100 nm.

Map of hits from TOT meas.
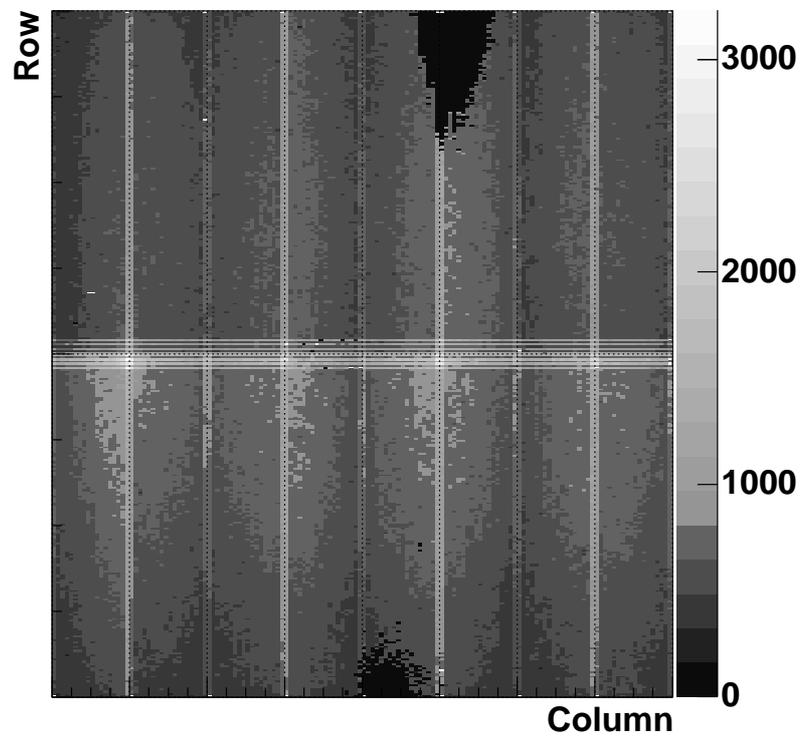
Figure 9.20: Hitmap of MCM–D Module 2 from source measurement $\left(^{109}_{48}\text{Cd}\right)$.
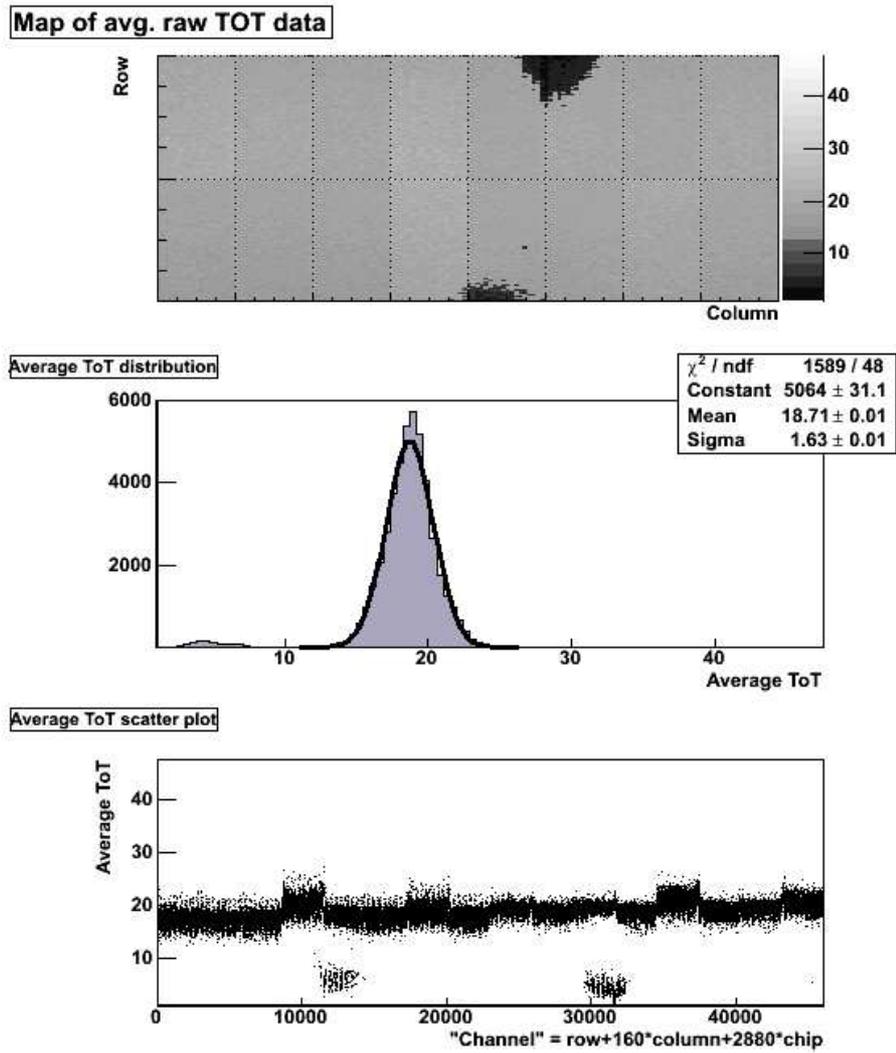
Figure 9.21: ToT measurement of MCM–D Module 2 from source measurement ($^{109}_{48}$Cd).

Chapter 10

Test Beam Measurements

In August 2002 the opportunity to operate MCM–D prototypes in a realistic working environment was taken. Test beam facilities are used frequently for testing newly developed detector systems. At H8, a test beam facility at CERN, the Pixel Collaboration regularly places prototypes in a particle beam of 180 GeV/c pions, which is provided by the SPS. A total of four MCM–D prototypes with different sensor geometries were operated in this test beam environment and an analysis of the accumulated data is presented in this chapter. For a comparison with measurements done with conventional device see [63, 64].

10.1   Test Beam Setup

Major device of the test beam setup is the telescope system, which provides precise tracking information of the incident particles. A dedicated data acquisition system reads out the telescope and several devices under test (DUTs) in parallel. Up to three DUTs were operated in parallel. Furthermore a cooling box monitored by a prototype version of the ATLAS pixel DCS[1] system was available. Both the data of the telescope system and of the devices under test is written to permanent storage at the CERN CASTOR[2] system.

The analysis of the data is a two staged process. At first the stored raw detector data have to be decoded and treated, which is done by the h8 software, developed by the Milano ATLAS pixel test beam group. H8 produces correlated data on the basis of individual trigger events with detailed track description and the DUT data in the form of *ntuples*. As a second step, these informations have to be treated by a local analysis procedure. In our case this was based on ROOT, an object oriented data analysis framework developed at CERN.

10.1.1   BAT

The *Bonn* ATLAS *telescope*, BAT, is a novel high speed beam telescope based on several individual modules of silicon microstrip detectors. It consists of four double sided detector

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[1] DCS: **D**etector **C**ontrol **S**ystem
[2] CASTOR: **CERN** **A**dvanced **Stor**age Manager

assemblies. These are commercially available detectors with a sensitive are of $3.2 \times 3.2\,\mathrm{mm}^2$, featuring 640 AC–coupled strips on each side, with a stereo angle of $90\,^\circ$. Figure 10.1 illustrates the setup. The rate of recordable events has been $7.6\,\mathrm{kHz}$. Details on this system can be found in [65]. There the resolution of the system is calculated to be better than $\sigma_{BAT} = 5.5\,\mathrm{\mu m}$.
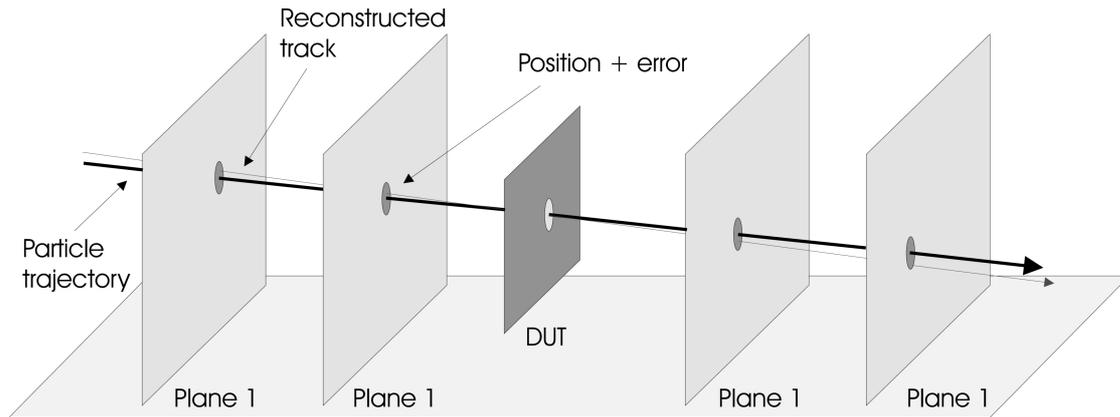
Figure 10.1: Cartoon of the test beam telescope system, from [65].

10.1.2   H8 Software Package

The h8 software package is able to decode the recorded data from the BAT system as well as the earlier system of the *Marseille telescope* and is based on FORTRAN. The package features the treatment of different DUT orientations as shown in Figure 10.2. The procedure for the treatment of test beam data with h8 is to initialize a database with the main information about the run and the DUT (chip type, orientation etc.) one wants to analyze.

Consecutively one then wants to:

- provide a mask information and determine noisy and dead strips in the telescope system and pixel of the DUT.

- Determine the charge weighing function for double hits in the strip detectors to increase the precision of the reconstructed track (η–distribution, similar for pixel double hits, see 10.4 on page 115).

- Do the alignment between the strip planes and the DUT planes. The alignment procedure determines the relative position between the 4×2 strip detectors and the DUT. The first plane of strip detectors defines the origin of the coordinate system (see Figure 10.2). The alignment procedure uses events of isolated, single clusters in the strip and the pixel system. The offset between the planes in x, y and z and a possible tilt angle is determined by an iterative fitting procedure. The determination of the strip position is done by multiplying the strip number by the strip pitch of
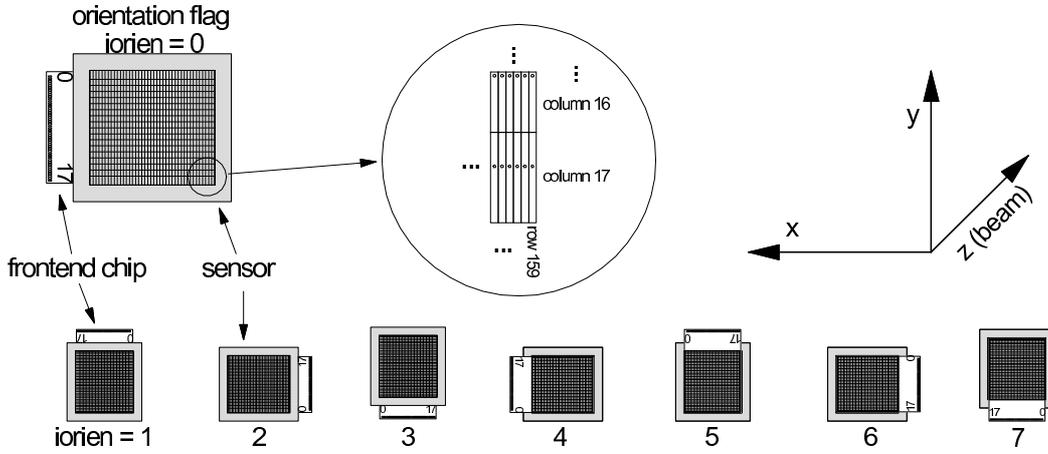
Figure 10.2: DUT Orientation and coordinate system for Test beam Analysis.

50 µm and applying the η–correction. The pixel position cannot be easily determined due to the different pixel cell sizes. The transformation from row and column number to xy–position is done by subroutines in the file transform.f, which is part of h8. The custom geometries of the equal sized and equal sized bricked devices are implemented in a local version of h8 in transform.f.

- Last step is the production of the ntuple, which contains a full description of a triggered event, including track parameters, pixel hits, track extrapolation to the pixel plane. The alignment data from the last step are used during this procedure. A mask file can be included during this step, to exclude noisy or dead pixels from the analysis. An optional ToT calibration file can also be provided. The ToT calibration file includes information on the response of the individual pixel cells to the injection of charge in terms of the ToT. The correlation between charge and ToT is well described by a function of three parameters A,B and C, which are determined by a least square fit and saved in the calibration file. This is done by a standard laboratory measurement. In Figure 10.3 the dependance of the ToT on the injected charge Q is plotted for 1/10 of all pixels of the Wu–1–B device. The function:

$$Q = \frac{B}{\text{ToT} - A} - C \tag{10.1}$$

allows the calculation of the energy deposited by a hit in the pixel detector. If the calibration file is provided to the h8 software, the charge information will be stored in the resulting ntuple file.

More detailed information on the h8 software as well as on the data format of the ntuple is available in [66]. Version h8-03_04_03 of the software package has been used throughout this analysis.
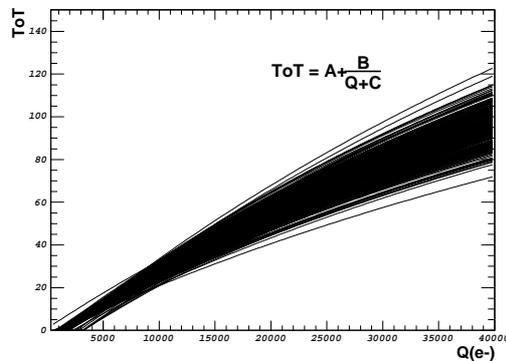
Figure 10.3: ToT Calibration Curves of Wu–1–B as used for the test beam analysis.

10.1.3   Data Analysis

To obtain a sample of conclusive events, a couple of cuts are applied to the data. The basic strategy is described here.

1. The track of the incident particle must have been fitted through the telescope's reference points with a reasonable probability. The corresponding variables prbx and prby, which give the probability of determining a χ^2 greater than the observed one, are required to be > 0.02, which leaves $\simeq 50\%$ of the data for analysis.

2. The track extrapolation has to be in the pixel matrix of the DUT. This is done keeping a margin of 40 μm to the border of the DUT. The fraction of lost events due to this cut is determined by the quality of the positioning during data taking.

3. Tracks that are predicted to hit a pixel adjacent to a noisy or dead pixel are also discarded.

A typical run of a total of $\simeq 300\,000$ events loses about $\approx 60\%$ of the events due to these cuts, so that a reasonable statistics is available for the analysis.

10.2   Devices Under Test

The following MCM–D prototypes have been tested in the August 2002 test beam period:

- WU–1–B, equal sized bricked, bias grid in zigzag configuration,

- WU–2–B, standard pixel design,

- WU–3–A, equal sized,

- WU5A, equal sized bricked, bias grid in parallel configuration.

All devices have been operated without problems. Figure 10.4 shows a 2–dimensional histogram of the hits registered by two pixel devices (Wu–1–B and Wu–2–B) during one run of 300 kevents. The position of the beam spot is visible in both devices. As expected the equal sized bricked device Wu–1–B shows a uniform behavior, while Wu–2–B (standard geometry) shows increased count rate in the column 0 and 17 (long pixel) as well as in the region of the ganged pixel of row 152 and above.
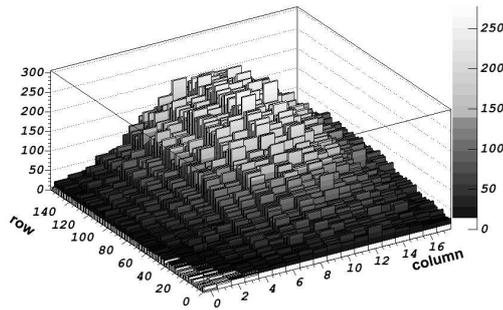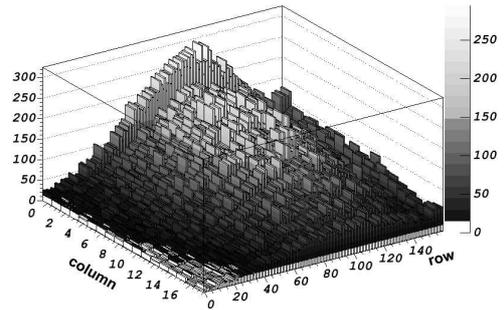
(a) WU–1–B   (b) Wu–2–B

Figure 10.4: Beam spots on single chip devices (single run, single hits).

10.3   Charge Collection

The energy deposited by a particle is reconstructed by using the ToT calibration files as described in Section 10.1.2. In Figure 10.5 the measured energy deposition is shown for all reconstructed hits, including clusters. This example (Wu–1–B) shows the distribution of the measured charge, which is well described by a convolution of a landau distribution, describing the energy deposition in the sensor, and a gauss distribution describing the noise influences and other uncertainties. The most probable value of deposited energy is 24.27 ± 0.01 kelectrons. This is determined from more than $1\,370\,000$ hits in the pixel detector.

Figure 10.5:   Reconstructed energy from test beam data for all hits in Wu–1–B.

In Figure 10.5 the data of single hits and all multiple hits (clusters) are combined. These clusters are built whenever more than one hit in the pixel system is reported. If the row or column difference of an additional pixel hit is too large, a new cluster is established. If more than one cluster is registered, the one closest to the track prediction is chosen for the analysis. In Figure 10.6 the reconstructed energy of single hits and of double, triple and quad hit clusters is plotted separately as histograms for each DUT on a semilogarithmic scale.

The behavior for single and double hits of the four devices is very similar. All devices show a small fraction of decreased charge for the single hits. A major difference can be seen in the rate and measured charge of triple and quad hit clusters, where the equal sized bricked devices show an increased triple and a decreased quad hit count rate, which is expected due to the geometry of the sensor cells. The equal sized device (Wu–3–A) shows an almost identical behavior compared to the standard sensor Wu–2–B. The complex routing structure in the feed–through area of the equal sized device introduces no measurable charge losses.

Figure 10.7: Pixel symmetry unit of Wu–5–A.

To take a closer look on the different geometries, one can examine the mean collected charge versus the extrapolation of the track relative within groups of pixel that form a symmetry unit. As a symmetry unit, a group of four pixels has been chosen for the standard, equal sized and equal sized bricked with zigzag bias grid devices. The parallel grid implementation (Wu–5–A) requires a group of three pixel cells as unit as indicated in Figure 10.7. The pixel cell metallization is shown in grey; the bias grid implementation is also visible. The upper pixel cell has an intersected met-
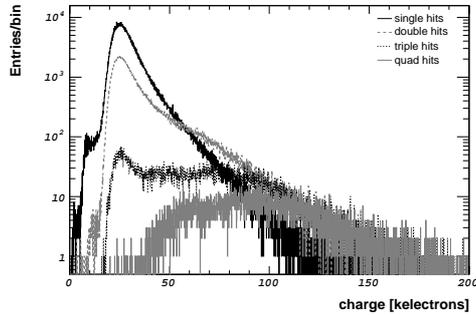
(a) Wu–1–B (EQBZZG)
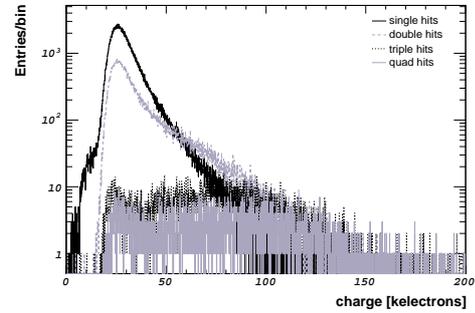
(b) Wu–2–B (Standard)
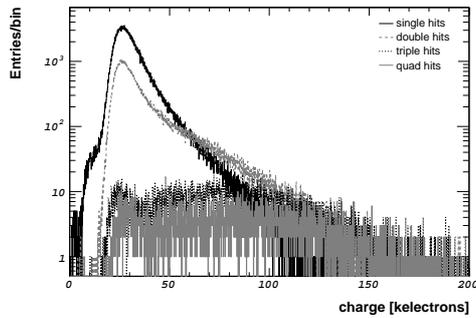
(c) Wu–3–A (EQ)
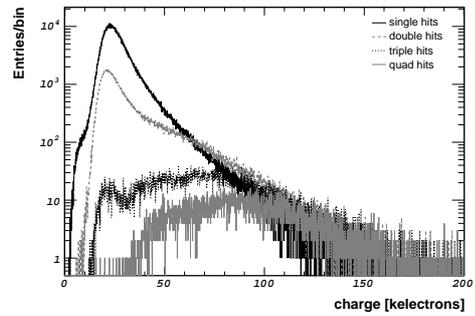
(d) Wu–5–A (EQBPG)

Figure 10.6: Measured charge reconstructed from ToT measurement.

allization. In Figure 10.8 the predicted local position in the symmetry unit of the devices are shown. The pixel surface defines the xy–plane. On the z–axis the mean charge per bin is plotted.

Points of decreased collected charge are visible for all devices. These areas are the positions of the bias dots. It is known that charge losses in these areas exist. The level of charge loss is also visible in Figure 10.6 as single hits with reduced charge, visible as left shoulder in the single hit curves.
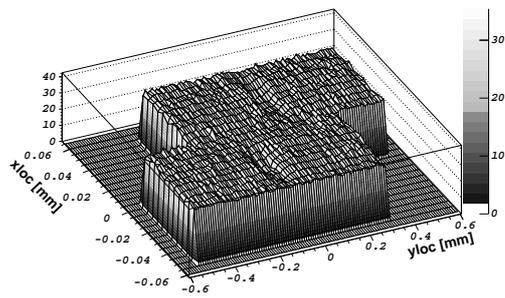
(a) Wu–1–B (EQBZZG)
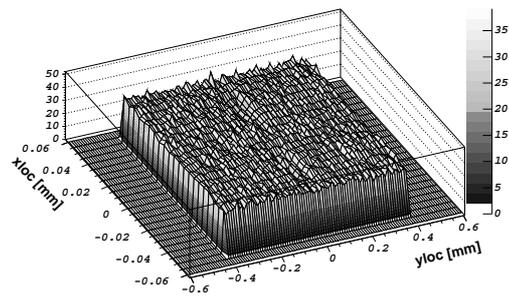
(b) Wu–2–B (STD)
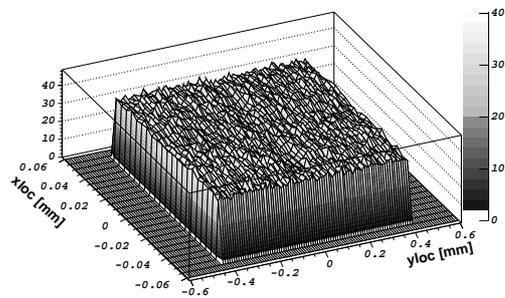
(c) Wu–3–A (EQ)
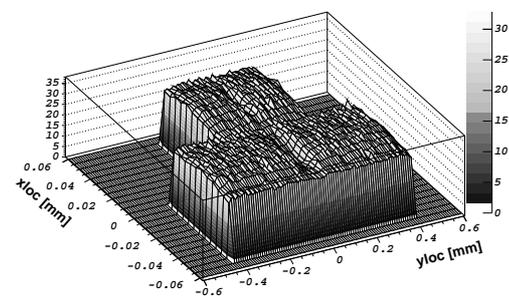
(d) Wu–5–A (EQBPG)

Figure 10.8: Collected charge vs. local track prediction of different MCM–D single chip assemblies.

10.4   Spatial Resolution

To determine the spatial resolution of the devices under test, one calculates the difference between the position of the particle's impact on the pixel detector surface, as predicted by the telescope. The measured hit corresponds to the center of the responding pixel in the case of single hits. For double hits, one can either calculate the mean of the positions (digital algorithm) or apply the charge weighted correction of the η–distribution to the position measurement (analog algorithm). The charge weighing function if given by:

$$\eta = \frac{Q_{hit1} - Q_{hit2}}{Q_{hit1} + Q_{hit2}} \times w \tag{10.2}$$

Where $Q_{hit1,2}$ corresponds to the charge registered for each hit and w is the width of the charge sharing area between the two pixel. w is determined experimentally. Note that the position of triple hits is determined by counting each row, from where hits were reported, only once.
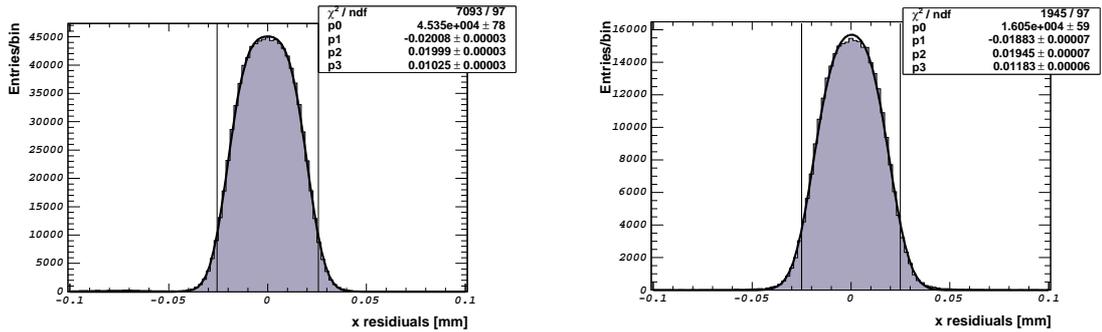
(a) Wu–1–B (EQBZZG)   (b) Wu–2–B (std)

Figure 10.9: Residuals in x for single hits (short pixel direction $= 50/51.25\,\mu$m) of different MCM–D single chip assemblies. The plotted vertical line corresponds to the borders of a pixel ($= \pm$ pitch/2).

Figure 10.9 shows the residuals in x of two DUTs. The x–direction corresponds to the short direction of the pixels ($50/51.25\,\mu$m) and was chosen as most data has been taken in the DUT orientation iorien $= 0$ (compare to 10.2 on page 109). The fitted function is an assembly of two error functions. Parameters p1 and and p2 correspond to the positions of 50% of the overall height (p0). Parameter p3 gives the σ of the error functions of the distribution. Both devices are in good agreement. Fitting the distribution by a simple gaussian distribution results in a resolution of 13.7 µm which is in agreement to the expectation of $51.25/\sqrt{12} = 14.8$ µm. In Figure 10.10 the absolute values of the residuals in x are shown for all four DUTs on a semilogarithmic scale. The double hit position has been calculated using the digital algorithm. Double, triple and quad hits have

been shifted by half of the pitch to visualize the position of their origin. The 0–position of
the x–axis correspond to the center of the pixel.

The residuals show the expected behavior and are very similar between the different
DUTs. This is as expected because the only difference is the slightly increased pixel size
of 50 µm for a standard sensor cell and 51.25 µm when using the equal sized option.

(a) Wu–1–B (EQBZZG)   (b) Wu–2–B (STD)

(c) Wu–3–A (EQ)   (d) Wu–5–A (EQBPG)
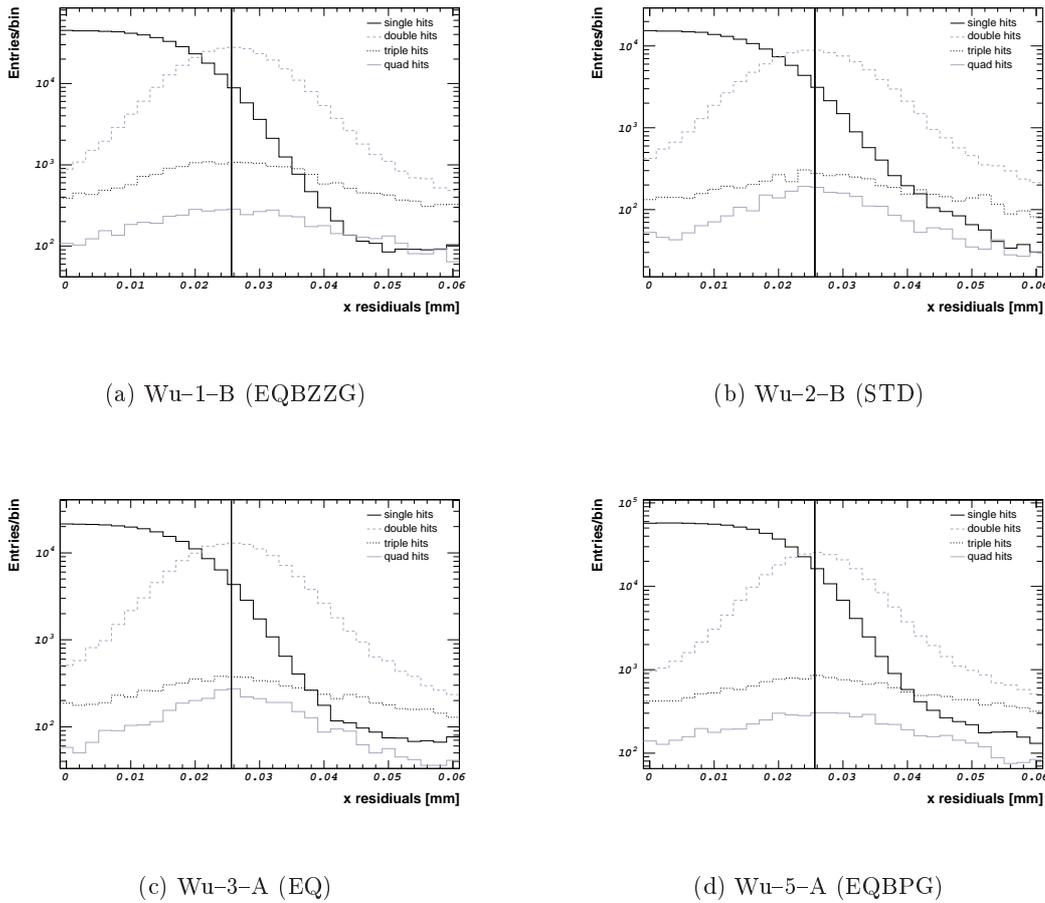
Figure 10.10: Residuals in x (short pixel direction = $50/51.25\,\mu$m) of different MCM–D
single chip assemblies.
The plotted vertical line corresponds to the border of a pixel (=pitch/2). Residuals for
double and triple and quad hits have been shifted by pitch/2 to emphasize the position of
the area, where most double/triple/quad hits are registered.

The double hit resolution for the digital reconstruction is shown in Figure 10.11 at the
example of the DUT Wu–1–B. The resolution is $\sigma = 8.5\,\mu$m. This can be improved by
applying the charge weighted correction (Equation 10.2). The double hit residuals in x
direction, calculated by using the analog algorithm, are shown Figure 10.12 for all devices
under test. The resolutions are between $\sigma_{EQBPG} = 7.3 \pm 0.1$ µm and $\sigma_{std} = 8.4 \pm 0.1$ µm.
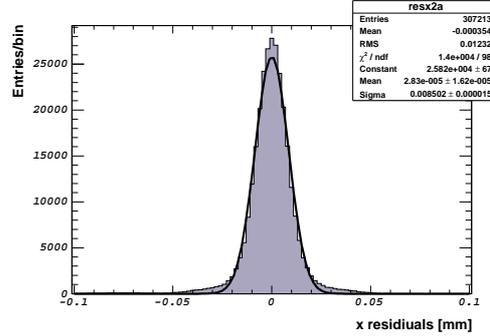
Figure 10.11: Residuals of double hits (digital algorithm) in x (short pixel direction = $51.25\,\mu$m) for Wu–1–B.

Note that the distribution for Wu–2–B (10.12(b)) includes the residuals of tracks that are predicted to hit the region of the ganged pixels.

The residuals in the y–direction (the $400/422.22\,\mu$m direction) are shown in Figure 10.13 for all devices. The single hit residual distribution of the standard device has a two step shoulder on the right flank. This is a result of the 600 µm long sensor cells in column 0 and 17 and of the 40 µm gap between track extrapolation and the border of the device. The sensor cells of $3/4 \times pitch$ and $5/4 \times pitch$ size of the equal–sized–bricked devices were taken out of the analysis for better illustration. This would lead to comparable effects in the residual distributions.

The double hit resolution is purely digital and has an additional cut of forcing the two pixel cells hits to be in a different row. Double hits from clusters, where the two hits are in adjacent columns and the same row, produce a sharp peak in the center of the double hit residual distribution. The double hit (and quad hit) residuals have been shifted by half of the y–pitch for better illustration. The benefit of bricking the sensor cells, i.e. shifting the rows by $\pm 1/4$, becomes clear in the double hit residuals. While the standard and the equal–sized devices cannot determine the position of a double hit more precise than the y–pitch (Figure 10.13(b) and 10.13(c)), the resolution is enhanced by a factor of two for the bricked devices (Figure 10.13(a) and 10.13(d)). For the bricked devices also the triple hits originate from a small area visible by the peak around zero in Figure 10.13(b) and 10.13(c). This corresponds to the center between three pixel (see Figure 10.7 on page 112), whereas a similar behavior is visible for quad hits in the standard designs.

Another feature of the bricked devices is a higher count rate for single hits at the y–center of the sensor cell. Figure 10.14 shows a 2–dimensional histogram of the single hit residuals for the device Wu–1–B. One notices that around the y–center of the hit distribution the origin of some hits is in the neighboring row. In the two adjacent pixel cells no hits are registered. The reason for this is that the deposited charge in these two pixels is to small to exceed the threshold of the electronics channel. However the hit is still recorded as a single hit and thus leads only to a slight decrease in resolution. In a standard design such hit would be invisible as the signal is spread to 4 pixel cells.
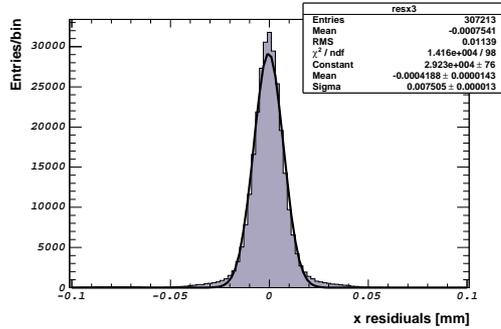
(a) Wu–1–B (EQBZZG)
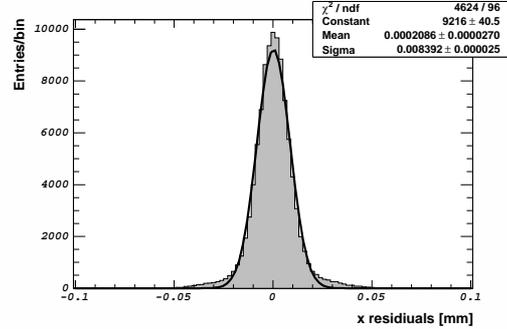
(b) Wu–2–B (STD)
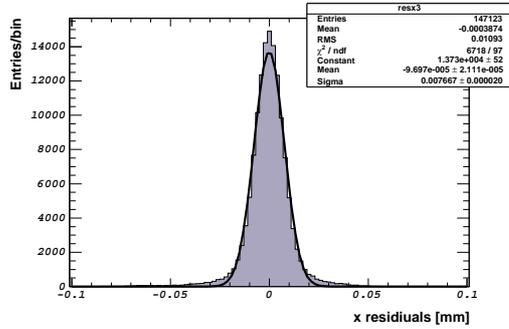
(c) Wu–3–A (EQ)
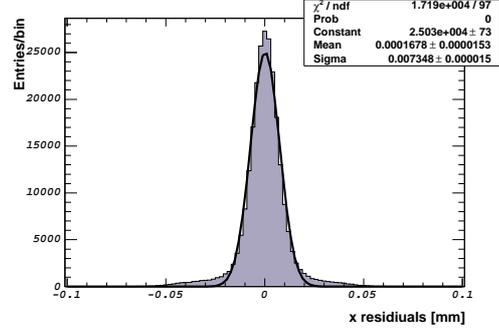
(d) Wu–5–A (EQBPG)

Figure 10.12: Residuals of double hits (analog algorithm) in x (short pixel direction = $50/51.25\,\mu$m) of different MCM–D single chip assemblies.

Considering the area where the double and triple hits originate, Figure 10.15 shows the predicted hit location relative in the same symmetry unit as in 10.8. Triple hits are recorded when the incident particle hits are close to the contact point of three pixel cells. Double hits are recorded along all sides of the pixel cells. The number of increased hits in Figure 10.15(a) and 10.15(b) in the area where the pixel cells border on each other is an artifact caused by the histograms' binning.

As a conclusion out of the test beam analysis done on four MCM–D type single chip assemblies with different geometries, one can state that the principle operation of the equal sized and equal sized bricked devices showed no difference compared to standard ATLAS pixel geometry. The benefits of the optimized devices were clearly observed. The charge collection of the sensors showed a slight decrease in signal size around the implemented bias grid dots, which is also known for standard devices. The influence of the routing structure on the performance was shown to be negligible. The spatial resolution of the

devices revealed the expected enhancement for double hit resolution in the long direction of the pixel cells while the single hit resolution remained of the same performance. Another advantage of the equal sized devices was the simplification of the reconstruction algorithm, compared to the unpleasant different treatment of the enlarged and ganged sensor cells, when using the standard ATLAS pixel geometry.
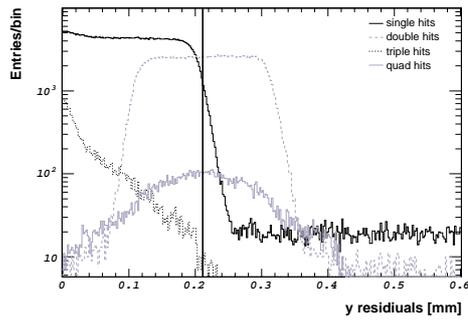
(a) Wu–1–B (EQBZZG)
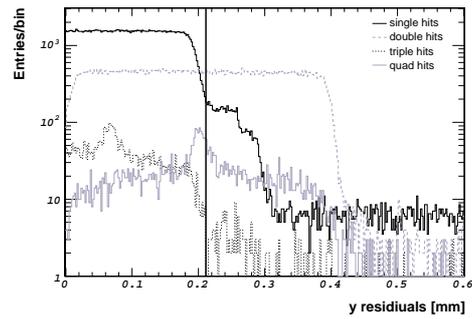
(b) Wu–2–B (STD)
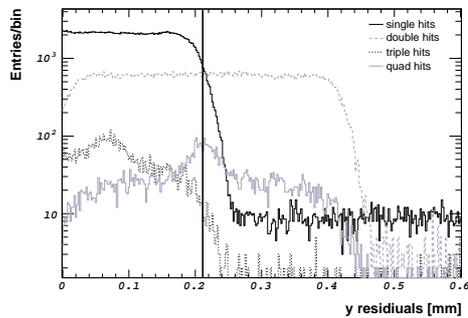
(c) Wu–3–A (EQ)
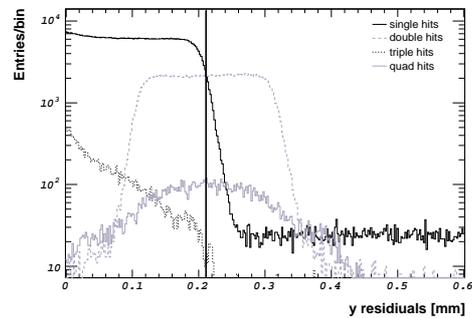
(d) Wu–5–A (EQBPG)

Figure 10.13: Residuals in y (long pixel direction = $400/422.22\,\mu$m) of different MCM–D single chip assemblies. The plotted vertical line corresponds to the border of a pixel (=pitch/2). Residuals for double/quad hits have been shifted by pitch/2 for better illustration.
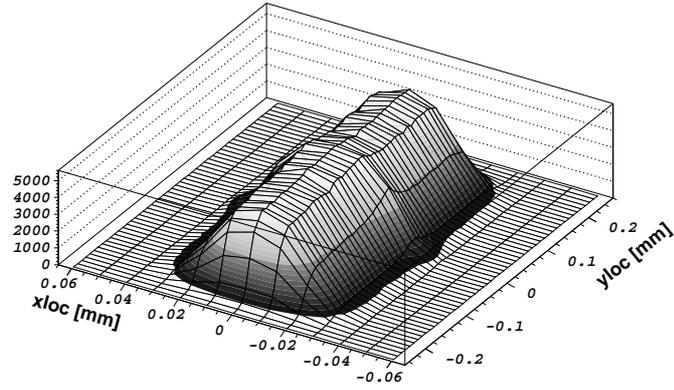
Figure 10.14: Residuals in x and y of single hits for Wu–1–B.
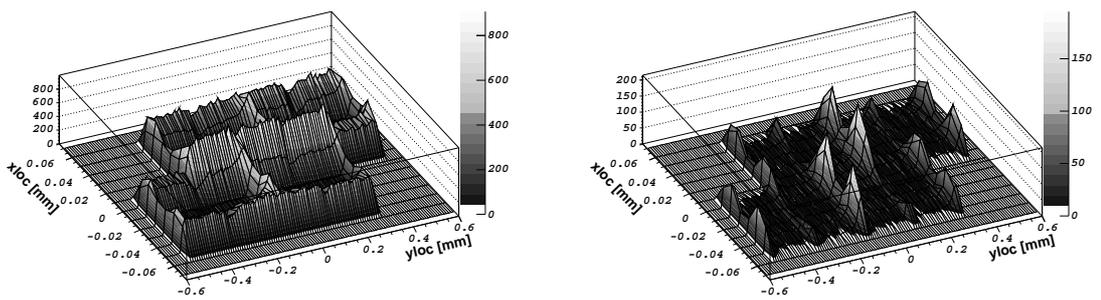
(a) Double hits

(b) Triple hits

Figure 10.15: Track prediction of different cluster sizes (Wu–1–B).

Chapter 11

Aspect of MCM–D Processing

Multi chip modules for high energy physics experiments can be improved by using technologies of the semiconductor industry, like thin film technologies and wafer level packaging. The MCM–D technique has been a field of research during the development of the ATLAS pixel detector over several years. A summarizing review based on our experience under the aspect of a production approach is given in this chapter.

11.1 Yield Aspects of the MCM–D Production

The production of MCM–D modules can, as described in this thesis, be split into two major parts. One major part is thin film processing, including the design of MCM–D structures and processing up to the time when an MCM–D module has been cut out of the wafer. The second part is the further assembly, which includes the flip chip process, pigtail attachment etc. until the module can be operated in laboratory.

11.1.1 The Thin Film Processing - MCM–D

This part of the production has undergone a major improvement. Starting from 11 sensor wafers, a total of 6 Modules was built and 5 of these have successfully gone through the MCM–D processing, which is a yield of 45 %. A variety of optimizations during the full MCM–D process was necessary to achieve this and further measures could improve the yield further:

- Cleanliness of the sensor wafer. The sensor tiles were not designed especially for MCM–D and therefore dicing streets were situated below the thin film bus system. This remained a problem even after the implementation of a new cleaning procedure. A sensor tile design better suited for MCM–D processing is recommended for a larger scale production.

- Instead of using large Cu areas for the power distribution system using mesh–type structures could be more appropriate. If the demands on the power distribution system allow this kind of implementation the increased thickness at the border of large metal areas can be prevented [67].

- Large part of automation. A modern fully automatized spin coater systems is able to process thin film layer like Photo-BCB or photo resist including the curing steps. After the final definition of all process parameters, which always takes some runs to achieve stable results, this involves a minimal amount of human interference. This should be combined with a fully automated processing including mask alignment and light exposure during production; preferably in the environment of an industrial semiconductor fabrication. This aims for the minimization of human interference in a process which is that sensible to particle contaminations as MCM–D.

- Automated pattern recognition systems are able to reliably detect deviations from a given target shape at high speeds and on any wafer scale that is available. Due to the small number of MCM–D wafers and the complicated non repeating structural shape of the bus system, the use of such a system was not feasible for the MCM–D wafers, but it has been used with great success for the front–end chip wafers of the Atlas pixel production. Such a system would also allow to optically inspect the opening of vias in a BCB layer. Until now via properties were only accessible by electrical test measurements after metal deposition, when repair options are not given any longer.

11.1.2   The Final Assembly

The yield after final assembly of the MCM–D modules suffered from unexpected issues that came up during the small scale production during this thesis. These issues are:

- In the area of the Flip Chip process: The connection of all IO contacts of the front–end chips was not reliable on all modules. This was due to the fact that a fraction of front–end chips was thinned down too much. While the thinning is desirable, from the physics point of view to reduce the amount of material in the detector, a temperature dependant process like solder bumping might face problems of chip bow during the heating procedure. This has been observed also for standard Atlas pixel modules with solder bumping. It is an increased problem for MCM–D as the IO pads of the chips are vital connections and are located at a rather isolated position in a distance of $2\,500\,\mu$m from the pixel matrix. This distance should be kept as low as possible in a design dedicated for MCM–D.

- The attachment of a dedicated flexible circuit. The failure of the last modules was due to the custom, non reliable connection of a pigtail. This requires some more effort to achieve a reliable solution that satisfies industrial standards. For a prototyping phase one should go for investigating different solutions in parallel on the basis of test pieces and for a backup contact option for module prototypes, e.g. wire bonding to a dedicated PCB.

Gluing and further handling of the module revealed no problems at all. This took advantage of the high robustness of such kind of modules after assembly. The replacement of front–end chips or even of the MCC after flip chip is possible. After final assembly it is still possible, but is dependant on the attached components, like pigtail and connector.

11.2 Areas of Possible Optimizations

A future design of MCM–D modules for upcoming experiments in high energy physics should be targeted to reduce the number of needed metal layers to a absolute minimum. This has to be a major design goal, as the effort of processing does not scale linear with the number of layers. It can be achieved by either reducing the power consumption, i.e. the currents, of the chips, the number of chips per module or using an advanced powering scheme like serial powering (described in [68]). One should also keep in mind, that changes at the IO layout during the design evolution of a front–end chip or controller chip will come along with a necessary major redesign of the MCM–D layers.

Together with the optimizations that follow out of Section 11.1, a successful production of MCM–D modules is possible. At the moment MCM–D is not a standard industrial process in the combination given here. The level of complexity would make a serious effort necessary until stable and reliable process parameters are established.

11.3 Further Upgrading of MCM–D

If the thin film technology of MCM–D is chosen for hybridization of a multi chip modules right from the start of a future project several options would be of interest. These are:

- Geometrically optimized sensors: The geometry of front–end chip and sensor would not have to be the same in an MCM–D approach. The design of routing structures for the devices investigated in this thesis was mainly done in the upper metal layer. A design in three metal layers would be possible without question; most probably also in two layers, but that depends on the actual geometry that one wants to adapt.

- The integration of passive components into the thin film layers is a field of ongoing research for further miniaturization of electronics systems. In [69] the integration of inductors, resistors and capacitors into a thin film MCM–D system is presented building several passive filter structures. First irradiation tests using existing structures of NiCr as resistor material were also done in this thesis and showed no major influence by the irradiation.

- Polymer waveguides for optical data transmission can be built directly in BCB. A design concept for single mode polymer optical waveguides has been presented in [70]. With the increasing effort in the industry to let silicon emit light [71], the implementation of waveguides into a multi chip system is of high interest.

Summary

In this thesis the MCM–D technique for the application of building pixel detector modules for high energy physics experiments has been examined.

In the year 2007 the ATLAS detector at the LHC will start to operate including a pixel detector built out of 1744 detector modules. These multi chip modules comprise of 16 electronics chips, a large sensor tile and a controller chip. A highly integrated interconnection system is needed to supply and read out these components. The ATLAS Pixel collaboration supported the research and development of the using MCM–D technique for this application.

In collaboration with the Fraunhofer Institute for Reliability and Microintegration, IZM, the technology of building MCM–D pixel detector modules has been reviewed and advanced. An interconnection system based on four layers of 3 µm thin electroplated copper as conductor and five layers of 5 µm intermediate BCB as dielectric material is suitable. This complex interconnection system has been designed in a defect tolerant approach. Single chip assemblies of geometrically optimized devices like equal sized and equal sized bricked devices were built. These devices feature a complex routing scheme between sensor and electronics chip. The prototypes have been tested in laboratory on their performance in critical aspects like threshold dispersion, noice performance, and crosstalk. All assemblies showed a behavior even better or at least comparable to conventional ATLAS pixel detector assemblies of the same generation of electronic chips (FE-I1A/B and FE-I2). An MCM–D single chip assembly has been irradiated in a hadron beam at the CERN up to a total dose of 50–55 Mrad. The assembly was well within the specifications after irradiation and showed no effect, that could be concluded to be MCM–D related.

An MCM–D module prototype was built with the radiation hard generation of readout electronics FE-I1A. The module is fully operational and was tested in laboratory. The MCM–D interconnection system is able to completely drive and read out the module. Voltage drops are within the limitations. The threshold dispersion of the electronics is $\sigma_{thres} =169\,e^-$ and the noise distribution is measured to $\mu_{ENC} = 257\,e^-$ and $\sigma_{ENC} = 23\,e^-$. Source measurements prove the functionality of the sensor after MCM–D processing.

An analysis of test beam data, taken with optimized devices, is given in this thesis. The measurement of the charge collection proves the concept and the determination of the spatial resolution shows the benefit of the geometrically optimized devices.

By summarizing our experience in the production of MCM–D modules, recommendations and an outreach of further possibilities the technology might offer for future experiments are given.

Appendix A

Overview of processed MCMD3 Runs at IzM

The Tables A.1, A.2 and A.3 show a summary of the MCM–D runs processed at IzM. Thickness, bow and warp are given in μm.

Wafer	Type	Thickness	Bow	Warp
47576	dummy	579.54	-0.68	5.79
47577	dummy	576.02	0.15	5.28
47578	dummy	558.38	-1.93	6.27
MCM5-02-D4	daisy	254.11	-1.06	10.10
MCM5-45-C6	daisy	250.36	-16.47	29.89
MCM5-28-B1	daisy	251.62	-1.06	13.04
MCM5-07-C5	daisy	251.43	-5.85	12.21
MCM5-42-G6	daisy	249.46	1.64	23.27
MCM5-35-A2	daisy	250.76	-7.87	14.26
MCM5-41-C4	daisy	248.05	-13.13	23.53
MCM5-46-B5	daisy	249.80	-23.90	38.75
3695-03	Prot. 2	268.16	11.20	20.83
BM-2-01	daisy	255.77	-96.85	229.41
BM-2-02	daisy	249.89	-86.86	191.61

Table A.1: MCMD3 Daisy Chain Run1 Overview, 2002-058

Wafer	Type	Thickness	Bow	Warp
47728	dummy	521.05	-3.44	7.44
final		543.41	-42.73	69.13
47729	dummy	519.05	-0.70	13.32
47730	dummy	520.02	-0.44	5.63
3695-10	Prot. 2	264.40	7.02	25.39
final		285.50	-103.92	174.86
IRST 13	Prot. 2	251.17	2.61	8.59
final		271.15	-10.73	180.84
3695-05	Prot. 2	265.47	7.74	19.00
final		287.27	-89.01	161.34
3696-14	Prot. 2	252.29	15.57	27.59
final		271.79	-94.01	153.71
IRST 7	Prot. 2	257.58	1.96	8.70
BM-2-05	dummy	248.03	-106.26	232.41
BM-2-06	dummy	248.65	-110.78	238.80

Table A.2: MCMD3 Sensor Run2 Overview, 2002-096

Wafer	Type	Thickness	Bow	Warp
47976	dummy	na	na	na
47977	dummy	na	na	na
MCM5-21-A7	daisy	252.93	-24.77	42.02
MCM5-20-E0	daisy	252.23	-13.92	25.27
MCM5-37-B3	daisy	250.93	8.86	23.40
IRST 38	Prot. 2	261.09	10.25	21.77
IRST 39	Prot. 2	257.32	3.41	10.93
3695-13	Prot. 2	260.70	8.47	21.28
3696-02	Prot. 2	268.54	5.22	14.98
final		289.78	-83.95	149.15
3696-12	Prot. 2	265.49	19.93	35.79
BM-2-08	dummy	256.64	-98.38	233.35
BM-2-10	dummy	255.27	-94.08	213.29

Table A.3: MCMD3 Sensor Run3 Overview, 2002-147

Appendix B

Schematic View of ATLAS Pixel Test Setup

Figure B.1 shows a schematic view of the test system used for the measurements performed on single chips and module prototypes. At the test beam facility H8 at CERN a similar setup was used for the readout of the devices under test. This kind of setup is also used for production tests of the front–end chips on wafer level. The main components of the setup are:

- Power supplies providing the supply voltages for the DUT (LV supply) as well as a power supply providing the bias voltage for the detector (HV supply).

- The adapter card providing connectors for the voltage supplies, for the data transmission link to the TPCC and a connector for the Type0 cable, which is used to connect a module. In the case of a single chip prototype as DUT, the assembly is glued to a custom PCB, which is acting as adapter card for itself. This adapter card features a single active component, a LVDS receiver, which loops back the clock signal in the case of a single chip and refreshes the signal of module for further readout.

- The Turbo Pixel Control Card , TPCC. The purpose of the TPCC is mainly to provide signal conversion from LVDS which is send to and from the module via the adapter card to the PECL standard needed by the TPLL. The TPCC also provides a digitally adjustable charge injection circuit and a digitization of the analog NTC signal for further readout. A total of four modules can be connected to the TPCC, which can be provided with the clock signal in parallel.

- The Turbo Pixel Low Level Card, TPLL. The TPLL features a VME interface and can be read out using an additional VME–PCI interface to a personal computer. Central component of the TPLL is a FPGA. The FPGA does the conversion of the data stream to the protocols of MCC or front–end chip. The data stream from the module's side can be computed in real time even in highest data rates of up to 160 MBps. An additional feature is the ability to produce histograms of the module's data in a 16 MB large RAM, which is also part of the TPLL [60].
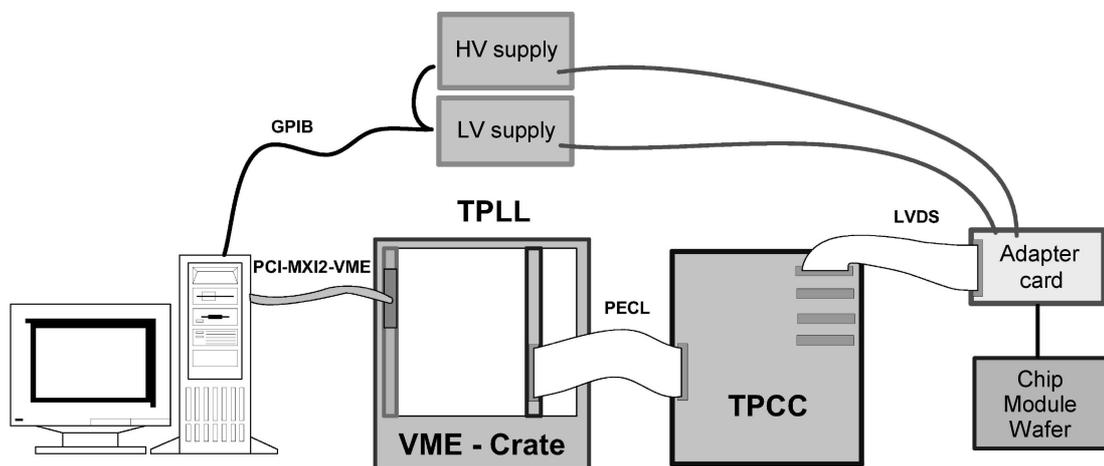
Figure B.1: Schematic view of the ATLAS Pixel Test Setup, from [60].

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Bibliography

[1] EIDELMAN, S. et al.: *Particle Data Group*. Physics Letters, B 592(1), 2004.

[2] HIGGS, P.: *Broken Symmetries and the Masses of Gauge Bosons*. Physical Review Letters, 13(6):508, October 1964.

[3] DJOUADI, A.: *The Search for Higgs particles at high–energy colliders: Past, Present and Future*. hep–ph/0205248v1, May 2002.

[4] G. ABBIENDI, ET AL. (THE LEP WORKING GROUP FOR HIGGS BOSON SEARCHES): *Search for the Standard Model Higgs Boson at LEP*. Phys. Lett. B, 565:61–75, 2003.

[5] THE ATLAS COLLABORATION: ATLAS *Detector and Physics Performance TDR*. Technical Report, CERN, May 1999. CERN/LHCC/99–14 (Vol.I) und CERN/LHCC/99–15 (Vol.II).

[6] LHCC: *The* ATLAS *Technical Proposal for a General Purpose pp Experiment at the Large Hadron Collider at* CERN. Technical Report, CERN, December 1994. CERN/LHCC/94–43.

[7] THE ATLAS COLLABORATION: *Muon spectromenter technical design report*. CERN/LHCC/97-22.

[8] THE ATLAS COLLABORATION: *The Inner Detector Design Report*. ATLAS TDR 4, CERN/LHCC/97-16 und CERN/LHCC/97-17, April 1997.

[9] THE ATLAS COLLABORATION: ATLAS *Pixel Detector Technical Design Report*. Technical Report, CERN, May 1998. CERN/LHCC/98–13 ATLAS TDR 11.

[10] THE ATLAS COLLABORATION: ATLAS *Level–1 Trigger–Technical Design Report*. Technical Report, CERN, June 1998.

[11] LEO, WILLIAM R.: *Techniques for Nuclear and Particle Physics Experiments: A How-to Approach*. Springer-Verlag, New York, Berlin, Heidelberg, Second Revised Edition edition, 1994.

[12] LANDAU, L.: *On the energy loss of fast particles by ionization*. J. Phys. (USSR), 8:201, 1944.

[13] BICHSEL, HANS: *Straggling in thin silicon detectors*. Reviews of Modern Physics, 60(3):663–699, July 1988.

[14] LUTZ, GERHARD: *Semiconductor Radiation Detectors: Device Physics.* Springer-Verlag, Berlin, Heidelberg, New York, 1999.

[15] VIA, C. DA: *Radiation hard silicon detectors lead the way.* CERN Courier, January 2003.

[16] M. TRIMPL, L. ANDRICEK, P. FISCHER G. LUTZ R.H. RICHTER L. STRÜDER J. ULRICI N. WERMES: *A fast readout using switched current technique for a DEPFET–pixel vertex detector at TESLA.* Nucl. Inst. and Meth. A, 511:257–264, 2003.

[17] ADAM, W. et al.: *The development of diamond tracking detectors for the LHC.* Nucl. Instrum. Meth., A514:79–86, 2003.

[18] KERSTEN, SUSANNE: *Requirements for the Power Supply System of the* ATLAS *Pixel Detector.* ATL-IP-ES-0005, December 2000.

[19] THE ROSE COLLABORATION: *3$^{\text{rd}}$ RD48 Status Report.* CERN/LHCC 2000-009, 2000.

[20] ALAM, M. S. et al.: *The ATLAS silicon pixel sensors.* CERN-EP-99-152, 1999.

[21] WUNSTORF, R.: *Radiation tolerant sensors for the* ATLAS *Pixel Detector.* Nucl. Inst. and Meth., A466:308–326, 2001. präsentiert auf der Hiroshima Konferenz, 2000.

[22] RICHTER, R.H. et al.: *Strip detector design for* ATLAS *and* HERA–B *using two–dimensional device simulation.* Nucl. Inst. and Meth., A377:412, 1996.

[23] HÜGGING, FABIAN: *Der* ATLAS *Pixelsensor – Der state-of-the-art Pixelsensor für teilchenphysikalische Anwendungen mit extrem hohen Strahlungsfeldern.* PhD thesis, Fachbereich Physik der Universität Dortmund, June 2001.

[24] EINSWEILER, KEVIN: *Overview of On–Detector Electronics and Requirements.* In *Talk given at the Pixel On–Detector PRR*, dec 2003.

[25] EINSWEILER, K., A. JOSHI, R. MARCHESINI, F. PENGG and G. ZIZKA: *On the performance and limitations of a dual threshold discriminator pixel readout circuit for LHC.* IEEE Trans. Nucl. Sci., 46:792, 1999.

[26] MEUSER, S.I.: *Pixel Readout Chip for the* ATLAS *Experiment.* In *Proc. of IEEE Nuclear Science Symposium, Toronto, Canada*, November 1998.

[27] JAEGER, J.J. et al.: *A Sparse Scan Circuit for Pixel Detector Readout.* IEEE Trans. Nucl. Sci., NS-40:400, 1993.

[28] EINSWEILER, K. et al.: *On the Performance and Limitations of a Dual Threshold Discriminator Pixel Readout Circuit for LHC.* In *Proc. of IEEE Nuclear Science Symposium, Toronto, Canada*, 1998.

[29] FISCHER, P.: *The ATLAS Pixel Front–End Chip FE–I in 0,25 μm Technology.* In *Proceedings 8th workshop on Electronics for LHC*, Colmar, France, September 2002.

[30] ANELLI, GIOVANNI MARIA: *Design and characterization of radiation tolerant integrated circuits in deep submicron CMOS technologies for the LHC experiments.* PhD thesis, Institut National Polytechnique de Grenoble, December 2000.

[31] GLITZA, K. W.: *Hochsteife, ultraleichte CFK-Trägerstrukturen für den ATLAS-Pixeldetektor.* Contribution to the 3. Workshop Konstruktionstechnik, Rostock, September 2001.

[32] GREGOR, INGRID-MARIA: *Optical Links for the* ATLAS *Pixel Detector.* PhD thesis, University of Wuppertal, 2001. WU DIS 2001-03.

[33] M.IMHÄUSER, K.H.BECKS, S.KERSTEN P.KIND P.MÄTTIG J.SCHULTES: *The Control System for the ATLAS Pixeldetector.* IEEE Transactions on Nuclear Science, 51(3), June 2004.

[34] DABO, GIOVANNI: *Atlas Pixel Demonstrator.* INFN, Genua, 2000.
located at the time of creation:
`http://www.ge.infn.it`

[35] GERLACH, PETER: *Entwicklung eines Pixeldetektor Moduls für das* ATLAS *Experiment unter Verwendung einer Kupfer/Benzocyclobuten basierten Dünnfilmtechnologie.* PhD thesis, University of Wuppertal, 2001. WUB DIS 2001-12.

[36] P.SKUBIC, G. BOYD, S. KRISHNAMA H. SEVERINI: *Flex circuits for the* ATLAS *pixel detector.* Nucl. Inst. and Meth., A 465:219–223, 2001.

[37] Personal communication with *W.Ockenfels*, University of Bonn.

[38] HEUSER, JOHANN M.: *Construction, Operation and Application of the DELPHI Pixel Detector at LEP2.* PhD thesis, University of Wuppertal, 1999. WU B DIS 99-01.

[39] BECKS, K.-H. et al.: *A Multi-Chip Module, the Basic Building Block for Large Area Pixel Detectors.* In *Proc. of IEEE Multi-Chip Module Conference,* 1996.

[40] TÖPPER, M., L. DIETRICH, G. ENGELMANN, S. FEHLBERG, P. GERLACH, J. WOLF, O. EHRMANN, K.-H. BECKS and H. REICHL: *Fabrication of a High-Density MCM-D for a Pixel Detector System using BCB/Cu Technology.* In *International Conference on HD Packaging and MCMs,* April 1999. Denver.

[41] TÖPPER, M., L. DIETRICH, S. FEHLBERG, P. GERLACH, C. KARDUCK, C. MEINERZ, J. WOLF, O. EHRMANN, K.-H. BECKS and H. REICHL: *Fabrication of a High-Density MCM-D for a Pixel Detector System using BCB/Cu/PbSn Technology.* International Journal of Microcircuits and Electronic Packaging, Issue 4, 22(4):305–311, April 1999. Proceedings of International Conference on HD Packaging and MCMs, Denver, USA.

[42] GUPTA, KULDIP C., RAMESH GARG, INDER BAHL and PRAKASH BHARTIA: *Microstrip Lines and Slotlines.* Artech House, Inc., 2 edition, 1996.

[43] IBM – TECHNOLOGY PRODUCTS, C4 PRODUCT DESIGN CENTER: *C4 Product Design Manual, Vol. I: Chip and Wafer Design,* 2000.

[44] GEMME, CLAUDIA: *Study of indium bumps for the* ATLAS *pixel detector*. In L.ROSSI (editor): *International Workshop on Semiconductor Pixel Detectors for Particles and X-rays, PIXEL2000*, volume A465, pages 200–203. Nucl. Inst. and Meth., June 2001. Genua, Italy.

[45] PIETER, P. and C. TRUZZI: *Results of the HF network analyser measurements on the* ATLAS *wafer after p+ radiation*. Technical Report, Interuniversity Microelectronics Center (IMEC, Leuven, Belgien), 1997.

[46] THE DOW CHEMICAL COMPANY: *Cyclotene® data sheet*.
located at the time of creation:
http://www.dow.com

[47] GRAH, CHRISTIAN: *Testmessungen an Auslesechips für den* ATLAS–*Pixeldetektor*. Master's thesis, University of Wuppertal, February 2000. WU D 00-02.

[48] GRAH, CHRISTIAN: *Pixel detector modules using MCM–D technology*. Nucl. Inst. and Meth. A, 465:211–218, 2001.

[49] T.FLICK, K.H.BECKS, P.GERLACH, C.GRAH, P.MÄTTIG and T.ROHE: *Studies on MCM–D Pixel-Detector-Modules*. In *8th topological seminar on innovative particle and radiation detectors*, volume 125, Siena, 2002. Nucl. Phys. B.

[50] BÄSKEN, OLLIVER: *Messungen an* ATLAS–*Pixeldetektor-Modulen in MCM-D-Technologie*. Master's thesis, University of Wuppertal, April 2000. WU D 00-06.

[51] K. SCHERPINSKI, M. TÖPPER, F. KRAUSE K. HALSER R. HAHN O. EHRMANN H. REICHL: *Integration of NiCr Resistors in a Multilayer Cu/BCB Wiring System*. In *Int. Symp. and Exhibition on Advanced Packaging Materials, Braselton, USA*, pages 178–185. Technical University of Berlin and Fraunhofer Institut for Reliability and Microintegration, Berlin, March 1999.

[52] FLICK, TOBIAS: *Vorstudien zur Modulproduktion für den* ATLAS–*Pixeldetektor*. Master's thesis, University of Wuppertal, March 2002. WU D 02-03.

[53] RM WARNER, JR: *Applying a Composite Model to the IC Yield Problem*. IEEE Journal of Solid State Circuits, 9(3):86–95, 1974.

[54] Personal communication with *Dr. J. Im*, The Dow Chemical Company.

[55] BECHERLE, R.: *The Module Controller Chip (MCC) of the* ATLAS *Pixel Detector*. In *Proc. of IEEE Nuclear Science Symposium, Toronto, Canada*, November 1998.

[56] RAICU, DAN: *Universal Taper for Compensation of Step Discontinuities in Microstrip Lines*. IEEE Mirowave and Guided Wave Letters, 1(9), September 1991.

[57] TÖPPER, MICHAEL: *Entwicklung einer auf Photo–BCB basierenden Technologie für das Waferlevel Packaging*. Master's thesis, Technical University of Berlin, 2003. D 83 (Diss. TU Berlin).

[58] WERMES, NORBERT: *Trends in Pixel Detectors: Tracking and Imaging.* In *Invited Review given at IEEE2003, Portland, Oct, 2003*, volume 51, pages 1006–1015. IEEE Trans. Nucl. Sci., 2004.

[59] NEW MEXICO, UNIVERSITY OF: *IV data of Wafer 3695–03.*
located at the time of creation:
http://www-hep.phys.unm.edu/atlas_pixel/2_prototypes/

[60] STOCKMANNS, TOBIAS: *Multi–Chip–Modul–Entwicklung für den ATLAS–Pixeldetektor: Analyse der Front–End–Elektronik in strahlenharter 0,25–µm–Technologie und Entwicklung und Realisierung einer Serial–Powering–Konzeptes.* PhD thesis, Universitity of Bonn, 2004. BONN-IR-2004-06.

[61] Personal communication with *P. Sicho*, Academy of Science, Prague.

[62] ROHE, TILMAN: *Design and test of pixel sensors for the* ATLAS *pixel detector.* Nucl. Inst. and Meth. A, 460:55, 2001.

[63] I. GORELEV, M. HOEFERKAMP, S.C. SEIDEL A. CIOCIO K. EINSWEILER: *A Measurement of Lorentz Angle and spatial resolution of radiation hard Silicon Pixel Sensors.* Nucl. Inst. and Meth. A, 481:204–221, 2002.

[64] ANDREAZZA, A.: *Performance of* ATLAS *pixel detector prototype modules.* Nucl. Inst. and Meth. A, 135:103–106, 2003.

[65] TREIS, J.: *Development and operation of a novel PC-based high speed beam telescope for particle tracking using double sided silicon microstrip detectors.* PhD thesis, University of Bonn, 2002. BONN–IR–2002–10.

[66] A. ANDREAZZA, T. LARI, C. MERONI F. RAGUSA C. TRONCON: *H8* ATLAS *pixel test beam analysis program - User Guide*, October 2002.
located at the time of creation:
http://troncon.home.cern.ch/troncon/testbeamhome.html

[67] Personal communication with *E. Beyne*, Interuniversity Microelectronics Center (IMEC, Leuven, Belgien).

[68] STOCKMANNS, TOBIAS: *Serial Powering of Pixel Modules.* Nucl. Inst. and Meth. A, 511:174–179, 2003.

[69] K. ZOSCHKE, J. WOLF, M. TÖPPER O. EHRMANN T. FRITZSCH K. SCHERPINSKI H. REICHL F.-J. SCHMÜCKLE: *Thin Film Integration of Passives - Single Components, Filters, Integrated Passive Devices.* In *Electronic Components and Technology Conference*, pages 294–301, Las Vegas, Nevada USA, June 2004.

[70] G. FISCHBECK, R. MOSSBURGER, M. TÖPPER K. PETERMANN: *Design concept for singlemode polymer waveguides.* Electronics Letters, 32(3):212–213, February 1996.

[71] FAIST, JEROME: *Silicon Shines On.* Nature, 433:691–692, February 2005.

Glossary

ambiguities Non unique information. Strip detectors provide an ambiguous hit information in the case of multiple hits.

Au stud bumping Connection technique. A Au stud provides the electrical connection while the mechanical stability is provided by gluing.

bare module Intermediate assembly state of an ATLAS pixel detector module (only for Flex–Hybrid technology) after flip chip. Sensor and bump bonded front–end chips.

benzocyclobutene BCB, sold by Dow under the trademark CYCLOTENE. Photosensitive polymer used as dielectric in the MCM–D process.

Bethe–Bloch equation Equation describing the energy loss per path length (dE/dx) of charged particles in matter.

bias grid Test structure to contact all pixel cells. Grid like metal structure covering the complete pixel matrix of a sensor. The punch–through effect allows to establish a conducting channel to each pixel and thus allows to test the full sensor without front–end chips.

B–layer Innermost layer of the barrel part of the ATLAS pixel detector.

bump Solder or Indium deposition for the flip chip connection

bump bond Single welded micro–connection established by using a bump.

bump bonding Connecting front–end chip and sensor by using bump connections.

bump pad Contact area of a bump.

CP violation Symmetry violation in the application of the combined C– (charge conjugation) and P–transformation (parity inversion).

CYCLOTENE Trademark of BCB sold by Dow Chemical Corp..

Descum Processing step in the MCM–D process. Dry plasma etching to remove BCB remnants.

Dow Chemical Corp. USA. Manufacturer of Cyclotene.

electroplating Processing step used in the MCM–D process for the metal layers. Galvanic growth of the desired metal on a plating base deposited by sputtering.

equal–sized Sensor design, where the complete area of the sensor, including the interchip region, is equally distributed to all readout pixel cells. Can only be realized by using MCM–D.

equal–sized–bricked Sensor design, where the complete area of the sensor, including the interchip region is equally distributed to all readout pixel cells. Additionally the pixel rows are shifted alternately for $\pm$ row/4 to enhance the resolution for double hits. Can only be realized by using MCM–D.

η–distribution Energy weighting factor for the correction of the impact position of a hit. Applying the factor improves the resolution in the case of double or more hits.

Fano factor Correction factor to the energy resolution of detectors. A Fano factor of one would mean that the fluctuation of the mean number of electron–hole pairs is following Poisson statistics.

feed–through Contact through all thin film layers.

Flex Short term for multilayer flexible printed circuits. Used as interconnection system for the standard ATLAS pixel detector modules.

Flex–Hybrid Short term for the ATLAS pixel detector modules built in the standard technique of using a Flex.

flip chip The flip chip technique allows to contact a chip in a complete plane by connecting it face down to a substrate.

guard ring Structure on the p–side of the ATLAS pixel sensor for the controlled reduction of the electric potential from the bias to ground level. Thus the conducting edges of the substrate are grounded.

H8 The H8 test beam facility at CERN.

Higgs The Higgs–boson is the last yet unobserved particle of the Standard Model. P.Higgs introduced the Higgs–field to explain the mass of the gauge bosons by the Higgs–mechanism. The existence of the Higgs–boson is a consequence of this. The limits on the Higgs–boson mass are: 114.4 GeV and 1 TeV.

hybridization Term for the technique to connect the components of the ATLAS pixel detector modules. In particular used for bump bonding the front–end chips to the sensor.

immersion develop Processing step formerly used in the MCM–D process. Application of the developer in a separate bath.

interchip region Region of the ATLAS pixel detector modules with enlarged or ganged pixel to cover the necessary gap between the front–end chips. Can be avoided by using the MCM–D technique.

Kapton® Trademark of a Polyimid– (Pyralin–)foil sold by DuPont.

luminosity Luminosity is a measure of a collider's *event rate*, given in cm^{-2}s^{-1}. The LHC will run in two phases of different luminosity: $\mathcal{L}_{low} = 1 \times 10^{33}$ cm^{-2}s^{-1} and $\mathcal{L}_{high} = 1 \times 10^{34}$ cm^{-2}s^{-1}.

mask Mask with the positive or negative pattern of the structures one wants to transfer to a wafer. E.g. chromium on a glass substrate patterned by an electron beam.

photoresist Radiation sensitive compound. Structured by exposure to the sensitive radiation followed by development. Negative or positive pattern of the desired structures remain on the wafer.

pigtail Short flexible printed circuit connected to the modules. The plug–in for the Type0 cable is situated on the pigtail.

pixel 2–dimensional segmentation of the sensor and front–end chip. Originating from *picture* and *element*.

plasma etching Plasma–assisted dry etching methods. E.g. Reactive Ion Etching.

pn–junction Contact area between a *p*–doped and an *n*–doped area of a semiconductor. A charge carrier free area forms in this region, the depleted area. Current can flow only in one (forward bias) direction. If reversely biased the charge carrier free region grows.

probecard PCB with multiple attached probes. Usually used to contact all vital contacts of an IC to test completely the bare die.

Prototype 2.0 ATLAS pixel sensor generation featuring equal–sized(–bricked) single chip sensors and a centrally positioned module in production design.

pseudorapidity $\eta = -\ln\tan(\theta/2)$; measure of the angle to the beam, used instead of the polar angle θ.

puddle develop Processing step used in the MCM–D process. Application of the developer while the wafer is on the rotating chuck.

punch–through Establishment of a conducting channel. For ATLAS pixel sensors this technique is used to contact all pixel cells for test measurements with the bias–grid. This is done by the lateral enlargement of depleted areas in a sensor, until two depleted areas are merged. Thus a not contacted floating metallization can be brought to a defined potential.

reflow Processing step for bump bonding and the flip chip process.

Standard Model The theory of the fundamental particles and their interactions. Includes the strong and the electroweak interactions.

spin coating Processing step used in the MCM–D process for BCB deposition. Procedure of applying a thin film layer on a rotating wafer. The layer thickness is determined by rotation speed and the viscosity of the applied material.

sputtering Processing step used in the MCM–D process for the deposition of a thin metal layer. By an ion bombardment atoms of the desired metal type or mixture are extracted from the sputter target and deposit on a substrate facing the target. Only applicable for relatively thin layers of some hundred nm.

SUSY Short term for Super Symmetry. Extension of the Standard Model.

thin film Layers of deposited material with thicknesses of atomic layers up to some 10 µm.

Type0 Connection cable between the ATLAS pixel detector modules and the first patch panel

type inversion Bulk irradiation effect of the ATLAS pixel sensors. By the increase of p–type damages due to non ionizing energy loss, the n–type bulk will convert to p–type behavior. This is compensated by using a n^+ on n design.

Upilex® Trademark of a multilayer capable foil sold by UBE.

wafer–prober Automatic or semi–automatic device for contacting an unhoused IC with a probecard. A full wafer can be loaded in the wafer–prober and the wafer–prober tests each die.

wire bonding Standard connection technique used for the Flex–Hybrid module. Wires of some μm diameter are ultrasonically welded to the IO pads of an IC. Usually the fragile wires are protected by an encapsulation, which is not applicable for ATLAS pixel.

wafer level packaging By using the technique of wafer level packaging the die and its package are manufactured and tested on wafer level, i.e. before singulation.

Description of Acronyms

ADC . . . . Analog Digital Converter. Circuit for the conversion of analog voltage/current levels into a digital information of a certain bit length.

AMS . . . . Alenia Marconi Systems, Italy.

ASIC . . . . Application Specific Integrated Circuit. Integrated circuit, which is especially designed for one purpose. E.g. the FE chips of the ATLAS pixel detector.

ATLAS . . . . A Toroidal LHC ApparatuS. High energy physics experiment, detector, planed for the LHC.

BAT . . . . Bonn ATLAS Telescope. Reference system at the H8 test beam facility.

BCB . . . . Benzocyclobutene. Dielectricum sold by Dow under the trademark Cyclotene. Used in the MCM–D process.

C4 . . . . Controlled Collapse Chip Connection Flip chip process developed in the sixties by IBM.

CASTOR . . . . . CERN Advanced Storage Manager.

CCD . . . . Charge Coupled Device. Pixel detector widely used for video/camera applications. Due to its serial readout too slow for the ATLAS experiment.

CERN . . . . European Laboratory for Particle Physics. Original name: *Conseil Européenne pour la Recherche Nuclèaire.*

CKM . . . . Cabibbo Kobayashi Maskawa. The CKM matrix relates the quark mass eigenstates to their weak eigenstates.

CMOS . . . . Complementary Metal Oxide Silicon. Technology for the integration of electronic circuits in a semiconductor.

CTE . . . . Coefficient of Thermal Expansion.

DAC . . . . Digital Analog Converter.

DCS .... Detector Control System. Monitoring and control system for the subsystem of the ATLAS experiment.

DELPHI .... Detector with Large Parton and Hadron Identification. Experiment at LEP, CERN. First HEP experiment at a synchrotron which was equipped with a pixel detector.

DELTA .... Danish Electronics, Light & Acoustics, Hørsholm. Company testing the MCC wafers for the ATLAS pixel collaboration.

DEPFET ..... DEPleted Field Effect Transistor. Detector concept which imports a first amplification stage into the sensor.

DMILL .... Durcie Mixte sur Isolant Logico-Lineaire. Radiation tolerant 0.8 µm process.

DOFZ........ Diffusion Oxygenated Float Zone. Technique to diffuse oxygen into a silicon substrate at high temperatures. Used for the sensors of the ATLAS pixel detector. Increases radiation hardness of the sensor.

DSM .... Deep Submicron. Term for chip technologies which allow to produce minimal structures below 0.5 µm. FE–I and MCC–DSM and later prototypes for the ATLAS pixel detector are produced in this technique, thus sometimes these generations are labelled with this acronym.

DUT .... Device Under Test.

ENC .... Equivalent Noise Charge. Charge which - if present at a preamplifiers input - would generate the observed voltage noise level at the output of a circuit.

EoC .... End of Column logic. Circuit which is part of the front–end chips of the ATLAS pixel detector. Here the hit data are buffered.

FE .... Front–end Chip. Term for integrated readout circuits.

FE–A .... Front–end Chip A. Prototype of the ATLAS pixel front–end chip. Developed by the university of Bonn and the CPPM.

FE–B .... Front–end Chip B. Prototype of the ATLAS pixel front–end chip. Developed by LBNL.

FE–C .... Front–end Chip C. Advanced version of FE–A.

FE–D .... Front–end Chip D. FE chip in DMILL technology combining FE–A and FE–B. The versions of FE–D and FE–D2 were produced.

FE–I .... Front–end Chip I. Transfer of the FE design in DSM technology. Versions of FE–I1 (A and B), FE–I2 and FE–I3 were produced. FE–I3 is the production version for the ATLAS pixel detector.

GUT . . . . Grand Unified Theories. Theory predicting the unification of strong, weak and electromagnetic force at high energy scales (10^{14} GeV).

HDI . . . . High Density Interconnect. Collective term for technologies for building dense interconnection layers on IC's.

HEP . . . . High Energy Physics. Also known as Particle Physics. The science of the fundamental particles and their interactions.

IBM . . . . International Business Machines Corp., USA.

I–Box . . . . Interlock Box. Part of the DCS. Monitors the temperature on the pixel detector modules and switches off the corresponding power supply in case of overheating.

IMEC . . . . Interuniversity Microelectronics Center, Leuven (Belgium).

INFN . . . . Instituto Nazionale di Fisica Nucleare, Italy.

IzM . . . . german: Institut für Zuverlässigkeit und Mikrointegration. Fraunhofer Institute for Reliability and Microintegration, Berlin.

KgD . . . . Known good Die. Short term for the problem of the necessary knowledge of the functionality of parts of a MCM to get reasonable yield, see Equation 7.1 on page 75.

LBNL . . . . Ernest Orlando Lawrence Berkeley National Laboratory, Berkeley, USA.

LEP . . . . Large Electron Positron Collider. e^+–e^- accelerator, operating at Cern until 2000.

Lhc . . . . Large Hadron Collider. p^+–p^+ accelerator, will be operating at Cern from 2007.

LV–CMOS . . . . Low Voltage CMOS.

LVDS . . . . Low Voltage Differential Signal.

LVL1 . . . . Level–1 trigger. Highest order trigger architecture of Atlas.

MCC . . . . Module Control Chip.

MCM . . . . Multi Chip Module.

MCM–D . . . . . . Multichip Module Deposited.

MIP . . . . Minimum Ionizing Particle. Particle of an energy corresponding to the minimum in the Bethe–Bloch equation.

MIPS . . . . Million Instructions Per Second.

NTC . . . . Negativ Temperature Coefficient Resistor. Ceramic resistor with negative coefficient of temperature. Used to monitor the temperature on the pixel detector modules.

PCB . . . . Printed Circuit Board.

PS . . . . Proton Synchrotron. 28 GeV proton synchrotron at CERN.

ROD . . . . ReadOut Driver.

RoI . . . . Region of Interest. Information about regions of high interest, e.g. jets, passed from the Level–1 trigger system to the Level–2 trigger system.

ROSE . . . . Research and development On Silicon for future Experiments (CERN – RD48).

SCT . . . . Semiconductor Tracker. One of the three tracking subsystems of ATLAS.

SPS . . . . Super Proton Synchrotron. 450 GeV proton synchrotron at CERN.

ToT . . . . Time Over Threshold. Rough energy information obtained from the time a signal remains above a discriminator's threshold. Used in the front–end chips of the ATLAS pixel detector and quantized in units of 25 n sec.

TPCC . . . . Turbo Pixel Control Card. Part of the standard laboratory equipment in the ATLAS collaboration for testing the front–end chips or modules.

TPLL . . . . Turbo Pixel Low Level card. Part of the standard laboratory equipment in the ATLAS collaboration for testing the front–end chips or modules.

TRT . . . . Transition Radiation Tracker. One of the three tracking subsystems of ATLAS.

UBM . . . . Under Bump Metallization. Necessary for the flip chip process. Interface between chip metallization and bump.

WIMP . . . . Weakly Interacting Massive Particle. Candidate for dark matter.

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