Wideband Circuit Design Techniques for Ultra-High Data-Rate Wireless Communication in Silicon Technologies

Faculty of Electrical, Information, Media Engineering
University of Wuppertal

A thesis submitted for the degree of
Doktor der Ingenieurwissenschaften

Neelanjan Sarmah
from Assam, India

Wuppertal, August 2016

Die Dissertation kann wie folgt zitiert werden:

urn:nbn:de:hbz:468-20170815-134447-9
[http://nbn-resolving.de/urn/resolver.pl?urn=urn%3Anbn%3Ade%3Ahbz%3A468-20170815-134447-9]

I would like to dedicate this thesis to my loving and dearest parents and sister, my sweet little nephew Vishnu and my wife Papori.

Declaration

I, Neelanjan Sarmah, herewith declare that I have produced this thesis without the prohibited assistance of third parties and without making use of aids other than those specified; notions taken over directly or indirectly from other sources have been identified as such. This work has not previously been presented in identical or similar form to any other German or foreign university examination board.

This thesis work was conducted from 2011 to 2016 under the supervision of Prof. Dr. rer. nat. Ullrich. R. Pfeiffer in the Institute for High-Frequency and Communication Technology at the University of Wuppertal, Germany. This work was partially funded by the European Commission within the DOTSEVEN project (no. 316755) and, the DFG funded Real100G project.

Neelanjan Sarmah
August 2016

Acknowledgements

This thesis is a culmination of 4.5 years of my life spent in Wuppertal, Germany. Firstly, I would like to thank Professor. rer. nat. Ullrich R. Pfeiffer for giving me this opportunity. I appreciate his support in finishing this thesis. Overall, it was a very nice learning experience, and the excellent lab infrastructure made it possible to try out a lot of things.

I would like to thank my parents, sister Neena and, my brother-in-law Sathya for their immense love, and the unconditional support. I missed some of the important moments in my life, and sorry for being away in some good and tough times. The words are too few to express more so I will better not try. My wife Papori stood behind me like a rock and was extremely supportive, loving and extremely caring. If not for her, I would not have finished this thesis. Again, words are too few, so probably I will not try. My little nephew Vishnu, I missed playing with you, and see you growing from a toddler to a naughty little big boy but in the future, you will see a lot of me. We all love you a lot!!!

At work, I would like to thank all my fellow colleagues Pedro, Stefan, Phillip, Hans, Janusz, Wolfgang and Martina for all the help and support. It was a pleasure to work and know you guys. So, a very very big “Thank you”.

Abstract

The transition towards sub-mmWave frequencies offer tremendous potential due to the abundantly available RF bandwidth, reduced form-factor of the passives like on-chip antennas, and better lateral and range resolution (as a consequence of high bandwidth). At frequencies below 100 GHz, the limited bandwidth puts an upper limit on the maximum data-rate for communication systems, and it also limits the range resolution for FMCW RADAR systems. Hence, operation towards sub-mmWave frequencies provides an alternative in mitigating the limitations of the existing wireless systems at low frequencies. It also opens the possibility for new applications like high-resolution imaging for security and non-destructive testing, and material identification and characterization. The traditional optical techniques for signal generation and detection at sub-mmWave frequencies are bulky and expensive. The low integration density of III-V based electronic systems limits its scalability, especially for mass volume applications. The recent advancements in silicon process technologies have made it a viable low-cost alternative as compared to III-V based compound semiconductors. A significant advantage of silicon technologies is the high integration density. This allows the implementation of the digital and baseband electronics in the same chip resulting in a compact, and single-chip solution. This gives silicon-based systems a significant edge over the III-V semiconductors in terms of economies of scale. This thesis addresses the various circuit design challenges and system level considerations for the realization of a fully-integrated Tx and Rx chipset towards sub-mmWave frequencies in SiGe BiCMOS technologies.

The first part of the thesis is focused on the challenges at the individual circuit building-blocks of the RF front-end. The challenges associated with the implementation of wideband amplifiers with high gain and output power at frequencies close to $f_{max}/2$ are addressed here. The limited output power of power amplifiers (PAs) limits the maximum range of wireless links, and is one of the significant impediments. In this thesis, the special considerations for loadline matching of PAs towards sub-mmWave frequencies are presented, and power combination techniques for PAs are explored for high power generation.

Another key challenge addressed here is the implementation of a high-power wideband tunable local oscillator (LO) source operating at the fundamental frequency with low dc-power consumption. This is one of the key aspects in giving the chipset a generic attribute, which makes it suited for applications requiring a fixed (communication) or a wideband tunable LO (FMCW RADAR, imaging, material characterization). In terms of output power, bandwidth and figure-of-merit (FoM) at the individual building-block level, the results presented in this thesis are beyond the current state-of-the-art in silicon technologies and are comparable to implementations in III-V technologies.

Based on the circuit building-blocks presented in the first part, a generic wideband fully-integrated direct-conversion 240 GHz quadrature Tx and Rx chipset is implemented and presented in the second part of the thesis. The focus here is on the integration of wideband on-chip antennas designed to be used with an external replaceable silicon lens for high directivity. The chip-lens assembly is mounted on a low-cost PCB material (Rogers 4350B) for an overall compact form-factor. The on-chip antenna and chip-lens assembly is done in a collaborative teamwork and leverages the expertise of our research group in low-cost packaging. For wideband IF matching, stepped impedance microstrip-line based low-pass filters are implemented on the PCB. The packaged chipset was used to demonstrate a high data-rate communication system at 240 GHz over a wireless link of 70 cm. For QPSK and BPSK modulation schemes, the maximum measured data-rates using this chipset are 24 Gbps and 25 Gbps respectively. At the time of writing this thesis, this is the highest data-rate reported in the literature for fully-integrated wireless systems above 200 GHz in silicon technologies. A different version of this chipset is used for the demonstration of a monostatic FMCW RADAR system operating in the 210-270 GHz frequency range, and it uses identical circuit building blocks. This proves the generic attribute of this implementation.

Hence, the results from this work provide a holistic foundation towards mitigating the challenges at the circuit and system level for the realization of compact, low-cost and fully-integrated silicon-based systems for emerging applications towards sub-mmWave frequencies.

Books

1. U. R. Pfeiffer, and N. Sarmah, *Linearization and Efficiency Enhancement Techniques for Silicon Power Amplifiers*, 1st ed. Academic Press, 1 2015, ch. Efficiency Enhancement for THz Power Amplifier, pp. 6–1.

List of Publications

Journals

1. N. Sarmah, J. Grzyb, K. Statnikov, S. Malz, P. R. Vazquez, W. Foerster, B. Heinemann, and U. R. Pfeiffer, "A Fully Integrated 240-GHz Direct-Conversion Quadrature Transmitter and Receiver Chipset in SiGe Technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 562–574, Feb 2016.

2. J. Grzyb, K. Statnikov, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 210-270 GHz Circularly-Polarized FMCW Radar with a Single Lens-Coupled SiGe HBT Chip," *accepted for publication in the IEEE Trans. on Terahertz Science and Technology*, 2016.

3. U. R. Pfeiffer, Y. Zhao, J. Grzyb, R. A. Hadi, N. Sarmah, W. Foerster, H. Ruecker, and B. Heinemann, "A 0.53 THz reconfigurable source module with up to 1 mW radiated power for diffuse illumination in terahertz imaging applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2938–2950, 2014.

4. K. Statnikov, J. Grzyb, N. Sarmah, S. Malz, B. Heinemann, and U. R. Pfeiffer, "A 240-GHz circularly polarized FMCW radar based on a SiGe transceiver with a lens-coupled on-chip antenna," *International Journal of Microwave and Wireless Technologies*, vol. FirstView, pp. 1–9, 7 2015.

5. N. Sarmah, P. Chevalier, and U. R. Pfeiffer, "160-GHz power amplifier design in advanced SiGe HBT technologies With P_{sat} in Excess of 10 dBm," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 939–947, 2013.

Conferences

1. N. Sarmah, K. Aufinger, R. Lachner, and U. R. Pfeiffer, "A 200-225 GHz SiGe Power Amplifier with peak P_{sat} of 9.6 dBm using wideband power combination," *European Solid-State Circuits Conf.*, September 2016.

2. N. Sarmah, P. R. Vazquez, J. Grzyb, W. Foerster, B. Heinemann, and U. R. Pfeiffer, "A Wideband Fully Integrated SiGe Chipset for High Data Rate Communication at 240 GHz," *"European Microwave Integr. Circuits Conf."*, October 2016.

3. P. R. Vazquez, N. Sarmah, K. Aufinger, and U. R. Pfeiffer, "An OOK-modulator at 240 GHz with 20 GHz bandwidth," *German Microwave Conference (GeMiC)*, pp. 345–348, March 2016.

4. N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 246 GHz fundamental source with a peak output power of 2.8 dBm," *"European Microwave Integr. Circuits Conf."*, pp. 184–187, Sept 2015.

5. J. Grzyb, K. Statnikov, N. Sarmah, and U. R. Pfeiffer, "A wideband 240 GHz lens-integrated circularly polarized on-chip annular slot antenna for a FMCW radar transceiver module in SiGe technology," *Microwave and Optoelectronics Conference (IMOC)*, pp. 1–4, Nov 2015.

6. J. Grzyb, K. Statnikov, N. Sarmah, and U. R. Pfeiffer, "A broadband 240 GHz lens-integrated polarization-diversity on-chip circular slot antenna for a power source module in SiGe technology," *European Microw. Conf.*, pp. 570–573, Sept 2015.

7. J. Grzyb, K. Statnikov, N. Sarmah, and U. R. Pfeiffer, "A lens-integrated on-chip circular slot antenna for a 240 GHz power source in SiGe technology," *IEEE International Symposium on Antennas and Propagation USNC/URSI National Radio Science Meeting*, pp. 2055–2056, July 2015.

8. K. Statnikov, J. Grzyb, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A lens-coupled 210-270 GHz circularly polarized FMCW radar transceiver module in SiGe technology," *European Microw. Conf.*, pp. 550–553, Sept 2015.

9. N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "235−275 GHz (x16) frequency multiplier chains with up to 0 dBm peak output power and low DC power consumption," *IEEE Radio Freq. Integr. Circuits Symp.*, pp. 181–184, June 2014.

10. K. Statnikov, J. Grzyb, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 240 GHz circular polarized FMCW radar based on a SiGe transceiver with a lens-integrated on-chip antenna," *European Microw. Conf.*, pp. 1750–1753, Oct 2014.

11. R. Al Hadi, J. Grzyb, W. Foerster, S. Malz, H. M. Keller, N. Sarmah, and U. R. Pfeiffer, "All-silicon based terahertz integrated components: The next generation of terahertz imaging systems," in *Optical Sensors*. Optical Society of America, 2014.

12. U. R. Pfeiffer, Y. Zhao, J. Grzyb, R. A. Hadi, N. Sarmah, W. Foerster, H. Ruecker, and B. Heinemann, "A 0.53 THz reconfigurable source array with up to 1mW radiated power for terahertz imaging applications in 0.13 μm SiGe BiCMOS," *IEEE Int. Solid-State Circuits Conf.*, pp. 256–257, Feb 2014.

13. U. R. Pfeiffer, J. Grzyb, R. Al Hadi, N. Sarmah, K. Statnikov, S. Malz, and B. Heinemann, "SiGe transmitter and receiver circuits for emerging terahertz applications," *IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 1–4, 2014.

14. N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 135-170 GHz power amplifier in an advanced SiGe HBT technology," *IEEE Radio Freq. Integr. Circuits Symp.*, pp. 287–290, June 2013.

Contents

Contents x

List of Figures xiii

List of Tables xxiii

Nomenclature xxiii

1 Introduction 1

1.1 Motivation towards sub-mmWave frequencies 1

1.2 Application scenarios towards sub-mmWave frequencies 2

1.2.1 High data-rate communication systems 2

1.2.2 FMCW RADAR systems 4

1.2.3 Imaging systems 5

1.3 sub-mmWave system implementation 5

1.3.1 Optical based sub-mmWave systems 5

1.3.2 Electronics based sub-mmWave systems 6

1.3.2.1 III-V semiconductor based sub-mmWave systems 6

1.3.2.2 Silicon based sub-mmWave systems 7

1.4 Scientific contribution 10

1.5 Thesis outline 12

1.6 Contribution of others 14

2 Circuit design considerations towards sub-mmWave frequencies 15

2.1 LO signal-generation towards sub-mmWave frequencies 16

2.1.1 High-frequency oscillator-based LO signal source 16

2.1.2 Frequency multiplier-based LO signal source 17

2.1.2.1 Even-harmonic frequency mutiplier topologies 17

2.1.2.2 Odd-harmonic frequency mutiplier topologies 19

2.1.3 Conclusion . . . 20
2.2 Wideband techniques towards sub-mmWave frequencies . . . 21
2.2.1 Coupled-resonators . . . 21
2.2.2 Stagger frequency tuning . . . 22
2.2.3 Distributed amplifiers . . . 23
2.2.4 Conclusion . . . 24
2.3 Power Amplifiers towards sub-mmWave frequencies . . . 25
2.3.1 General PA design considerations . . . 25
2.3.2 Loadline matching considerations . . . 26
2.3.3 Conclusion . . . 29
2.4 Power-combiner PAs towards sub-mmWave frequencies . . . 30
2.4.1 Discussion on the general on-chip power combining techniques . . . 30
2.4.1.1 Series power-combiners . . . 31
2.4.1.2 Parallel power-combiners . . . 31
2.4.2 Conclusion . . . 33

3 Tx and Rx circuit building-blocks for frequencies above 200 GHz 34
3.1 240 GHz wideband PA . . . 35
3.1.1 PA output stage design . . . 36
3.1.1.1 EM-modeling considerations . . . 37
3.1.1.2 Maximum device size limitations . . . 37
3.1.1.3 Loadline considerations . . . 38
3.1.1.4 PA output matching . . . 38
3.1.2 PA drive stages and wideband interstage matching . . . 41
3.1.2.1 Capacitor-coupled LC resonator based interstage matching 41
3.1.3 240 GHz PA characterization results . . . 45
3.1.3.1 240 GHz PA small-signal characterization . . . 46
3.1.3.2 240 GHz PA large-signal characterization . . . 50
3.2 200-225 GHz 4:1 combiner Power Amplifier . . . 53
3.2.1 Coupled microstrip-line based ZDC for 4:1 power combination . . . 54
3.2.1.1 Optimization of the ZDC for efficient power combination . 56
3.2.2 Measurement results for the 200-225 GHz combiner-PA . . . 60
3.3 240 GHz wideband LO signal source . . . 66
3.3.1 Impact of the LO spurious harmonics on the system performance . . . 66
3.3.2 Circuit design considerations for wideband LO . . . 67
3.3.2.1 Optimum device size . . . 68
3.3.2.2 Interstage drive power requirements . . . 68

3.3.2.3 Wideband operation . . . 69
3.3.2.4 Spurious harmonics . . . 71
3.3.3 240 GHz LO signal source characterization results . . . 75
3.3.3.1 Absolute power measurements . . . 75
3.3.3.2 Harmonic measurements . . . 77
3.4 Mixers for 240 GHz quadrature Tx and Rx chipset . . . 81
3.4.1 240 GHz quadrature up-conversion mixer . . . 81
3.4.2 240 GHz quadrature down-conversion mixer . . . 85
3.5 Conclusion . . . 89

4 240 GHz fully-integrated quadrature Tx and Rx chipset 90
4.1 240 GHz quadrature Tx and Rx architecture . . . 90
4.2 High-speed PCB design and packaging . . . 92
4.3 240 GHz quadrature Tx and Rx characterization . . . 98
4.3.1 On-wafer RF characterization of the 240 GHz Tx and Rx chipset . . . 98
4.3.2 Free-space RF characterization of the 240 GHz Tx and Rx chipset . . . 103
4.3.2.1 Antenna radiation pattern measurement . . . 106
4.3.3 IF bandwidth characterization of the 240 GHz chipset . . . 107
4.3.4 Conclusion . . . 108
4.4 240 GHz ultra-high data-rate wireless communication . . . 110
4.4.1 Link-budget and modulation scheme . . . 110
4.4.2 240 GHz wireless communication data-rate measurements . . . 111
4.4.2.1 Measurement results for BPSK modulation scheme . . . 112
4.4.2.2 Measurement results for QPSK modulation scheme . . . 112
4.4.2.3 Summary of the data-rate measurements . . . 115
4.4.3 Conclusion . . . 116

5 Conclusion and future outlook 118
5.1 Recommendations for future work . . . 120

References 121

List of Figures

1.1 Block diagram of a FMCW RADAR system. The down-converted IF signal can be used to estimate the range (R) of the target. In general, the higher the bandwidth, the better is the range resolution. 4

2.1 Schematic of a frequency doubler circuit based on the Gilbert-cell topology. The RF and LO signal inputs are ac-coupled, and self-multiplication results in the generation of a dc-offset and a 2^{nd} harmonic component. 18

2.2 Schematic of a two-stage tuned CE amplifier. A passive network X(jω) isolates the capacitors C_1 and C_2. The network X(jω) can be implemented using a) a series-capacitor C_c, b) a series-LC circuit L_3, C_3, and c) a series-inductor L_4. 21

2.3 Schematic of a distributed amplifier. The overall amplifier architecture is additive, which results in wideband operation from DC to very high frequencies. 23

2.4 Equivalent current source representation of the output stage of a class-A PA. The output matching network transforms the load impedance R_L to R_t. Here, R_o is the real part of the output impedance after tuning out the parasitic capacitance [130]. 26

2.5 Layout cross-section of a SiGe HBT from IHP Microelectronics based on the double-polysilicon self-aligned (DPSA) architecture [131] with a lateral intrinsic-to-extrinsic base link. 27

2.6 Small-signal lumped equivalent circuit for the device shown in Figure 2.5 with the various parasitic elements [130, 131]. 28

2.7 Simulated real part of the output impedance of a cascode stage at different resonant frequencies. The output impedance decreases only by 14% from 60 to 120 GHz range while it decreases by 44% from 140 to 280 GHz [23]. . . . 29

2.8 Transformer-based series power-combiner. In this topology, the output voltages from the unit PAs are summed at the combiner output. At the output of the unit PAs, the load impedance Z_L is transformed to Z_L/n. 31

2.9 Transformer-based parallel power-combiner. In this topology, the output current from the unit PAs are added at the output of the combiner. At the output of the unit PAs, the load impedance Z_L is transformed to n×Z_L. 32
2.10 Transmission-line based parallel power-combiner. This topology is preferred at mmWave frequencies and higher. The small line dimensions reduce the insertion loss and ensures wideband operation [139, 140]. 33

3.1 Simulated MAG for a single-ended cascode stage is 9.4 dB at 240 GHz. The HBTs are biased at the peak f_{max} current of 12.5 mA, and transistors with an emitter area of 8×(0.96× 0.12) μm^2 are used. 35
3.2 Schematic of the output stage of the 240 GHz PA. The transistors Q1-Q4 have an emitter area of 8×(0.96× 0.12) μm^2. The microstrip-line based inductors TL1, coupled microstrip-line CL1 and the capacitor C_{out} forms part of the output matching network. 36
3.3 EM modeling of the parasitic via-inductance in HFSS, port1 is defined as a wave-port and port2 is defined as a lumped-port. The ground plane is in the M3 metal layer. 37
3.4 Tuning inductance versus transistor size at 240 GHz for a single-ended cascode stage. The emitter area of the transistor is N×(0.96× 0.12) μm^2. The required tuning inductance at 240 GHz is 28 pH for N=8. 38
3.5 Simulated P_{sat} at 240 GHz for different R_L. The optimum impedance at the collector of the output stage is 320 Ω, and the corresponding P_{sat} is 11.3 dBm. The P_{sat} is reduced only to 10.2 dBm for R_L= 100 Ω. 39
3.6 3D model for full EM simulation of the output stage. The via arrays connecting the inductor TL1 to the transistor are approximated as solid metals. The capacitors C_{out} and C_{cas} shown in Figure 3.2 are also included in the simulation. 40
3.7 Simulated small-signal gain for the full EM simulated model of the output stage of the 240 GHz PA shown in Figure 3.6. The peak gain is 6.5 dB at 240 GHz. 40
3.8 a) Wideband interstage matching of the 240 GHz PA based on capacitor-coupled LC resonators. The series capacitor C_c couples resonator1 and resonator2. b) Impedance transformation from Zin1 (input impedance of stage4) to Zin3 (synthesis of resonator2) from 200-300 GHz. 43
3.9 Simulated small-signal gain variation of the 240 GHz PA for different C_c. The bandwidth and gain-ripple increases with C_c. For C_c=15 fF, the simulated peak gain is 25 dB and the 3-dB bandwidth is 40 GHz. 44

3.10 Simulated small-signal common-mode gain of the 240 GHz PA. The attenuation is higher than 15 dB above 225 GHz. This makes the design robust against parasitic common-mode oscillations. 44
3.11 Simulated IIP3 of the 240 GHz PA. At 240 GHz, IIP3 is -6.5 dBm and OIP3 is 15 dBm. 45
3.12 Chip-micrograph of the 240 GHz PA. The total chip area including the auxiliary Marchand-baluns and pads is 0.345 mm^2. 45
3.13 Hardware correlation for the small-signal characterization of the 240 GHz PA. a) At 230 GHz, the measured S_{21} is 26 dB and the 3-dB RF bandwidth is 28 GHz. From 215-255 GHz, the measured $S_{11} \leq$ -10 dB. b) From 210-300 GHz, the measured reverse isolation S_{12} is less than -25 dB. 47
3.14 Hardware correlation for the Edwards and Sinsky's stability factor μ and μ' of the 240 GHz PA. Since a) μ >1 and b) μ' >1, the PA is unconditionally stable from 210-300 GHz. 48
3.15 Hardware correlation for the group-delay variation of the 240 GHz PA. From 220-260 GHz, the simulated group-delay varies only within 34-44 ps. The average measured group-delay matches closely with simulation results from 230 GHz. 49
3.16 Measurement setup for the large-signal bandwidth and linearity characterization of the 240 GHz PA. An external WR03 wideband high power source capable of delivering up to 6 mW at 240 GHz is used at the input. 50
3.17 Hardware correlation for the large-signal characterization of the 240 GHz PA. a) Linearity: The measured P_{sat} is 7.5 dBm, IP_{1dB} is -16.5 dBm and OP_{1dB} is 3.7 dBm at 240 GHz. b) P_{sat} versus frequency: From 225-260 GHz, the measured $P_{sat} \geq$ 6 dBm. 51
3.18 Hardware correlation for the PAE measurements of the 240 GHz PA. At 240 GHz, the peak PAE is 1% which is 0.5% less than simulation results. 52
3.19 Block diagram of the 200-225 GHz combiner-PA [146]. The output power from the core-PA is split using a 1:4 power-splitter (CL2-CL7). A 4:1 coupled microstrip-line based ZDC (CL8-CL13) combines the output from the unit PAs (PA1-PA4). 53
3.20 Impedance transformation at the 4:1 power-combiner input taking into account the loading effect of the unit PAs. a) The differential input impedance is Z_d. b) The common-mode input impedance is Z_c. Here, ZPA_d and ZPA_c are the respective large-signal differential and common-mode output impedances of the unit PAs. 54

3.21 Simulated Z_{odd} and Z_{even} versus trace-separation s for coupled microstrip-lines on the M6 metal layer of the BEOL. For this design, s=7 μm is optimum. For w=2.4 μm, this corresponds to a Z_{odd} of 105 Ω and Z_{even} of 38 Ω. 57
3.22 Simulated Z_d at the 4:1 power-combiner input from 200-240 GHz for three line dimensions: a) lc_1=35 μm, lc_2=65 μm. b) lc_1=lc_2=70 μm. c) lc_1=100 μm, lc_2=200 μm. 57
3.23 Simulated Z_c at the 4:1 power-combiner input from 200-240 GHz for three line dimensions: a) lc_1=35 μm, lc_2=65 μm. b) lc_1=lc_2=70 μm. c) lc_1=100 μm, lc_2=200 μm. 58
3.24 3D-model for full EM simulation of a) 1:4 power-splitter, and b) 4:1 power-combiner in HFSS. At the input and output, wave-ports are defined (not shown here) for higher accuracy. 59
3.25 Chip-micrograph of the 200-225 GHz a) breakout-PA: The chip area is 0.67 mm^2, and b) combiner-PA: The chip area is 1.44 mm^2. The unit PAs are identical to the core-PA. 60
3.26 Chip-micrograph of the additional breakout structures for estimating the insertion loss of the 1:4 power-splitter and 4:1 power-combiner. a) Back-to-back Marchand-baluns. b) Back-to-back 4:1 power-combiner with Marchand-baluns. c) Back-to-back 1:4 power-splitter with Marchand-baluns. 61
3.27 Hardware correlation for the insertion-loss of the 1:4 power-splitter and 4:1 power-combiner. From 200-240 GHz, the measured insertion loss is in the 1-2 dB range. 62
3.28 Hardware correlation for the large-signal bandwidth characterization of the 200-225 GHz combiner-PA and breakout-PA. The peak P_{sat} for the combiner-PA is 9.6 dBm at 215 GHz, and the 3-dB large-signal bandwidth is 34 GHz (200-234 GHz). 62
3.29 Hardware correlation for the linearity characterization of the 200-225 GHz combiner-PA at 215 GHz. The measured P_{sat} is 9.6 dBm, IP_{1dB} is -19 dBm and OP_{1dB} is 5.5 dBm. 63
3.30 Hardware correlation for small-signal bandwidth characterization of the 200-225 GHz combiner-PA. At 213 GHz, the peak gain is 25 dB and the small-signal 3-dB bandwidth is 20 GHz. 63
3.31 From 200-240 GHz, the measured $S_{11} \leq$ -10 dB and $S_{12} \leq$ -30 dB for the 200-225 GHz combiner-PA. 64

3.32 Top-level block diagram of the 240 GHz frequency multiplier-based LO signal source [7, 88]. It consists of an active balun, followed by four cascaded frequency doubler stages (D1-D4) and a three-stage 240 GHz PA. 67
3.33 Effect of spurious LO harmonics on the down-converted IF signal for coherent detection. For this illustration, only the spurious 15^{th} and 17^{th} harmonics were considered to simplify the analysis. 67
3.34 Schematic of the unit frequency doubler stage. The inductances TL_b and TL_c are implemented as shielded microstrip-lines in the TM2 metal layer with lengths l_b and l_c respectively. The capacitor C_{in} ac-couples the input signal to the switching quad and the transconductance stage. The doublers D1 and D2 are biased using the resistors R_b instead of TL_b to save chip area [7, 88]. . 68
3.35 Simulated large-signal characteristics for the doublers D1+D2, D3 and D4 for an overall output frequency of 240 GHz. For an output power of -2.8 dBm at 240 GHz, the corresponding LO power at the input of D1 is -10 dBm. 69
3.36 Simulated CG and P_{out} versus output frequency. The doublers D1 and D3 are tuned higher, and the doublers D2 and D4 are tuned lower. The overall 3-dB bandwidth is 50 GHz. At 240 GHz, a) the overall CG is 7.2 dB, and b) P_{out} is -2.8 dBm. 70
3.37 Interstage matching network of the 240 GHz LO signal source. The inputs of D3 and D4 are matched to a differential 100 Ω impedance. The doubler D4 is connected to a three-stage 240 GHz PA with 50 Ω lines, and is not shown here. 71
3.38 Simulated time-domain waveform at the output of the active balun and doubler D1 for an external input LO signal at 15 GHz. As the input power is increased from -10 to 0 dBm, the 3^{rd} harmonic component at the output of the balun increases, which results in a distorted waveform at the output of D1. 72
3.39 The 3^{rd} harmonic component in the input signal (15 GHz) of D1 results in a spurious 18^{th} harmonic at the overall output. The 90 GHz mixing product at the output of D1 is too high for D2, and is hence rejected. 72
3.40 Simulated P_{out} at the different harmonics for an input LO power of -10 dBm. At 15 GHz, P_{out} at the 16^{th} harmonic is 7.3 dBm. The relative attenuation of the 14^{th}, 15^{th} and 17^{th} harmonic is at least 25 dB. The effect of the 18^{th} harmonic only starts at input frequency less than 13.25 GHz, and hence can be ignored. 73

3.41 Simulated P_{out} at the different harmonics for an input LO power of 0 dBm. The effect of the spurious 18^{th} harmonic increases significantly below 14.25 GHz, and this results in P_{total} remaining constant. This substantially limits the usable input frequency range. Hence, the optimum input LO power is -10 dBm. 74
3.42 Chip-micrograph for the breakout of the 240 GHz LO signal source. The total chip area including the pads is 1.218 mm^2. For single-ended on-wafer measurements, an auxiliary Marchand-balun has been added at the output [88]. 74
3.43 Measurement setup for large-signal bandwidth characterization of the 240 GHz LO signal source. The low-frequency input signal (below 20 GHz) from the synthesizer is coupled to the chip using a GSG probe (DC-40 GHz) with a 2.9 mm K-connector. The output signal is measured using a WR03 GSG waveguide probe using an Erickson calorimeter and harmonic mixer. 75
3.44 Absolute power measurement of the 240 GHz LO signal source. For an input LO power of -10 dBm, the peak output power is 6.4 dBm at 230 GHz, and the 3-dB RF bandwidth is 50 GHz (215-265 GHz). For an input LO power of 0 dBm, the output power remains constant below 13.75 GHz. 76
3.45 Measured P_{out} at the different harmonics at the output of the 240 GHz LO signal source for an input power of -10 dBm. The output power at the 16^{th} harmonic (220-270 GHz) is close to absolute power measurements for input frequencies in the 13.75-16.875 GHz range. 77
3.46 Measured P_{out} at the different harmonics at the output of the 240 GHz LO signal source for an input power of 0 dBm. The output power at the 16^{th} harmonic (220-270 GHz) is close to absolute power measurements in the 13.75-16.875 GHz input frequency range. The 17^{th} and 18^{th} harmonic dominates below 13.75 GHz, and hence P_{total} remains constant. 78
3.47 The 2^{nd} and 3^{rd} harmonic component of the input signal at D1 and LO leakage from D3 results in spurious tones at 14^{th}, 17^{th} and 18^{th} harmonic of the input signal. 78
3.48 Measured phase-noise of the 240 GHz LO signal source. An external 15 GHz signal (-10 dBm) with a phase-noise of -135 dBc/Hz (1 MHz offset) is used. The measured phase-noise at 240 GHz is -110 dBc/Hz, which is a degradation of 25 dB. 79

3.49 Schematic of the 240 GHz quadrature up-conversion mixer. The transistors Q1-Q4 (I-mixer) and Q7-Q10 (Q-mixer) are part of the switching quads, and Q5-Q6 (I-mixer) and Q11-Q12 (Q-mixer) are part of the transconductance stage. At the IF inputs, common-collector based buffer amplifiers with shunt 50 Ω resistances are used for wideband matching. 82
3.50 Simulation results from the linearity characterization of the 240 GHz up-conversion mixer. The peak CG is 0.7 dB, P_{sat} is -5 dBm and OP_{1dB} is -8 dBm. A 25 MHz IF signal (-5 dBm) is used for this simulation. 83
3.51 Simulation results for the IF bandwidth characterization of the 240 GHz up-conversion mixer. The 3-dB IF bandwidth is 38 GHz. 83
3.52 Simulation results for the RF bandwidth characterization of the 240 GHz up-conversion mixer. The 3-dB large-signal RF bandwidth is 50 GHz. 84
3.53 Simulation results for the variation of P_{out} with LO power for the 240 GHz up-conversion mixer. For stronger switching, an LO power of 5 dBm and higher is required at the input of the 90° coupler. 84
3.54 Schematic of the 240 GHz quadrature down-conversion mixer. The transconductance stage (Q9-Q10) injects the RF current into the switching quads of the I-mixer (Q1-Q4) and Q-mixer (Q5-Q8). The optimum load impedance is 200 Ω. 85
3.55 Simulation results for the RF bandwidth characterization of the 240 GHz down-conversion mixer. The 3-dB RF bandwidth is 52 GHz. At 240 GHz, CG is -0.5 dB and NF is 14.2 dB. 86
3.56 Simulation results for the IF bandwidth characterization of the 240 GHz down-conversion mixer. For R_c=200 Ω, the peak CG is -0.5 dB and the 3-dB IF bandwidth is 35 GHz. An IF frequency of 33 MHz is used for this simulation. 86
3.57 Simulation results for the variation of CG and NF of the 240 GHz down-conversion mixer at different LO drive power levels. At an LO frequency of 240 GHz, the optimum LO drive power is greater than -2.5 dBm. 87
3.58 Simulation results for IP_{1dB} of the 240 GHz down-conversion mixer. At 240 GHz, IP_{1dB} is -2.5 dBm. For this simulation, a LO drive power of 5 dBm is used. 87

4.1 Block-diagram of the 240 GHz fully-integrated direct-conversion quadrature Tx and Rx chipset with wideband on-chip antennas. The IF inputs of the Tx and Rx are terminated with on-chip 50 Ω resistances for wideband IF matching [11]. 91

4.2 Schematic of the 8^{th} order low-pass LC filter from the 1^{st} design iteration. The filter is synthesized using the design methodology presented in [113, 142]. . . 93
4.3 Simulated 3-dB bandwidth of the ideal lumped LC low-pass filter is 15 GHz without the wire-bond inductance. A wire-bond inductance of 1 nH reduces the bandwidth and introduces a gain ripple of 3-dB at the passband edges. . . 94
4.4 Microstrip-line based stepped impedance low-pass filter from the final design iteration in the Rogers 4350B PCB material. For this optimization, wire-bond inductance and feed-lines are included as elements of the filter. 95
4.5 Simulated 3-dB bandwidth of the stepped impedance low-pass filter shown in Figure 4.4. The 3-dB bandwidth decreases from 16 to 14 GHz as the wire-bond inductance increases from 0.6 nH to 1.8 nH, and ringing in the passband is eliminated. 95
4.6 3D model for EM simulation of the PCB filter (including the effect of wire-bond connections) using HFSS. The chip and PCB ground pads are included to accurately model the ground return current. 96
4.7 Simulation results from the full-EM simulation of the PCB filter. The S_{21} in the passband is -0.5 dB, 3-dB bandwidth is 15 GHz and S_{11} is less than -10 dB up to 14 GHz. The group-delay variation is less than 10% up to 9 GHz. . . 97
4.8 Lens-mounted 240 GHz packaged-Tx. The chip is glued to an external silicon lens with a diameter of 9 mm and wire bonded onto a low-cost PCB material (ROGERS 4350B). The 240 GHz packaged-Rx looks similar and is not shown here. 97
4.9 Chip-micrograph of the 240 GHz fully-integrated quadrature Tx and Rx with on-chip antennas. The chip area including the pads is a) 1.535 mm^2 for the Rx, and b) 1.627 mm^2 for the Tx. 98
4.10 Measurement setup for the on-wafer characterization of the 240 GHz Tx. A GSG probe (DC-40 GHz) with a 2.9 mm K-connector is used to couple the external LO signal to the chip. A WR03 GSG probe is used at the Tx output. 99
4.11 Measurement setup for the on-wafer characterization of the Rx. A GSG probe (DC-40 GHz) with a 2.9 mm K-connector is used to couple the external LO signal to the chip. A WR03 GSG probe is used at the Rx input. 99
4.12 Hardware correlation for the on-wafer large-signal bandwidth and linearity characterization of the 240 GHz Tx. a) The measured P_{sat} at 240 GHz is 6 dBm, and the 3-dB large-signal bandwidth is 40 GHz (223-263 GHz). b) At 240 GHz, the measured IP_{1dB} is -11 dBm and OP_{1dB} is 3 dBm. 101

4.13 Hardware correlation for the on-wafer bandwidth and linearity characterization of the 240 GHz Rx. a) The peak CG is 13.5 dB at 228 GHz, and the minimum SSB NF is 15 dB. From 220-240 GHz, the average peak gain is 11 dB, and hence the 3-dB RF bandwidth is 28 GHz (218-246 GHz). b) Linearity characterization: At 240 GHz, the measured IP_{1dB} is -17 dBm. 102
4.14 Measurement setup for the free-space RF characterization of the 240 GHz Tx and Rx over a 30 cm wireless link. a) Tx: A pre-calibrated WR03 VNA extension module with an external horn-antenna with WR3.4 waveguide interface is used as the Rx. b) Rx: A pre-calibrated WR03 VNA extension module with an external horn-antenna with WR3.4 waveguide interface is used as the Tx. 103
4.15 Free-space RF characterization of the 240 GHz packaged-Tx and Rx. a) Tx: The peak P_{rad} is 8.5 dBm, and EIRP is 34.8 dBm at 238 GHz. The 3-dB bandwidth is 38 GHz (214-252 GHz). b) Rx: The peak CG is 17.8 dB at 223 GHz, and the minimum SSB NF is 13.5 dB. The average peak gain is 15 dB from 220-240 GHz, and hence the 3-dB RF bandwidth is 28 GHz (214-242 GHz). 105
4.16 Setup for the measurement of the antenna radiation pattern of the 240 GHz packaged-Tx. A 2-D rotational stage controlled by a stepper motor is used for precise alignment. An external WR03 VNA extension module is used as Rx. 106
4.17 Measured directivity of the on-chip antenna of the 240 GHz packaged-Tx and Rx. The FWHP is $\pm 4^\circ$ in the E-plane and $\pm 4.5^\circ$ in the H-plane, and this yields an estimated directivity of 26.4 dBi at 240 GHz. 106
4.18 Measurement setup for the IF bandwidth characterization of the 240 GHz packaged-Tx and Rx chipset. The Tx and Rx are placed back-to-back over a 90 cm distance. The IF inputs are connected to a VNA using external 90° and 180° hybrids for single-sideband modulation. 107
4.19 Measurement results from the IF bandwidth characterization at a carrier frequency of 240 GHz. This measurement is performed over a wireless link of 90 cm, and the 6-dB IF bandwidth is 13 GHz. 108
4.20 Simulated differential input impedance for a 50 Ω load termination at the single-ended output of the Marchand-balun. From 200-300 GHz, the input impedance is complex and the real part varies from 75-80 Ω. 109
4.21 Simulated maximum range for a high data-rate communication system using the 240 GHz packaged-Tx and Rx chipset for different modulation schemes. For a BER of 10^{-6}, the maximum estimated range for QPSK modulation is 6.2 m, for 16-QAM it is 1.4 m, and for 64-QAM it is 0.8 m. 111

4.22 Measurement setup for the 240 GHz high data-rate communication system for a wireless link of 70 cm. An AWG is used to feed the Tx IF input with PRBS9 data, and the IF outputs of the Rx are connected to a real-time oscilloscope. . 112
4.23 Eye-diagram and constellation for BPSK modulation scheme at a carrier frequency of 240 GHz. The measured rms EVM is a) 16% at 10 Gbps, b) 17.8% at 15 Gbps, c) 24% at 20 Gbps and d) 30% at 25 Gbps. 113
4.24 Eye-diagram and constellation diagram for QPSK modulation scheme at a carrier frequency of 240 GHz. The measured rms EVM is a) 15.7% at 17 Gbps, b) 17% at 20 Gbps and c) 24% at 24 Gbps. 114

List of Tables

3.1 Summary of the simulation and measurement results of the 240 GHz PA . . . 52
3.2 PAs/amplifiers above 200 GHz reported in the literature 65
3.3 Simulation and measurement results of the 240 GHz LO signal source 76
3.4 Signal sources above 200 GHz reported in the literature 80
3.5 Summary of the simulation results for the 240 GHz mixers 88

4.1 Summary of the on-wafer and free-space characterization of the 240 GHz Tx and Rx chipset 109
4.2 Summary of the 240 GHz communication system 115
4.3 Tx and Rx chips in the 220-325 GHz range reported in the literature 117

Chapter 1

Introduction

1.1 Motivation towards sub-mmWave frequencies

The decade-wide spectral band that extends from 0.3-3 THz is referred to as the sub-mmWave frequency band. This frequency band is also referred to as the terahertz gap ("THz gap") as the frequency is low to be bridged by the traditional optical and photonic based systems, and high to be bridged by the conventional electronics [1, 2]. The transition towards sub-mmWave frequencies is motivated by the limitations of the existing systems at lower frequencies, and also by the potential of new and novel applications. The abundant unregulated RF bandwidth [3] available at sub-mmWave frequencies is one of the key advantages. From 200-300 GHz, a contiguous 100 GHz spectrum (largest below 1 THz) is available, and this is unimpeded by atmospheric attenuation maxima and rain attenuation levels [4, 5]. Since data-rate for communication systems is directly proportional to the available RF bandwidth, it is particularly interesting for the implementation of wireless systems with data-rates towards 100 Gbps [6–13]. For Frequency Modulated Continuous Wave (FMCW) Radio Detection And Ranging (RADAR) systems [14–18], a higher RF bandwidth improves the range resolution, and a higher frequency of operation improves the lateral resolution. Another significant advantage of a higher frequency of operation is the reduced form-factor of the passives, and this makes the on-chip integration of antennas possible. Hence, a single-chip solution is feasible, and this results in an overall cost reduction. Moreover, the improved lateral resolution and the ability of sub-mmWave radiation to penetrate most non-conductive materials, along with its non-ionizing nature (compared to X-rays) makes it attractive for applications like imaging [19–21] for security and medical applications, material characterization [7], and non-destructive testing.

The electronic systems are preferred over the bulky optical and photonic systems [1, 22] for sub-mmWave systems due to the advantages like scalability, smaller form-factor and lower

cost. The significant strides in semiconductor process technology development in the recent past [23–25] have made electronics based system a strong contender towards bridging the THz gap. For electronics-based systems, silicon technologies are preferred as they allow the baseband and the digital circuitry to be integrated on the same chip. The resulting compact form-factor allows scalability, and results in a significant reduction of the cost thereby making it economically viable for large volumes. The III-V semiconductor based systems which are typically encapsulated in split-block waveguide packaging [13] are bulky and not easily scalable. The intense research in low-cost silicon-based mmWave systems in the last decades have already resulted in the commercialization of mass market solutions like the 77 GHz automotive RADAR among others. Such systems will be indispensable for the future of autonomous self-driven cars and intelligent driver assistance systems [26, 27].

The search for compact, scalable and cost-efficient systems towards sub-mmWave frequencies is a topic of active research. This thesis addresses the various circuit design challenges and system level considerations for the realization of a fully-integrated Tx and Rx chipset towards sub-mmWave frequencies in SiGe BiCMOS technologies.

1.2 Application scenarios towards sub-mmWave frequencies

In this section, a brief discussion of the different application scenarios towards sub-mmWave frequencies is presented. These applications leverage the significant advantages of operation at sub-mmWave frequencies like abundant RF bandwidth, compact form-factor of passives, and better lateral and range resolution.

1.2.1 High data-rate communication systems

The demand for ubiquitous wireless systems and the proliferation of high-definition (HD) multimedia content have resulted in a voracious appetite for anytime, anywhere high data-rate systems. This demand has pushed the existing systems to their limits. The maximum data-rate is limited by the RF bandwidth, and this follows from the Shannon-Hartley equation 1.1 [28]

$$C = B \times log_2(1 + \frac{S}{N}) \tag{1.1}$$

Here, C is the channel capacity in bits per second, B is the bandwidth and $\frac{S}{N}$ is the required signal to noise ratio (SNR) for error-free communication.

A consequence of operation towards sub-mmWave frequencies is the high Friis loss or the free-space-propagation-loss (FSPL). At 240 GHz, the FSPL over a 1 m distance is 80 dB while

it is only 46 dB at 5 GHz. The high FSPL can be compensated to some extent by using high gain antennas. However, the typical Tx output power above 200 GHz in silicon technologies is in the mW range [4, 6–11, 21, 29, 30]. Hence, only short range high-directive point-to-point wireless links are feasible [31]. Such links can be used within the realm of existing systems for further performance enhancement. Some of the potential application scenarios are summarized below [32].

- 5G cellular networks: As part of the hierarchical cellular networks, the wireless links towards sub-mmWave frequencies can be used as part of small cells (femto and pico cells) with typical coverage range less than 10 m. The typical operational environment includes static and mobile users for indoor and outdoor scenarios, and also as high data-rate backhaul networks for small cells [32, 33].

- Ultra high data-rate chip-to-chip communication: The ever shrinking feature size of high-performance transistors (CMOS gate length) have led to a considerable reduction in the size of the on-chip interconnects as well. However, the RC delay of physical interconnects far exceeds the transistor delay. This is one of the fundamental performance limiting factors. This challenge is further aggravated by the fact that contemporary microprocessor architectures are based on multiple core-level parallelizations. This requires high-speed communication between the various cores over the bus [34, 35]. A wireless bus where different cores communicate over a wireless link provides an alternative to the performance limiting physical interconnects. For high data-rate chip-to-chip communication, the operation towards sub-mmWave frequencies is attractive due to the advantage of significant form-factor reduction of the passives, particularly for the on-chip antennas.

- Close-proximity high data-rate communication: A typical scenario involves the wireless transfer of HD movie and audio between wireless gadgets within seconds over a very short link (1 m and less) like data kiosk [32].

- Wireless nanosensor networks: In this application, distributed autonomous nanosensors communicate among themselves over a very short range high data-rate wireless link. The sense parameters are relayed to a hub which communicates to the outside world using conventional WiFi and cell-phone networks. This is particularly interesting for applications like remote health monitoring of patients. The other application scenario can be Internet of Nano-things (IoNT) which enable interconnection of nanoscale devices with the existing communication networks [32, 36].

1.2.2 FMCW RADAR systems

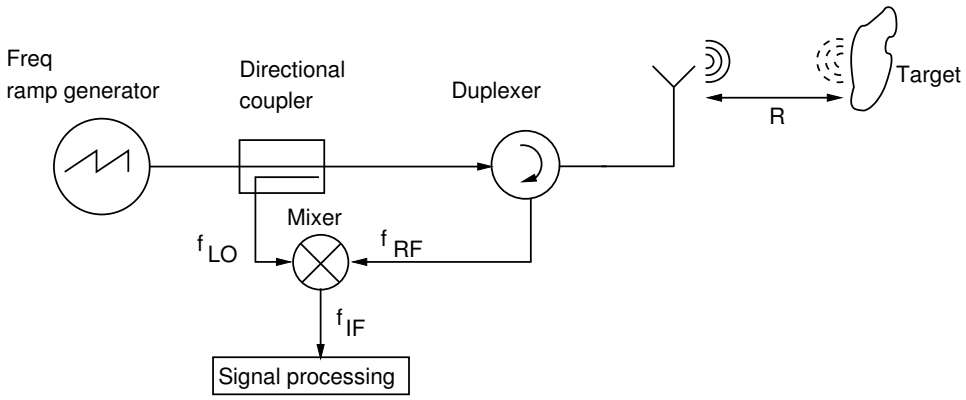


Figure 1.1: Block diagram of a FMCW RADAR system. The down-converted IF signal can be used to estimate the range (R) of the target. In general, the higher the bandwidth, the better is the range resolution.

The advancement in silicon process technologies have resulted in the proliferation of low-cost RADAR sensors for a variety of applications like contact-less motion and range detection systems [37], automotive RADAR for active safety [38–41], and recently even for hand gesture recognition for intelligent driver assistance [26]. The 77 GHz automotive RADAR is now commercially available in Silicon Germanium (SiGe) technology. In modern feature loaded cars, RADARs with different ranges for various functions are available [27, 38]. For RADAR based systems, the continuous-wave (CW) mode is preferred over the pulse-mode of operation. This is primarily due to the lower peak-power requirements in the CW mode. Figure 1.1 shows the block diagram of a widely used CW-based FMCW RADAR system. The directional coupler samples a part of the transmitted signal from the frequency ramp generator, and this is used as the LO signal for the mixer. The reflected signal f_{RF} from the target is mixed with f_{LO}, and the range (R) can be estimated from the down-converted IF signal f_{IF}. In general, the higher the bandwidth, the better is the range resolution [42, 43]. Since there is abundant RF bandwidth available at sub-mmWave frequencies, wideband FMCW RADAR systems at these frequencies are attractive. The other advantages of transition towards sub-mmWave frequencies are better lateral resolution and form-factor reduction of the passives like on-chip antennas.

1.2.3 Imaging systems

The non-ionizing nature of the sub-mmWave radiation and its ability to penetrate most non-conductive materials makes it well suited for imaging for security and medical applications, material identification and characterization, and other non-destructive evaluation systems [19–21, 29, 44–46]. The typical imaging systems are based either on the transmission mode or the reflection mode. In the transmission based system, the attenuation and phase change of the transmitted signal through the material-under-test (MUT) is measured. In the reflection mode system, the reflected signal from the MUT is measured either in a monostatic or bistatic configuration [47]. In general, imaging systems can be classified as active or passive imaging systems. For active imaging, a source of illumination is required for higher contrast or better signal-to-noise ratio. The coherence of the illumination source can sometimes cause unwanted specular effects which can destroy the image quality [21]. Hence, typically stochastically independent non-coherent sources are preferred. In contrast, passive imagers do not require any source of illumination and it measures the naturally-emitted thermal (black-body) radiation from an object [48]. For outdoor systems, the "cold" sky provides the reference for passive imagers, and there are low atmospheric attenuation windows at 94, 140 and 220 GHz [49].

1.3 sub-mmWave system implementation

The implementation of sub-mmWave systems can be realized either using optical or electronic techniques or a combination of both. The laser-based complex optical techniques are bulky, not easily scalable, and hence not cost efficient for certain applications. Although it is not always possible for electronic based systems to replace optical techniques, it does provide a promising and viable alternative. In this section, a comparative discussion between the optical and the various electronic based systems for the implementation of sub-mmWave systems are presented.

1.3.1 Optical based sub-mmWave systems

The optical techniques for sub-mmWave systems can be classified as CW and pulse-mode techniques [22]. The pulsed technique is extensively used for sub-mmWave or THz time domain spectroscopy (TDS) and imaging [50]. In this technique, femtosecond lasers are used to illuminate a photoconductive (PC) antenna [51] to generate THz pulses. For many applications like communication, CW signals are required. For CW generation of THz signals, the technique of photo mixing is frequently used [52]. The output power is low (typically μW range) in this case due to the high conversion-loss of the photomixer. A relatively high

power (typically mW range) CW THz generation technique involves quantum cascade lasers (QCL). The QCL use intersubband transitions in a repeated stack of semiconductor multiple quantum well heterostructures for laser action [53]. However, to make QCL operate at frequencies in the THz gap requires cryogenic cooling [1]. For the detection of CW THz radiation, various strategies based on direct detection and coherent detection exists. Some of the detectors based on the direct detection principle are calorimeters [54], bolometers [55], pyroelectric detectors [56] and pneumatic detectors like Golay cells [57]. The heterodyne detection techniques which require cryogenic cooling for operation include superconductor-insulator-superconductor (SIS) devices [58] and Josephson junctions [59].

1.3.2 Electronics based sub-mmWave systems

The implementation of sub-mmWave systems using electronics can be broadly categorized as vacuum electronic devices (VED) and solid state devices (SSD). In general, electronic sources convert the kinetic energy of the electron to electromagnetic radiation. Hence, VED is superior to SSD as the electron transport is collision-less in the vacuum with very little or no scattering which results in higher output power [60, 61]. The backward wave oscillators (BWO) are commonly used VED due to their wideband performance and high output power. In [62], a 0.65 THz source with 52 mW output power, and in [63] BWOs operating above 1 THz and output power in the 0.5-2 mW range are reported. The BWOs require high voltage (typically kV) and high magnetic field (0.6 T at 1 THz) [64], which is a significant disadvantage. Hence, it is not a scalable and cost-efficient solution.

1.3.2.1 III-V semiconductor based sub-mmWave systems

The III-V based compound semiconductor technologies have a higher maximum frequency of oscillation (f_{max}), higher output power, and lower noise in comparison to the silicon technologies. The commonly used III-V based transistors are the high-electron-mobility transistors (HEMT), metamorphic HEMT (mHEMT) and hetero-junction bipolar transistors (HBT). For HEMTs, Indium phosphide (InP) is among the fastest [61] while Gallium Nitride (GaN) based technologies have tremendous potential for high power application due to its higher breakdown voltage. In [25], an amplifier at 1 THz with 9 dB gain is reported in a 25-nm InP HEMT technology with a f_{max} of 1.5 THz. For GaN-based HEMTs, f_{max} greater than 600 GHz have been reported [32]. In [65], a THz imaging system using InP is reported, and in [66] a 100 Gbps wireless link is demonstrated using a mix of 35-nm mHEMT technology and optical techniques. In comparison to the VED, the III-V based systems are compact, and hence preferable. In [13], a 64 Gbps high data-rate communication system over a wireless

link of 850 m is demonstrated in a mHEMT technology. The III-V based systems are based on split-block waveguide components, and the digital and baseband circuitry cannot be integrated on the same chip. Hence, the scalability is limited, and it is not suitable for high volume applications.

1.3.2.2 Silicon based sub-mmWave systems

A significant advantage of silicon over the III-V semiconductor process technologies is the unmatched integration density. Such high level of integration is made possible due to the ability to implement the digital and baseband electronics in the same die. By integrating on-chip antennas, a single chip solution can be implemented. This makes silicon-based systems highly scalable, and hence economically viable for high volume applications. The last decades have seen tremendous improvements in silicon process technologies thereby making it a strong contender as a low-cost alternative towards bridging the THz gap. In [24], a 130-nm SiGe BiCMOS technology is reported with f_T/f_{max} of 300/500 GHz at room temperature. The integration of a CMOS backend in this technology gives the advantage of using the high-performance HBTs for the radio-frequency (RF) front-end, and CMOS for the digital and baseband circuitry. In [67], it is demonstrated that the achievable f_T/f_{max} for this technology is 479/798 GHz at 4.3 K. Recently as part of the DOTSEVEN project, SiGe HBTs with f_{max} approaching 700 GHz at room temperature [23] are targeted. For CMOS technologies, the gate length is reduced for increasing the f_T, and this results in the reduction of the breakdown voltage. For a 22-nm CMOS technology, the estimated f_T is 500 GHz, and it is expected by appropriate device layout f_{max} can be increased by 35-50% [1]. However, interconnect parasitics reduces the maximum achievable f_{max} considerably [1]. In [6], the reported f_{max} for a 40-nm SOI CMOS process is 300 GHz including the interconnects up to the top metal layer. An undesired consequence of increasing the device speed in silicon technologies is the reduced breakdown voltage. For SiGe HBTs, the Johnson limit given by $f_T \times BV_{CEO} \leq 200$ GHzV defines the relationship between f_T and BV_{CEO} [68]. Similarly, for CMOS technologies where the gate length is reduced for increasing the f_T, the breakdown voltage goes down. This limits the maximum voltage swing and hence the maximum output power. Among silicon technologies, the higher breakdown voltage of SiGe HBTs ($BV_{CEO} = 1.5V$, $BV_{CBO} = 4.5V$) [23] in comparison to CMOS technologies (maximum drain voltage of 1 V [69]) gives it an edge for applications towards sub-mmWave frequencies.

By leveraging the abundant RF bandwidth available at sub-mmWave frequencies, numerous high data-rate communication systems have been demonstrated above 200 GHz in low-cost silicon technologies. Since output power is typically limited, simpler modulation schemes like on-off keying (OOK) are preferred as it allows the Tx to be operated in saturation. The

OOK based communication systems have been demonstrated at 210 GHz [6] in a 32-nm SOI CMOS technology, and also at 260 GHz [8] in a 65-nm CMOS technology with a maximum data-rate of 10 Gbps. In [70], an OOK based communication system operating from 397-428 GHz is demonstrated in a 130-nm SiGe BiCMOS technology with a maximum data-rate of 10 Gbps. In [11], a fully-integrated 240 GHz I/Q Tx and Rx chipset with on-chip antennas is reported in a 130-nm SiGe BiCMOS technology. For quadrature-phase-shift-keying (QPSK) and bipolar-phase-shift-keying (BPSK) modulation schemes, the maximum measured data-rates using this chipset are 24 Gbps and 25 Gbps respectively over a wireless link of 70 cm. This chipset is also capable of supporting higher order modulation schemes like quadrature-amplitude-modulation (QAM), which is reported in the first generation of this chipset in [7]. A 240 GHz wideband QPSK transmitter and receiver in [9, 10] is demonstrated in a 65 nm CMOS technology with a maximum data-rate of 16 Gbps. In this implementation, frequency triplers are used for power generation at 240 GHz from an 80 GHz VCO. A 6-channel 300 GHz transmitter in a 40-nm CMOS technology capable of supporting 32-QAM modulation scheme is recently reported in [71] with a data-rate of 17.5 Gbps/channel.

In the literature, numerous implementations of FMCW RADAR systems above 200 GHz are demonstrated in low-cost silicon technologies which leverage on the high available RF bandwidth for better range resolution. Also, the higher frequency of operation results in a better lateral resolution. In [16], a 0.32 THz FMCW RADAR system in a 130-nm SiGe BiCMOS technology is demonstrated. The architecture is based on frequency multiplication, and the operational bandwidth is 27 GHz which results in a range resolution of 6.8 mm. A very wideband monostatic circular polarized FMCW RADAR system operating from 210-270 GHz [72] is demonstrated in a 130-nm SiGe BiCMOS technology with f_T/f_{max} of 300/450 GHz. The high RF bandwidth of 60 GHz for this chipset resulted in a range resolution of 2.75 mm. In this implementation, the use of a circularly polarized antenna eliminates the need for circulators. The other ultra-wideband FMCW RADAR systems at 240 GHz are reported in [17, 18, 73], and a 3D FMCW synthetic-aperture-RADAR (SAR) system at 240 GHz is reported in [17].

For imaging applications, a 160 GHz to 1 THz multi-color imaging system operating simultaneously at six harmonics is reported in a 130-nm SiGe BiCMOS technology in [20]. In [29], a fully integrated 825 GHz chipset with on-chip patch antennas is demonstrated in a 250-nm SiGe BiCMOS technology for heterodyne imaging. A 650 GHz SiGe receiver front end in a 250-nm SiGe BiCMOS technology is reported in [74]. This receiver is based on a sub-harmonic mixer topology, and the peak conversion-gain (CG) is -13 dB and the noise-figure (NF) is 42 dB at 650 GHz. A 1 k-pixel (32×32) camera chip for active terahertz video recording at room-temperature is reported for the first time in [19] in a 65-nm CMOS bulk

process technology. The individual pixels are based on square law detectors, and a wideband on-chip antenna designed to be used with an external silicon lens is used. The camera operates from 0.7-1.1 THz and operates up to 500 fps in the video mode. At 856 GHz, the total noise-equivalent-power (NEP) is 12 nW integrated over its 500-kHz video bandwidth. At the source side, free-running systems for active imaging are reported in [75] at 246 GHz in a 130-nm SiGe BiCMOS technology, and 288 GHz [76] in a 65-nm CMOS technology. In [21], a 0.53 THz reconfigurable free-running source array consisting of 16 (4×4) pixels with a total radiated power up to 1 mW is reported. The individual pixels are based on two triple-push oscillators locked 180° out of phase. In this implementation, the scalability of silicon technologies for array based systems together with a low-cost packaging system is demonstrated. In [77, 78], a tunable 500 GHz gas spectroscopy system in a 130-nm SiGe BiCMOS technology is demonstrated to detect toxic gases like nitrogen dioxide (493.28 GHz) and sulfur dioxide (491.93 GHz).

Based on the discussion above, it can be concluded that silicon process technologies are a promising low-cost alternative to the III-V technologies for different applications towards sub-mmWave frequencies.

1.4 Scientific contribution

This thesis addresses the various circuit design challenges and system level considerations for the realization of a fully-integrated Tx and Rx chipset towards sub-mmWave frequencies in SiGe BiCMOS technologies. The primary focus and the scientific contribution of this thesis are on the aspects of wideband circuit building-blocks with high gain (for amplifiers) and output power at frequencies of operation close to $f_{max}/2$. The results presented here are a significant improvement in comparison to the previous designs where the maximum frequency of operation for the amplifiers was up to $f_{max}/3$, and frequency multiplier stages were used for power generation beyond $f_{max}/3$. To circumvent the limited room for gain-bandwidth trade-off close to $f_{max}/2$, a comprehensive circuit design methodology encompassing optimum interstage matching for wideband operation, accurate parasitic modeling, and special loadline considerations for PAs (due to the low output impedance at high frequencies) is presented for the first time. Based on this approach, a 4-stage PA at 240 GHz using the capacitor-coupled LC resonator based bandwidth enhancement technique is reported with a record output power of 7.5 dBm, a peak small-signal gain of 26 dB and a 3-dB bandwidth of 28 GHz. In terms of International Technology Roadmap for Semiconductors (ITRS) figure-of-merit (FoM), this PA has the best FoM above 200 GHz among all other implementations of PAs in silicon technologies at the time of writing this thesis. Also, power combination for PAs operating above 200 GHz is demonstrated for the first time in a silicon technology. At 215 GHz, a 4:1 combiner-PA with a peak saturated output power (P_{sat}) of 9.6 dBm (record number) is reported, which is comparable with III-V technologies.

For LO signal-generation, sub-harmonic techniques were previously used for frequencies above 200 GHz. This was due to the challenge of generating sufficient output power over a wide bandwidth at fundamental frequencies. In this thesis, a high power wideband frequency multiplier-based LO signal source at 240 GHz is presented with a 3-dB bandwidth of 50 GHz. The technique of stagger frequency tuning is used for wideband operation, and this source is optimized for low dc-power consumption. The 240 GHz LO signal source presented in this thesis have the highest output power, bandwidth and DC-RF efficiency for frequency multiplier-based sources in the 200-325 GHz range in silicon technologies. This circuit can also be used as a standalone source, and also to pump sub-harmonic receivers at 480 GHz with an overall bandwidth of 100 GHz. By cascading non-linear stages at the output of this source, a wideband signal source at sub-mmWave frequencies can be implemented.

At the system level, a direct-conversion 240 GHz I/Q Tx and Rx chipset with wideband on-chip antennas is presented. The chipset is integrated into a low-loss chip-on-board (COB) packaging. The packaged chipset was used to demonstrate a high data-rate communication system at 240 GHz over a wireless link of 70 cm. For QPSK and BPSK modulation schemes,

the maximum measured data-rates using this chipset are 24 Gbps and 25 Gbps respectively. At the time of writing this thesis, this is the highest data-rate reported in the literature for fully-integrated wireless systems operating above 200 GHz in silicon technologies. The generic attribute of this chipset was demonstrated previously for the demonstration of a monostatic 210-270 GHz FMCW RADAR system implemented using identical circuit building-blocks.

Hence, the results presented in this work contribute further in establishing silicon-based fully integrated, low-cost systems with a compact form-factor as a viable alternative to the existing III-V based systems towards sub-mmWave frequencies. This work was partially funded by the European Commission within the DOTSEVEN project (no. 316755), and the DFG funded Real100G project. The results presented in this work contribute significantly to the success of these projects.

1.5 Thesis outline

This thesis is divided into five chapters in total including the Introduction. The outlines for the subsequent chapters are as follows.

- A general discussion of the different circuit design considerations towards sub-mmWave frequencies is presented in Chapter 2. The topics addressed here are wideband LO signal-generation using the frequency multiplier-based approach versus oscillator-based approach, and wideband amplifier design. Also, presented are the challenges in PA design for high output power, and the special considerations for loadline matching towards sub-mmWave frequencies. Furthermore, a discussion on the different power combination techniques for PAs is presented. The motivation for the choice of an appropriate circuit design topology for the individual circuit building-blocks for a 240 GHz quadrature Tx and Rx chipset is presented at the end of each section.

- The design and characterization results of the individual circuit building-blocks for a 240 GHz quadrature Tx and Rx chipset (presented in Chapter 4) are presented in Chapter 3. The circuit design of a four-stage 240 GHz PA with a peak P_{sat} of 7.5 dBm, a peak small-signal gain of 26 dB and a 3-dB bandwidth of 28 GHz is presented. Also presented is the design of a 4:1 combiner-PA operating from 200-225 GHz. For parallel power combination, the microstrip-line based zero-degree-combiner (ZDC) topology is used. For this design, the peak P_{sat} at 215 GHz is 9.6 dBm. For LO signal-generation, a 240 GHz wideband frequency multiplier-based signal source with a 3-dB bandwidth of 50 GHz, and a peak output power of 6.4 dBm at 230 GHz is presented. This wideband LO source is used to drive the mixers in the 240 GHz quadrature Tx and Rx chipset. This source uses four cascaded Gilbert-cell based frequency doubler stages. The individual doubler stages are optimized to eliminate the need for intermediate drive amplifiers and reduce the overall dc-power consumption. Furthermore, the design and simulation results for the 240 GHz up-conversion and down-conversion mixers are presented. It is challenging to characterize the breakout structures of the mixers with an external LO due to the drive power requirements, and hence only the simulation results are presented here.

- The RF and IF bandwidth characterization results from a fully-integrated 240 GHz quadrature Tx and Rx chipset with on-chip antennas is presented in Chapter 4. The chipset is based on the direct-conversion topology with on-chip antennas, and is integrated into a low-loss chip-on-board (COB) packaging. For wideband IF matching, a high-speed PCB (Rogers 4350B) with stepped-impedance microstrip-line based low-

pass filters is used. The packaged chipset was used to demonstrate a high data-rate communication system at 240 GHz over a wireless link of 70 cm. For QPSK and BPSK modulation schemes, the maximum measured data-rates using this chipset are 24 Gbps and 25 Gbps respectively.

- A summary of this thesis and the main conclusions are presented in Chapter 5. An outlook for the further improvement and enhancement of this work is also presented.

1.6 Contribution of others

This thesis work is a culmination of original contributions from my side. The contribution of the other group members in the Institute for High-Frequency and Communication Technology (IHCT) at the University of Wuppertal is acknowledged, and their specific contributions are listed here.

- For the 200-225 GHz combiner-PA presented in Chapter 3, a high gain driver-PA is added to facilitate on-wafer measurements. This is done to compress the core-PA since no external drive amplifiers are available in this frequency band, and the total waveguide and probe losses at the input and output are 10 dB. The driver-PA is based on a high gain LNA previously designed by Mr. Stefan Malz. The core-PA which is optimized for high output power is designed by Prof. Dr. rer. nat. Ullrich R. Pfeiffer. My contribution here is the investigation and the complete design and implementation of an efficient power-combiner for the maximum enhancement of the output power from the unit PAs. I have done the top-level layout and top-level simulation, which involves EM-circuit co-simulation using the full layout of the combiner.

- For the fully integrated 240 GHz I/Q Tx and Rx chipset presented in Chapter 4, the on-chip wideband 90° hybrid for quadrature LO generation, and the on-chip antennas were designed by Dr. Janusz Grzyb. The contributions of Mr. Pedro Rodriguez Vazquez in the top-level layout of the Tx and Rx chipset, and sample preparation for measurements are acknowledged. Prof. Dr. rer. nat. Ullrich R. Pfeiffer contributed in the top-level layout in the first version of the chipset.

- The high-speed PCB design activity was initiated as part of a bachelor thesis work for Mr. Robin Zatta with support from Mr. Pedro Rodriguez Vazquez. The insights and learnings from this design activity are acknowledged. The PCB design presented in this work is a completely new design implemented by me, and it is optimized for much higher bandwidth, flatter group-delay and return loss of less than -10 dB up to 14 GHz. Also, for mechanical stability, the overall filter size is minimized to reduce the size of the overall PCB. The suggestions from Dr. Janusz Grzyb for the full EM simulation of the filter is acknowledged. The contribution of Mr. Wolfgang Foester in preparing the PCB layout and communication with the PCB manufacturers is acknowledged.

Chapter 2

Circuit design considerations towards sub-mmWave frequencies

In Chapter 1, the various advantages and motivation for systems operating towards sub-mmWave frequencies have been presented. The implementation of "all-silicon" based sub-mmWave systems offer significant incentives like overall cost reduction and scalability. In this chapter, the different circuit design techniques and considerations for operation towards sub-mmWave frequencies are presented. The particular emphases are on the aspects of wideband operation, high power generation and wideband LO signal-generation.

This chapter is divided into four sections. At the conclusion of each section, the motivation for the choice of an appropriate topology for the implementation of the different 240 GHz circuit building-blocks in Chapter 3 is presented. In section 2.1, the pros and cons for LO signal-generation using oscillator-based and frequency multiplier-based approaches are presented. The different wideband circuit design techniques are presented in section 2.2. In section 2.3, the fundamental challenges limiting the output power of PAs operating towards sub-mmWave frequencies are presented, along with the special considerations for loadline matching. The different power combining techniques for PAs are presented in section 2.4.

2.1 LO signal-generation towards sub-mmWave frequencies

One of the primary challenges towards operation at sub-mmWave frequencies is wideband LO power generation for driving the mixers in the Tx and Rx chain. The choice of an appropriate LO topology depends on the application. A wideband tunable LO is preferred as it makes the implementation generic, and hence well-suited for different applications like communication, FMCW RADAR and imaging. The output power, bandwidth and phase-noise of a LO signal source are the important parameters. For communication systems, LO phase-noise contributes to the overall phase-modulation (PM) distortion at the output, which results in an increased error-vector-magnitude (EVM) and consequently a higher bit-error-rate (BER). For FMCW RADAR applications, LO phase-noise decreases the dynamic range which results in a significant reduction in the capability of resolving smaller targets against a high-density background clutter [79]. In this section, a discussion on the pros and cons of LO signal-generation techniques based on high-frequency oscillators and frequency multipliers is presented.

2.1.1 High-frequency oscillator-based LO signal source

The implementation of a fundamental VCO based LO signal source towards sub-mmWave frequencies in silicon technologies is confronted with the multiple challenges of limited transistor gain, and the low Q-factor of the passives primarily varactors. This results in low output power, and consequently a higher phase-noise. Also, the varactor parasitics at frequencies above 100 GHz severely limit the tuning range [80]. Another disadvantage of a higher fundamental frequency of oscillation is the challenge of implementing frequency dividers. The highest frequency of operation for static frequency dividers is 133 GHz, and is fundamentally limited by the gate delay [81, 82]. The maximum frequency of operation for the dynamic frequency dividers is comparatively higher. However, it requires high input power (greater than 0 dBm above 200 GHz) [83], which is a significant disadvantage. Hence, due to these challenges, the fundamental oscillators above 200 GHz in silicon technologies are free-running implementations with very limited tunability [4, 6, 75, 84]. This restricts their usability only for applications requiring non-coherent operation like OOK based communication. By lowering the fundamental frequency of oscillation to the 120-180 GHz range, power generation towards sub-mmWave frequencies are demonstrated using a push-push topology in [4, 85] and a triple-push topology in [21, 86]. In [87], a 240 GHz synthesizer is reported where the fundamental frequency of the VCO is 120 GHz, and a frequency doubler is used for power generation at 240 GHz. A lower fundamental frequency, in this case, makes it feasible to implement the frequency dividers. However, the tunability in all these cases is still very limited. By significantly reducing the fundamental frequency (below 20 GHz) and using frequency

multipliers, most of the limitations for high-frequency oscillators discussed in this section can be circumvented for LO signal-generation towards sub-mmWave frequencies.

2.1.2 Frequency multiplier-based LO signal source

In comparison to the high-frequency oscillators, the wideband frequency multipliers offer significant advantages like higher tunability and flexible phase-noise performance towards operation at sub-mmWave frequencies. This makes them well suited for applications requiring both a fixed and a tunable LO [7, 88]. Also, this approach is well-suited for process technologies without high-Q varactors at high frequencies. For an overall frequency multiplication factor of N, the degradation in phase-noise is $20 \times log(N)$ [89]. In comparison to oscillators, better and flexible phase-noise performance can be achieved using a frequency multiplier-based approach towards sub-mmWave frequencies. The phase-noise at an offset of 10 MHz for fundamental oscillators operating in the frequency range from 218-245 GHz is -98 dBc/Hz [4]. In contrast, the phase-noise at an offset of 1 MHz at 240 GHz is -110 dBc/Hz for a $\times 16$ frequency multiplier-based LO signal source. An external input signal at 15 GHz with a phase-noise of -135 dBc/Hz at an offset of 1 MHz offset is used in this case. This is shown in Figure 3.48 of section 3.3. The important requirements for frequency multiplier-based LO signal-generation are wideband operation, high output power, low dc-power consumption and suppression of spurious harmonics. A typical frequency multiplier chain consists of cascaded non-linear stages with intermediate drive amplifiers. The choice of an optimal frequency multiplication scheme is important as the drive amplifiers can contribute significantly to the overall dc-power consumption [29, 90]. A detailed discussion on the even-harmonic and odd-harmonic frequency multiplier topologies are presented in the next sections.

2.1.2.1 Even-harmonic frequency mutiplier topologies

The push-push topology is commonly used for even-harmonic generation due to its simplicity, wideband performance and inherent fundamental suppression [4, 91, 92]. For this circuit topology, the output load can either be connected at the collector node [90] or the emitter node [4]. For improving the conversion gain [92] harmonic traps (short at the even harmonic of interest) are sometimes used, but this limits the bandwidth and is hence not preferred. Some of the wideband push-push frequency doublers reported in the literature operate from 160-310 GHz with output power from 3 to -8 dBm in a 65-nm CMOS technology [93], 245-285 GHz with a peak output power of -7 dBm in a 40-nm CMOS technology [94], 215-240 GHz with a peak output power of -3 dBm, and 308-328 GHz with a peak output power of -1 dBm [90] in a 130-nm SiGe BiCMOS technology. The push-push topology for frequency quadru-

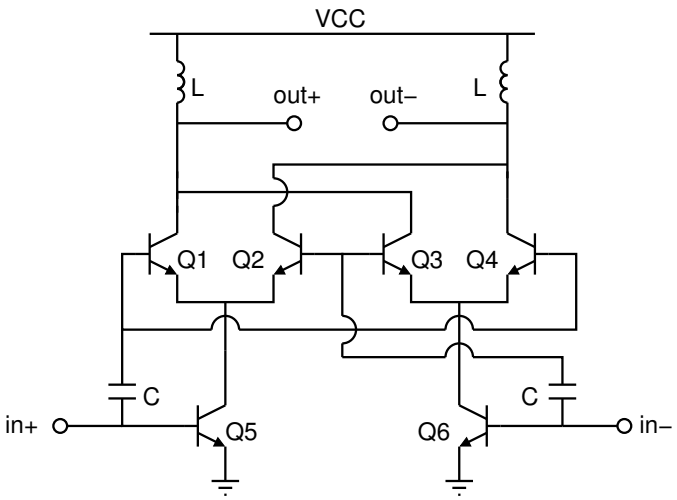


Figure 2.1: Schematic of a frequency doubler circuit based on the Gilbert-cell topology. The RF and LO signal inputs are ac-coupled, and self-multiplication results in the generation of a dc-offset and a 2^{nd} harmonic component.

pling is demonstrated for signal-generation at 500 GHz in [95] and 120 GHz in [96]. The disadvantage of the push-push topology is the inherent single-ended output. For differential operation, two push-push stages should be driven in quadrature. However, the 90° hybrids are lossy, narrowband and can occupy significant chip area [97]. The injection locked frequency doublers (ILFD) can also be used for even-harmonic generation. In this technique, the even-harmonic of the input signal from a non-linear stage is injected into an oscillator tuned to the even harmonic of interest. In general, ILFDs can operate with a low input power at the center frequency. However, the required input power increases and phase-noise degrades as the frequency-offset increases. The overall bandwidth depends on the locking range of the oscillator, which is related to the Q of the oscillator tank [98]. The complexity of implementing oscillators at higher frequencies limits the maximum frequency of operation for ILFDs to the lower mmWave frequencies [99, 100]. The injection locking technique can also be used for frequency quadrupling as reported in [101] for a 60 GHz injection-locked-qadrupler in a 65-nm CMOS technology.

In comparison to the other techniques, the balanced Gilbert-cell topology offers significant advantages like inherent differential operation, wideband operation, high conversion gain and inherent fundamental suppression [100]. In this topology, the self-mixing of the input signal results in the generation of a 2^{nd} harmonic signal at the output. Figure 2.1 shows the schematic of a Gilbert-cell based frequency doubler circuit. The input RF signal is coupled to the switching quad (Q1-Q4) using the coupling capacitors C. In this topology, the signals can be multiplied in phase or quadrature. For an input RF signal $A\cos\theta$, in-phase multiplication

results in a dc-offset of $\frac{A^2}{2}$, and a 2^{nd} harmonic component of $\frac{A^2}{2}\cos 2\theta$. For quadrature multiplication, no dc-offset is generated and the 2^{nd} harmonic component is $\frac{A^2}{2}\sin 2\theta$. The quadrature generation requires 90° hybrids which are lossy, narrowband and can consume significant chip area. Hence, effectively the power at the desired 2^{nd} harmonic is higher for in-phase multiplication as compared to the quadrature multiplication in typical implementations. The problem of dc-offset in the case of in-phase multiplication can easily be mitigated by using blocking capacitors, which form part of the interstage matching networks. In [102], V-band Gilbert-cell based frequency doublers operating from 55-75 GHz (31% fractional bandwidth) with a peak output power of 0.3 dBm is reported in a 130-nm SiGe HBT technology. A 235-275 GHz wideband (16% fractional bandwidth) frequency multiplier chain, consisting of 4 cascaded Gilbert-cell based doubler stages, with a peak output power of 0 dBm is reported in a 130-nm SiGe BiCMOS technology in [88].

2.1.2.2 Odd-harmonic frequency mutiplier topologies

For odd-harmonic generation, diode-based techniques based on anti-parallel diode pairs and anti-serial (back-to-back) diode pairs can be used to exploit the non-linearities of the p-n junction, and maximize the odd-harmonic of interest [103, 104]. The problems for the diode based frequency multipliers are high conversion loss and strong input drive power requirements. Hence, active frequency multiplier techniques using transistors are typically preferred. An overdriven CE amplifier stage is the simplest implementation of a single-ended frequency tripler. If a large input signal is applied to the input, then it results in a square wave at the output due to clipping. In the ideal case, a square wave contains only odd-order harmonics, and the odd-harmonic of interest can be maximized by an appropriate output matching network. The overdriven differential amplifier is a commonly used circuit topology for odd-harmonic generation as the differential operation eliminates any even-order harmonics at the output. In contrast to the push-push and Gilbert-cell based doubler topologies, which provides inherent fundamental suppression, there is a significant fundamental component at the output of a differential amplifier based odd-harmonic generator. In [29], cascaded $\times 3$ and $\times 5$ frequency multiplier stages are used for signal-generation at 820 GHz for an overall $\times 45$ frequency multiplication. This resulted in an Effective-Isotropic-Radiated-Power (EIRP) of -17 dBm at 823 GHz. Other examples of differential amplifier based frequency triplers are reported in [90, 105]. Similar to ILFDs, ILFTs can also be used for frequency tripling in the lower mmWave region [106–108].

2.1.3 Conclusion

A comparative discussion of high-frequency oscillator-based versus frequency multiplier-based approaches for wideband LO signal-generation towards sub-mmWave frequencies was presented. At sub-mmWave frequencies, frequency multiplier-based approach offers significant advantages like wideband tunability (without high-Q varactors at mmWave frequencies and higher) and better phase-noise performance. This also gives the Tx and Rx chipset a generic attribute, making it suitable for applications with a fixed LO (communication) or a tunable LO (FMCW RADAR, imaging) requirement. Based on these considerations, a wideband frequency multiplier-based LO signal source at 240 GHz is presented in section 3.3. The design goals for this LO signal source are a 3-dB bandwidth of at least 40 GHz, an output power greater than 5 dBm above 240 GHz, low external drive power (-10 dBm), and also the minimization of the overall dc-power consumption (less than 1 W). This source consists of four cascaded frequency doubler stages. The choice of the doubler topology over higher-order frequency multiplication factors are motivated by the factors of higher conversion gain and output power. The high output power from the individual doubler stages allows the stages to be cascaded without any intermediate drive amplifiers. This helps to reduce the overall dc-power consumption. The Gilbert-cell topology is preferred over the class-B and ILFD based frequency doublers due to its inherent differential operation, higher conversion gain and inherent fundamental suppression. For the Gilbert-cell topology, in-phase multiplication is preferred since hybrids are required for quadrature multiplication. The hybrids make the implementation narrowband, introduce loss and occupy significant chip area. The dc-offset generated due to in-phase multiplication can be eliminated by ac-coupling capacitors, which form part of the interstage matching networks.

2.2 Wideband techniques towards sub-mmWave frequencies

The implementation of wideband circuit building-blocks is important to leverage the abundant RF bandwidth available at sub-mmWave frequencies. At low frequencies, negative feedback is extensively used for bandwidth enhancement as sufficient gain is available. The other benefits of negative feedback are lower noise, better linearity and higher stability. The low maximum-available-gain (MAG) at operation frequencies close to $f_{max}/2$ leaves limited room for gain-bandwidth trade-off, and hence negative feedback cannot be used. In this section, some of the wideband circuit design techniques towards sub-mmWave frequencies are presented.

2.2.1 Coupled-resonators

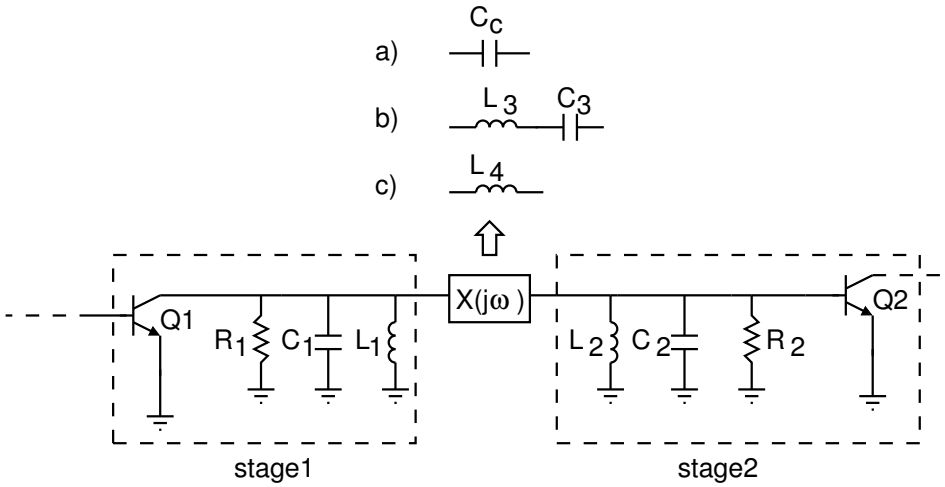


Figure 2.2: Schematic of a two-stage tuned CE amplifier. A passive network X(jω) isolates the capacitors C_1 and C_2. The network X(jω) can be implemented using a) a series-capacitor C_c, b) a series-LC circuit L_3, C_3, and c) a series-inductor L_4.

This section presents a summary of the discussions presented in [109–113] for bandwidth enhancement using coupled-resonators. The gain-bandwidth (GBW) product of an amplifier stage is independent of frequency, and it is limited by the inherent parasitic capacitance. The low gain per stage makes cascading of multiple stages inevitable as the gain from a single stage is not enough, especially at high frequencies. The cascading of stages result in a further reduction of the GBW product. Figure 2.2 shows a two-stage tuned common-emitter (CE) amplifier. Here, the equivalent resistance and capacitance of the output impedance of stage1 is R_1 and C_1, and it is R_2 and C_2 for the input impedance of stage2. L_1 and L_2 are the respective tuning inductors at the output of stage1 and input of stage2. The GBW product for stage1 alone is given by g_m/C_1. If stage1 and stage2 are directly coupled, the GBW product for the

first stage reduces to $g_m/(C_1+C_2)$ due to the loading of the succeeding stage. The reduction in GBW product can be mitigated by isolating the capacitors C_1 and C_2 with a passive coupling network $X(j\omega)$. The network $X(j\omega)$ can be implemented using a) a series-capacitor C_c, b) a series-LC circuit L_3, C_3, and c) a series-inductor L_4. The network $X(j\omega)$ introduces zeroes in the passband. By the optimum placement of the poles and zeroes, the bandwidth can be significantly enhanced. The inductively coupled-resonator, and the series-LC coupled-resonator require three inductors in total (including L_1 and L_2), which can consume significant chip area. Also, the self-resonance-frequency (SRF) of the inductors at high frequencies is a significant issue. The problem of low SRF for the shunt inductors L_1 and L_2 can be mitigated by using shorted transmission lines, but the problem with the series inductor persists. In contrast, the capacitor-coupled LC resonator technique gives similar performance, and is relatively simpler to implement with significantly less chip area. Hence, it is well suited for operation towards sub-mmWave frequencies. The bandwidth and gain-ripple increases with increasing C_c. The choice of an optimum C_c is based on the considerations of bandwidth, gain-ripple, peak gain and group-delay. In [109], the capacitor-coupled resonator technique is used for a wideband RF front-end with a fractional bandwidth of 20% at 60 GHz.

2.2.2 Stagger frequency tuning

For a multi-stage amplifier, if the individual stages are tuned to the identical center frequency then the overall bandwidth of the amplifier is significantly reduced. Another significant disadvantage of cascading identically tuned stages is the drastic increase in the overall group-delay variation as the number of cascaded stages increases. For communication applications, amplifiers with high group-delay variation are not suitable. If BW is the bandwidth of a single stage, then the overall bandwidth $BW_{overall}$ for N cascaded stages is $BW\times\sqrt{2^{\frac{1}{N}}-1}$ [111]. For a four-stage amplifier with identically tuned stages, $BW_{overall}$ is only 43.5% of the bandwidth of a single-stage. If the overall fractional bandwidth requirement is 15% for a 4-stage amplifier, then the required fractional bandwidth for the individual stages is 35%. Such high fractional bandwidth per stage can be quite challenging to achieve. To circumvent this limitation, stagger frequency tuning is an attractive option. In this technique, the individual stages are tuned to different frequencies. By appropriately choosing the center frequency of the individual stages, the overall bandwidth can be significantly enhanced. Another important consequence of frequency staggering between the individual stages of a multi-stage amplifier is the considerably reduced overall group-delay variation in comparison to identically tuned cascaded stages. This makes this technique well suited for applications like high data-rate communication where flat group-delay performance is important. The technique of stagger

frequency tuning has been demonstrated for wideband PAs in the D-band with a peak gain of 17 dB, and a fractional bandwidth of 23% (135-170 GHz) in a 130-nm SiGe technology in [114]. In [115], a 140 GHz amplifier using stagger frequency tuning is demonstrated in a 65-nm CMOS technology, and the resulting group-delay variation is 10 ps over a 12 GHz bandwidth.

2.2.3 Distributed amplifiers

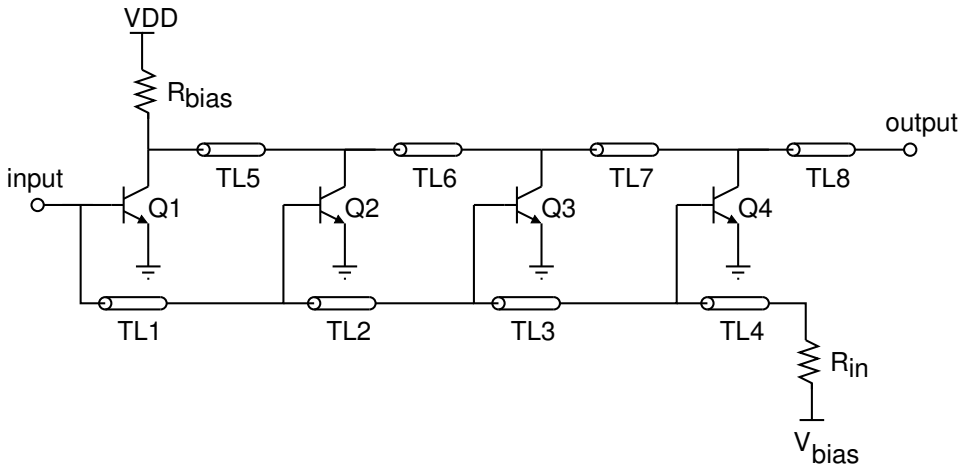


Figure 2.3: Schematic of a distributed amplifier. The overall amplifier architecture is additive, which results in wideband operation from DC to very high frequencies.

The distributed amplifiers (DA), which are also called traveling wave amplifiers, were first reported in [116, 117]. This technique uses gain-delay trade-off which results in wideband operation from DC to very high frequencies. Figure 2.3 shows the schematic for a distributed amplifier where the inputs of the transistor are fed by tapped delay lines and the outputs are fed into another tapped delay lines. These delay lines are typically implemented using transmission lines [118, 119]. The signal on the input line is amplified by each transistor, and the delay in the lines is such that each transistor adds power in phase at the output resulting in signal amplification. The overall amplifier architecture is additive i.e. the overall gain is obtained by adding up the gains of the individual stages, and not from multiplication as is typically the case with multi-stage amplifiers. Hence, the overall gain can be greater than 1 even at frequencies where gain per stage is less than 1. The overall voltage gain of the DA [118] is given by $n \times g_m \times (Z/2) \times L$ where Z is the characteristic impedance of the input and the output lines, g_m is the transconductance of each transistor, n is the number of stages, and L is the end-to-end loss of the overall transmission line. In the ideal case, unlimited bandwidth (from DC) is achievable from this amplifier topology. However, L is frequency dependent (skin-effect

and dielectric losses), and the parasitic capacitance at the input and output of the transistor modify the complex propagation constants and puts an upper limit on the maximum achievable bandwidth [120]. Some of the distributed amplifiers reported in literature operate from 14-105 GHz [121] in a 90-nm CMOS technology, 15-125 GHz in a 130-nm SiGe BiCMOS technology [122]. In [123], a distributed amplifier with 10 dB gain, and a 3-dB bandwidth of 110 GHz is reported in a 130-nm SiGe BiCMOS technology. A wideband traveling wave frequency multiplier operating from 220-275 GHz is reported in a 65-nm CMOS technology in [124]. For an overall required gain, more stages are required for distributed amplifiers as compared to the conventional multi-stage amplifier topology.

2.2.4 Conclusion

A discussion on the different wideband circuit design techniques towards sub-mmWave frequencies was presented. For the 240 GHz RF front-end components in Chapter 3, the distributed amplifier topology is the least preferred topology for bandwidth enhancement due to high dc-power consumption and large chip area requirements. The accurate modeling of the parasitics is very challenging above 200 GHz, and small modeling errors can result in a significant shift of the center frequency. The 240 GHz wideband PA presented in section 3.1 consists of four identical cascaded stages. By using identical stages, the impact due to any modeling errors can be significantly reduced. Hence, the capacitor-coupled LC resonator based bandwidth enhancement technique is used for the 240 GHz PA. The value of the coupling capacitor is chosen based on the considerations of bandwidth, measurement limitations, gain ripple, peak gain and group-delay variations. For the 240 GHz frequency multiplier-based wideband LO signal source presented in section 3.3, the individual doubler stages are frequency-staggered for wideband operation. This technique is used for the ease of implementation. Moreover, the sensitivity of the initial doubler stages to parasitics and modeling errors are less due to lower operation frequency.

2.3 Power Amplifiers towards sub-mmWave frequencies

In this section, the different circuit design considerations for the implementation of PAs towards sub-mmWave frequencies are presented. The particular emphasis is on the special load-line matching considerations due to the low output impedance of PAs.

2.3.1 General PA design considerations

The key performance parameters for a PA are gain, output power, linearity and power-added-efficiency (PAE). The optimum load impedance for a required output power and gain can be derived from the loadpull simulations. From loadpull simulations, contours of constant gain and output power for different load impedances can be obtained [125]. However, the loadline approach provides a simpler and an intuitive alternative to the loadpull simulation. In this approach, the optimum frequency independent load impedance (R_{opt}) which results in the simultaneous maximization of the voltage and current swing can be calculated from the equation 2.1. Here, V_{knee} is the knee voltage which is the saturation voltage for a CE stage, I_{DC} is the dc bias current (corresponding to peak f_{max}) [125, 126], and the maximum V_{DD} depends on the breakdown voltage.

$$R_{opt} \sim \frac{V_{DD} - V_{knee}}{I_{DC}} \tag{2.1}$$

For SiGe HBTs, the maximum V_{DD} is limited by the collector-emitter breakdown voltage for an open base configuration (BV_{CEO}) for a CE stage. If a low impedance biasing network is used, V_{DD} can exceed BV_{CEO} to a certain extent as it provides an escape path for hot carriers generated due to avalanche. Hence, the output power (P_{out}) is given by the equation 2.2. Here, x is the factor by which BV_{CEO} can be exceeded.

$$P_{out} = (\frac{xBV_{CEO} - V_{knee}}{2\sqrt{2}})^2 / R_{opt} \tag{2.2}$$

As the f_T of a process technology increases, BV_{CEO} decreases (Johnson limit). This limits the voltage swing, and hence the maximum P_{out}. To circumvent this, cascode topology is frequently used where the maximum V_{DD} is limited by the collector-base breakdown voltage for an open emitter configuration (BV_{CBO}) which is much higher than BV_{CEO} [127]. This allows a larger voltage swing, and hence a higher P_{out}. The power-added-efficiency (PAE) is another important performance metric which quantifies the DC-RF conversion efficiency. It is given by the equation 2.3.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}(1 - 1/Gain)}{P_{DC}} \tag{2.3}$$

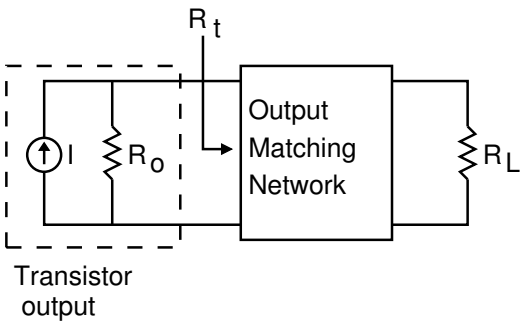


Figure 2.4: Equivalent current source representation of the output stage of a class-A PA. The output matching network transforms the load impedance R_L to R_t. Here, R_o is the real part of the output impedance after tuning out the parasitic capacitance [130].

The non-linear PA topologies like class-B, class-AB and class-C have higher PAE as compared to the linear class-A stage. This is because the device is on only for a certain duration of a cycle for the non-linear stages. The switch-mode PAs like class-E are another class of non-linear PAs which are highly efficient. For switch-mode PAs, the transistor is operated as a switch rather than a current source [126]. The parasitic capacitance makes the implementation of switches challenging towards sub-mmWave frequencies, and hence class-E PAs are limited to 100 GHz and below (low mmWave). In [128], the highest frequency class-E amplifier at 93 GHz is reported in a silicon technology with a PAE of 40.4%. In general, the non-linear topologies have lower gain than the linear topologies. At frequencies of operation close to $f_{max}/2$, the limited gain restricts the choice of topology to class-A. Hence, the PAE is very low. To compare the different linear PA implementations at different frequencies of operation (f), an ITRS FoM is defined. It is given by the equation 2.4 [129].

$$FoM_{PA} = P_{out} \times Gain \times PAE \times f^2 \tag{2.4}$$

2.3.2 Loadline matching considerations

The output stage of a class-A PA can be represented using an equivalent current source shown in Figure 2.4. Here, R_o is the output resistance (at resonance), and R_t is the transformed load impedance R_L due to the output matching network. The output matching network should be implemented so that the condition $R_o \parallel R_t = R_{opt}$ is satisfied. The R_{opt} (frequency independent) is the optimum loadline impedance from the equation 2.1, and this results in the simultaneous maximization of the voltage and the current swing. As the frequency of operation increases, R_o decreases and this effect is more evident above 100 GHz.

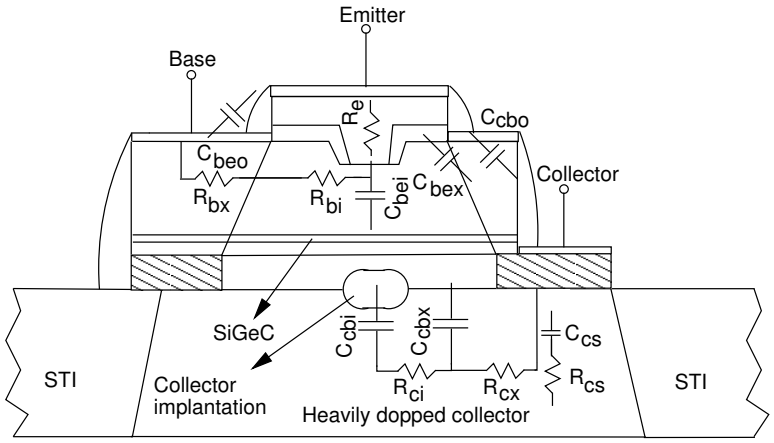


Figure 2.5: Layout cross-section of a SiGe HBT from IHP Microelectronics based on the double-polysilicon self-aligned (DPSA) architecture [131] with a lateral intrinsic-to-extrinsic base link.

Figure 2.5 shows the layout cross-section of a SiGe HBT from IHP Microelectronics with the different parasitic elements. This HBT is based on the double-polysilicon self-aligned (DPSA) architecture with lateral intrinsic-to-extrinsic base link. Here, R_{bi} is the internal base resistance, R_{bx} is the external base resistance, R_{cx} is the external collector resistance, R_{ci} is the internal collector resistance, R_e is the emitter resistance, R_{CS} is the collector-substrate resistance, C_{cbx} is the external base capacitance, C_{cbi} is the internal base-collector capacitance, C_{cbo} is the collector-base overlap capacitance, and C_{CS} is the collector-substrate capacitance [130, 131]. The corresponding small-signal equivalent circuit with all the parasitics is shown in Figure 2.6. For the CB stage of a cascode amplifier where the base is grounded, a tuning inductor at the collector node only tunes out the effective parasitic capacitance at the output which is dominated by the collector-substrate capacitance. The parasitic capacitances from the intrinsic device which are not accessible cannot be tuned out completely, and this introduces frequency dependence in R_o (at resonance). Based on the detail analysis presented in [130], $R_o \propto 1/f^2$.

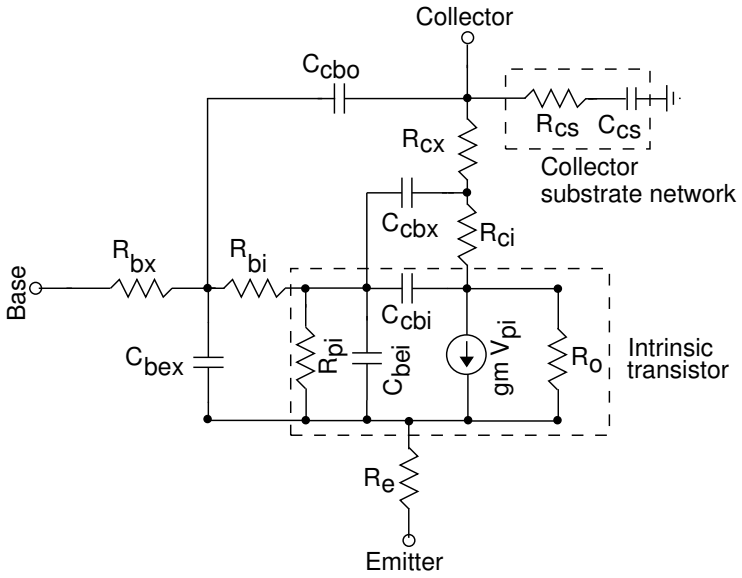


Figure 2.6: Small-signal lumped equivalent circuit for the device shown in Figure 2.5 with the various parasitic elements [130, 131].

Figure 2.7 shows the simulated output impedance for a single-ended cascode amplifier at different resonant frequencies. For this simulation, transistors with an emitter area of $8\times(0.96\times\ 0.12)\ \mu m^2$ from a 130-nm SiGe HBT technology [23] are used. From 60-120 GHz, the output impedance decreases only by 14% while it decreases by 44% in the 140-280 GHz frequency range. As R_o decreases with frequency, the loadline matching may not always be optimum depending on the relative values of R_t and R_o. The following scenarios need special consideration.

1. If $R_o \leq R_{opt}$, then the condition $R_o \parallel R_t = R_{opt}$ (from loadline matching) cannot be satisfied for any value of R_t. In this case, conjugate matching is the optimum.

2. If $R_o > R_{opt}$ and the required R_t for satisfying the condition $R_o \parallel R_t = R_{opt}$ is $R_t < R_o$, then loadline matching is the optimum.

3. If $R_o > R_{opt}$ and the required R_t for satisfying the condition $R_o \parallel R_t = R_{opt}$ is $R_t > R_o$, then more power is dissipated in the transistor output impedance than in the load. Hence, conjugate matching is the optimum in this case also.

Hence, due to the low output impedance of PAs towards sub-mmWave frequencies the loadline matching may not always be optimum. In that case, conjugate matching is the best option provided it ensures stable operation.

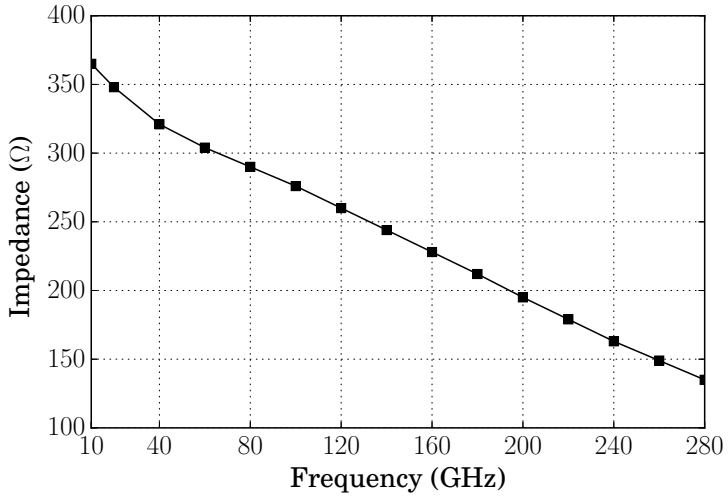


Figure 2.7: Simulated real part of the output impedance of a cascode stage at different resonant frequencies. The output impedance decreases only by 14% from 60 to 120 GHz range while it decreases by 44% from 140 to 280 GHz [23].

2.3.3 Conclusion

A discussion of the different circuit design considerations for PAs towards sub-mmWave frequencies was presented. The low MAG above 200 GHz in silicon technologies restricts the choice of the PA topology to class-A. Moreover, the low output resistance of a tuned amplifier stage with increasing frequency makes it challenging to efficiently couple the output power to the load, and the loadline matching may not always be optimum. Based on these considerations, the design of a four-stage class-A PA at 240 GHz is presented in section 3.1. In this case, conjugate matching is used at the output of the PA.

2.4 Power-combiner PAs towards sub-mmWave frequencies

The device size of the output-stage of a PA determines the maximum P_{sat}. This is based on the assumption that the output matching network provides the optimum load impedance at the PA output. As the frequency of operation increases, the required tuning inductance decreases for a given device size. Hence, the minimum synthesizable tuning inductance limits the maximum device size as discussed in details in section 3.1.1.2. At frequencies above 200 GHz, the effect of via-inductance can be substantial and hence the maximum device size is further limited. For the further enhancement of P_{sat}, power-combination networks provide an alternative. The power combination network combines the output power from multiple PAs. For a n-way power-combiner, the enhancement in the overall output power is by a factor of $10 \times \log(n)$ in the ideal case. For efficient power combination, the insertion loss of the combiner should be as low as possible. The power from the multiple unit PAs can be added in free-space or on-chip. The on-chip power combination networks are preferable [132–140] for fully-integrated systems due to its smaller form-factor, low chip-area requirement, and comparatively easier implementation over the free-space power combination topology [77, 78, 141].

2.4.1 Discussion on the general on-chip power combining techniques

The Wilkinson power-combiner [142] is the simplest power combination topology based on the quarter-wave impedance transformers. For n-way Wilkinson power-combiner, the required characteristic impedance of the transmission lines scales by a factor of $\sqrt{n}$. The minimum trace-width (from process technology) for microstrip-lines determine the maximum line impedance, and hence limits the scalability. To mitigate this, n-way Wilkinson power-combiners are based on a hierarchial structure or corporate ladder structure [143]. This significantly increases the chip-area requirements and the overall loss. Moreover, this approach is inherently narrowband since the line dimension is $\lambda/4$. Alternatively, the transformer-based power-combiners are preferable since they offer a significant advantage of simultaneous wideband impedance transformation and power combination in a compact form-factor. The common transformer-based power-combiners can be broadly classified as series power-combiners and parallel power-combiners [144]. Recently, a combination of the series and parallel power-combination topology is also reported in [136].

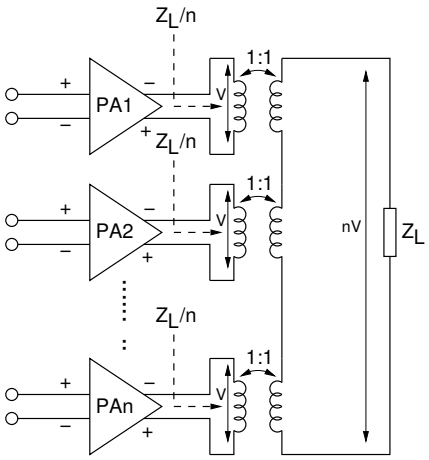


Figure 2.8: Transformer-based series power-combiner. In this topology, the output voltages from the unit PAs are summed at the combiner output. At the output of the unit PAs, the load impedance Z_L is transformed to Z_L/n.

2.4.1.1 Series power-combiners

The transformer-based series power-combiner is based on voltage addition. The output voltages from the unit PAs are combined at the output as shown in Figure 2.8. For 1:1 turns ratio, n-way series power combination results in the load impedance Z_L being transformed to Z_L/n at the output of the unit PAs. This allows larger device size for the unit PAs as the optimum load impedance goes down with increasing device size. However, this comes at the cost of increased sensitivity to parasitics. The distributed-active-transformer (DAT), which was first reported in [133], is a commonly used series power-combiner. In [134], a DAT based power combining PA (4:1) with an output power of 23 dBm at 60 GHz is demonstrated. As discussed in [134, 136], the scalability of DAT based power-combiner at mmWave frequencies is challenging beyond 2-way combination. The primary issue is the asymmetric load impedances seen by the unit PAs due to the inter-winding parasitic capacitances which can have implications on the stability.

2.4.1.2 Parallel power-combiners

The transformer-based parallel power-combiner adds the output current from the unit PAs at the combiner output as shown in Figure 2.9. For 1:1 turns ratio, n-way parallel power combination results in the load impedance Z_L being transformed to $n \times Z_L$ at the output of the unit PAs. Since the transformed load impedance at the output of the PA goes up (for 1:1 turns ratio), the sensitivity to parasitics is decreased. However, the power delivered from each PA is reduced due to the increase in the impedance at the output. This issue can be allevi-

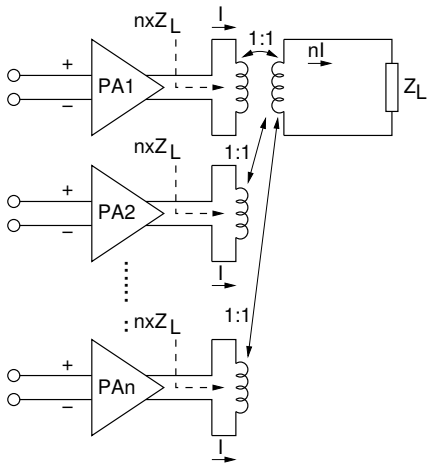


Figure 2.9: Transformer-based parallel power-combiner. In this topology, the output current from the unit PAs are added at the output of the combiner. At the output of the unit PAs, the load impedance Z_L is transformed to $n \times Z_L$.

ated by using an optimum impedance transformation ratio. The layout of the transformer-based parallel power-combiner is complex which results in a much lower SRF as compared to the transformer-based series power-combiner. Hence, transformer-based parallel power-combiners are typically used at low-frequencies (up to a few GHz) [138]. The parallel power-combiners at mmWave frequencies are based on transmission-lines as shown in the Figure 2.10. In this approach, transmission lines are used to add the output current from the unit PAs. The unit PAs drive the power-combiner in phase which results in a higher port-to-port isolation. By choosing the optimum line parameters, the line lengths can be significantly reduced to minimize the insertion-loss, and ensure optimum impedance-transformation and wideband operation. The Zero-Degree-Combiner (ZDC) based power combination networks have been demonstrated at mmWave frequencies for 8-way power combination in [139] and 16-way power combination in [140]. A combination of series and parallel power combining techniques is proposed in [145]. In this approach, the output currents from two DAT based series power-combiners are combined in parallel using transmission line based parallel power-combiner. This approach takes advantages of both series and parallel power combination while getting rid of their drawbacks. In [136], a 4-way power combination based on the series-parallel combiners is demonstrated for the entire E-band with a P_{sat} of 20.9 dBm and PAE of 22% in a 40-nm CMOS technology.

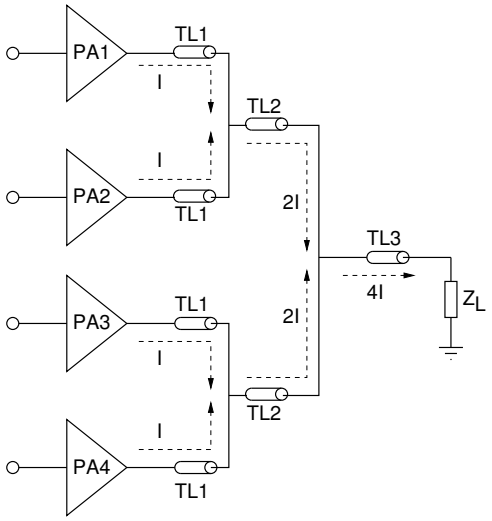


Figure 2.10: Transmission-line based parallel power-combiner. This topology is preferred at mmWave frequencies and higher. The small line dimensions reduce the insertion loss and ensures wideband operation [139, 140].

2.4.2 Conclusion

A discussion of the different on-chip power combining techniques for PAs was presented in this section. The transformer-based power combination networks, which also provide impedance transformation, result in an overall compact form-factor. The complex layout restricts the transformer based parallel combiners to the low GHz range, and typically DAT based series combiners are widely used at mmWave frequencies. However, the scalability of DAT beyond 2:1 is confronted with the challenge of asymmetric load impedances which can impact the stability. Moreover, the low SRF of transformers does not allow the implementation of DAT above 200 GHz. The compact transmission line based ZDC provides a viable alternative for power combination of PAs towards sub-mmWave frequencies. By keeping the line lengths smaller, insertion loss can be minimized and wideband performance can be ensured. Based on these considerations, a 200-225 GHz wideband power combining amplifier based on ZDC for 4:1 power combination with a peak output power of 9.6 dBm at 215 GHz is presented in section 3.2.

Chapter 3

Tx and Rx circuit building-blocks for frequencies above 200 GHz

In Chapter 2, the various circuit design considerations and challenges towards sub-mmWave frequencies are presented. This chapter presents the design and characterization results from the different Tx and Rx circuit building-blocks for a 240 GHz fully-integrated quadrature Tx and Rx chipset presented in Chapter 4. This chapter is divided into four sections. In section 3.1, a 240 GHz wideband PA optimized for high gain and output power is presented. To drive the mixers in the Tx and Rx chipset, a frequency multiplier-based wideband LO signal source at 240 GHz is presented in section 3.3. This source can also be used as a standalone tunable high-power source. In section 3.4, the design considerations for the up-conversion and down-conversion mixers of the 240 GHz Tx and Rx chipset are presented. The mixers are characterized as part of the overall Tx and Rx chipset since it is difficult to characterize breakout structures of the mixers due to the challenge of providing sufficient LO drive power from external sources. In [7, 88], the first generation of these circuits were reported, and the second generation of these circuits are presented in this work. These circuits are implemented in a 130-nm SiGe BiCMOS technology from IHP Microelectronics, and is developed within the DOTSEVEN project [23]. The peak f_T/f_{max} for this technology is 350/550 GHz, and the back-end-of-the-line (BEOL) offers seven metalization layers. This process technology offers silicided and unsilicided polysilicon resistors, MIM capacitors (1.5 fF/μm^2), and two thick top metal layers with a thickness of 2 μm (TM1) and 3 μm (TM2) for RF applications.

In section 3.2, a 200-225 GHz wideband power combining amplifier is presented. For 4:1 parallel power combination, a microstrip-line based zero-degree-combiner (ZDC) is used. This circuit is implemented in a 130-nm SiGe BiCMOS technology from Infineon Technologies AG which is also developed within the DOTSEVEN project [23]. The process technology features high-speed npn-HBTs with peak f_T/f_{max} of 250/370 GHz. The BEOL offers

seven metalization layers with thick low-loss copper layers at the topmost layer for mmWave applications. The results from this work have been reported in [146].

3.1 240 GHz wideband PA

The design of a 240 GHz wideband PA with high gain and output power is presented in this section. In the ideal case, the MAG for this process technology at 240 GHz is 9.4 dB as shown in Figure 3.1. For this simulation, a single-ended cascode amplifier is used. By taking into account the typical implementation losses of 3-3.5 dB, the net MAG is 6-6.5 dB. The 240 GHz wideband PA consists of four cascaded stages. For on-wafer characterization, auxiliary Marchand-baluns [142] have been added at the input and output. The individual stages of the PA are based on the pseudo-differential cascode topology due to the advantages (over the CE stage) like higher breakdown voltage and better isolation as presented in section 2.3.

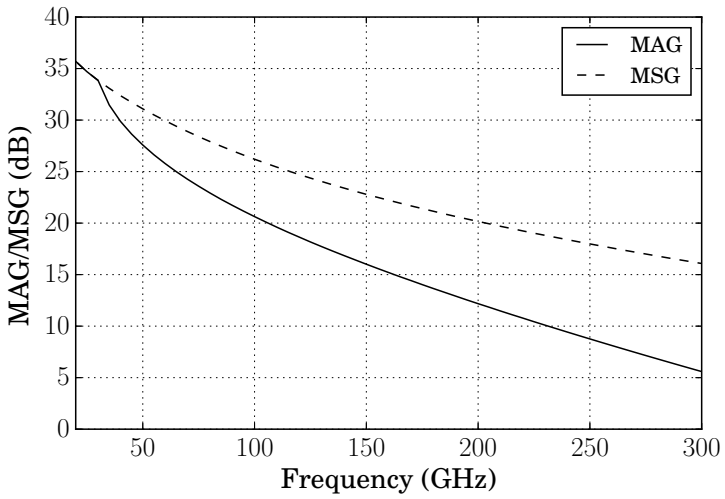


Figure 3.1: Simulated MAG for a single-ended cascode stage is 9.4 dB at 240 GHz. The HBTs are biased at the peak f_{max} current of 12.5 mA, and transistors with an emitter area of $8\times(0.96\times\ 0.12)\ \mu m^2$ are used.

The implementation of a true differential amplifier with a tail current source above 200 GHz is challenging. An active tail current source is not effective anymore due to its low output impedance. The other option of using inductor-based current source is not effective as the low SRF limits the maximum synthesizable inductance. Ideally, the inductance should be as high as possible for the current source implementation. The other alternative of implementing transmission line based inductors (λ/4 lines) is inherently a narrowband solution. Hence,

for this design a pseudo-differential topology is used. For wideband operation, the capacitor-coupled LC resonator based interstage matching technique is used. This technique is discussed in details in section 2.2.1. The detail considerations of the different circuit design aspects are presented in the following sections.

3.1.1 PA output stage design

The design of a PA starts with the optimization of the output stage, and the schematic of the output stage of the 240 GHz PA is shown in Figure 3.2. The microstrip-line based tuning inductor TL1, coupled microstrip-line CL1 and the capacitor C_{out} forms part of the output matching network. The transistors Q1-Q4 are biased using current mirrors (not shown). The total decoupling capacitances C_{decap} (at the Vcc node) and C_{cas} (at the bases of Q3 and Q4) are 5 pF and 100 fF respectively.

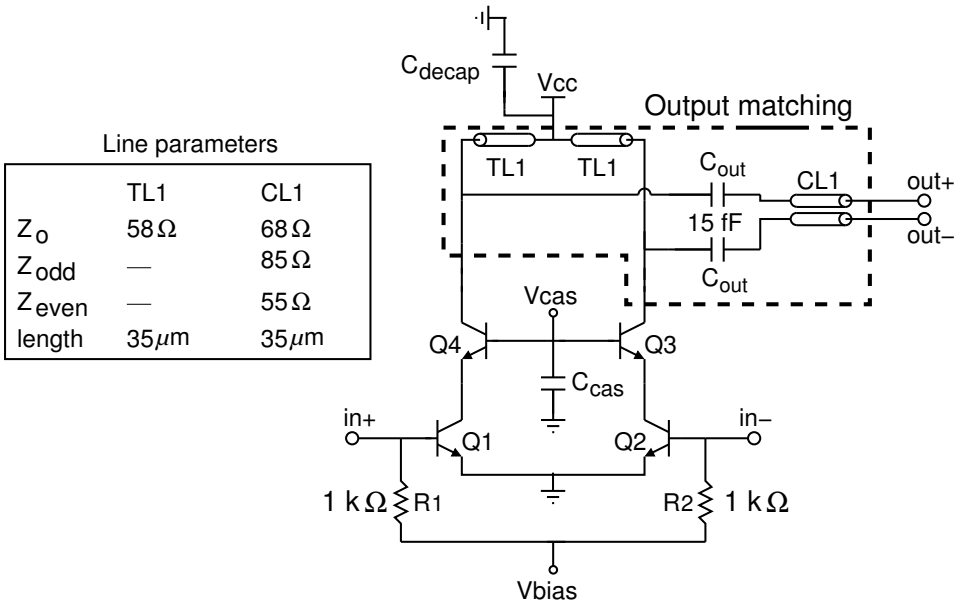


Figure 3.2: Schematic of the output stage of the 240 GHz PA. The transistors Q1-Q4 have an emitter area of $8\times(0.96\times\ 0.12)\ \mu m^2$. The microstrip-line based inductors TL1, coupled microstrip-line CL1 and the capacitor C_{out} forms part of the output matching network.

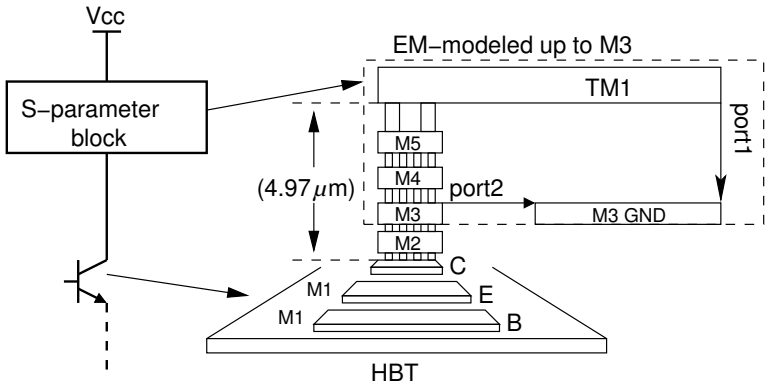


Figure 3.3: EM modeling of the parasitic via-inductance in HFSS, port1 is defined as a wave-port and port2 is defined as a lumped-port. The ground plane is in the M3 metal layer.

3.1.1.1 EM-modeling considerations

The inductor TL1 can be implemented in the low-loss TM1 or TM2 metal layers of the BEOL. The TM1 layer is preferable over the TM2 layer as the distance to the transistor interconnect (M1 layer) is 4.97 μm while the distance is 9.77 μm for the TM2 layer. Smaller distance to the ground plane results in a lower parasitic via-inductance. Based on the dc-routing and other layout considerations, the M3 metal layer is used as the ground plane. The effect of the via-inductance is EM simulated up to the M3 layer. The 3D model shown in Figure 3.3 is used for full EM simulation in HFSS, port1 is defined as a wave-port and port2 is defined as a lumped-port.

3.1.1.2 Maximum device size limitations

Although large devices are preferred for a higher P_{sat}, the required tuning inductance at the collector limits the maximum device size of the output stage. For this design, transistors with an emitter area of $8\times(0.96\times\ 0.12)\ \mu m^2$ are used, and the required tuning inductance at 240 GHz is 28 pH as shown in Figure 3.4. Any further device scaling will require smaller inductances, and the parasitic via-inductance can be a significant proportion of it. Based on the maximum dc current requirement of 12.5 mA, the trace width for TL1 in Figure 3.2 is 2 μm. From EM simulation in HFSS, the characteristic impedance Z_o for this line dimension with the ground plane in the M3 metal layer is 58 Ω and attenuation is 2666 dB/m.

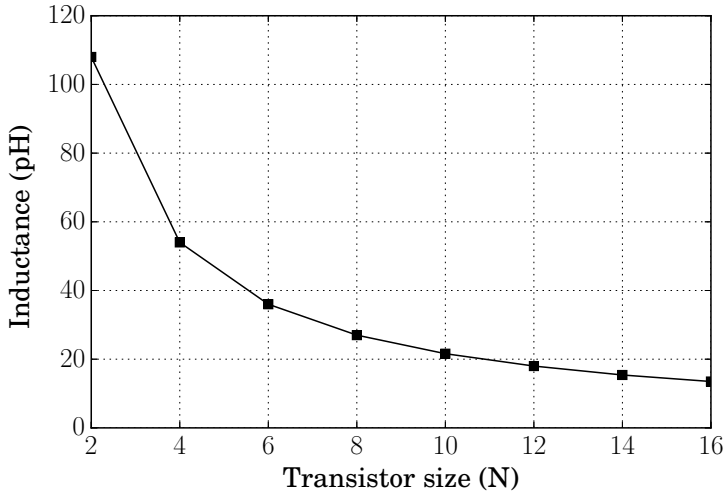


Figure 3.4: Tuning inductance versus transistor size at 240 GHz for a single-ended cascode stage. The emitter area of the transistor is N×(0.96× 0.12) μm^2. The required tuning inductance at 240 GHz is 28 pH for N=8.

3.1.1.3 Loadline considerations

For a single-ended cascode stage, R_{opt} from the loadline analysis is 208 Ω which is calculated using the equation 2.1 in section 2.3. Here, V_{CC} is 4 V, V_{knee} is 1.4 V and I_{dc} is 12.5 mA. The R_o for a single-stage cascode amplifier at resonance is 160 Ω for transistors with an emitter area of 8×(0.96× 0.12) μm^2 as shown in Figure 2.7 in section 2.3. Since R_o is less than R_{opt}, conjugate matching is optimum in this case based on the considerations in section 2.3.2.

3.1.1.4 PA output matching

For conjugate matching, the differential load impedance R_L of 100 Ω must be transformed to 320 Ω (an impedance transformation ratio of 3.2). The transformer-based impedance transformation networks, which are widely used at mmWave frequencies [135, 136, 147, 148], can not be used anymore due to the lower SRF of transformers. The other alternative is the microstrip-line based quarter-wave (λ/4) transformer. The disadvantages of this technique are narrowband operation, higher loss and larger chip-area requirement (156 μm at 240 GHz). To simplify the output matching network, a 1:1 impedance transformation ratio is used in this case. In this case, the simulated P_{sat} for the output stage is 10.2 dBm at 240 GHz which is only 1.1 dB less as compared to an impedance transformation ratio of 1:3.2 as shown in Figure 3.5. For implementing the output matching, coupled microstrip-line CL1 in the topmost TM2 metal layer of the BEOL is used. The TM2 layer facilitates easier routing since the tuning

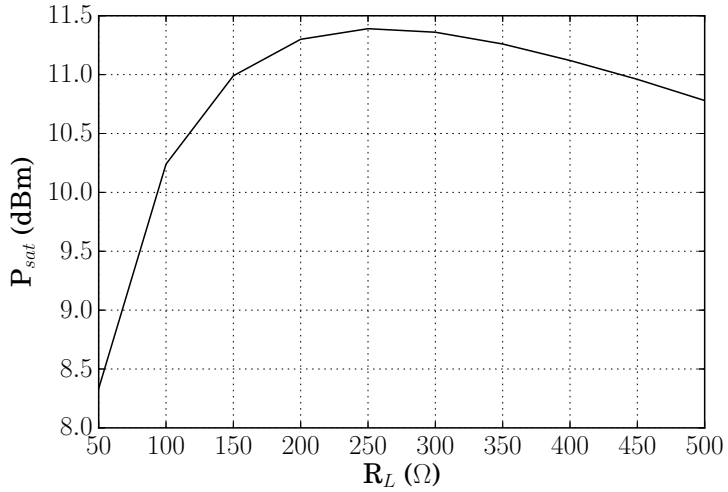


Figure 3.5: Simulated P_{sat} at 240 GHz for different R_L. The optimum impedance at the collector of the output stage is 320 Ω, and the corresponding P_{sat} is 11.3 dBm. The P_{sat} is reduced only to 10.2 dBm for R_L= 100 Ω.

inductors are implemented in the TM1 layer below. From EM simulations, a coupled line with w=2.5 μm and s=4 μm corresponds to Z_{odd} of 85 Ω and Z_{even} of 55 Ω. The attenuation for the odd and the even modes are 2600 dB/m and 1420 dB/m respectively. For a line length of 35 μm, an impedance transformation ratio close to 1:1 can be realized, and the net transformed impedance has an imaginary part. Based on this consideration, the line length for TL1 is 35 μm. Figure 3.6 shows the 3D model for the full EM simulation of the output stage in HFSS. To reduce the computation time, the via arrays connecting the tuning inductor TL1 to the transistor are approximated as solid metal. The output matching capacitor C_{out} and the decoupling capacitor C_{cas} are also modeled to ensure that they operate well below their respective SRF. The simulated small-signal gain is 6.5 dB at 240 GHz as shown in Figure 3.7.

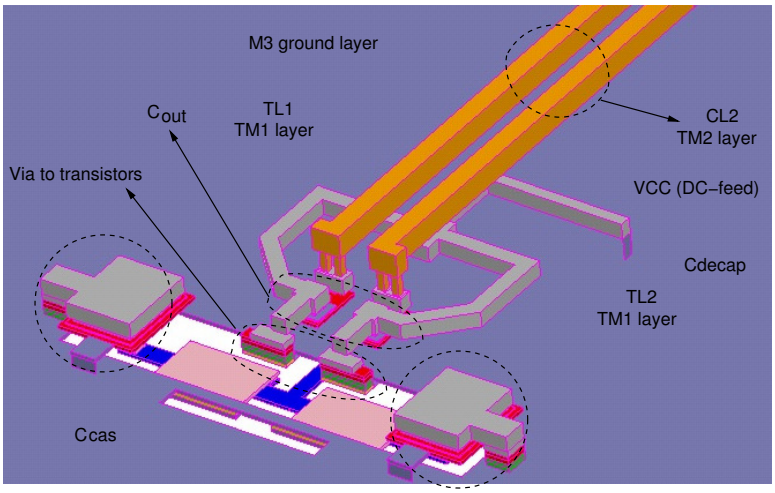


Figure 3.6: 3D model for full EM simulation of the output stage. The via arrays connecting the inductor TL1 to the transistor are approximated as solid metals. The capacitors C_{out} and C_{cas} shown in Figure 3.2 are also included in the simulation.

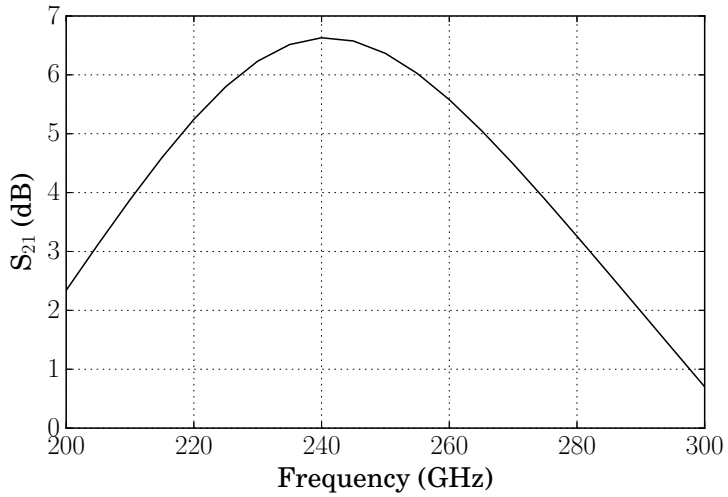


Figure 3.7: Simulated small-signal gain for the full EM simulated model of the output stage of the 240 GHz PA shown in Figure 3.6. The peak gain is 6.5 dB at 240 GHz.

3.1.2 PA drive stages and wideband interstage matching

For multistage PA design, the device sizes are typically scaled from the input stage to the output stage to cope up with the increasing input RF power at each stage [126, 149]. However, in this design, the transistor sizes for all the stages have been kept identical to that of the output stage. This gives the flexibility of cascading multiple stages (based on the overall gain requirement) without significantly altering the matching networks. By cascading identical stages, the probability of mutual frequency misalignment between the stages due to modeling uncertainties is also reduced.

3.1.2.1 Capacitor-coupled LC resonator based interstage matching

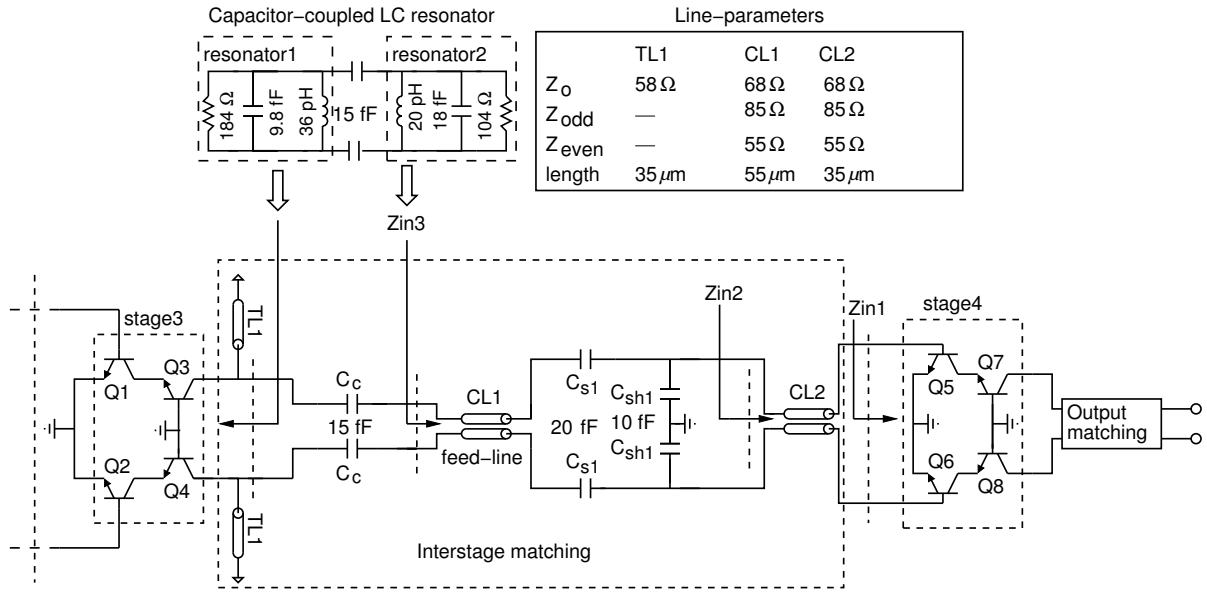
Figure 3.8a shows the schematic of the interstage matching for stage3 consisting of the transistors Q1-Q4, and stage4 consisting of the transistors Q5-Q8. The interstage matching networks for all the stages are identical. Hence, the interstage matching between stage3 and stage4 (output stage) is considered here. For wideband interstage matching, the technique of capacitor-coupled LC resonators presented in section 2.2.1 is used. The step-by-step design methodology is as follows.

1. Synthesis of resonator1 in Figure 3.8a: The shunt tuning inductor TL1 together with the parasitic output capacitance of stage3 forms part of resonator1. As discussed in section 3.1.1, TL1 is implemented in the TM1 metal layer (M3 ground) with a line length of 35 μm and width of 2 μm.

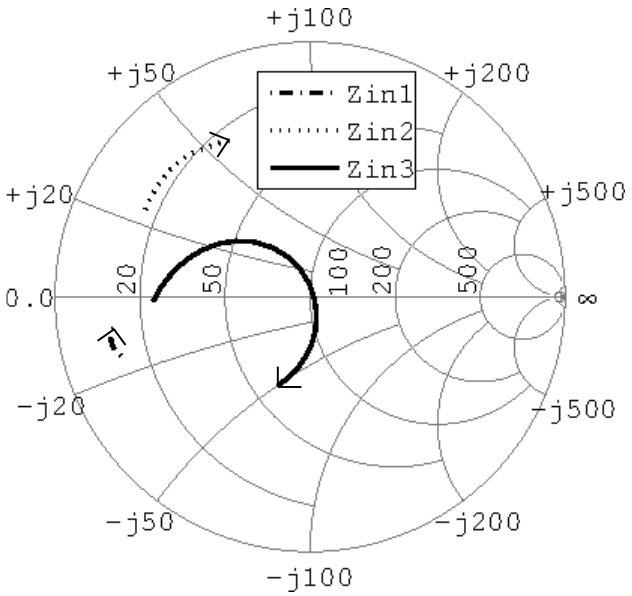
2. Synthesis of resonator2 in Figure 3.8a: To synthesize the LC tank resonator at the input of stage4, the required shunt tuning inductance is only 9 pH (18 pH differential) at 240 GHz. The accurate synthesis and modeling of such small inductances are challenging, especially since the via-inductance can contribute significantly. To circumvent this limitation, an alternative matching network consisting of the elements CL2, shunt capacitor C_{sh1} of 10 fF and series capacitor C_{s1} of 20 fF is used. The corresponding impedance transformation is shown in Figure 3.8b from 200-300 GHz. The input impedance Zin1 of stage4 is transformed to Zin2 by the inductive action of CL2. The element CL2 is a coupled microstrip-line implemented in the TM2 metal layer with w=2.5 μm and s=4 μm as discussed in 3.1.1. The capacitors C_{sh1} and C_{s1} together with the feed-line CL1 transforms Zin1 to Zin3, and this synthesizes resonator2. The optimum length of CL2 is 35 μm taking into account the effect of the feed-line CL1 (length of 55 μm). The coupled microstrip-line CL1 is added to ensure sufficient physical spacing in the layout between the stages.

3. Optimum coupling capacitor C_c: The series capacitor C_c introduces zeroes in the pass-band, and this results in bandwidth enhancement. Figure 3.9 shows the simulated small-signal gain along with the 3-dB bandwidth for different values of C_c. As C_c increases, the bandwidth and gain-ripple increases. For C_c=35 fF and 45 fF, the respective 3-dB bandwidths are 74 GHz and 86 GHz, and the corresponding gain ripples are 2 and 2.3 dB. The choice of an optimum C_c is also related to the measurement setup limitations. The prescribed lowest frequency for the WR03 source module used for on-wafer measurements is 220 GHz, but the minimum frequency can go only up to 200 GHz. For C_c greater than 15 fF, the gain of the PA at 200 GHz is still 20 dB. Based on the considerations of bandwidth, gain flatness, peak gain, group-delay variation and measurement limitations, C_c=15 fF is chosen for this design. This corresponds to a simulated 3-dB bandwidth of 40 GHz with no gain-ripple. The simulated peak differential S_{21} at 240 GHz is 25 dB. The simulated group-delay varies linearly only within 34-44 ps in the 220-260 GHz frequency range as shown in Figure 3.15.

The simulated common-mode gain is less than -15 dB from 225 GHz as shown in Figure 3.10. This helps in improving the stability since any common-mode parasitic inductance at the base node of the CB stage of the cascode topology can trigger oscillations if there is sufficient common-mode gain. At 240 GHz, the simulated P_{sat} is 8.7 dBm (including the losses due to the tuned pads and balun), the input-referred 1-dB compression point (IP_{1dB}) is -16.5 dBm and the output-referred 1-dB compression point (OP_{1dB}) is 3.7 dBm. This is discussed further in section 3.1.3. At 240 GHz, the simulated input-referred third-order intercept point (IIP3) is -6.5 dBm and the corresponding output-referred third-order intercept point (OIP3) is 15 dBm as shown in Figure 3.11.



(a)



(b)

Figure 3.8: a) Wideband interstage matching of the 240 GHz PA based on capacitor-coupled LC resonators. The series capacitor C_c couples resonator1 and resonator2. b) Impedance transformation from Zin1 (input impedance of stage4) to Zin3 (synthesis of resonator2) from 200-300 GHz.

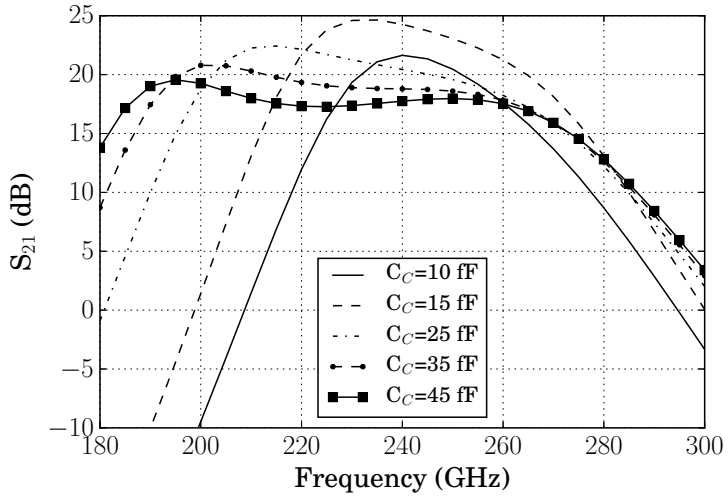


Figure 3.9: Simulated small-signal gain variation of the 240 GHz PA for different C_c. The bandwidth and gain-ripple increases with C_c. For C_c=15 fF, the simulated peak gain is 25 dB and the 3-dB bandwidth is 40 GHz.

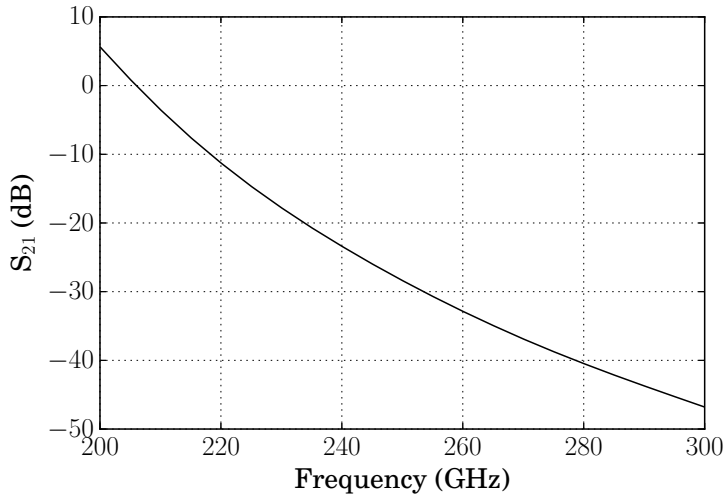


Figure 3.10: Simulated small-signal common-mode gain of the 240 GHz PA. The attenuation is higher than 15 dB above 225 GHz. This makes the design robust against parasitic common-mode oscillations.

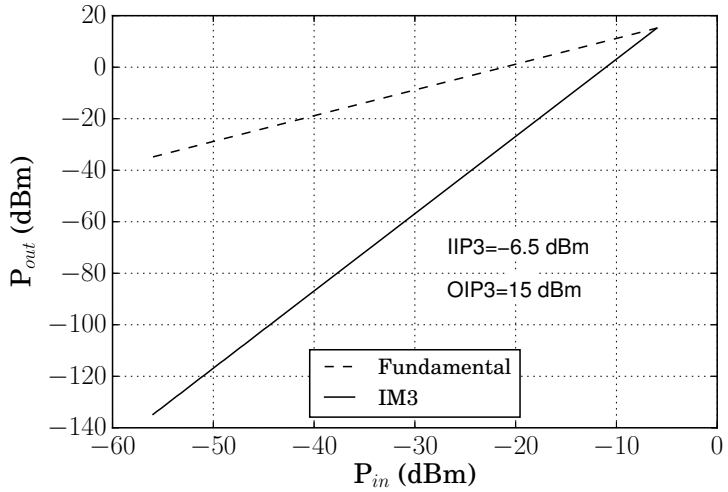


Figure 3.11: Simulated IIP3 of the 240 GHz PA. At 240 GHz, IIP3 is -6.5 dBm and OIP3 is 15 dBm.

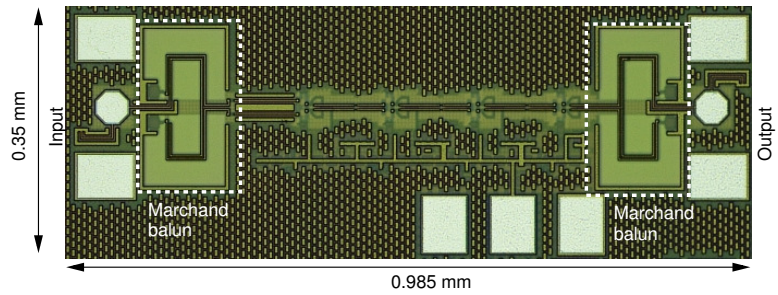


Figure 3.12: Chip-micrograph of the 240 GHz PA. The total chip area including the auxiliary Marchand-baluns and pads is 0.345 mm^2.

3.1.3 240 GHz PA characterization results

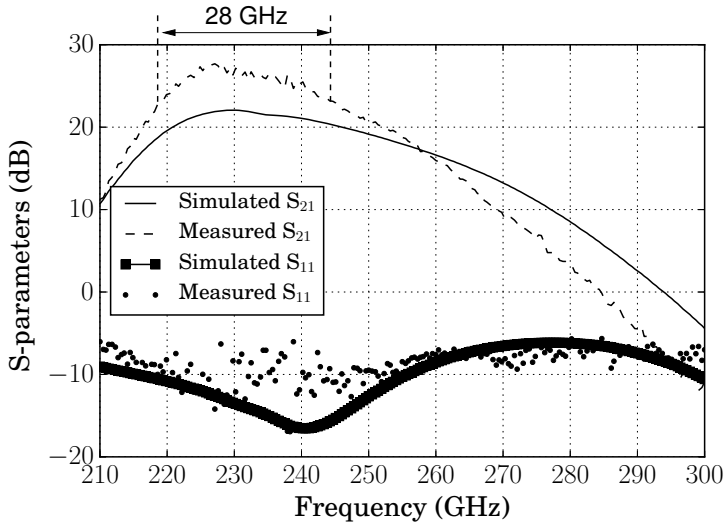
The chip-micrograph of the 240 GHz PA is shown in Figure 3.12. The chip area including the auxiliary baluns and pads is 0.345 mm^2. To facilitate single-ended on-wafer characterization, auxiliary Marchand-baluns have been added at the input and output. For on-wafer characterization, WR03 ground-signal-ground (GSG) waveguide probes are used. In this band, the probe and waveguide loss is estimated (using SOL calibration) to be 7.5 dB. By using breakout structures for TRL calibration, the loss due to the pad and balun is estimated to be 2.5 dB at 240 GHz.

3.1.3.1 240 GHz PA small-signal characterization

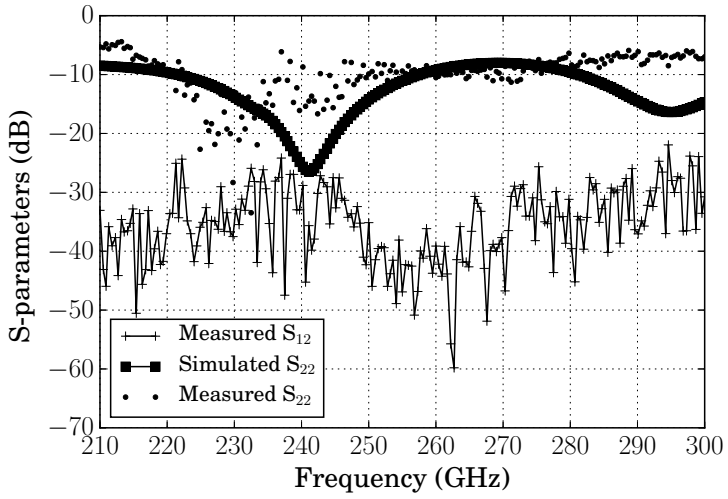
Figure 3.13 shows the hardware correlation for the small-signal s-parameter measurements. The EM simulated models of the tuned pads and the auxiliary baluns are used in this simulation. The HICUM/L2 [150] models for the HBTs are used in this simulation. At 230 GHz, the measured peak small-signal gain is 26 dB, 3-dB RF bandwidth is 28 GHz and $S_{11} \leq$ -10 dB as shown in Figure 3.13a. From 210-300 GHz, the measured reverse isolation S_{12} is less than -25 dB as shown in Figure 3.13b. The simulation results underestimate the overall measured small-signal gain by 4 dB. The average measured Edwards and Sinsky's stability-factor at the input μ and output $\mu^{'}$ is 2 from 210-300 GHz as shown in Figure 3.14a and b. Hence, the PA is unconditionally stable. The group-delay is an important metric to measure the phase distortion of amplifiers and is given by the equation 3.1 [113, 142]. Here, ϕ is the phase of S_{21} in degrees.

$$\text{group-delay} = -\frac{1}{360^{\circ}}\frac{d\Phi}{df} \tag{3.1}$$

Figure 3.15 shows the hardware correlation between the simulated and measured group-delay of the 240 GHz PA. From 220-260 GHz, the simulated group-delay varies only within 34-44 ps. The average measured group-delay matches closely with the simulation results from 230 GHz. The measured group-delay is noisy since the phase of S_{21} is very sensitive to noise in the measurement setup. The precise on-wafer calibration above 200 GHz is challenging. At 225 GHz, there is an abrupt variation in the measured group-delay which is not expected from simulations.

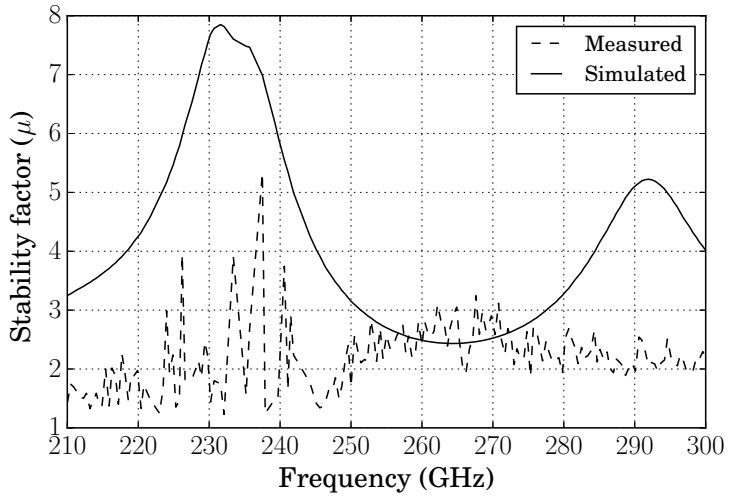


(a)

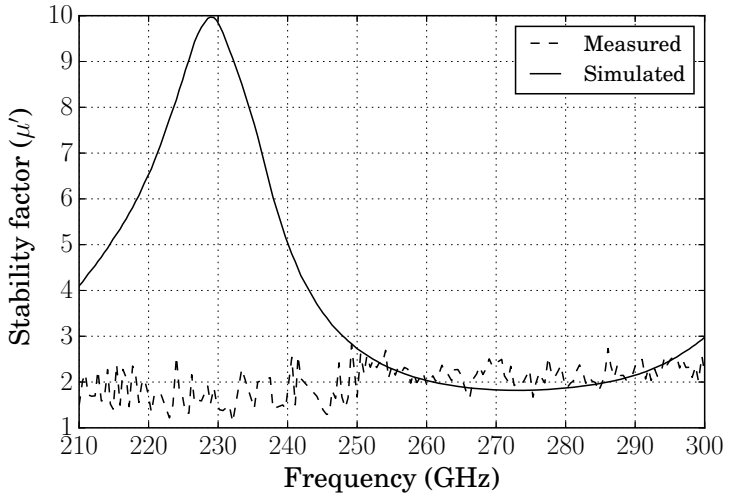


(b)

Figure 3.13: Hardware correlation for the small-signal characterization of the 240 GHz PA. a) At 230 GHz, the measured S_{21} is 26 dB and the 3-dB RF bandwidth is 28 GHz. From 215-255 GHz, the measured $S_{11} \leq$ -10 dB. b) From 210-300 GHz, the measured reverse isolation S_{12} is less than -25 dB.



(a)



(b)

Figure 3.14: Hardware correlation for the Edwards and Sinsky's stability factor μ and μ' of the 240 GHz PA. Since a) μ >1 and b) μ' >1, the PA is unconditionally stable from 210-300 GHz.

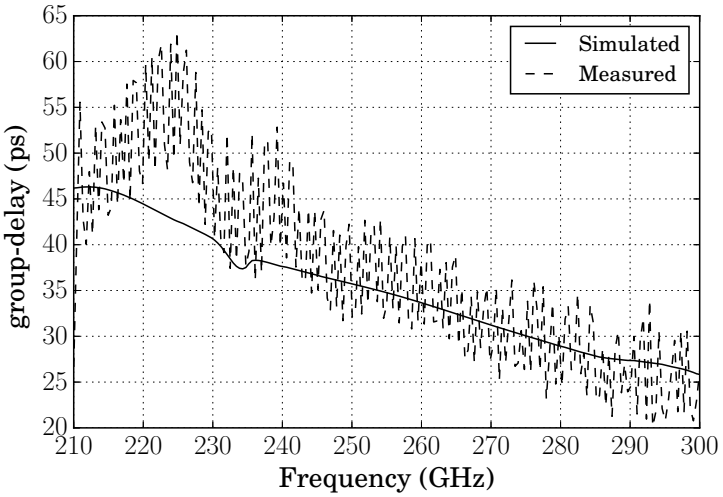


Figure 3.15: Hardware correlation for the group-delay variation of the 240 GHz PA. From 220-260 GHz, the simulated group-delay varies only within 34-44 ps. The average measured group-delay matches closely with simulation results from 230 GHz.

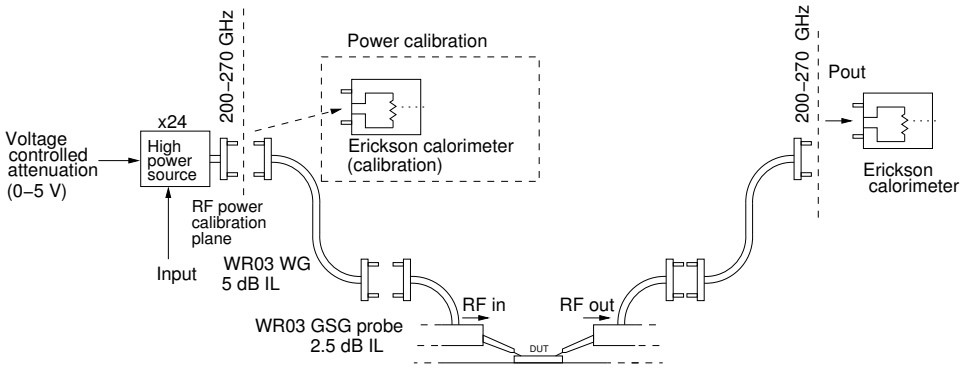
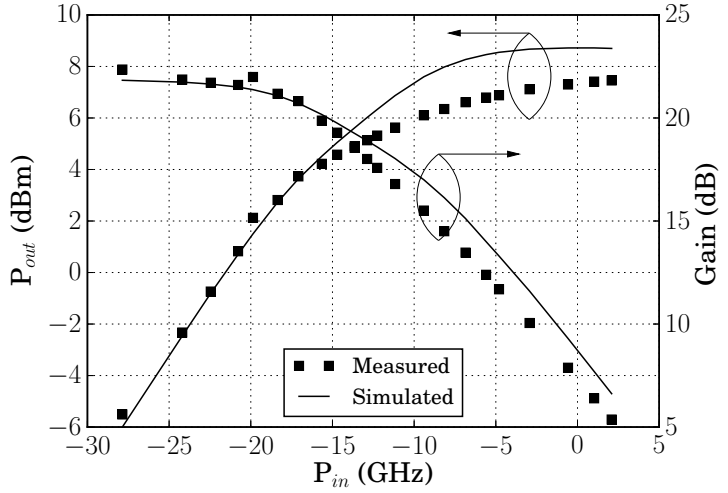


Figure 3.16: Measurement setup for the large-signal bandwidth and linearity characterization of the 240 GHz PA. An external WR03 wideband high power source capable of delivering up to 6 mW at 240 GHz is used at the input.

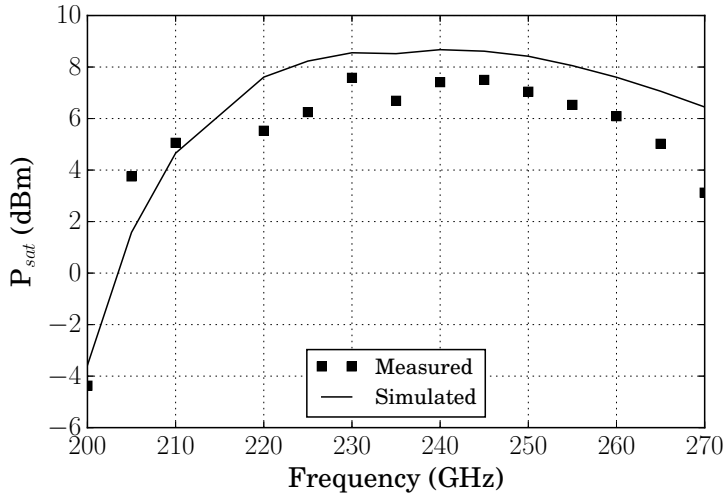
3.1.3.2 240 GHz PA large-signal characterization

The measurement setup for the on-wafer large-signal bandwidth and linearity characterization of the 240 GHz PA is shown in Figure 3.16. An external wideband high-power source operating in the WR03 waveguide band capable of delivering up to 6 mW at 240 GHz is used at the input. The output power from the source is calibrated using an Erickson calorimeter. For linearity measurements, the output power from the high-power source is varied using an external dc-voltage (0-5 V). The variation in output power from the high-power source with the voltage is not linear. For output power below -20 dBm, the change in output power with dc-voltage is considerable, and it is sensitive to the noise in the dc-power supply. This introduces 2-2.5 dB uncertainty in the measurements at low power levels.

The results from the hardware correlation for the large-signal characterization of the 240 GHz PA is shown in Figure 3.17a. The EM simulated models of the tuned pads and auxiliary baluns are used in this simulation, and HICUM/L2 [150] models for the HBTs are used. At 240 GHz, the measured P_{sat} is 7.5 dBm and the simulation overestimates the measurement results by 1.2 dB. The measured gain at compression is 12.5 dB at 240 GHz. The measured and simulated IP_{1dB} is -16.5 dBm and OP_{1dB} is 3.7 dBm. Hence, the estimated IIP3 is -6.5 dBm since IIP3 ~ IP_{1dB} + 10 dB [149, 151]. This is close to the simulation results in Figure 3.11. Figure 3.17b shows the hardware correlation for the variation of P_{sat} with frequency. The measured $P_{sat} \geq 6$ dBm from 225-260 GHz. Figure 3.18 shows the hardware correlation for the PAE of the 240 GHz PA. The measured peak PAE at 240 GHz is 1%, which is 0.5% less than expected from simulations. Table 3.1 summarizes the key results from the small-signal and large-signal characterization of the 240 GHz PA.



(a)



(b)

Figure 3.17: Hardware correlation for the large-signal characterization of the 240 GHz PA. a) Linearity: The measured P_{sat} is 7.5 dBm, IP_{1dB} is -16.5 dBm and OP_{1dB} is 3.7 dBm at 240 GHz. b) P_{sat} versus frequency: From 225-260 GHz, the measured $P_{sat} \geq 6$ dBm.

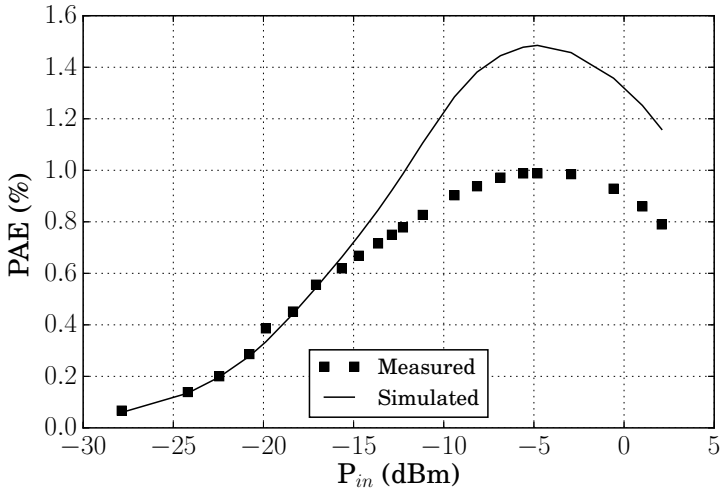


Figure 3.18: Hardware correlation for the PAE measurements of the 240 GHz PA. At 240 GHz, the peak PAE is 1% which is 0.5% less than simulation results.

Table 3.1: Summary of the simulation and measurement results of the 240 GHz PA

	Small-signal BW (GHz)	Peak small-signal gain (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	peak PAE (%)
Simulated (differential)	40	25	10.2@240		
Simulated (with balun)	35	22	8.7@240	3.7	1.5
Measured	28	26	7.5@240	3.7	1.0

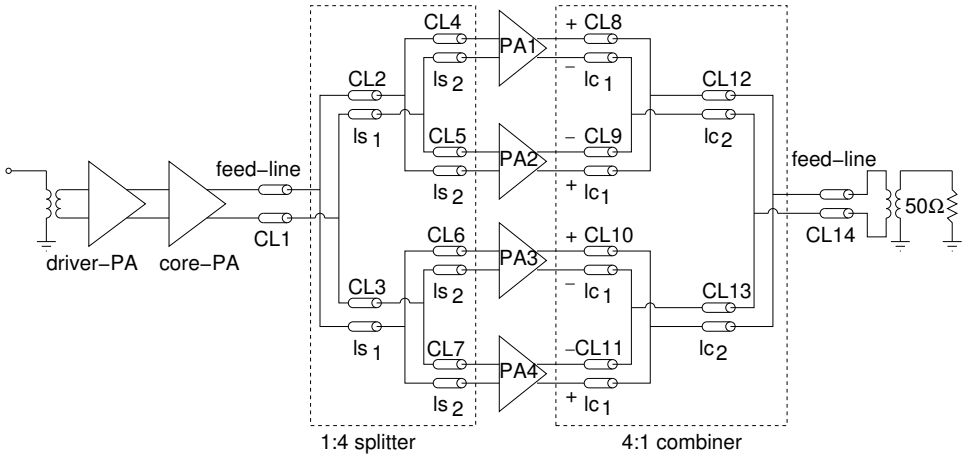


Figure 3.19: Block diagram of the 200-225 GHz combiner-PA [146]. The output power from the core-PA is split using a 1:4 power-splitter (CL2-CL7). A 4:1 coupled microstrip-line based ZDC (CL8-CL13) combines the output from the unit PAs (PA1-PA4).

3.2 200-225 GHz 4:1 combiner Power Amplifier

In this section, the design of a combiner-PA operating from 200-225 GHz is presented. As motivated in section 2.4, a microstrip-line based ZDC for parallel power combination is used in this design. Figure 3.19 shows the block diagram of the combiner-PA. The driver-PA which is reported in [152] consists of four identical stages based on the pseudo-differential cascode topology similar to the 240 GHz PA in section 3.1. For the driver-PA, transistors with an emitter area of $0.22\times5\ \mu m^2$ are used. For gain enhancement, inductive gain peaking at the base of the CB stage of the cascode amplifier is used. At 212 GHz, the measured S_{21} for the driver-PA is 19.5 dB and the 3-dB bandwidth is 21 GHz. The succeeding core-PA is optimized for high output power, and it consists of four cascaded pseudo-differential cascode stages. For the core-PA, transistors with an emitter area of $0.22\times10\ \mu m^2$ are used. For this PA, the simulated P_{sat} at 215 GHz is 6 dBm (100 Ω differential load impedance). The measured peak S_{21} of the core-PA is 8 dB at 215 GHz. A 1:4 power-splitter consisting of the coupled microstrip-lines CL2-CL7 splits the output power from the core-PA. At the output, a 4:1 power-combiner consisting of the coupled microstrip-lines CL8-CL13 combines the output power from PA1-PA4. The amplifiers PA1-PA4 are identical to the core-PA. The coupled microstrip-lines are used for the implementation of the combiner due to the ease of interfacing with differential PAs. Moreover, the coupled microstrip-lines give an additional degree of freedom of selecting the Z_{even} independent of Z_{odd}. By selecting a lower Z_{even} and using an appropriate line dimension, the transformed common-mode load impedance at the outputs of the PA can be made significantly smaller. This results in little or no common mode gain and makes the system

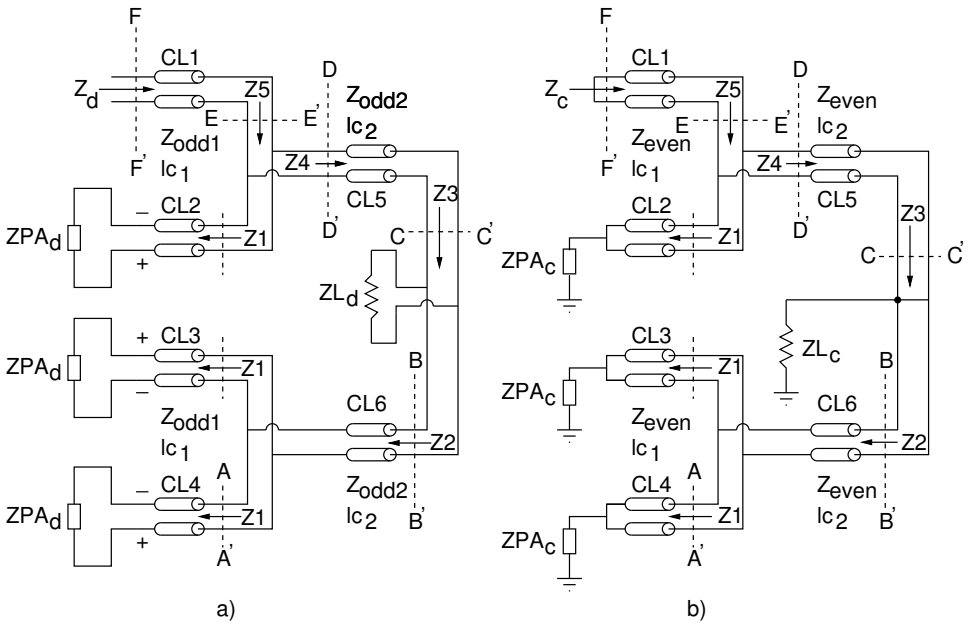


Figure 3.20: Impedance transformation at the 4:1 power-combiner input taking into account the loading effect of the unit PAs. a) The differential input impedance is Z_d. b) The common-mode input impedance is Z_c. Here, ZPA_d and ZPA_c are the respective large-signal differential and common-mode output impedances of the unit PAs.

robust against parasitic oscillations in common mode. This is particularly important as the parasitic inductance at the base of the CB stage can result in instability, if there is sufficient common-mode gain. At the input and output, auxiliary Marchand-baluns have been added for single-ended on-wafer measurements.

3.2.1 Coupled microstrip-line based ZDC for 4:1 power combination

For the coupled microstrip-line based ZDC shown in Figure 3.19, the design variables are the line impedances Z_{odd} and Z_{even}, and line lengths lc_1 and lc_2. At each of the combiner inputs, the effective differential input impedance Z_d and common-mode impedance Z_c include the effect of the transformed load impedance ZL. This also includes the loading effect of the other PAs as shown in Figure 3.20. At each of the combiner inputs, Z_d can be expressed by the equation 3.7, which follows from equations 3.2 to 3.6 [142]. Here, Z_{odd1}, Z_{odd2} are the odd-mode characteristic impedances of the coupled line sections with lengths lc_1 and lc_2 respectively, ZPA_d is the large-signal differential mode output impedance of PA1-PA4, Z1-Z5 are the respective impedances looking into the planes A-A$'$ to E-E$'$ in Figure 3.20, ZL_d is 100 Ω, α is the line attenuation per unit length, and β is the propagation constant. The Z_c at the combiner inputs can be calculated similarly by replacing Z_{odd} with Z_{even}, ZPA_d with ZPA_c

(common mode large-signal output impedance of PA1-PA4) and ZL_d (100 Ω) with ZL_c (50 Ω) in these equations.

$$Z1 = Z_{odd1}\frac{ZPA_d + jZ_{odd1}\tan[(\alpha+j\beta)lc_1]}{Z_{odd1} + jZPA_d\tan[(\alpha+j\beta)lc_1]} \tag{3.2}$$

$$Z2 = Z_{odd2}\frac{(Z1/2) + jZ_{odd2}\tan[(\alpha+j\beta)lc_2]}{Z_{odd2} + j(Z1/2)\tan[(\alpha+j\beta)lc_2]} \tag{3.3}$$

$$Z3 = \frac{Z2 \times ZL_d}{Z2 + ZL_d} \tag{3.4}$$

$$Z4 = Z_{odd2}\frac{Z3 + jZ_{odd2}\tan[(\alpha+j\beta)lc_2]}{Z_{odd2} + jZ3\tan[(\alpha+j\beta)lc_2]} \tag{3.5}$$

$$Z5 = \frac{Z4 \times Z1}{Z4 + Z1} \tag{3.6}$$

$$Z_d = Z_{odd1}\frac{Z5 + jZ_{odd1}\tan[(\alpha+j\beta)lc_1]}{Z_{odd1} + jZ5\tan[(\alpha+j\beta)lc_1]} \tag{3.7}$$

The impedance Z_d from the equation 3.7 has multiple solutions. It is very time consuming to solve this equation analytically. A complex frequency dependent ZPA_d makes it even more complicated. A computationally intensive brute-force method of goal minimization provides little insight. Also, it is a time-consuming approach as multiple iterations with EM simulations are required to verify the results. Hence, boundary conditions need to be imposed to minimize the solution search space. The typical boundary conditions are the maximum and minimum synthesizable Z_{odd} and Z_{even}, and minimum line lengths due to the pitch of the unit PAs.

The design goal is wideband power combination with the minimum possible line dimensions. The line dimensions of the power-combiner should be chosen so that it presents a differential impedance of 100 Ω and a very low common-mode impedance at the output of the unit PAs. In the first iteration, scalable models for the coupled microstrip lines are used, and the line parameters are extracted from full EM simulation. In the final step, a full EM simulation of the 4:1 power-combiner is used to accurately model all the parasitic effects. The step-by-step design methodology for the 4:1 power-combiner is summarized in the next section.

3.2.1.1 Optimization of the ZDC for efficient power combination

1. Synthesis of the optimum line impedances: To simplify the design process, the line impedances of the different sections of the combiner are assumed to be identical (Z_{odd} for the odd-mode and Z_{even} for the even-mode). In general, a high Z_{odd} result in smaller line lengths. For coupled microstrip-lines, a high Z_{odd} can be synthesized by increasing the trace-separation s. However, the maximum Z_{odd} saturates beyond a certain s. For this design, the coupled microstrip-lines were implemented in the low-loss topmost metal layer M6 of the BEOL. Figure 3.21 shows the variation in Z_{odd} with s for widths of 2.4 μm and 4.8 μm. As s increases from 2.4 μm (minimum for this process technology) to 12 μm, Z_{odd} increases from 67 to 120 Ω for w=2.4 μm, and it varies from 59-100 Ω for w=4.8 μm. A higher Z_{odd} can be realized for a given s for narrower lines (due to lesser fringe capacitance), and is hence preferable. Another goal is to minimize Z_{even}, which can be achieved by reducing the distance of the trace to the ground plane. For this design, the ground plane is implemented in the M3 metal layer of the BEOL based on dc routing and other layout constraints. This corresponds to a distance of 4.63 μm from the ground plane. For w=2.4 μm, the maximum Z_{odd} of 120 Ω corresponds to s of 12 μm, which is almost 2.6 times the distance of the trace in the M6 metal layer from the ground plane in the M3 metal layer. Also, the increase in Z_{odd} for s greater than 7 μm is very gradual. Hence, for this design s=7 μm is chosen. For w=2.4 μm, the simulated Z_{odd} is 105 Ω and Z_{even} is 38 Ω. The simulated attenuation for the odd-mode is 1300 dB/m, and for the even-mode it is 1100 dB/m.

2. Optimum line lengths: The insertion loss can be minimized by keeping the line lengths smaller, and also it results in a wideband performance. If the line length is such that $\beta l \leq \pi/6$ then $\tan(\beta l) \approx \beta l$, and the change of the impedance with frequency is gradual. However, the pitch between the unit PAs (PA1-PA4 in Figure 3.19) in the layout limit the minimum lc_2 and lc_1 to 50 μm and 25 μm respectively. Figure 3.22 shows the simulated Z_d of the power-combiner from 200-240 GHz for three different line dimensions. For lc_1=100 μm and lc_2=200 μm, Z_d is closer to the required 100 Ω only over a narrow frequency range due to the larger line dimensions. For lc_1=lc_2=70 μm, the real part of Z_d is closer to 100 Ω over a relatively much wider bandwidth, and it has a significant reactive part. For lc_1=35 μm and lc_2=65 μm, Z_d varies from 54+j$\times$63 Ω to 83.5+j$\times$35 Ω from 200-240 GHz. By using lc_1=35 μm and lc_2=65 μm, P_{sat} from the unit PAs at 215 GHz decreases from 6 dBm (100 Ω differential load impedance) to only 4.8 dBm (decrease of 1.2 dB). Also, this line dimension also results in the least Z_c as shown in Figure 3.23. Hence, the optimum line dimensions are lc_1=35 μm and lc_2=65 μm.

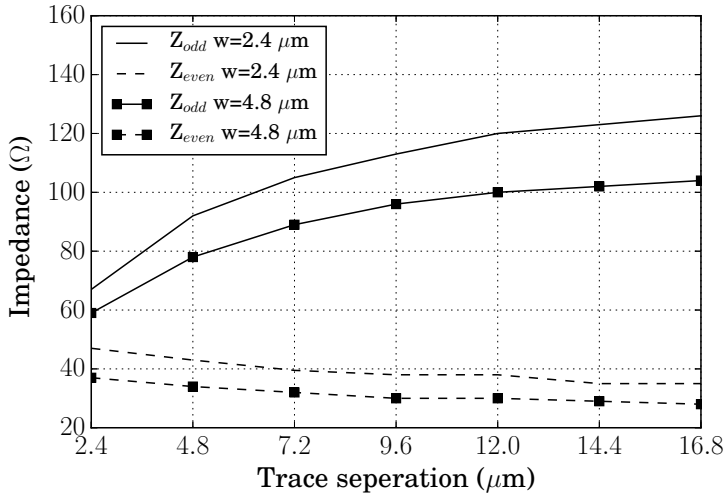


Figure 3.21: Simulated Z_{odd} and Z_{even} versus trace-separation s for coupled microstrip-lines on the M6 metal layer of the BEOL. For this design, s=7 μm is optimum. For w=2.4 μm, this corresponds to a Z_{odd} of 105 Ω and Z_{even} of 38 Ω.

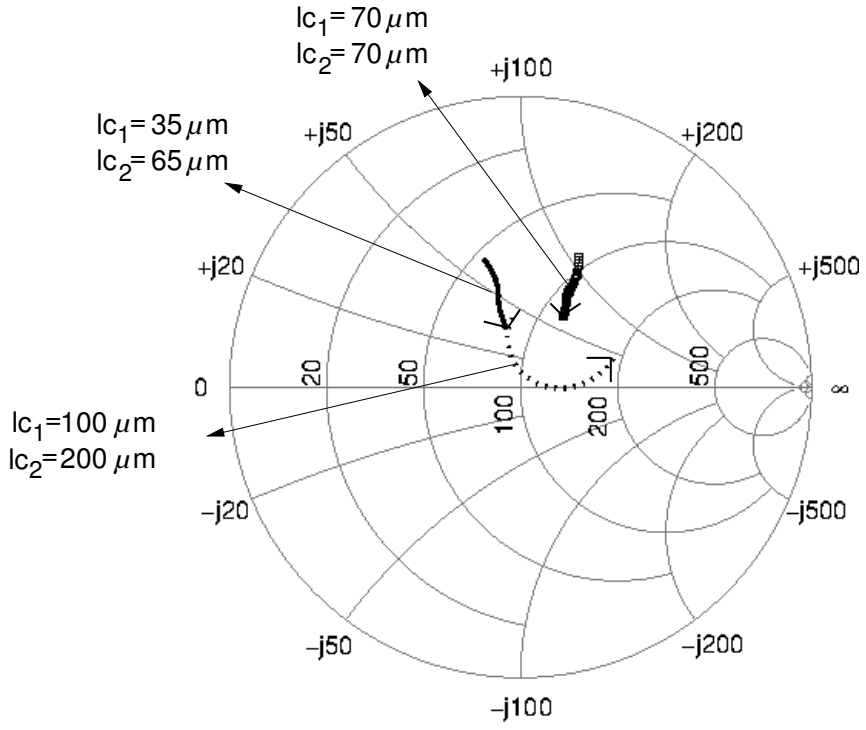


Figure 3.22: Simulated Z_d at the 4:1 power-combiner input from 200-240 GHz for three line dimensions: a) lc_1=35 μm, lc_2=65 μm. b) lc_1=lc_2=70 μm. c) lc_1=100 μm, lc_2=200 μm.

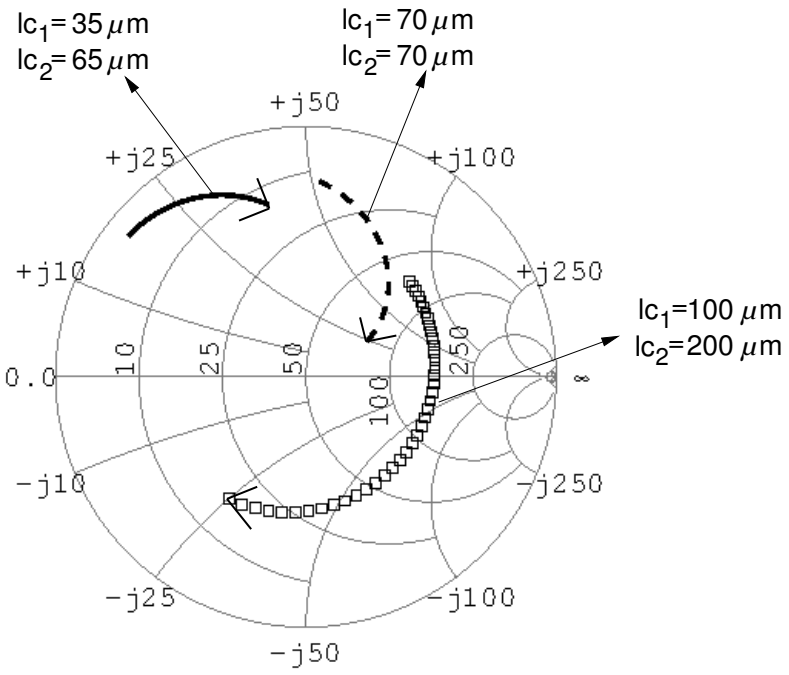


Figure 3.23: Simulated Z_c at the 4:1 power-combiner input from 200-240 GHz for three line dimensions: a) lc_1=35 μm, lc_2=65 μm. b) lc_1=lc_2=70 μm. c) lc_1=100 μm, lc_2=200 μm.

For the 1:4 power-splitter, the optimum line dimensions are $ls_1 = 180$ μm and $ls_2 = 50$ μm (to transform the input 100 Ω differential impedance of PA1-PA4 to 100 Ω at the input of the power-splitter). Figure 3.24 shows the full-EM simulation model for the 1:4 power-splitter and 4:1 power-combiner. At the input and output, wave-ports are defined (not shown here) for accurate EM simulation. In the simulation, the underpass in the M5 metal layer for routing and connecting the different combiner segments along with the via connections are also included. From 200-240 GHz, the simulated excess loss of the power-splitter is in the 1.8-1.9 dB range, and for the 4:1 power-combiner it is in the 0.8-1.1 dB range as shown in Figure 3.27. From 200-240 GHz, the simulated common-mode gain is less than -30 dB. The simulated P_{sat} for the combiner-PA varies from 9.8 to 10.8 dBm from 200-225 GHz as shown in Figure 3.28, and is discussed further in section 3.2.2.

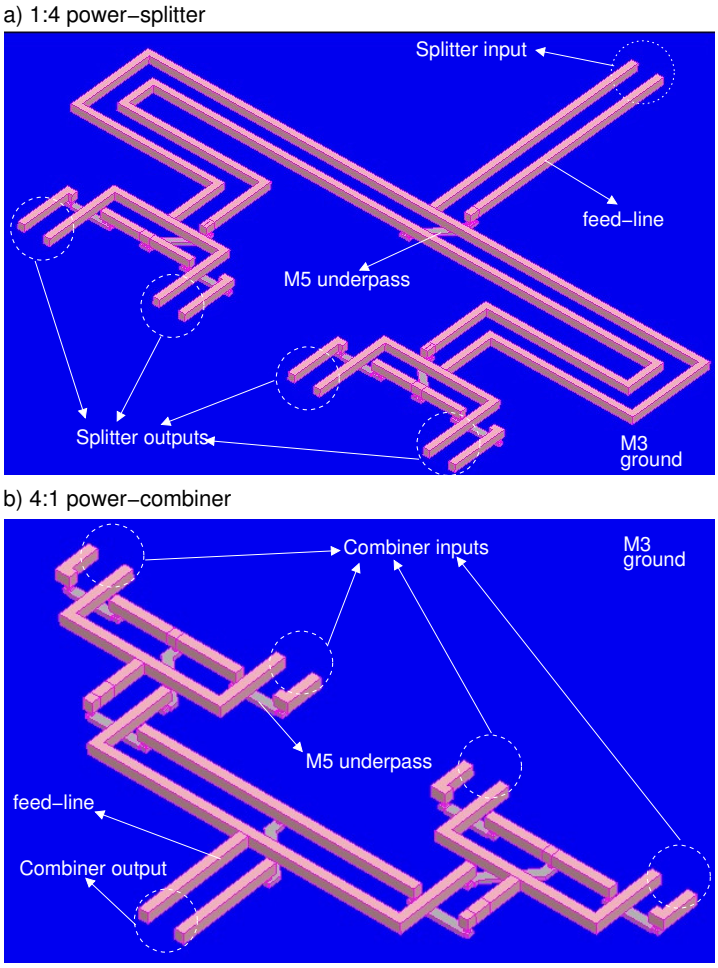


Figure 3.24: 3D-model for full EM simulation of a) 1:4 power-splitter, and b) 4:1 power-combiner in HFSS. At the input and output, wave-ports are defined (not shown here) for higher accuracy.

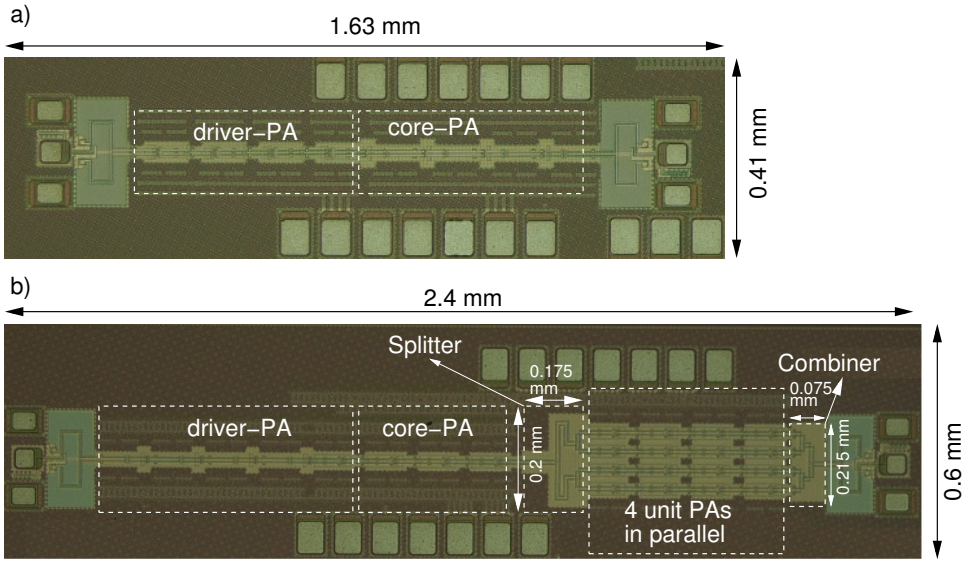


Figure 3.25: Chip-micrograph of the 200-225 GHz a) breakout-PA: The chip area is 0.67 mm^2, and b) combiner-PA: The chip area is 1.44 mm^2. The unit PAs are identical to the core-PA.

3.2.2 Measurement results for the 200-225 GHz combiner-PA

The chip-micrographs for the 200-225 GHz breakout-PA and combiner-PA are shown in Figure 3.25a and b respectively. The chip area of the 200-225 GHz breakout-PA, which consists of the driver-PA and core-PA, is 0.67 mm^2. This breakout circuit is used to measure the P_{sat} of the core-PA. The chip area of the combiner-PA is 1.44 mm^2, and it consists of the driver-PA, core-PA, 1:4 power-splitter, four PA cells in parallel and 4:1 power-combiner. To facilitate single-ended on-wafer measurements, auxiliary Marchand-baluns have been added at the input and output. For on-wafer characterization, WR03 GSG waveguide probes are used as discussed in section 3.1. To estimate the insertion loss due to the power-combiner and power-splitter separately, additional breakout structures were implemented as shown in Figure 3.26. Figure 3.27 shows the hardware correlation for the insertion loss of the splitter and combiner. For EM simulations, the 3D-model shown in Figure 3.24 is used. The measured insertion loss is in the 1-2 dB range from 200-240 GHz.

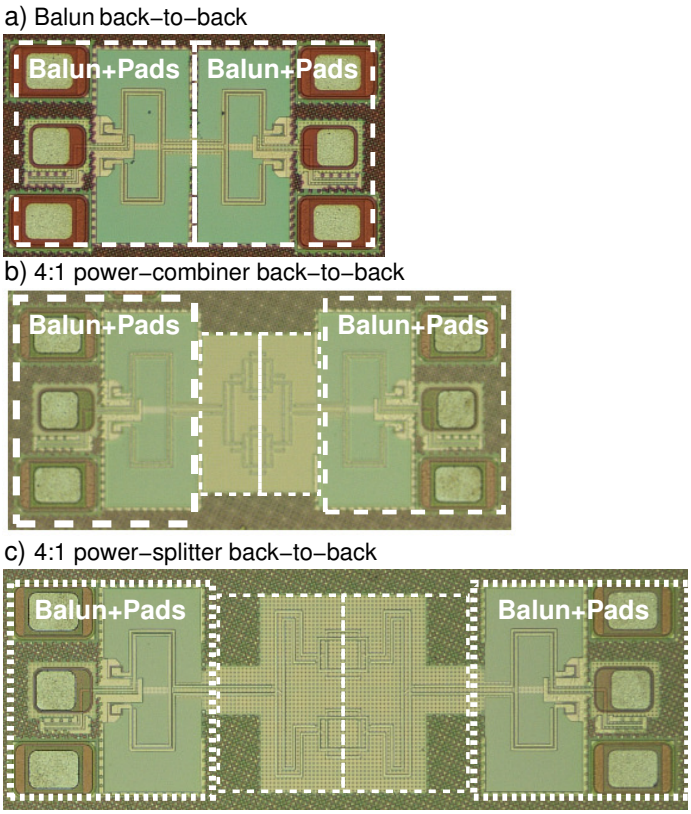


Figure 3.26: Chip-micrograph of the additional breakout structures for estimating the insertion loss of the 1:4 power-splitter and 4:1 power-combiner. a) Back-to-back Marchand-baluns. b) Back-to-back 4:1 power-combiner with Marchand-baluns. c) Back-to-back 1:4 power-splitter with Marchand-baluns.

For large-signal characterization of the 200-225 GHz combiner-PA, the measurement setup shown in Figure 3.16 is used. The hardware correlation for the large-signal bandwidth characterization of the 200-225 GHz combiner-PA and the breakout-PA is shown in Figure 3.28. At 215 GHz, the peak P_{sat} for the combiner-PA is 9.6 dBm and the 3-dB large-signal bandwidth is 34 GHz (200-234 GHz). From 200-225 GHz, the combiner-PA enhances the overall output power from the unit PA cells by 3.5-4.5 dB. In simulations, EM simulated models of the balun and tuned pads are included, and HICUM/L2 [150] model for the HBTs are used. The hardware correlation for the linearity characterization of the combiner-PA at 215 GHz is shown in Figure 3.29. The measured IP_{1dB} for the combiner-PA is -19 dBm and OP_{1dB} is 5.5 dBm. At 215 GHz, the peak measured PAE is 0.5%. The hardware correlation for the small-signal bandwidth characterization of the combiner-PA is shown in Figure 3.30. At 213 GHz, the peak gain is 25 dB and small-signal 3-dB bandwidth is 20 GHz. The simulation results overestimate the overall measured S_{21} by 4 dB. The measured $S_{11} \leq$ -10 dB and $S_{12} \leq$ -30 dB from 200-240 GHz as shown in Figure 3.31.

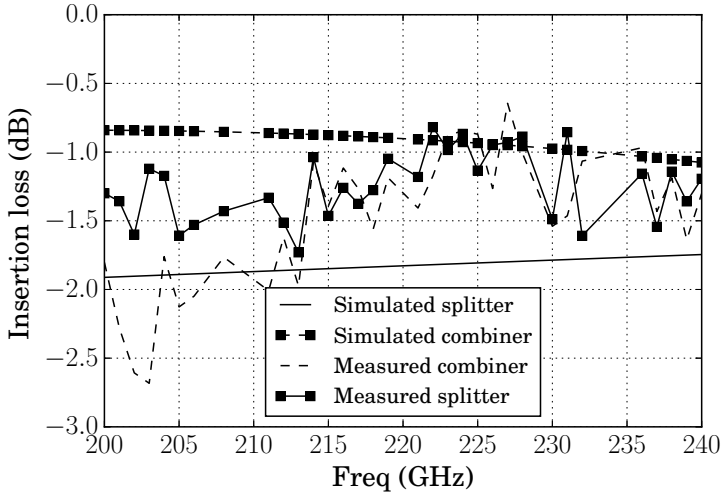


Figure 3.27: Hardware correlation for the insertion-loss of the 1:4 power-splitter and 4:1 power-combiner. From 200-240 GHz, the measured insertion loss is in the 1-2 dB range.

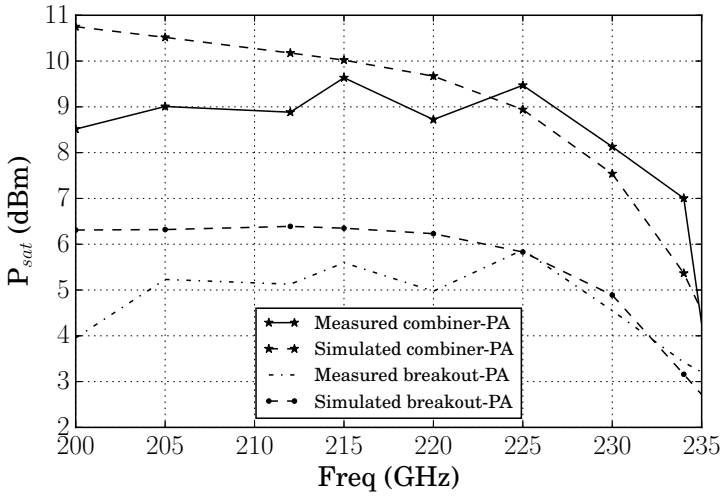


Figure 3.28: Hardware correlation for the large-signal bandwidth characterization of the 200-225 GHz combiner-PA and breakout-PA. The peak P_{sat} for the combiner-PA is 9.6 dBm at 215 GHz, and the 3-dB large-signal bandwidth is 34 GHz (200-234 GHz).

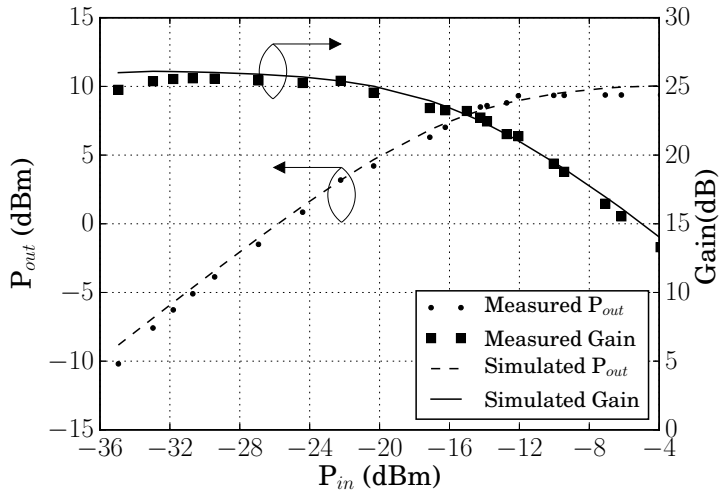


Figure 3.29: Hardware correlation for the linearity characterization of the 200-225 GHz combiner-PA at 215 GHz. The measured P_{sat} is 9.6 dBm, IP_{1dB} is -19 dBm and OP_{1dB} is 5.5 dBm.

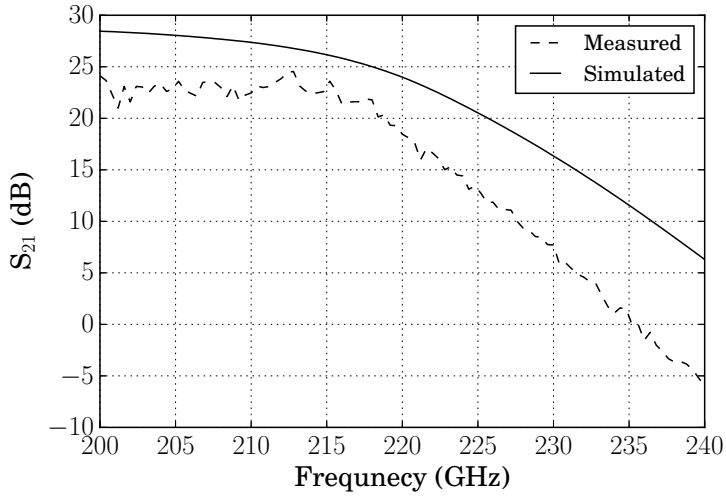


Figure 3.30: Hardware correlation for small-signal bandwidth characterization of the 200-225 GHz combiner-PA. At 213 GHz, the peak gain is 25 dB and the small-signal 3-dB bandwidth is 20 GHz.

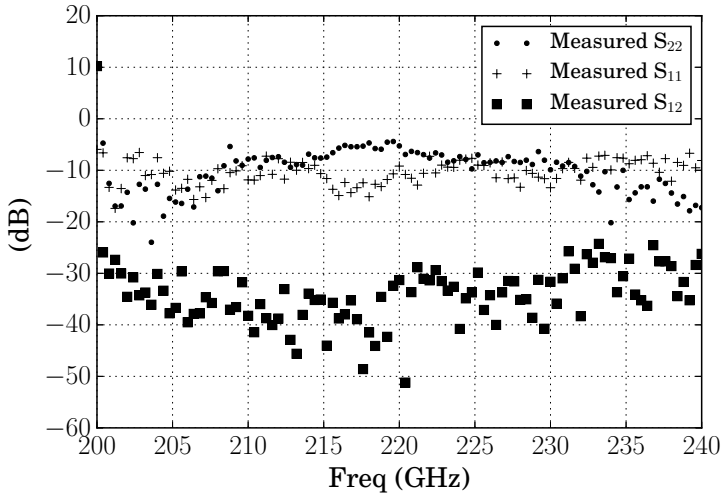


Figure 3.31: From 200-240 GHz, the measured $S_{11} \leq$ -10 dB and $S_{12} \leq$ -30 dB for the 200-225 GHz combiner-PA.

Table 3.2 summarizes and compares the results of PAs presented in this thesis with PAs and amplifiers above 200 GHz reported in the literature. The PAs reported in this thesis have the highest P_{sat} (with and without power combination), gain, and the best FoM among all the silicon PAs reported in the literature above 200 GHz. The results of the PAs reported in this thesis are conservative numbers, and have not been corrected for the balun and pad losses of 2-2.5 dB each at the input and output. These results are comparable to III-V technologies, which have the advantage of much higher f_{max} in comparison to silicon technologies. The frequency of operation in [153, 154] is less than $f_{max}/3$ while in this thesis work the frequency of operation is close to $f_{max}/2$, and yet the results are comparable. This work strongly affirms the position of silicon technologies (which have the advantage of much higher integration density) as a viable low-cost alternative to III-V technologies towards sub-mmWave frequencies.

Table 3.2: PAs/amplifiers above 200 GHz reported in the literature

Ref	Tech	f_T/f_{max}	Freq (GHz)	Max gain (dB)	3-dB BW[2] (GHz)	P_{sat} (dBm)	OP $_{1dB}$ (dBm)	peak PAE (%)	FoM[1]
Section 3.1	130-nm SiGe BiCMOS	350/550	219-247	26	28	7.5*	4	1	1289
Section 3.2	130-nm SiGe BiCMOS	250/370	200-225	25	20	9.6$^+$	5.5	0.5	666
[155]	130-nm SiGe	200/450	200	17	44	-	-3.5	-	-
[152]	130-nm SiGe	250/360 300/450	212 233	19.5 22.5	21 10	- -	- -	- -	- -
[156]	130-nm SiGe BiCMOS	300/500	245	18	8	-	-	-	
[157]	130-nm SiGe BiCMOS	350/550	275	10	7	-	-10	-	-
[158]	65-nm CMOS	200/350	200	8.1	-	-10	-	0.09	2.32
[6]	32-nm SOI CMOS	250/320	210	15	-	4.6	2.7	6	241
[159]	28-nm FDSOI CMOS	-/420	325	4.5	-	-	-	-	-
[30]	65-nm CMOS	200/350	265	9.2	12.2	-3.9	-	1.35	3.21
Comparison with III-V technology									
[153] [154]	InP-HEMT InP- HEMT	500/1200 -	334-344 240-270	15 16.5	10 30	10 7.8	- -	- 4	- 728
[160]	mHEMT	-/750	220-320	13.5	100	-	-	-	-
[161, 162]	InP-HEMT	400/800	205-225	18	20	18.7[3]	-	4	8250
[25]	InP-HEMT	610/1500	1000	9	90	-	-	-	-
[163]	InAlAs/InGaAs mHEMT	515/>1000	610	20.3	59	-	-	-	-

[1] Calculated from ITRS FoM [129] *Measured at the output pad at 240 GHz.

$^+$4:1 coupled microstrip-line based power-combiners. Measured at the output pad at 215 GHz.

[2] small-signal bandwidth.[3]8:1 power combination.

3.3 240 GHz wideband LO signal source

In this section, the design of a wideband frequency multiplier-based LO signal source at 240 GHz is presented. It is used to drive the mixers in the 240 GHz quadrature Tx and Rx chipset presented in Chapter 4. This source can also be used as a tunable standalone high-power source. Figure 3.32 shows the top-level block diagram of this source. It consists of an active balun at the input followed by four cascaded frequency doubler stages (D1-D4), and a three-stage PA. The PA used here is identical to the one presented in section 3.1 except for three stages in total instead of four. The individual frequency doubler stages are based on the Gilbert-cell topology for in-phase multiplication as motivated in section 2.1.3. For the up-conversion mixer, the optimum LO power is greater than 5 dBm at 240 GHz as discussed later in section 3.4.1. Hence, the design goal is an overall output power of at least 5 dBm over a 3-dB RF bandwidth of at least 40 GHz. Another important design goal is to reduce the external LO drive power requirements at the input of the 240 GHz LO signal source. This reduces the parasitic harmonic generation from the first frequency doubler stage and relaxes the output power requirement from the external frequency synthesizer. The $\times 16$ frequency multiplier core is optimized to generate enough power (-5 dBm and higher) to saturate the succeeding 240 GHz PA without any intermediate drive amplifiers (between the doubler stages). This also reduces the overall dc-power consumption. The active balun used in this design is based on a standard differential circuit topology with one of its inputs ac-shorted for single-ended to differential conversion [164], and a detail discussion of this circuit is skipped in this section.

3.3.1 Impact of the LO spurious harmonics on the system performance

The spectral purity of the LO signal source is important. At the system level, the implication of the spurious harmonics can be explained by considering a scenario where a multi-tone LO is used at the Tx and Rx side. On mixing with the spurious harmonics from the LO chain, the up-converted signal is $s_{TX}(t) = m(t) \times [a_1 \cos(15\omega_{LO}t) + \cos(16\omega_{LO}t) + a_2 \cos(17\omega_{LO}t)]$. Here, $m(t)$ is the input IF signal and $\cos\omega_{LO}t$ is the external input signal to the $\times 16$ frequency multiplier-based LO signal source. For simplicity, only the 15^{th} and 17^{th} harmonics are considered here, and a_1, a_2 are the normalized amplitudes relative to the desired 16^{th} harmonic. Assuming coherent detection at the Rx and neglecting the high-frequency components at $30 \times \omega_{LO}$, $31 \times \omega_{LO}$ and $32 \times \omega_{LO}$, the down-converted IF signal $s_{IF}(t)$ is given by the equation 3.8. The effect of the spurious LO harmonics (15^{th} and 17^{th} in this case) results in the IF signal $m(t)$ also getting modulated around ω_{LO} and $2 \times \omega_{LO}$. This is not desirable and limits the maximum bandwidth of $m(t)$ as shown in Figure 3.33. This puts an upper limit on the maximum data-rate for communication systems. In the case of FMCW RADAR, a multi-tone

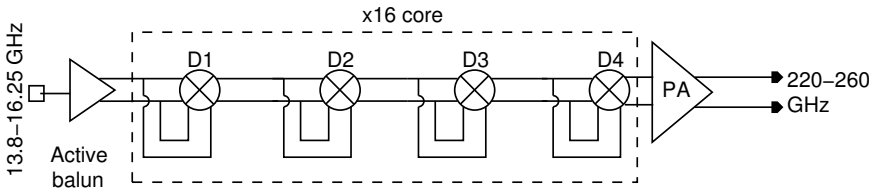


Figure 3.32: Top-level block diagram of the 240 GHz frequency multiplier-based LO signal source [7, 88]. It consists of an active balun, followed by four cascaded frequency doubler stages (D1-D4) and a three-stage 240 GHz PA.

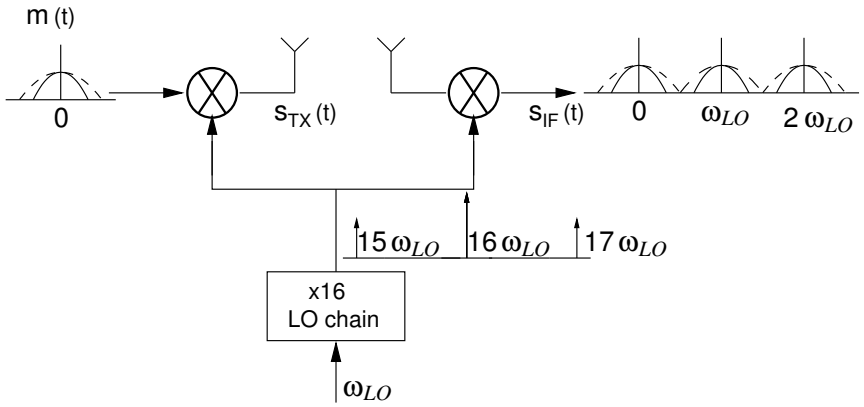


Figure 3.33: Effect of spurious LO harmonics on the down-converted IF signal for coherent detection. For this illustration, only the spurious 15^{th} and 17^{th} harmonics were considered to simplify the analysis.

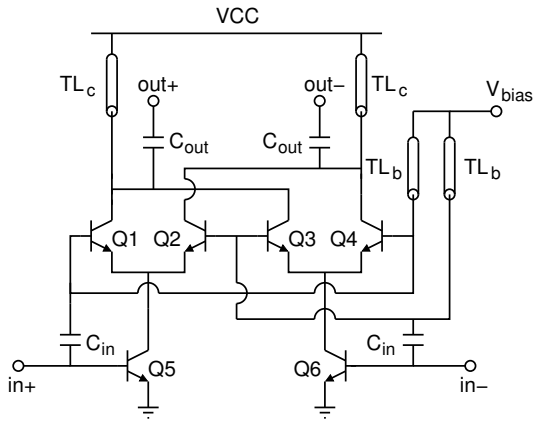
LO results in multiple IF frequencies which create ambiguity in the range estimation.

$$s_{IF}(t) = m(t)(1+\frac{a_1^2+a_2^2}{2}) + m(t)(a_1+\frac{a_2}{2})(\cos\omega_{LO}t) + m(t)a_1a_2\cos 2\omega_{LO}t \tag{3.8}$$

If the amplitudes of a_1, a_2 are small and order of magnitudes lower than the desired 16^{th} harmonic, then the power from the spurious harmonics is not sufficient to pump the mixers in the Tx and Rx. This makes their impact at the output negligible.

3.3.2 Circuit design considerations for wideband LO

Figure 3.34 shows the circuit schematic of the unit frequency doubler stage. The transistors Q1-Q4 are part of the switching quad, and the transistors Q5-Q6 are part of the transconductance stage. The tuning inductances TL_c and TL_b are implemented as shielded microstrip-lines [114] in the TM2 metal layer with lengths l_c and l_b respectively. The electric field in the case of shielded lines is confined within the ground shield, which reduces the unwanted parasitic coupling between the different part of the circuits. The capacitor C_{in} ac-couples the input



	D1	D2	D3	D4
l_c (μm)	535	285	90	30
Z_0 (Ω)	70	70	70	83
C_{out}(fF)	105	33	20	20
C_{in} (fF)	200	200	75	80
R_b (Ω)	1k	1k		
l_b (μm)			265	90

Figure 3.34: Schematic of the unit frequency doubler stage. The inductances TL_b and TL_c are implemented as shielded microstrip-lines in the TM2 metal layer with lengths l_b and l_c respectively. The capacitor C_{in} ac-couples the input signal to the switching quad and the transconductance stage. The doublers D1 and D2 are biased using the resistors R_b instead of TL_b to save chip area [7, 88].

signal to the switching quad for in-phase multiplication. For the low-frequency doublers D1 and D2, TL_b is replaced with R_b for dc biasing to save chip area. The important design considerations are optimum device size, interstage drive power requirements, wideband operation and spurious harmonic suppression. These aspects are addressed in details in the following sections.

3.3.2.1 Optimum device size

In general, higher output power (P_{out}) requires larger devices. The size of the tuning inductance TL_c limits the maximum device size as shown in Figure 3.4. Since the collectors of Q1, Q3 and Q2, Q4 are connected, the maximum device size for this design is limited to transistors with an emitter area of $4 \times (0.96 \times 0.12)\ \mu\text{m}^2$.

3.3.2.2 Interstage drive power requirements

In this design, the quadrupler consisting of the frequency doublers D1 and D2 is optimized for high conversion gain to make it operate from low input LO power. Besides the reduced harmonic generation from the first doubler stage, a low LO input power minimizes the LO leakage by reducing the inherent asymmetry associated with the Gilbert-cell based frequency doublers [102]. Figure 3.35 shows the simulated large-signal characteristics for D1+D2, D3, and D4 for an overall output frequency of 240 GHz. For linear operation, the input power (P_{in}) should be from the point of maximum conversion gain up to IP_{1dB}. Based on this con-

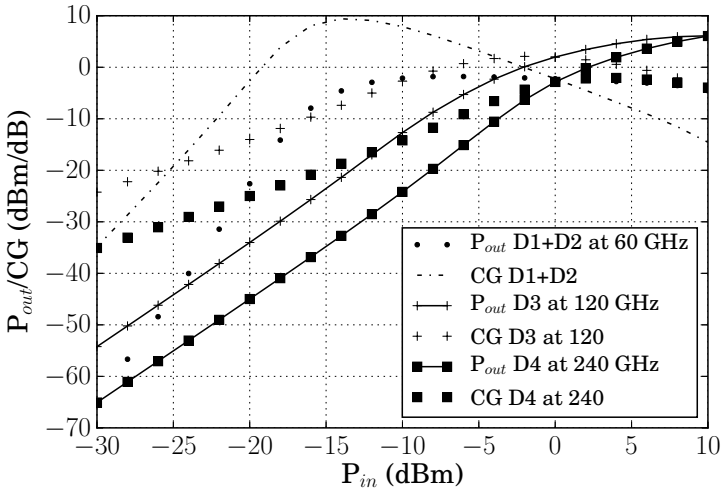
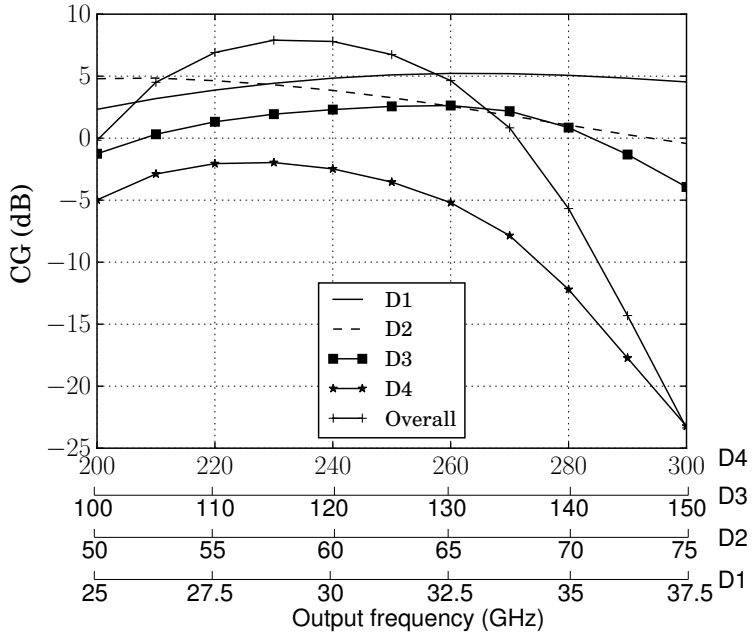


Figure 3.35: Simulated large-signal characteristics for the doublers D1+D2, D3 and D4 for an overall output frequency of 240 GHz. For an output power of -2.8 dBm at 240 GHz, the corresponding LO power at the input of D1 is -10 dBm.

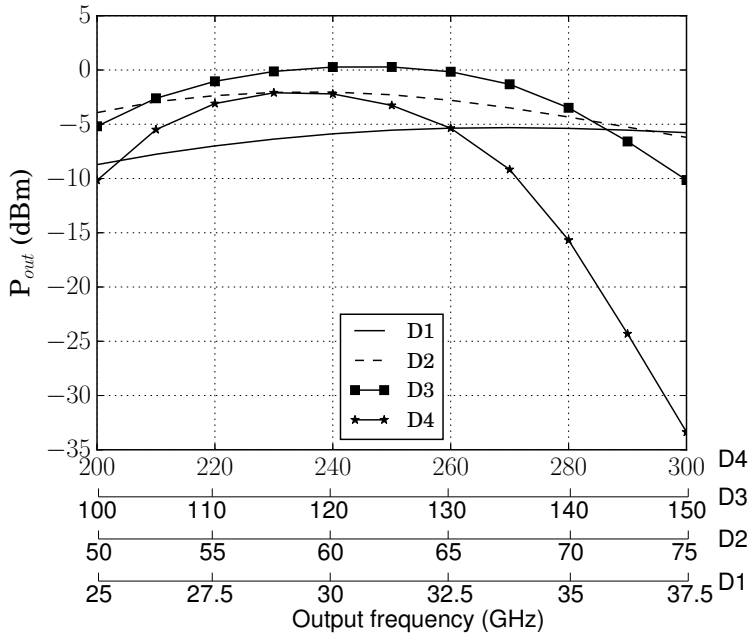
sideration, 0 < P_{in} < 7 dBm for D4, -2 < P_{in} < 3 dBm for D3, and -15 < P_{in} < -10 dBm at the input of D1+D2. For a P_{out} of -2.8 dBm at 240 GHz from D4, the required P_{in} at 120 GHz is 0 dBm. For a P_{out} of 0 dBm at 120 GHz from D3, the required P_{in} at 60 GHz is -2 dBm. This corresponds to an input LO power of -10 dBm at 15 GHz at the input of D1. Hence, the overall conversion gain is 7.2 dB (without the three-stage PA succeeding the $\times$16 frequency multiplier core).

3.3.2.3 Wideband operation

For this design, the individual doubler stages of the $\times$16 frequency multiplier are frequency staggered for wideband operation. The motivation of this technique in comparison to other bandwidth enhancement techniques have been presented in section 2.2.2. The doublers D2 and D4 are tuned lower in frequency, and the doublers D1 and D3 are tuned higher. As shown in Figure 3.36a, the peak CG at the outputs of D1, D2, D3 and D4 are at 35 GHz, 55 GHz, 130 GHz and 230 GHz respectively, and the corresponding output powers are shown in Figure 3.36b. For this simulation, the external input power to the LO chain is -10 dBm, and the simulation results are only from the active balun and the $\times$16 frequency multiplier core without the three-stage 240 GHz PA. The stagger frequency tuning between the stages resulted in an overall 3-dB bandwidth of 50 GHz (210-260 GHz) with a peak P_{out} of -2.8 dBm at 240 GHz. Figure 3.37 shows the interstage matching networks. The inputs of D3 and D4 are matched to 100 Ω (differential) at the input for the ease of breakout characterization



(a)



(b)

Figure 3.36: Simulated CG and P_{out} versus output frequency. The doublers D1 and D3 are tuned higher, and the doublers D2 and D4 are tuned lower. The overall 3-dB bandwidth is 50 GHz. At 240 GHz, a) the overall CG is 7.2 dB, and b) P_{out} is -2.8 dBm.

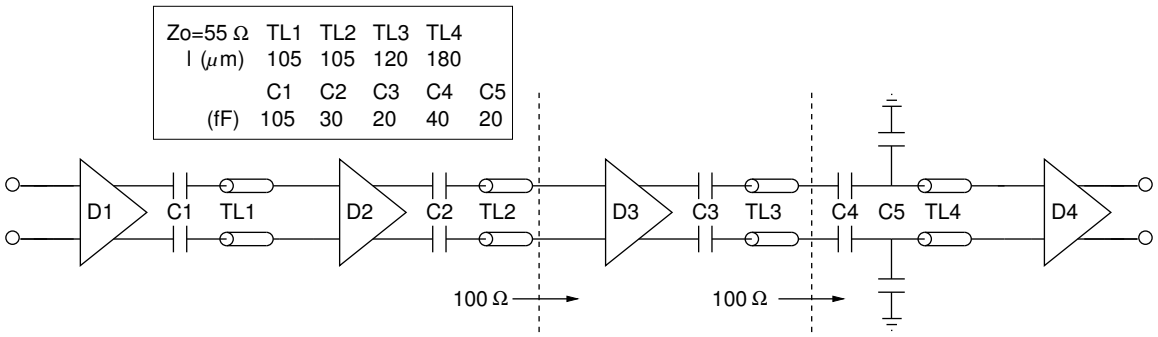


Figure 3.37: Interstage matching network of the 240 GHz LO signal source. The inputs of D3 and D4 are matched to a differential 100 Ω impedance. The doubler D4 is connected to a three-stage 240 GHz PA with 50 Ω lines, and is not shown here.

and interfacing with other circuit components. The input of the 240 GHz three-stage PA is connected to the output of D4 using 50 Ω lines, and are not shown here. The components TL2, C2 and TL1, C1 transform the input impedance of D3 and D2 based on the conversion gain considerations for the quadrupler D1+D2. Based on the chip area considerations, the input of the doubler D1 is not matched. The mismatch at the input of D1 can be easily compensated by increasing the power from the external source.

3.3.2.4 Spurious harmonics

For an external LO input signal at 15 GHz with 0 dBm power, the output of the active balun has a significant 3^{rd} harmonic component in comparison to an input signal with -10 dBm power. Figure 3.38 shows the simulated time domain waveform at the output of the active balun and the doubler D1 for these LO power levels. The consequence of an input signal with a strong 3^{rd} harmonic component results in mixing products at the spurious 18^{th} harmonic as shown in Figure 3.39. This problem is particularly aggravated as the input of D1 is not matched (due to chip area considerations), and the 3^{rd} harmonic component cannot be selectively rejected over the fundamental signal.

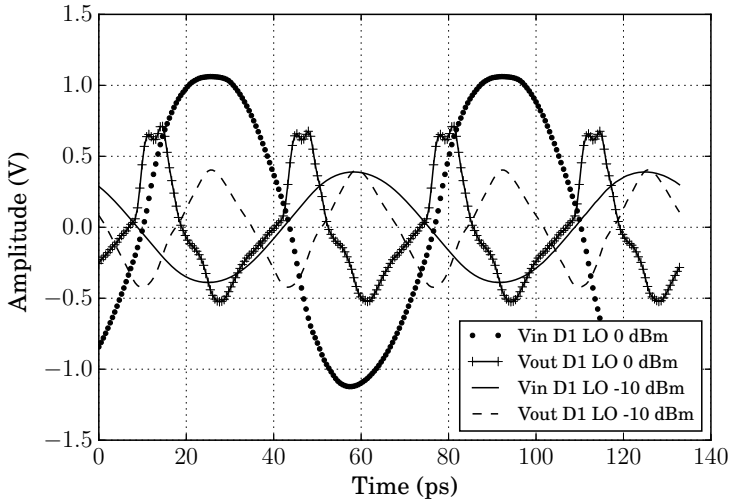


Figure 3.38: Simulated time-domain waveform at the output of the active balun and doubler D1 for an external input LO signal at 15 GHz. As the input power is increased from -10 to 0 dBm, the 3^{rd} harmonic component at the output of the balun increases, which results in a distorted waveform at the output of D1.

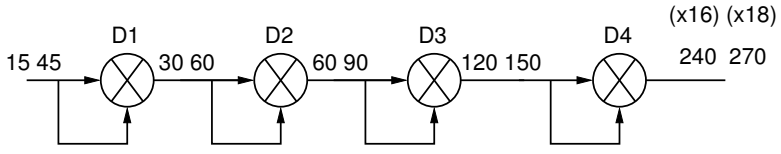


Figure 3.39: The 3^{rd} harmonic component in the input signal (15 GHz) of D1 results in a spurious 18^{th} harmonic at the overall output. The 90 GHz mixing product at the output of D1 is too high for D2, and is hence rejected.

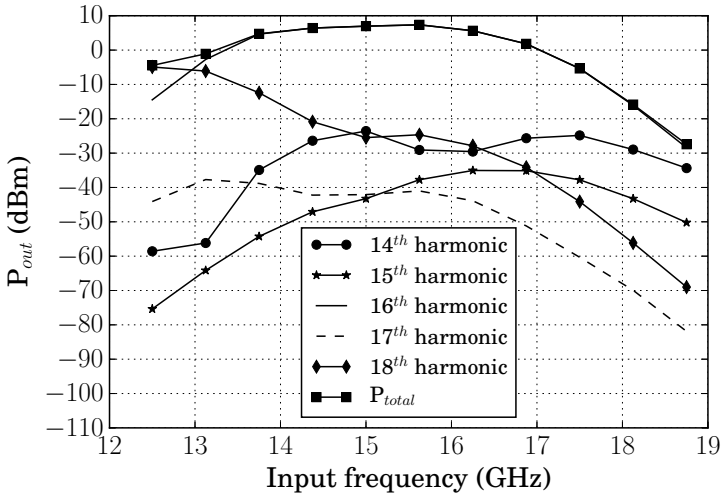


Figure 3.40: Simulated P_{out} at the different harmonics for an input LO power of -10 dBm. At 15 GHz, P_{out} at the 16^{th} harmonic is 7.3 dBm. The relative attenuation of the 14^{th}, 15^{th} and 17^{th} harmonic is at least 25 dB. The effect of the 18^{th} harmonic only starts at input frequency less than 13.25 GHz, and hence can be ignored.

The simulated output power of the overall LO signal source (active balun + $\times$16 frequency multiplier + three-stage PA) at the different harmonics versus input frequency for an input LO power of -10 dBm is shown in Figure 3.40. The simulated peak P_{out} is 7.3 dBm at 240 GHz (corresponding to the input frequency of 15 GHz), and the 3-dB bandwidth at the output is 50 GHz (215-265 GHz). The spurious 14^{th}, 15^{th} and the 17^{th} harmonics are sufficiently suppressed (more than 25 dB), and this results in the total output power (P_{total}) closely following the desired 16^{th} harmonic signal. The effect of the 18^{th} harmonic signal starts dominating only at input frequencies less than 13.25 GHz, and hence can be ignored. The effect of increasing the LO input power to 0 dBm results in strong 18^{th} harmonic generation (as expected) below 14.25 GHz, and this results in P_{total} remaining constant as shown in Figure 3.41. Hence, the optimum input LO drive power is -10 dBm.

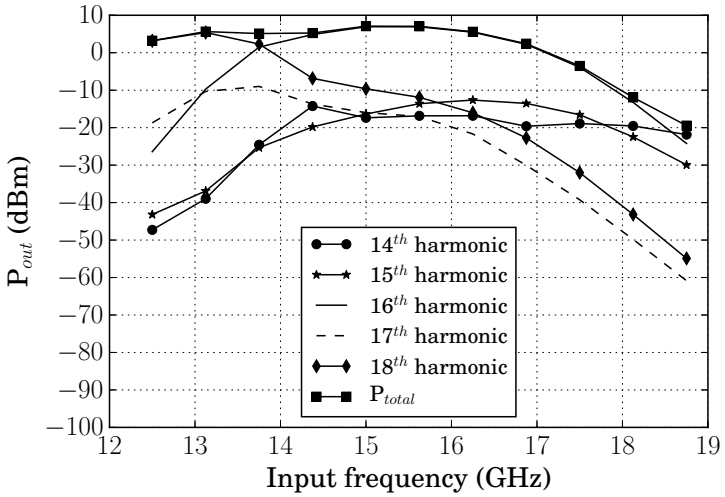


Figure 3.41: Simulated P_{out} at the different harmonics for an input LO power of 0 dBm. The effect of the spurious 18^{th} harmonic increases significantly below 14.25 GHz, and this results in P_{total} remaining constant. This substantially limits the usable input frequency range. Hence, the optimum input LO power is -10 dBm.

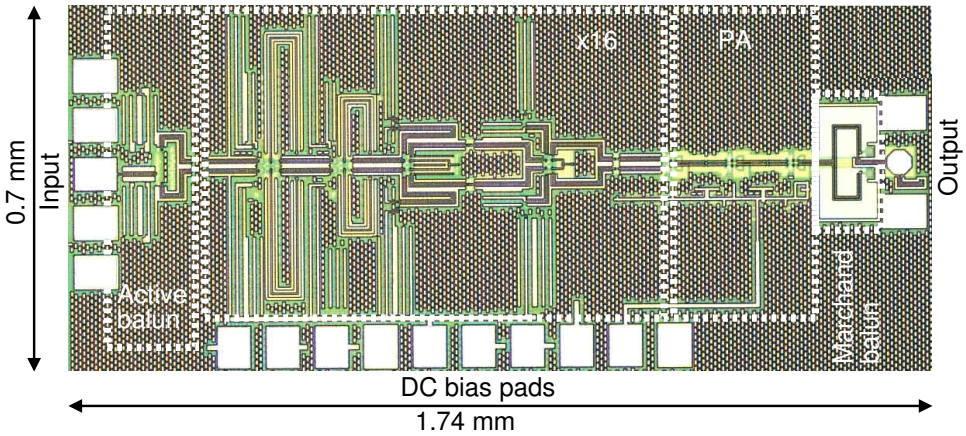


Figure 3.42: Chip-micrograph for the breakout of the 240 GHz LO signal source. The total chip area including the pads is 1.218 mm^2. For single-ended on-wafer measurements, an auxiliary Marchand-balun has been added at the output [88].

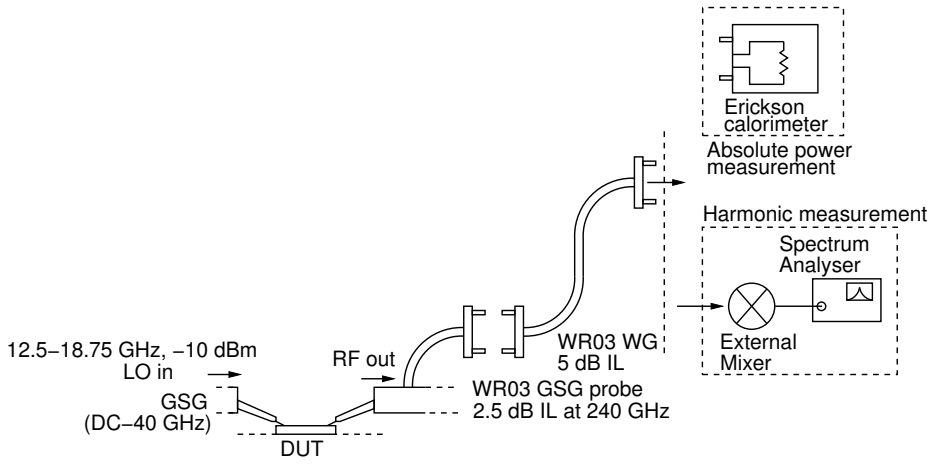


Figure 3.43: Measurement setup for large-signal bandwidth characterization of the 240 GHz LO signal source. The low-frequency input signal (below 20 GHz) from the synthesizer is coupled to the chip using a GSG probe (DC-40 GHz) with a 2.9 mm K-connector. The output signal is measured using a WR03 GSG waveguide probe using an Erickson calorimeter and harmonic mixer.

3.3.3 240 GHz LO signal source characterization results

Figure 3.42 shows the chip-micrograph for the breakout of the standalone 240 GHz LO signal source. An auxiliary Marchand-balun has been added at the output to enable single-ended on-wafer measurements. The total chip area including the pads is 1.218 mm^2. The measurement setup for the large-signal bandwidth characterization of the LO signal source is shown in Figure 3.43. A GSG probe (DC-40 GHz) with a 2.9 mm K-connector provides the low-frequency input signal (less than 20 GHz) to the chip using an external synthesizer. The output signal is measured using a WR03 GSG waveguide probe with an average insertion loss of 7.5 dB in the 220-325 GHz range. The output power has been measured using absolute power and harmonic measurement techniques.

3.3.3.1 Absolute power measurements

An Erickson calorimeter, equipped with a WR03 waveguide taper, is used for absolute power measurements. Figure 3.44 shows the output power from the standalone LO signal source. The peak output power is 6.4 dBm at 230 GHz, and the 3-dB RF bandwidth at the output is 50 GHz (215-265 GHz). The strong spurious harmonic generation at an LO input power of 0 dBm results in P_{out} remaining almost constant for input frequency in the 12.5-13.75 GHz range. This is expected from the discussions and the simulations presented in the preceding section. Table 3.3 summarizes the simulation and measurement results.

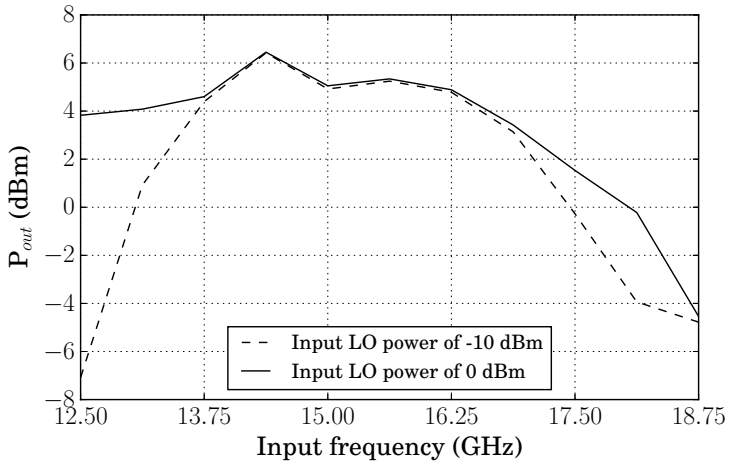


Figure 3.44: Absolute power measurement of the 240 GHz LO signal source. For an input LO power of -10 dBm, the peak output power is 6.4 dBm at 230 GHz, and the 3-dB RF bandwidth is 50 GHz (215-265 GHz). For an input LO power of 0 dBm, the output power remains constant below 13.75 GHz.

Table 3.3: Simulation and measurement results of the 240 GHz LO signal source

Parameters	Simulated	Measured
Peak P_{out} (dBm)	7.3 @ 240 GHz	6.4 @ 230 GHz
3-dB RF bandwidth (GHz)	50	50
DC power (W)	0.74	0.74

3.3.3.2 Harmonic measurements

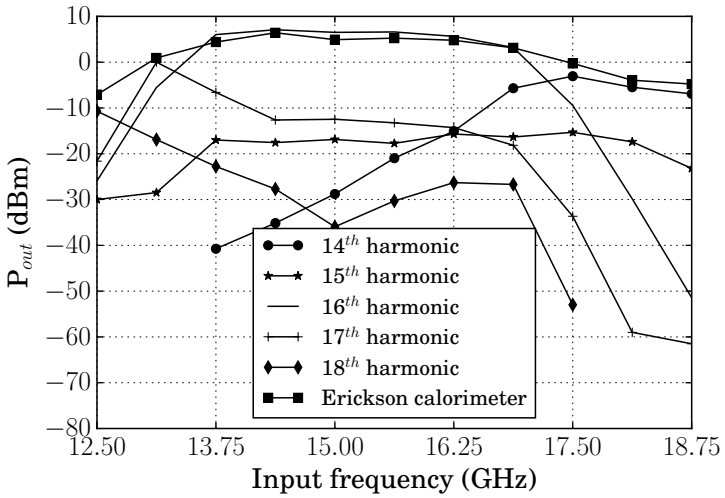


Figure 3.45: Measured P_{out} at the different harmonics at the output of the 240 GHz LO signal source for an input power of -10 dBm. The output power at the 16^{th} harmonic (220-270 GHz) is close to absolute power measurements for input frequencies in the 13.75-16.875 GHz range.

The power at the different harmonics is measured by down-converting the output signal using a WR03 harmonic ($\times$18) mixer. The mixer has been calibrated before using a power meter and a 220–325 GHz source module. The LO of the mixer is set at an offset of 33 MHz from the harmonic of interest. The down-converted IF signal at 33 MHz is measured using a spectrum analyzer. The P_{out} at the desired harmonic can then be estimated using the known conversion gain (prior calibration) of the harmonic mixer. Figure 3.45 shows the measured output power at the different harmonics for an LO input power of -10 dBm. For an input LO frequency in the 13.75-16.875 GHz range, the output power at the 16^{th} harmonic (220-270 GHz) is close to the absolute power measurements using the Erickson calorimeter. This is because the power in the other spurious harmonics is significantly lower. In this frequency span, the attenuation of the 15^{th} and the 18^{th} harmonics relative to the 16^{th} harmonic is at least 20 dB. At an input frequency of 13.75 GHz, the relative attenuation of the 17^{th} harmonic is 15 dB, and it is at least 20 dB beyond that frequency. For the 14^{th} harmonic, the relative attenuation is more than 20 dB up to an input frequency of 16.25 GHz. At an input frequency of 16.875 GHz, the relative attenuation of the 14^{th} harmonic decreases to 10 dB. Figure 3.46 shows the measured P_{out} at the different harmonics for an input LO power of 0 dBm. The 17^{th} and 18^{th} harmonic becomes significantly higher (compared to the case when LO input power is -10 dBm) at input frequencies below 13.75 GHz, and hence the output power remains constant. This is consistent with the simulations and absolute power measurements.

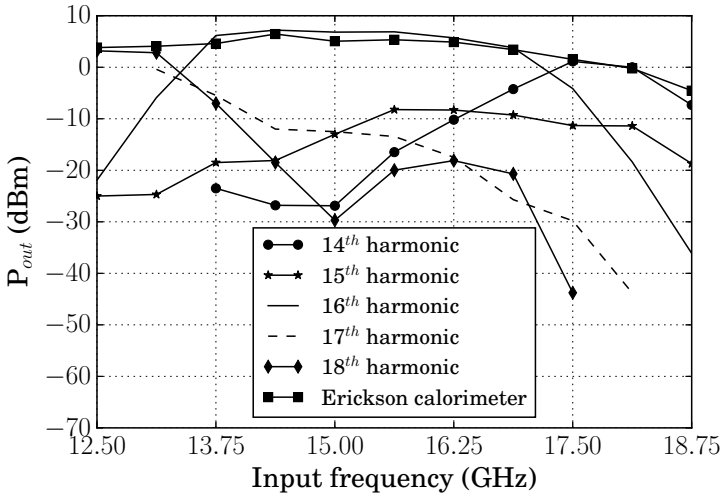


Figure 3.46: Measured P_{out} at the different harmonics at the output of the 240 GHz LO signal source for an input power of 0 dBm. The output power at the 16^{th} harmonic (220-270 GHz) is close to absolute power measurements in the 13.75-16.875 GHz input frequency range. The 17^{th} and 18^{th} harmonic dominates below 13.75 GHz, and hence P_{total} remains constant.

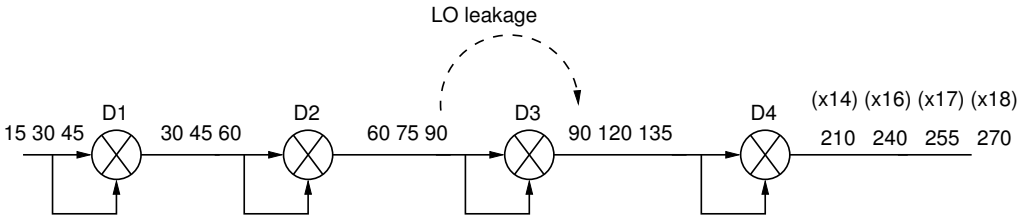


Figure 3.47: The 2^{nd} and 3^{rd} harmonic component of the input signal at D1 and LO leakage from D3 results in spurious tones at 14^{th}, 17^{th} and 18^{th} harmonic of the input signal.

From simulations, only the spurious 18^{th} harmonic is expected to dominate at the lower end of the input frequency span. However, in the harmonic measurements, the effect of the 17^{th} harmonic is also seen. Additionally, the effect of the 14^{th} harmonic is also seen at input frequency greater than 17.5 GHz. A possible reason can be due to the presence of the 2^{nd} harmonic at the active balun output in addition to the 3^{rd} harmonic. This along with LO leakage from D3 results in spurious mixing products at the 14^{th}, 17^{th} and 18^{th} harmonic as shown in Figure 3.47.

Figure 3.48 shows the results from the phase-noise measurement of the 240 GHz LO signal source. An external 15 GHz signal with a phase-noise of -135 dBc/Hz (1 MHz offset) is used for this measurement. At the output, the measured phase-noise at 240 GHz (1 MHz offset) is -110 dBc/Hz, which is a degradation of 25 dB. This is close to the theoretically expected degradation of 24.08 dB calculated using the expression $20\times\log(16)$.

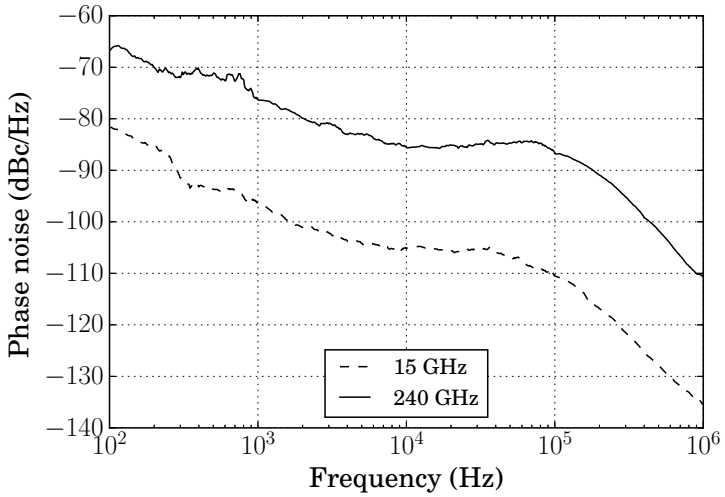


Figure 3.48: Measured phase-noise of the 240 GHz LO signal source. An external 15 GHz signal (-10 dBm) with a phase-noise of -135 dBc/Hz (1 MHz offset) is used. The measured phase-noise at 240 GHz is -110 dBc/Hz, which is a degradation of 25 dB.

Table 3.4 compares the results from this work with others reported in the literature. To demonstrate the feasibility of silicon technologies for sub-mmWave frequencies, sources operating at frequencies much higher than the targeted 200-325 GHz (in this thesis) range are also reported in this table. The results are classified based on the oscillator and frequency multiplier-based circuit topologies, and a comparison to III-V technologies is also presented. The 240 GHz LO signal source presented in this work reports the highest output power, bandwidth and DC-RF efficiency for frequency multiplier-based sources in the 200-325 GHz range in silicon technologies. The results reported here are conservative numbers, and are not corrected for the balun and pad losses of 2-2.5 dB at the output. If corrected for the balun and pad losses, the output power is comparable to the implementations in III-V technologies in [165]. The frequency of operation for the circuits reported in [166, 167] is $f_{max}/3$ while in this work the frequency of operation is close to $f_{max}/2$, and yet the output power is comparable and bandwidth is higher.

Table 3.4: Signal sources above 200 GHz reported in the literature

Tech	Freq/BW (GHz/%)	peak P_{out} (dBm)	Circuit/ overall mult factor	DC-RF (%)	Ref
Frequency multiplier-based					
130-nm SiGe	240/21	6.4[1]	cascaded x2+PA/ x16	0.6[1]	Section 3.3
130-nm SiGe	320/13	-4.9	x3+PA+x2/x18	0.017	[16]
130-nm SiGe	322.5/3.4	-3	x3+PA+x2/x18	0.033	[90]
	318/6.2	-1	3 stage PA+x2 /x2	0.19	
	227.5/11	-3	3 stage PA+x2 /x2	0.12	
130-nm SiGe	250/12	0	cascaded x2+PA/x16	0.143	[88]
65-nm CMOS	288/5.3	0	Tripler+PA/27	0.36	[168]
45-nm CMOS	420/10	-10	PA+quadrupler/x4	0.014	[169]
250-nm SiGe	825/1.8	-29	x3+PA+x5/x45	2.7e-4	[29]
Oscillator-based					
130-nm SiGe	240/9.1	2	VCO+ PA+x2	0.53	[170]
65-nm CMOS	260/9.5	0.4	Harmonic osc/2	0.14	[171]
65-nm CMOS	293/5.74	-2.74	VCO/x3	2.8	[172]
45-nm CMOS	280/3.2	-7.1	Distributed active radiator	-	[173]
65-nm CMOS	288/0.7	-4.1	Triple-push	1.4	[76]
65-nm CMOS	256	4.15	Harmonic osc/2	1.14	[174]
130-nm SiGe	530/3.2	0	Triple-push	0.4	[21]
65-nm CMOS	482/0	-7.9	Triple-push	-	[86]
130-nm SiGe	232/11.6	-3.6	Fund osc	0.81	[4]
	320/6.6	-13.3	Push-push osc	0.07	
	300/7.7	-1.7	VCO+x2	0.4	
130-nm SiGe	246/4	2	Fund VCO	0.43	[75]
130-nm SiGe	323.8	-6.3	push-push	0.7	[175]
Comparison to III-V technologies					
25-nm InP	400/9.4	7.8	x3+PA+x3/x9	-	[166]
25-nm InP	340/10.8	8	x3+x3+x2/x18	1.4	[167]
InP-HBV	271/5	8.1	x3	-	[165]
InP-BiCMOS	250/2	-1.6	VCO + Tripler	-	[176]
InP-HBT	286	-3.9	Fund VCO	-	[177]
InP-HBT	307/5.9	4.8	Fund VCO	3.4	[178]
InP-HBT	573	-19.2	Fund VCO	0.01	[179]

[1] Measured at the output pad.

3.4 Mixers for 240 GHz quadrature Tx and Rx chipset

In this section, the circuit design considerations for the mixers of the 240 GHz quadrature direct-conversion Tx and Rx chipset (Chapter 4) are presented. The mixers are based on the double-balanced Gilbert-cell topology due to the advantages like inherent differential operation, LO rejection, and high conversion gain [149]. The primary design considerations are wideband RF and IF operation, sufficient output power (up-conversion mixer), and low NF (down-conversion mixer). For quadrature LO generation, an on-chip wideband differential 90° coupler reported in [14] is used. For this coupler, the simulated isolation is less than -23 dB, the input return loss is less than -26 dB, and the amplitude and phase imbalances are less than 1.6 dB and 3° respectively from 160-340 GHz. The excess loss of the coupler at 240 GHz is 0.75 dB. The IF inputs of the mixers provide a differential input impedance of 100 Ω for wideband matching. The mixers are not individually characterized as breakout structures due to the challenge of providing high LO power from external sources above 200 GHz. In this section, only the simulation results are presented. The overall Tx and Rx characterization results are presented in Chapter 4. An IF frequency of 25 MHz is used for the Tx, and an IF frequency of 33 MHz is used for the Rx due to the measurement setup limitations.

3.4.1 240 GHz quadrature up-conversion mixer

The circuit schematic for the 240 GHz quadrature up-conversion mixer is shown in Figure 3.49. The switching quads of the I-mixer and Q-mixer consists of the transistors Q1-Q4 and Q7-Q10 respectively. The transistors Q5-Q6 and Q11-Q12 form part of the respective transconductance stages of the I-mixer and Q-mixer. The switching quads are driven by quadrature LO signals from the wideband on-chip 90° coupler [14]. The collector currents from the two quadrature mixers are combined at the output. The transistors Q15-Q16 for the I-mixer, and Q17-Q18 for the Q-mixer form part of the common-collector buffer amplifiers at the IF inputs. The buffer amplifiers have a shunt 50 Ω resistance at the input for wideband matching. The total degeneration resistance at the emitter of the buffer amplifiers is 434 Ω (resistive divider 127+307 Ω). The buffer outputs are dc-coupled to the transconductance stage of the mixers using a resistive divider. The resistive divider is used for dc-biasing of the transconductance stage, and it also helps in stability since direct capacitive loading (due to the input impedance of the transconductance stage) of the emitter node of the buffer can trigger parasitic oscillations. In terms of device size, minimum size devices with an emitter area of $1\times(0.96\times 0.12)\ \mu m^2$ are used at the switching quads to keep the LO drive power requirements to the lowest possible [180]. Hence, for the transconductance stage transistors with an emitter area of $2\times(0.96\times 0.12)\ \mu m^2$ are used. For the buffer amplifiers, transistors with an emitter area

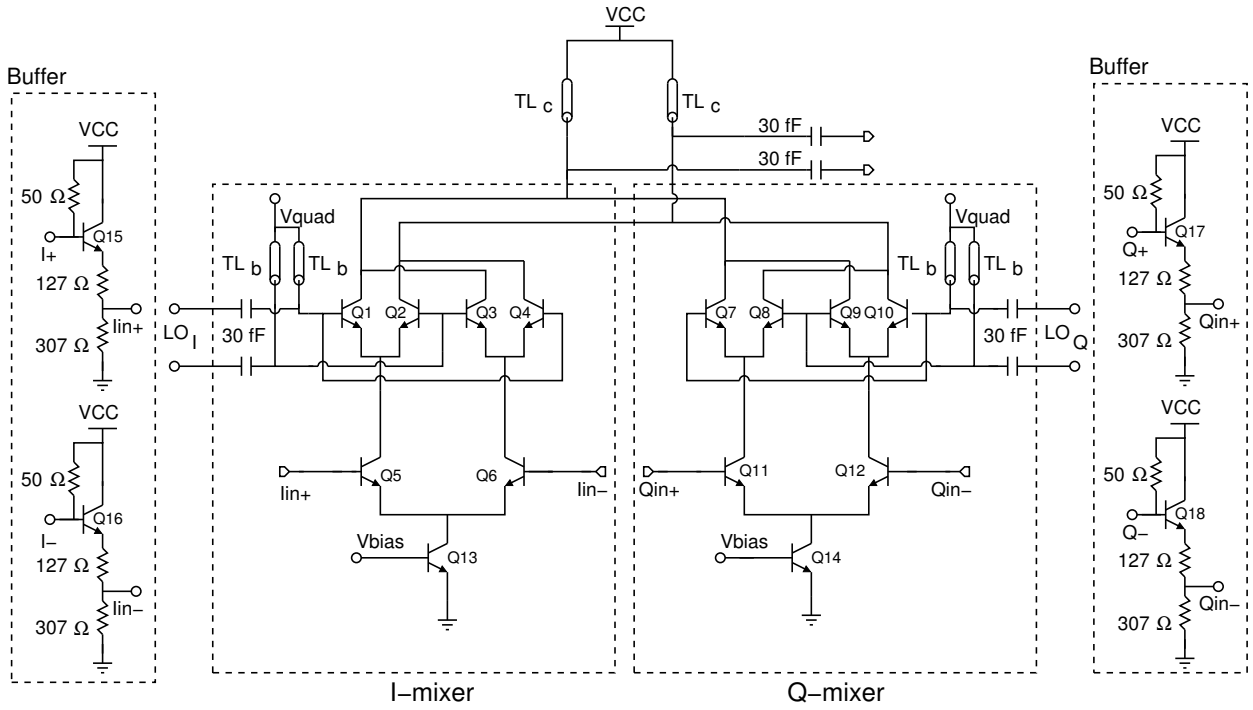


Figure 3.49: Schematic of the 240 GHz quadrature up-conversion mixer. The transistors Q1-Q4 (I-mixer) and Q7-Q10 (Q-mixer) are part of the switching quads, and Q5-Q6 (I-mixer) and Q11-Q12 (Q-mixer) are part of the transconductance stage. At the IF inputs, common-collector based buffer amplifiers with shunt 50 Ω resistances are used for wideband matching.

of $4\times(0.96\times0.12)\ \mu m^2$ are used for linearity reasons. A microstrip-line based tuning inductor TL_c with a length of 74 μm is used at the collector output. The Z_o of TL_c is 60 Ω and the attenuation is 3000 dB/m. At the base of the switching quads, microstrip-line based tuning inductor TL_b with a length of 63 μm is used to tune out the parasitic capacitance which enables stronger switching. The Z_o of TL_b is 70 Ω and the attenuation is 3000 dB/m. The ground plane for the microstrip-line is implemented in the M3 metal layer.

At an LO frequency of 240 GHz and drive power of 5 dBm at the input of the 90° coupler, the peak CG is 0.7 dB, P_{sat} is -5 dBm and OP_{1dB} is -8 dBm as shown in Figure 3.50. For this simulation, a 25 MHz IF signal (-5 dBm) is applied into one of the IF channels (I or Q). The simulated 3-dB IF bandwidth (with -5 dBm input IF power) is 38 GHz as shown in Figure 3.51, and the 3-dB RF bandwidth is 50 GHz (215-265 GHz) as shown in Figure 3.52. For RF bandwidth characterization, a 25 MHz IF signal (-5 dBm) is used for this simulation. For the up-conversion mixer, the optimum LO power at the input of the 90° coupler is 5 dBm at 240 GHz as shown in Figure 3.53.

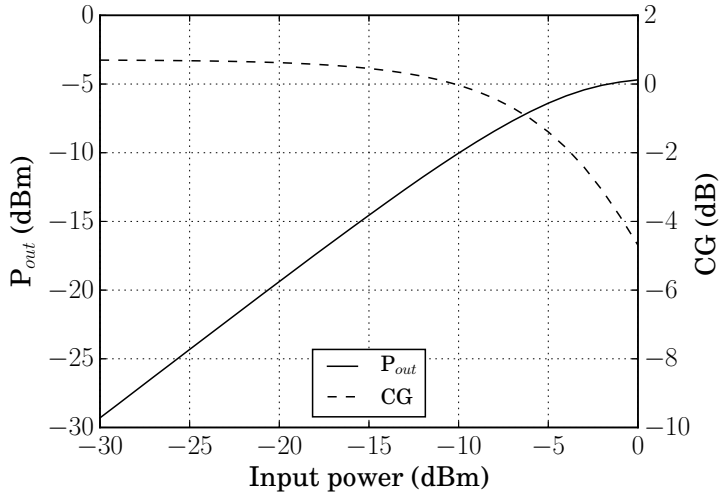


Figure 3.50: Simulation results from the linearity characterization of the 240 GHz up-conversion mixer. The peak CG is 0.7 dB, P_{sat} is -5 dBm and OP_{1dB} is -8 dBm. A 25 MHz IF signal (-5 dBm) is used for this simulation.

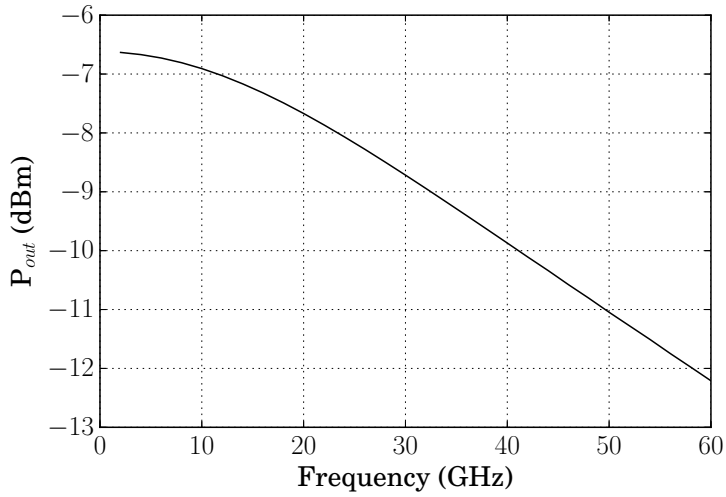


Figure 3.51: Simulation results for the IF bandwidth characterization of the 240 GHz up-conversion mixer. The 3-dB IF bandwidth is 38 GHz.

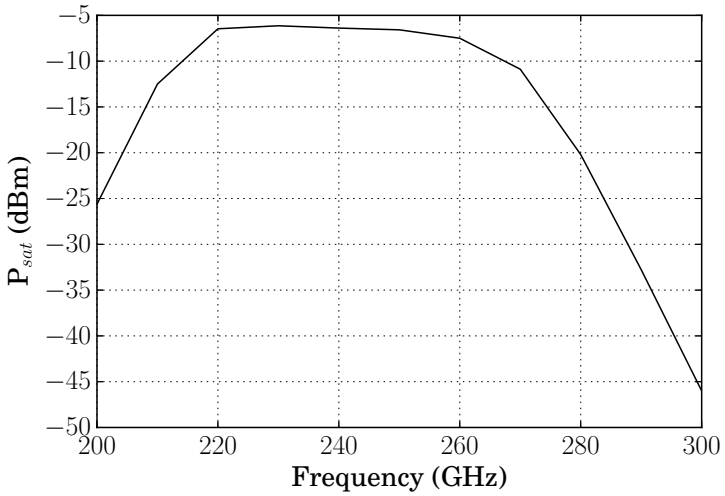


Figure 3.52: Simulation results for the RF bandwidth characterization of the 240 GHz up-conversion mixer. The 3-dB large-signal RF bandwidth is 50 GHz.

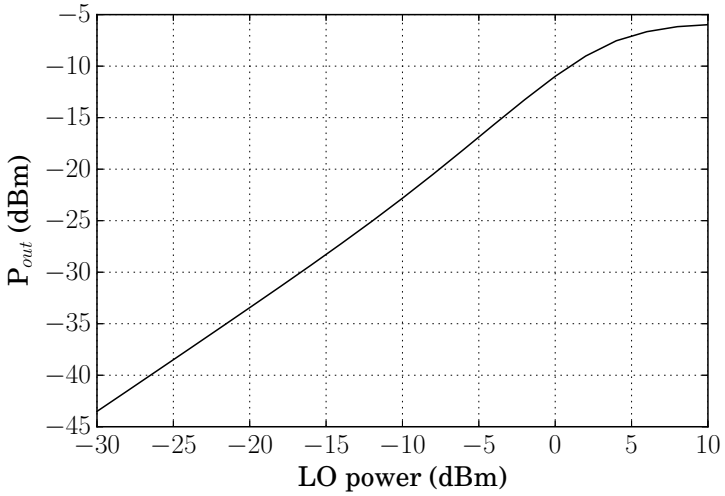


Figure 3.53: Simulation results for the variation of P_{out} with LO power for the 240 GHz up-conversion mixer. For stronger switching, an LO power of 5 dBm and higher is required at the input of the 90° coupler.

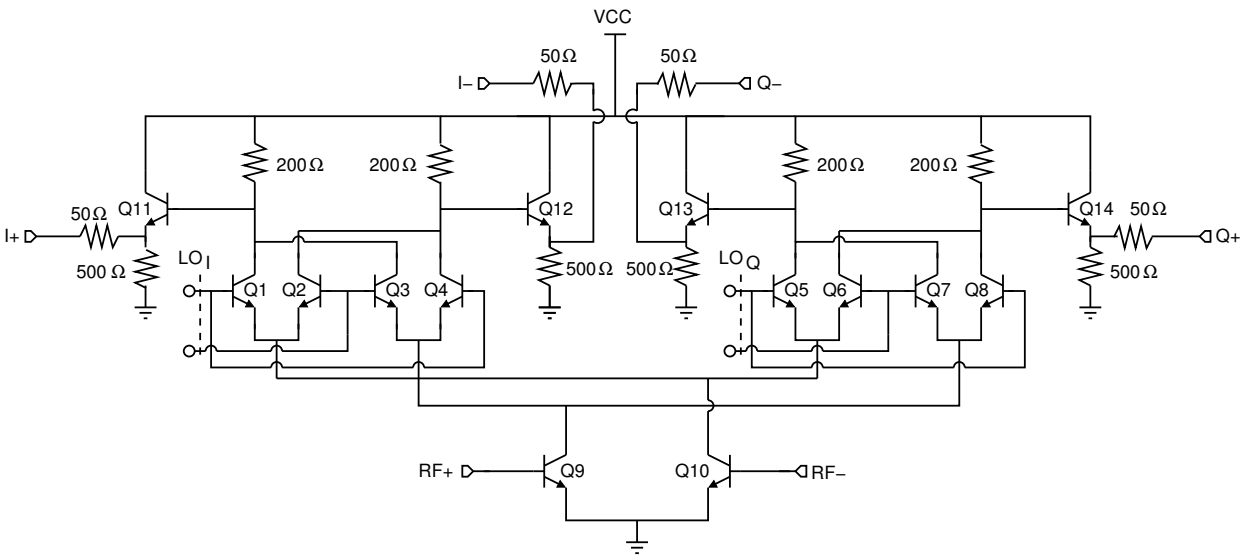


Figure 3.54: Schematic of the 240 GHz quadrature down-conversion mixer. The transconductance stage (Q9-Q10) injects the RF current into the switching quads of the I-mixer (Q1-Q4) and Q-mixer (Q5-Q8). The optimum load impedance is 200 Ω.

3.4.2 240 GHz quadrature down-conversion mixer

The circuit schematic of the 240 GHz quadrature down-conversion mixer is shown in Figure 3.54. The RF current from the transconductance stage, consisting of the transistors Q9-Q10, is injected into the switching quads which consists of the transistors Q1-Q4 for the I-mixer, and Q5-Q8 for the Q-mixer. The switching quads are driven by quadrature LO signals using an on-chip wideband 90° coupler. The outputs of the mixers are connected to the common-collector buffer amplifiers consisting of the transistors Q11-Q12 for the I-mixer, and Q13-Q14 for the Q-mixer. The buffers have an emitter degeneration resistance of 500 Ω. For wideband IF matching, a 50 Ω series resistance is connected at the IF outputs. The transistor sizes for the mixer core and buffer are identical to the 240 GHz up-conversion mixer presented in section 3.4.1. This is based on the LO drive power and linearity considerations. The choice of the load resistance is a trade-off between the peak CG and IF bandwidth due to the RC time constant of the collector output [180]. For this design, a load impedance of 200 Ω is chosen. This results in a 3-dB IF bandwidth of 35 GHz, and the peak CG is -0.5 dB as shown in Figure 3.56. For this simulation, the LO frequency is 240 GHz (33 MHz IF) and the drive power at the input of the 90° coupler is 5 dBm. The simulated 3-dB RF bandwidth (33 MHz IF) for the 240 GHz down-conversion mixer is 52 GHz as shown in Figure 3.55. The minimum NF is 14.2 dB at 240 GHz. The simulated minimum required LO power is -2.5 dBm at the input of the 90° coupler at an LO frequency of 240 GHz (33 MHz IF) as shown in Figure 3.57. At 240 GHz LO frequency, the simulated IP_{1dB} is -2.5 dBm as shown in Figure 3.58.

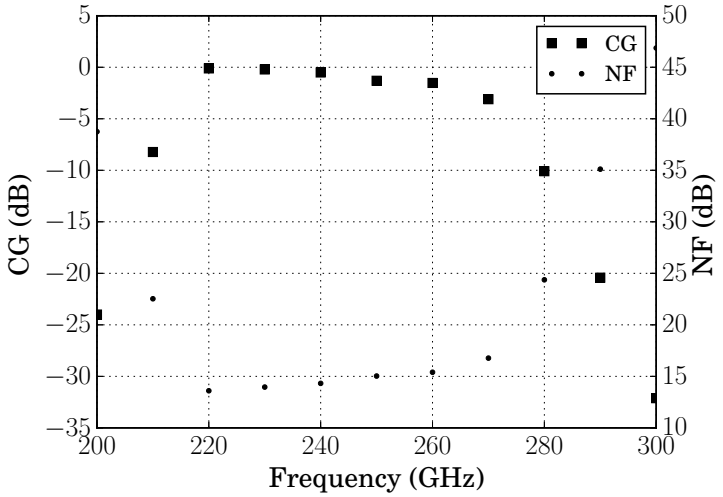


Figure 3.55: Simulation results for the RF bandwidth characterization of the 240 GHz down-conversion mixer. The 3-dB RF bandwidth is 52 GHz. At 240 GHz, CG is -0.5 dB and NF is 14.2 dB.

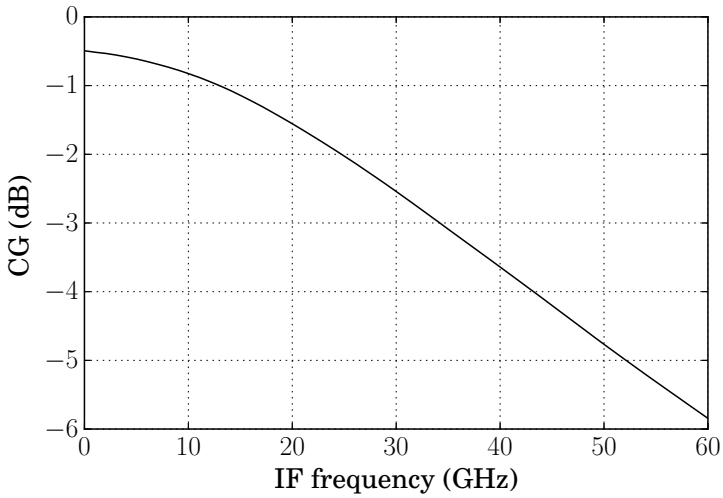


Figure 3.56: Simulation results for the IF bandwidth characterization of the 240 GHz down-conversion mixer. For R_c=200 Ω, the peak CG is -0.5 dB and the 3-dB IF bandwidth is 35 GHz. An IF frequency of 33 MHz is used for this simulation.

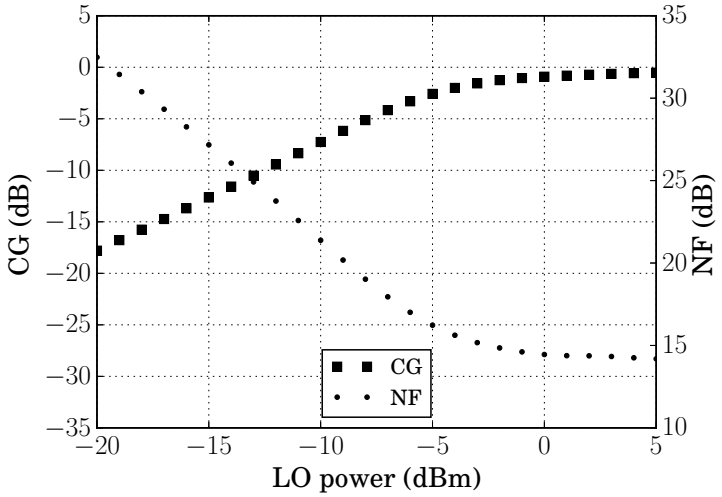


Figure 3.57: Simulation results for the variation of CG and NF of the 240 GHz down-conversion mixer at different LO drive power levels. At an LO frequency of 240 GHz, the optimum LO drive power is greater than -2.5 dBm.

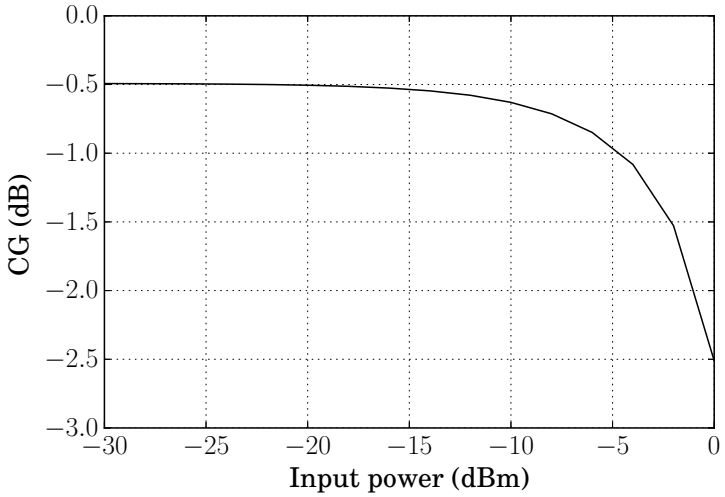


Figure 3.58: Simulation results for IP_{1dB} of the 240 GHz down-conversion mixer. At 240 GHz, IP_{1dB} is -2.5 dBm. For this simulation, a LO drive power of 5 dBm is used.

Table 3.5: Summary of the simulation results for the 240 GHz mixers

	RF BW (GHz)	IF BW (GHz)	CG (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	IP_{1dB} (dBm)	Optimum LO power (dBm)	NF (dB)
Up-conversion mixer	50	38	0.7	-5	-8	-8	≥ 5	-
Down-conversion mixer	52	35	-0.5	-	-	-2.5	$\geq$ -2.5	14.2

3.5 Conclusion

The detailed circuit design and characterization results for the wideband circuit building-blocks for a 240 GHz quadrature Tx and Rx chipset were presented in this chapter. In terms of output power, bandwidth and FoM at the individual component level, the results presented here are beyond the current state-of-the-art in silicon technologies. The results presented here are comparable to III-V technologies which have the advantage of much higher f_{max}. A 240 GHz 4-stage PA with a peak gain of 26 dB, a 3-dB bandwidth of 28 GHz and P_{sat} of 7.5 dBm was presented. A combiner-PA was demonstrated for the first time in silicon technologies above 200 GHz, and 4:1 power combination resulted in an overall P_{sat} of 9.6 dBm at 215 GHz. A $\times$16 frequency multiplier-based wideband 240 GHz LO signal source with a peak output power of 6.4 dBm, and a 3-dB RF bandwidth of 50 GHz was demonstrated. This LO signal source can be used as a standalone source, and can also be used for driving sub-harmonic receivers operating at 480 GHz over a 100 GHz bandwidth. The design of up-conversion mixers and down-conversion mixers for the 240 GHz Tx and Rx chipset were also presented. The simulated RF bandwidth of the up-conversion mixer is 50 GHz, and the IF bandwidth is 38 GHz. The simulated RF bandwidth of the down-conversion mixer is 52 GHz, and the IF bandwidth is 35 GHz. For the up-conversion mixer, P_{sat} at 240 GHz is -5 dBm and the peak CG is 0.7 dB. For the down-conversion mixer, peak CG is -0.5 dB and NF is 14.2 dB at 240 GHz.

By leveraging on the superior performance of these circuit building-blocks, a wideband fully-integrated 240 GHz quadrature Tx and Rx chipset is presented in Chapter 4. A high data-rate communication system with record data-rates is demonstrated using this chipset.

Chapter 4

240 GHz fully-integrated quadrature Tx and Rx chipset

In this chapter, the implementation of a wideband 240 GHz fully-integrated quadrature Tx and Rx chipset with on-chip antennas is presented. The circuit building blocks presented in Chapter 3 are used for the implementation of this chipset. The chipset is integrated into a low-cost chip-on-board (COB) packaging based on the low-loss Rogers 4350B printed-circuit-board (PCB) material for an overall compact form-factor. For wideband IF operation, microstrip-line based stepped-impedance low-pass filter is implemented on the PCB. This chipset is used to demonstrate a high data-rate communication system over a wireless link of 70 cm. For QPSK and BPSK modulation schemes, the maximum measured data-rates using this chipset are 24 Gbps and 25 Gbps respectively.

This chapter is divided into four sections. In section 4.1, a brief discussion on the Tx and Rx architecture is presented. The high-speed PCB design and the packaging aspects are presented in section 4.2. In section 4.3, the on-wafer and free-space characterization results for the 240 GHz quadrature Tx and Rx chipset are presented. A discussion on the link-budget, and other system level considerations for the 240 GHz high data-rate communication system along with the measurement results are presented in section 4.4.

4.1 240 GHz quadrature Tx and Rx architecture

The 240 GHz fully-integrated Tx and Rx chipset presented in this thesis is based on the direct-conversion topology. In this topology, the RF signal is directly up-converted from or down-converted to the baseband. This results in an overall compact form-factor and low dc-power consumption due to the smaller number of RF front-end components. This is in contrast to the

heterodyne architecture where the RF signal is converted to intermediate IF frequencies before up-converting from or down-converting to the baseband frequency. Furthermore, heterodyne systems have the problem of image frequencies which is not present in the case of direct-conversion systems. The vulnerability of the direct-conversion topology to LO leakage (dc-offset due to self-mixing) and quadrature imbalances can be compensated using analog and digital calibration techniques. Additionally, the sensitivity of the direct-conversion topology to even-order non-linearities can be mitigated to a large extent by using differential topologies [164, 181].

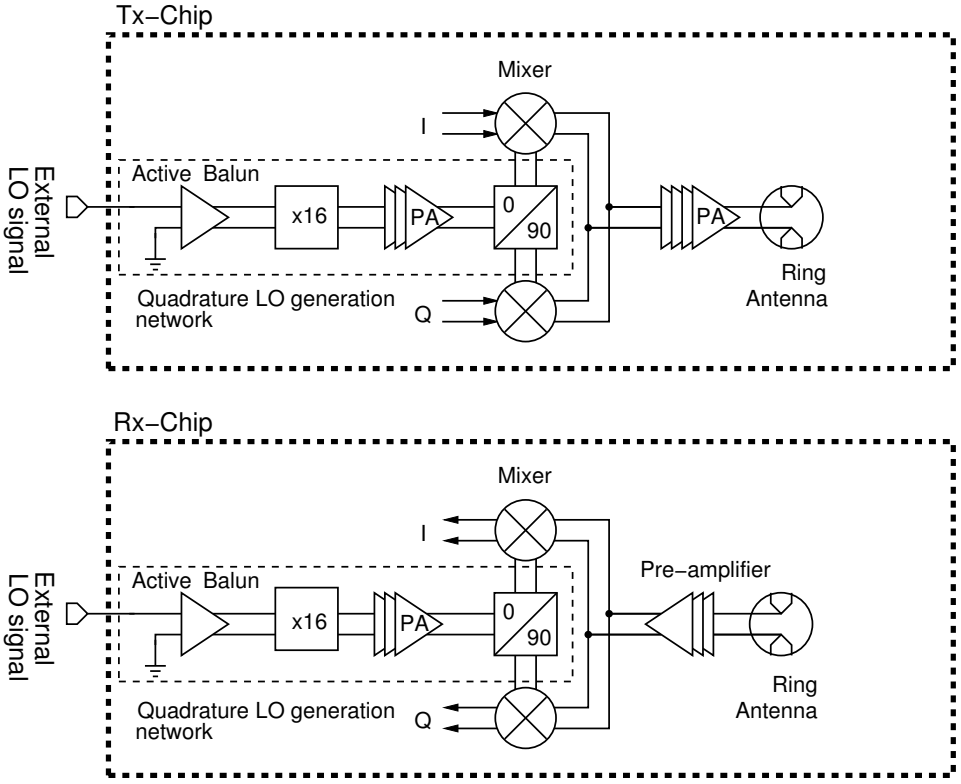


Figure 4.1: Block-diagram of the 240 GHz fully-integrated direct-conversion quadrature Tx and Rx chipset with wideband on-chip antennas. The IF inputs of the Tx and Rx are terminated with on-chip 50 Ω resistances for wideband IF matching [11].

Figure 4.1 shows the block-diagram of the 240 GHz quadrature Tx and Rx chipset. For simplicity, analog and digital calibration techniques are not included in this implementation. The on-chip quadrature LO generation network, which consists of a 240 GHz wideband LO signal source and an on-chip wideband 90° coupler [14], drives the mixers in the Tx and Rx. At the Tx side, an up-conversion mixer drives a four-stage 240 GHz PA. A three-stage version of the Tx PA is used as the pre-amplifier in the Rx to drive the down-conversion mixer. This reduces the probability of center-frequency misalignment between the Tx and Rx, and it

also ensures wideband operation. The circuit design considerations and characterization results for the 240 GHz wideband LO signal source, four-stage 240 GHz PA and the mixers are presented in Chapter 3.

In this chipset, the linearly polarized on-chip antenna used in the Tx and Rx is topologically similar to the differential wire-ring implementation presented in [7, 182, 183]. It consists of two wire semi-rings connected along the center feed. The feed is non-uniformly tapered using a step-wise approximation for wideband operation. The antenna is designed to illuminate a silicon hyper-hemispherical lens from the chip backside. The backside radiation through the silicon substrate results in wideband operation. This is in contrast to the front-side radiation where the distance to the ground plane limits the bandwidth like in the case of patch antennas. The lens also reduces the influence of surface waves on the radiation efficiency and radiation patterns, and inherently delivers a high gain in a compact form-factor to compensate for the high FSPL. The ability to mount external silicon lens gives the flexibility to have application specific directivities depending on the lens diameter and extension. The backside radiation also results in the form-factor reduction by a factor of $\sqrt{11}$ in comparison to $\sqrt{4}$ for front-side radiation, and is hence preferable. The on-chip antenna used in this chipset provides a differential impedance of 100 Ω from 180-330 GHz. The simulated cross-polarization is below 20 dB, and the parasitic common-mode radiation is minimized by providing a low impedance (4-5 Ω) for the common mode. Moreover, the antenna is optimized for the minimization of mode-conversion (differential to the common mode), and the simulated mode conversion is below 40 dB.

4.2 High-speed PCB design and packaging

The 240 GHz Tx and Rx chips are integrated into a low-loss COB packaging. The important parameters for high-speed PCB design are low dispersion and low dielectric loss. For this implementation, the ROGERS 4350B material from Rogers Corporation is used as it is well suited for high-frequency applications. From the data-sheets, the specified ε_r and $\tan\delta$ for this material are 3.66 and 0.0037 respectively from DC-20 GHz. The choice of an optimum thickness for the PCB material is a trade-off between mechanical stability and required line width.

If the PCB material is too thick, then the width of the low impedance lines become very high. The fan out of the PCB trace from the PCB bondpad becomes challenging to route for wider lines, especially for feeding the differential IF inputs where symmetry is required. Based on these considerations, a PCB thickness of 0.338 mm is found to be optimum. A 50 Ω microstrip-line for this PCB thickness corresponds to a line-width of 0.714 mm. Ideally, striplines are preferred for IF signal routing due to their low-dispersive behavior (TEM mode) in contrast to microstrip-lines (quasi-TEM mode) [142]. However, striplines require multi-layer PCB routing which increases the overall cost and complexity. The IF interface of the chip is connected to the PCB bondpad through wire bonding (manual). The wire-bond inductance limits the IF bandwidth, and hence a phase linear wideband filter must be implemented on the PCB. In terms of phase linearity, Bessel filter topology is the best while Chebyshev topology is the worst. Based on the consideration of feasible filter component values, maximally flat or Butterworth filter topology is chosen for this design. This topology has a flat amplitude response in the passband, and phase linearity is between Chebyshev and Bessel filters [142].

The PCB design goals are a 3-dB bandwidth of 15 GHz, S_{11} less than 10 dB up to the 3-dB bandwidth and stop-band attenuation of more than 20 dB at 20 GHz. Based on this specification, an 8^{th} order filter is required. A lumped low-pass LC filter is synthesized in the first design iteration as shown in Figure 4.2. The design methodology presented in [113, 142] for a 50 Ω load termination is used for this filter synthesis, and Richards transformation can be used to transform the lumped LC filter into a microstrip-line based filter. The simulated 3-dB bandwidth for the ideal lumped LC filter is 15 GHz as shown in Figure 4.3, and it does not include the effect of wire-bond inductance. A wire-bond inductance of 1 nH (corresponding to a wire-bond length of 1 mm) reduces the bandwidth to 12 GHz with significant ringing at the passband edges (more than 3-dB gain ripple), and this results in phase non-linearity. Additionally, for PCB routing a feed-line of 0.2 mm width and 1 mm length is required after the wire-bond. The feed-line contributes more inductance, and hence the filter needs further optimization.

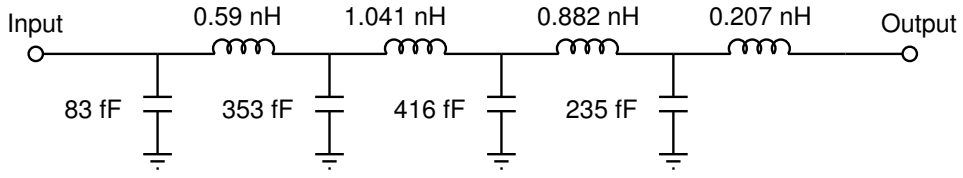


Figure 4.2: Schematic of the 8^{th} order low-pass LC filter from the 1^{st} design iteration. The filter is synthesized using the design methodology presented in [113, 142].

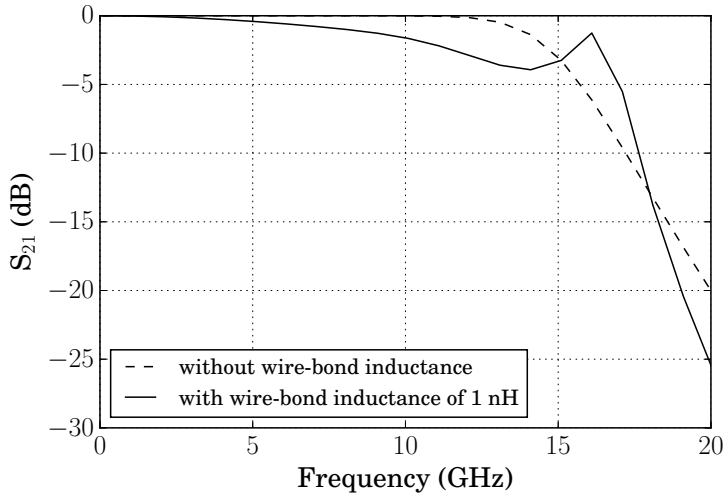
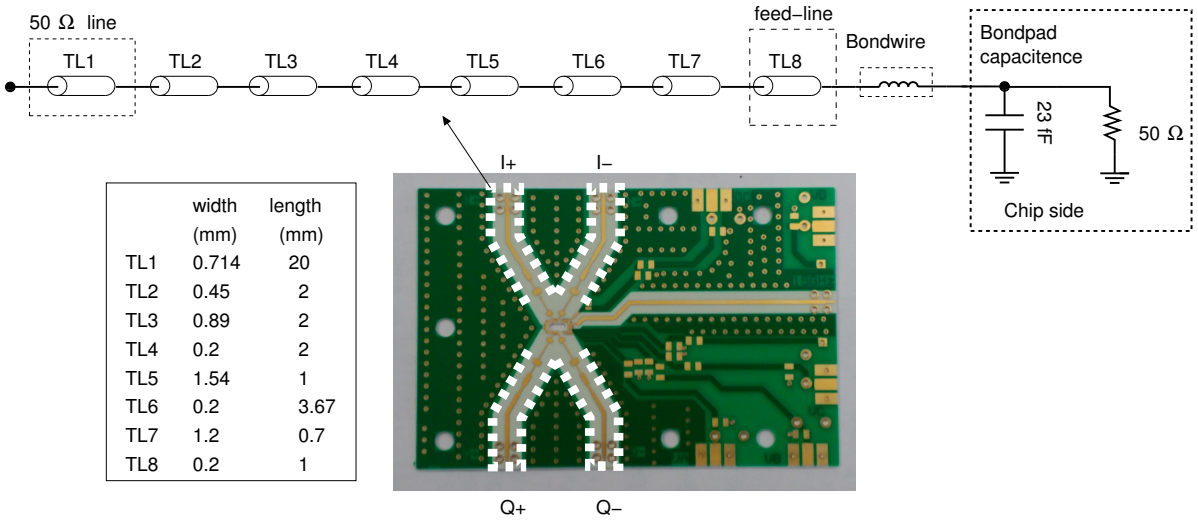


Figure 4.3: Simulated 3-dB bandwidth of the ideal lumped LC low-pass filter is 15 GHz without the wire-bond inductance. A wire-bond inductance of 1 nH reduces the bandwidth and introduces a gain ripple of 3-dB at the passband edges.

Figure 4.4 shows the overall microstrip-line based stepped impedance low-pass filter after an iterative design procedure, and taking into account the wire-bond inductance and feed-line as elements of the filter. For this filter implementation, the simulated 3-dB bandwidth varies insignificantly from 16 to 14 GHz as the wire-bond inductance is increased from 0.6 nH to 1.8 nH as shown in Figure 4.5. Also, there is no ringing in the passband. Hence, the filter implementation is robust against variation in the wire-bond inductance due to manual bonding.



	width (mm)	length (mm)
TL1	0.714	20
TL2	0.45	2
TL3	0.89	2
TL4	0.2	2
TL5	1.54	1
TL6	0.2	3.67
TL7	1.2	0.7
TL8	0.2	1

Figure 4.4: Microstrip-line based stepped impedance low-pass filter from the final design iteration in the Rogers 4350B PCB material. For this optimization, wire-bond inductance and feed-lines are included as elements of the filter.

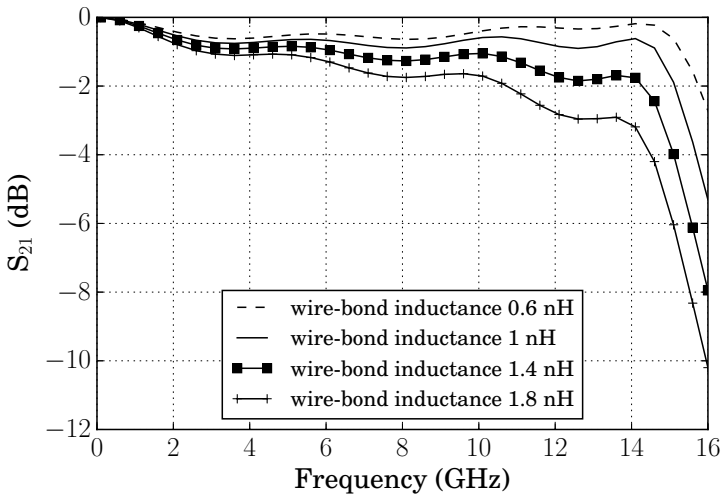


Figure 4.5: Simulated 3-dB bandwidth of the stepped impedance low-pass filter shown in Figure 4.4. The 3-dB bandwidth decreases from 16 to 14 GHz as the wire-bond inductance increases from 0.6 nH to 1.8 nH, and ringing in the passband is eliminated.

To accurately model all the parasitic effects, the 3D model shown in Figure 4.6 is used for EM simulation of the PCB filter. A wave-port is defined at the IF inputs of the filter, and a lumped-port is defined at the chip bondpad. To accurately model the ground return current, ground pads with wire-bond connections are included in this simulation. Figure 4.7 shows the simulation results from the full-EM simulation of the PCB filter. The S_{21} (insertion loss) in the passband is -0.5 dB, 3-dB bandwidth is 15 GHz and S_{11} is less than -10 dB up to 14 GHz. The group-delay variation is less than 10% up to 9 GHz.

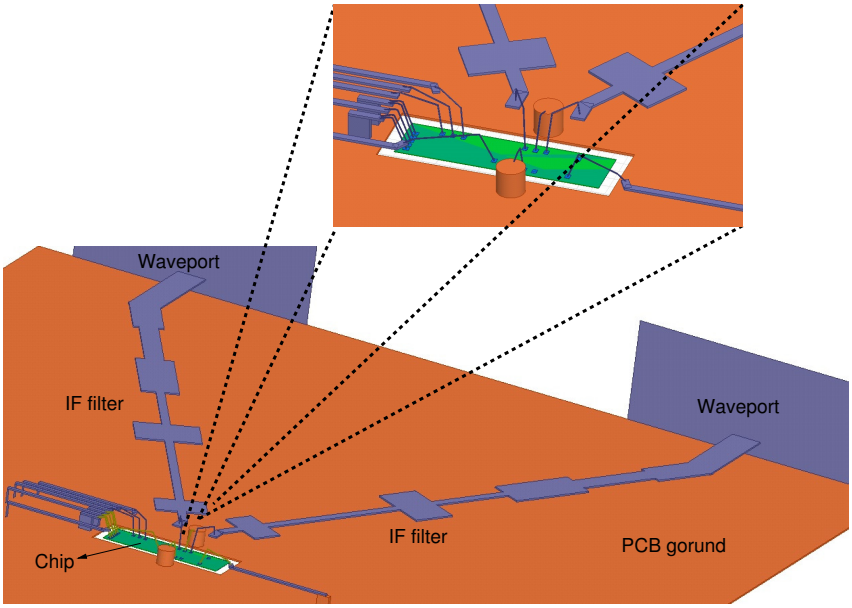


Figure 4.6: 3D model for EM simulation of the PCB filter (including the effect of wire-bond connections) using HFSS. The chip and PCB ground pads are included to accurately model the ground return current.

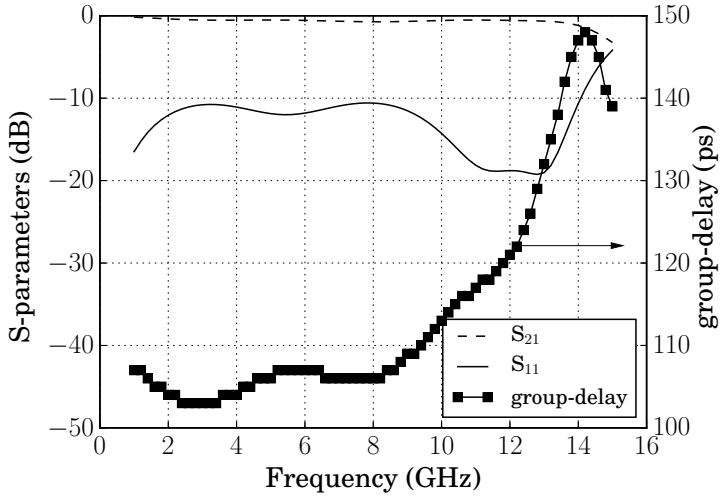


Figure 4.7: Simulation results from the full-EM simulation of the PCB filter. The S_{21} in the passband is -0.5 dB, 3-dB bandwidth is 15 GHz and S_{11} is less than -10 dB up to 14 GHz. The group-delay variation is less than 10% up to 9 GHz.

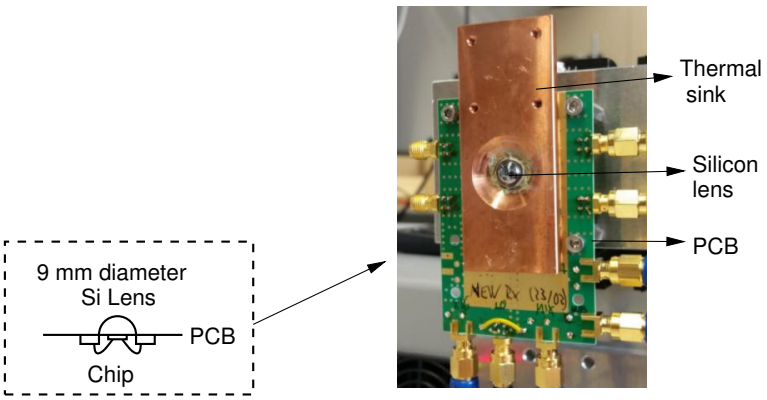


Figure 4.8: Lens-mounted 240 GHz packaged-Tx. The chip is glued to an external silicon lens with a diameter of 9 mm and wire bonded onto a low-cost PCB material (ROGERS 4350B). The 240 GHz packaged-Rx looks similar and is not shown here.

Figure 4.8 shows the 240 GHz packaged-Tx. The assembly involves chip-alignment to the lens center, and a low-shrinkage UV epoxy is used for gluing the chip to the lens. The lens extension is chosen to be close to the elliptical position with an extension to radius ratio of 34.4% (chip thickness included). This ratio helps in reducing the excessive reflection losses at the air-silicon interface, especially since no anti-reflection coating is used [7, 21, 184, 185]. The chip-lens sub-assembly is attached to the PCB. The PCB surface surrounding the chip at the lens side is metalized to minimize back radiation. A copper thermal-sink is also mounted, and itis connected to the lens with a thermally conductive glue.

4.3 240 GHz quadrature Tx and Rx characterization

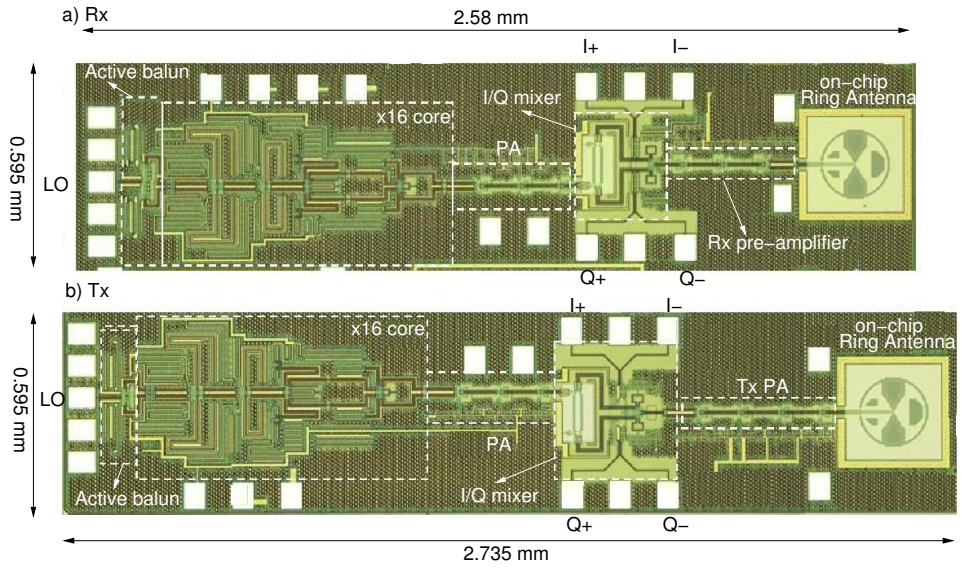


Figure 4.9: Chip-micrograph of the 240 GHz fully-integrated quadrature Tx and Rx with on-chip antennas. The chip area including the pads is a) 1.535 mm^2 for the Rx, and b) 1.627 mm^2 for the Tx.

In this section, the results from the on-wafer and free-space characterization of the 240 GHz quadrature Tx and Rx chipset are presented. Figure 4.9 shows the chip-micrograph of the Tx and Rx with wideband on-chip antennas. The chip area for the Rx is 1.535 mm^2, and for the Tx it is 1.627 mm^2. The Tx and Rx breakout circuits for on-wafer characterization have a balun at the output instead of on-chip antennas, and are not shown here.

4.3.1 On-wafer RF characterization of the 240 GHz Tx and Rx chipset

Figure 4.10 and Figure 4.11 shows the measurement setup for the on-wafer characterization of the 240 GHz Tx and Rx respectively. The Tx is characterized at an IF frequency of 25 MHz, and an IF frequency of 33 MHz is chosen for the Rx due to measurement setup limitations. A WR03 GSG waveguide probe is used to measure the Tx output, and similarly it is also used for applying the external RF signal to the Rx input. A GSG probe (DC-40 GHz) with a 2.9 mm K-connector is used to couple the external low-frequency LO signal to the chip. The output power of the Tx is measured using an Erickson calorimeter. For the Rx, an external WR03 VNA extension module in the transmit mode is used as a RF source. The output power from this module is known from a prior calibration using an Erickson calorimeter. The down-converted IF signal from the Rx is measured using a spectrum analyzer.

The external 90° and 180° hybrids are used for differential IF signal generation for single-sideband modulation at the Tx side, and they are used for combining the quadrature IF signals at the Rx side. For the Tx linearity characterization, the input power at the IF inputs is swept for a fixed LO carrier frequency of 240 GHz. For the Rx linearity characterization, a WR03 high-power source is used at the input, and output power from this source is varied using an external dc-voltage. This setup is identical to the setup shown in Figure 3.16.

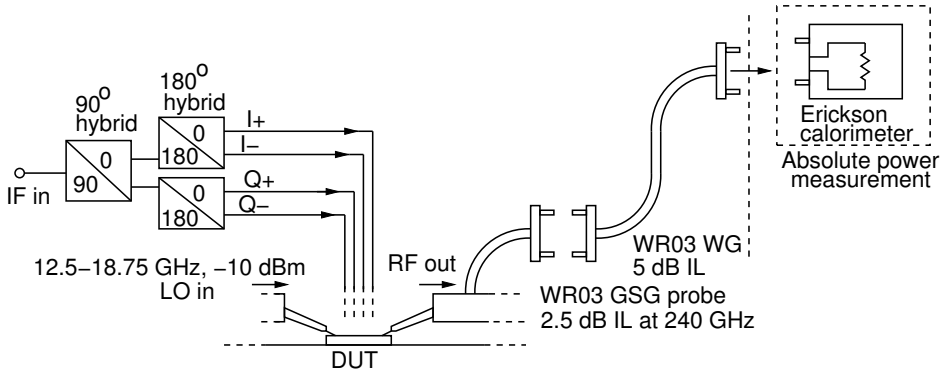


Figure 4.10: Measurement setup for the on-wafer characterization of the 240 GHz Tx. A GSG probe (DC-40 GHz) with a 2.9 mm K-connector is used to couple the external LO signal to the chip. A WR03 GSG probe is used at the Tx output.

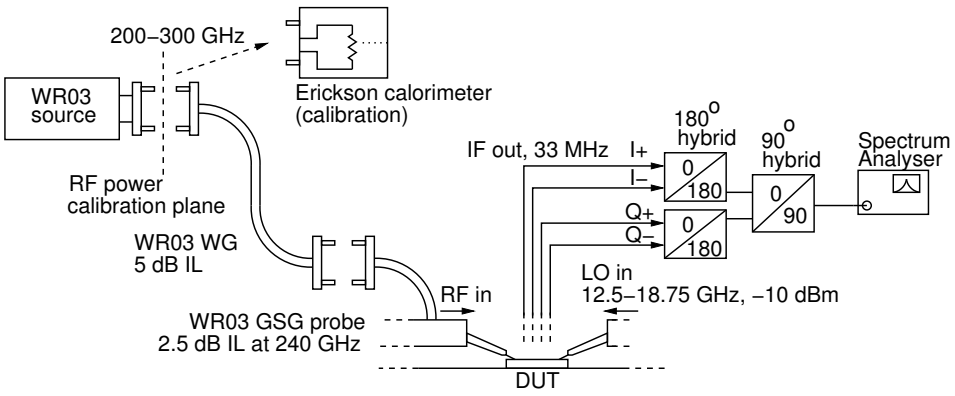
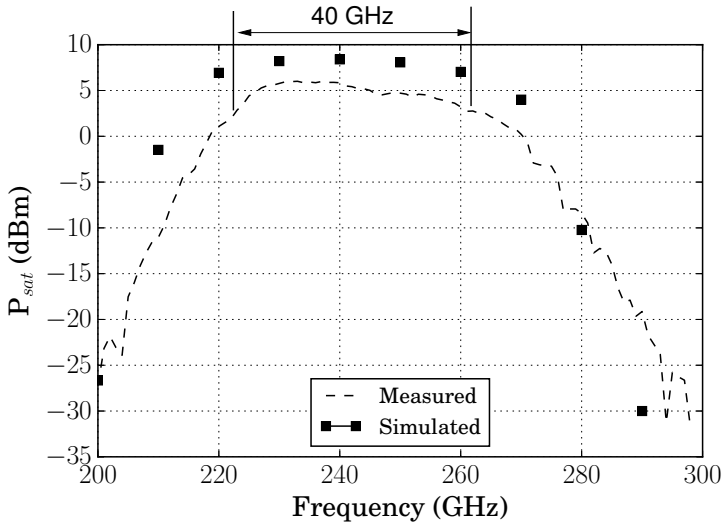


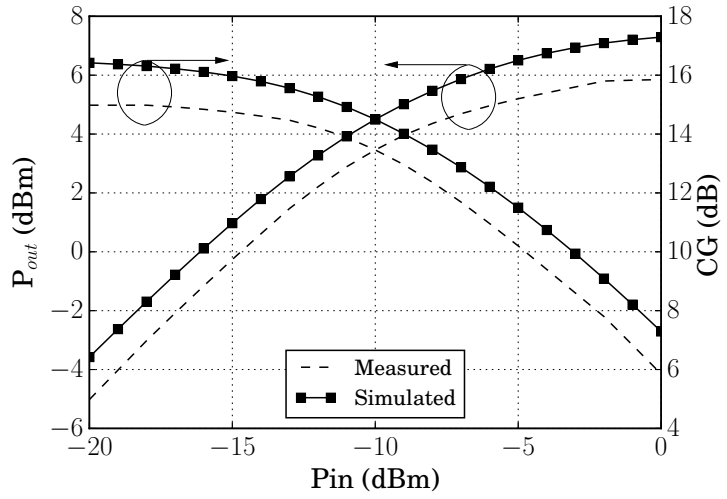
Figure 4.11: Measurement setup for the on-wafer characterization of the Rx. A GSG probe (DC-40 GHz) with a 2.9 mm K-connector is used to couple the external LO signal to the chip. A WR03 GSG probe is used at the Rx input.

Figure 4.12a shows the on-wafer hardware correlation for the large-signal bandwidth characterization of the 240 GHz Tx. The measured P_{sat} at 240 GHz is 6 dBm, and the 3-dB large-signal bandwidth is 40 GHz (223-263 GHz). The input IF power is -5 dBm for this measurement. At 240 GHz, the measured IP_{1dB} is -11 dBm and OP_{1dB} is 3 dBm as shown in Figure 4.12b.

Figure 4.13a shows the on-wafer hardware correlation for the small-signal bandwidth characterization of the 240 GHz Rx. The peak CG is 13.5 dB at 228 GHz, and the corresponding single-sideband (SSB) NF is 15 dB. From 230-240 GHz, a 2.5 dB notch is seen in the passband which is not expected from simulations. The average peak gain is 11 dB from 220-240 GHz, and hence the 3-dB RF bandwidth is 28 GHz (218-246 GHz). The SSB NF is calculated from the measured conversion gain, and the output noise floor is determined based on the direct method described in [7, 180]. At 240 GHz, the measured IP_{1dB} of the Rx is -17 dBm as shown in Figure 4.13b. In the simulations, EM simulated models of the balun and tuned pads are included, and HICUM/L2 [150] model for the HBTs are used.

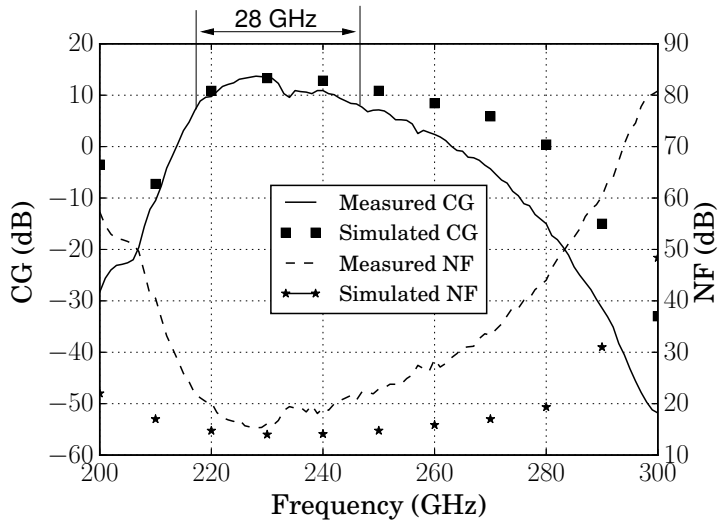


(a)

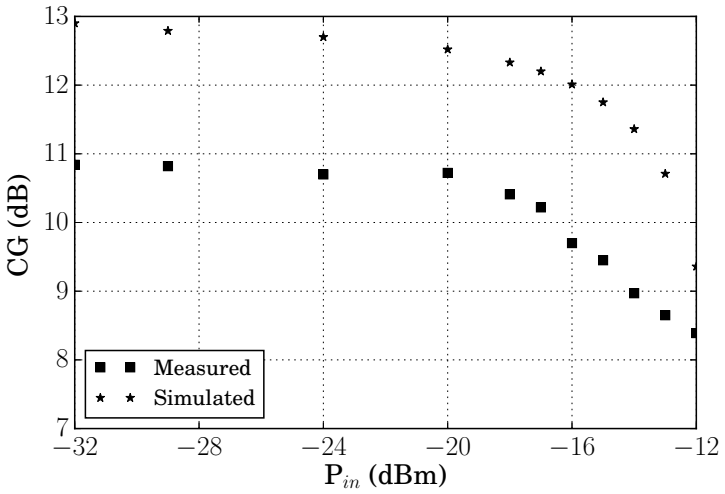


(b)

Figure 4.12: Hardware correlation for the on-wafer large-signal bandwidth and linearity characterization of the 240 GHz Tx. a) The measured P_{sat} at 240 GHz is 6 dBm, and the 3-dB large-signal bandwidth is 40 GHz (223-263 GHz). b) At 240 GHz, the measured IP_{1dB} is -11 dBm and OP_{1dB} is 3 dBm.



(a)



(b)

Figure 4.13: Hardware correlation for the on-wafer bandwidth and linearity characterization of the 240 GHz Rx. a) The peak CG is 13.5 dB at 228 GHz, and the minimum SSB NF is 15 dB. From 220-240 GHz, the average peak gain is 11 dB, and hence the 3-dB RF bandwidth is 28 GHz (218-246 GHz). b) Linearity characterization: At 240 GHz, the measured IP_{1dB} is -17 dBm.

4.3.2 Free-space RF characterization of the 240 GHz Tx and Rx chipset

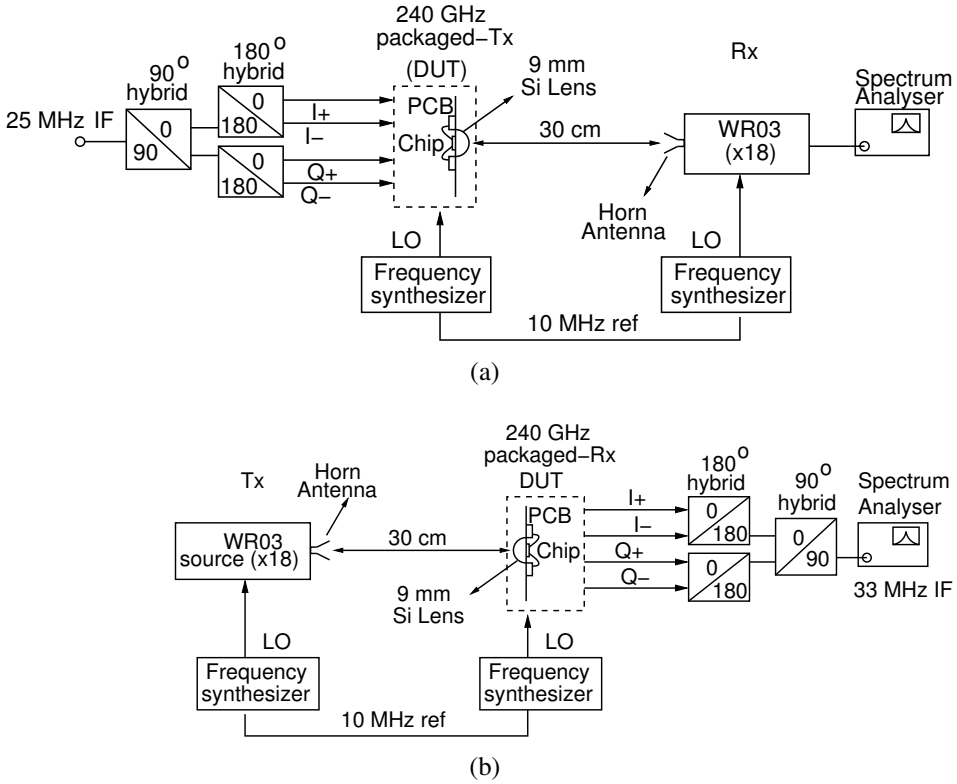


Figure 4.14: Measurement setup for the free-space RF characterization of the 240 GHz Tx and Rx over a 30 cm wireless link. a) Tx: A pre-calibrated WR03 VNA extension module with an external horn-antenna with WR3.4 waveguide interface is used as the Rx. b) Rx: A pre-calibrated WR03 VNA extension module with an external horn-antenna with WR3.4 waveguide interface is used as the Tx.

In this section, the results from the free-space RF characterization of the 240 GHz packaged-Tx and 240 GHz packaged-Rx are presented. For these measurements, the range is 30 cm which is twice the far-field distance [186] of 12.9 cm at 240 GHz. Figure 4.14a shows the measurement setup for the 240 GHz packaged-Tx. A WR03 VNA extension module in the receive mode is used as the Rx to measure the down-converted signal using a spectrum analyzer. The accurate conversion gain of this module is known from prior calibration. This module is mounted with an external corrugated horn-antenna with WR3.4 waveguide interface. The external 90° and 180° hybrids are used for single-sideband modulation from an external IF signal at 25 MHz (-5 dBm). From the received power P_{RX}, the transmitted power P_{TX} can be estimated using the Friis transmission equation given by the equation 4.1. Here R is the distance, D_{TX} is the directivity of the Tx antenna and A_r is the aperture of the Rx

antenna [186] given by $A_r = \frac{\lambda^2}{4\pi D_{RX}}$.

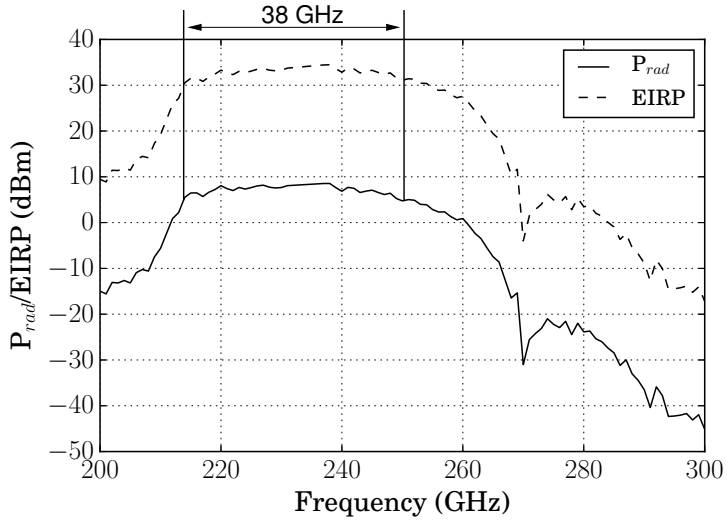
$$P_{TX} = \frac{P_{RX} \times (4\pi R^2)}{D_{TX} \times A_r} \tag{4.1}$$

The measured D_{TX} is 26.4 dBi at 240 GHz as shown in Figure 4.17. From the data-sheet, directivity of the Rx antenna D_{RX} is 20 dBi at 270 GHz. Hence, the directivities at other frequencies can be extrapolated using the equation 4.2.

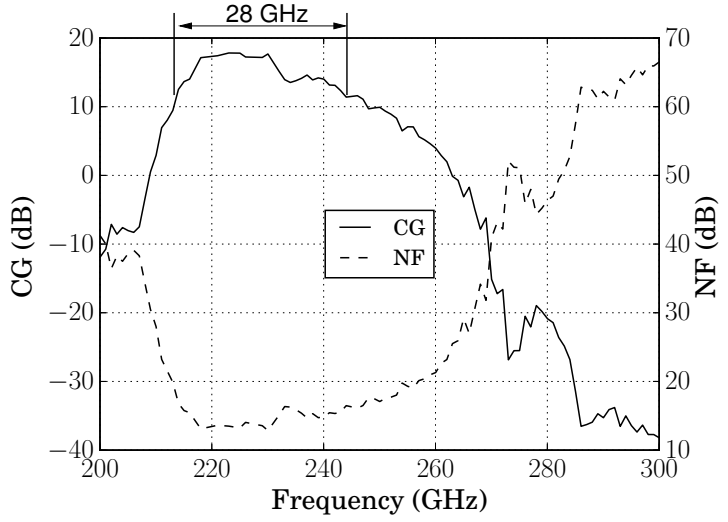
$$D_{f_2} = D_{f_1} \times (\frac{f_2}{f_1})^2 \tag{4.2}$$

Figure 4.14b shows the measurement setup for the 240 GHz packaged-Rx. The WR03 VNA extension module with an external horn-antenna is used as Tx in this case. The output power of this module is measured before using an Erickson calorimeter. For this measurement, an IF frequency of 33 MHz is chosen due to measurement setup limitations. For the Rx, the IF outputs are combined using external 90° and 180° hybrids. For calculating P_{RX} using the equation 4.1, A_r is assumed to be $\frac{\pi D^2}{4}$ where D is the lens diameter. This is based on the assumption that the Tx illuminates the entire circular cross-section of the lens antenna [19]. From P_{RX}, CG can be calculated and SSB NF can be accurately estimated [7, 180] as discussed in section 4.3.1.

Figure 4.15a shows the results from the large-signal RF bandwidth characterization of the 240 GHz packaged-Tx in free-space. At 238 GHz, the peak radiated power (P_{rad}) is 8.5 dBm, EIRP is 34.8 dBm, and the 3-dB RF bandwidth is 38 GHz (214-252 GHz). Figure 4.15b shows the results from the free-space characterization of the 240 GHz packaged-Rx. The peak CG is 17.8 dB at 223 GHz, and the minimum SSB NF is 13.5 dB. From 230-240 GHz, a 2.5 dB notch is seen in the passband. The average peak gain is 15 dB from 220-240 GHz, and hence the 3-dB RF bandwidth is 28 GHz (214-242 GHz).



(a)



(b)

Figure 4.15: Free-space RF characterization of the 240 GHz packaged-Tx and Rx. a) Tx: The peak P_{rad} is 8.5 dBm, and EIRP is 34.8 dBm at 238 GHz. The 3-dB bandwidth is 38 GHz (214-252 GHz). b) Rx: The peak CG is 17.8 dB at 223 GHz, and the minimum SSB NF is 13.5 dB. The average peak gain is 15 dB from 220-240 GHz, and hence the 3-dB RF bandwidth is 28 GHz (214-242 GHz).

4.3.2.1 Antenna radiation pattern measurement

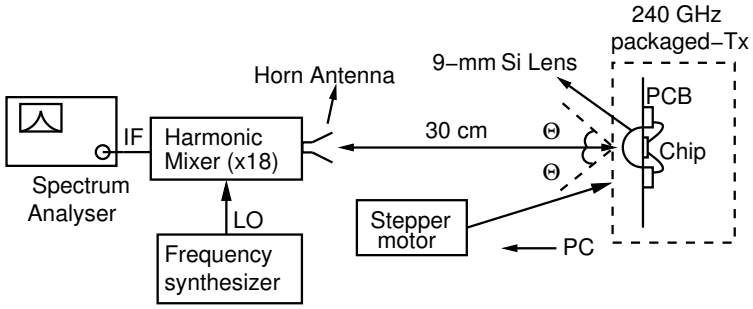


Figure 4.16: Setup for the measurement of the antenna radiation pattern of the 240 GHz packaged-Tx. A 2-D rotational stage controlled by a stepper motor is used for precise alignment. An external WR03 VNA extension module is used as Rx.

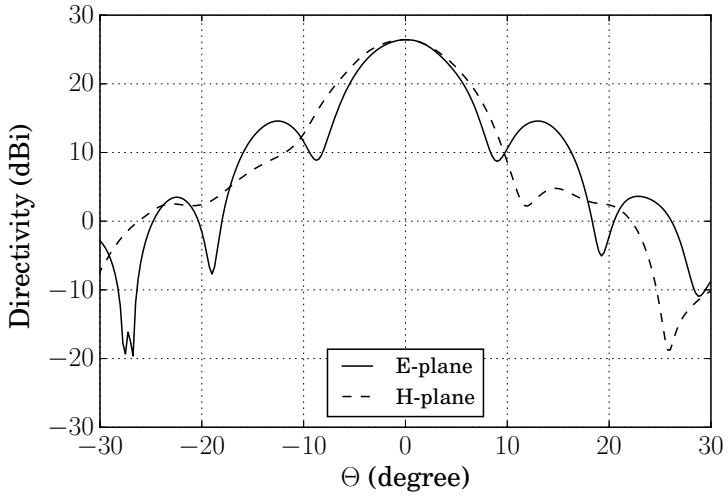


Figure 4.17: Measured directivity of the on-chip antenna of the 240 GHz packaged-Tx and Rx. The FWHP is $\pm 4^\circ$ in the E-plane and $\pm 4.5^\circ$ in the H-plane, and this yields an estimated directivity of 26.4 dBi at 240 GHz.

The radiation pattern of the 240 GHz packaged-Tx and Rx antenna is measured using a 2D-rotational stage, which is controlled by a stepper-motor for precision alignment as shown in Figure 4.16. For the 240 GHz packaged-Tx, a WR03 VNA extension module (in the receive mode) is used. The down-converted IF signal is measured using a spectrum analyzer (similar to the free-space packaged-Tx characterization). An IF frequency of 25 MHz is used for the characterization of the Tx. The distance between the Tx and Rx is 30 cm. For the 240 GHz packaged-Rx, a WR03 VNA extension module in the transmit mode is used as the source. An

IF frequency of 33 MHz is used for this measurement (similar to the free-space packaged-Rx characterization). The E-plane and H-plane cuts obtained over 30° rotation for the on-chip antenna pattern is shown in Figure 4.17. The full-width half-power (FWHP) is ±4° in the E-plane and ±4.5° in the H-plane, and this yields an estimated directivity of 26.4 dBi at 240 GHz.

4.3.3 IF bandwidth characterization of the 240 GHz chipset

For IF bandwidth characterization, the 240 GHz packaged-Tx and Rx are placed back-to-back at a distance of 90 cm as shown in Figure 4.18. The IF inputs are connected to a VNA using external 90° and 180° hybrids for single-sideband modulation. An external synthesizer feeds the external 15 GHz LO signal to the 240 GHz packaged-Tx and Rx, where it is multiplied on-chip by a factor of 16, for a carrier frequency of 240 GHz. The measured 6-dB IF bandwidth is 13 GHz as shown in Figure 4.19.

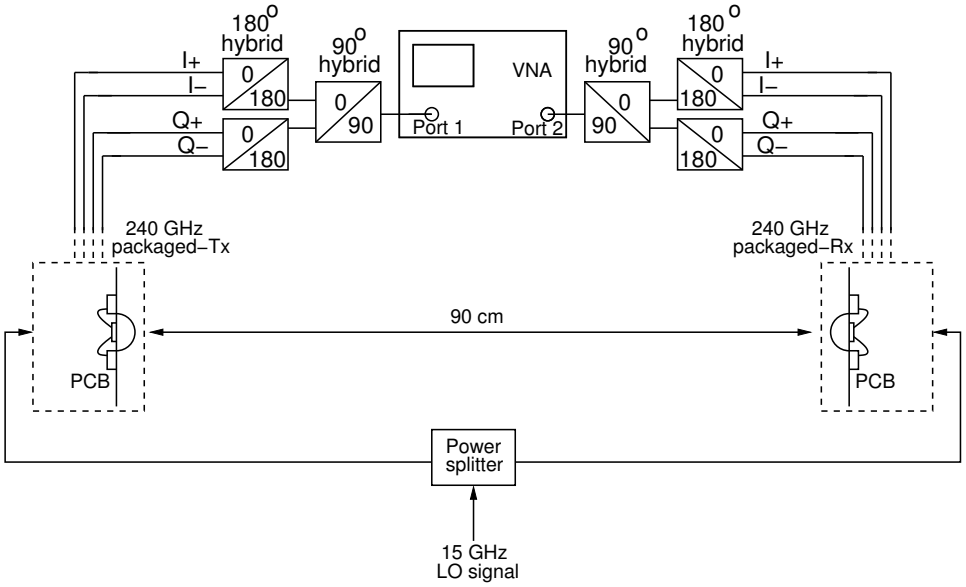


Figure 4.18: Measurement setup for the IF bandwidth characterization of the 240 GHz packaged-Tx and Rx chipset. The Tx and Rx are placed back-to-back over a 90 cm distance. The IF inputs are connected to a VNA using external 90° and 180° hybrids for single-sideband modulation.

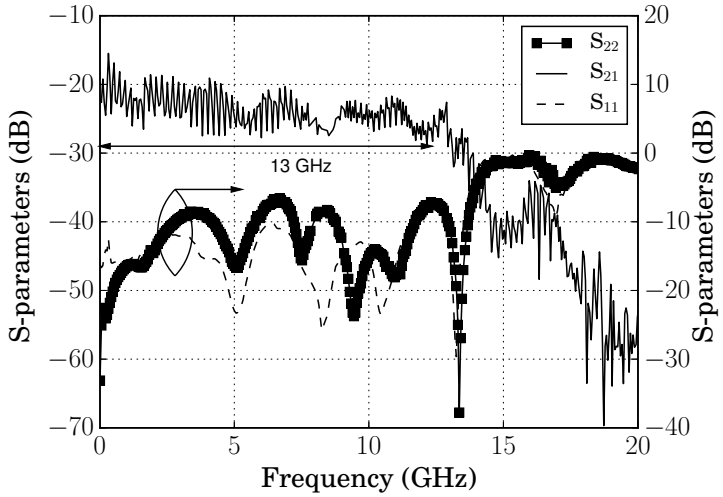


Figure 4.19: Measurement results from the IF bandwidth characterization at a carrier frequency of 240 GHz. This measurement is performed over a wireless link of 90 cm, and the 6-dB IF bandwidth is 13 GHz.

4.3.4 Conclusion

Table 4.1 summarizes the results from the on-wafer and free-space characterization of the 240 GHz quadrature Tx and Rx chipset. From the free-space measurement of the 240 GHz packaged-Tx, the measured output power is higher in the case of free-space measurements in comparison to the on-wafer measurements. For the Rx, CG is higher and NF is lower for free-space measurements in comparison to on-wafer measurements. This discrepancy is due to the lower losses in the antenna as compared to the on-chip balun. Also, the loading effect due to the balun and the on-chip antenna is different. The simulated differential input impedance of the antenna is close to 100 Ω from 200-300 GHz [7]. Figure 4.20 shows the simulated differential input impedance for a 50 Ω load termination at the single ended output of the Marchand-balun (used for on-wafer measurements). From 200-300 GHz, the input impedance is complex and the real part varies from 75-80 Ω. This difference in loading due to the balun and on-chip antenna contributes further to the discrepancy between the on-chip and free-space measurement results.

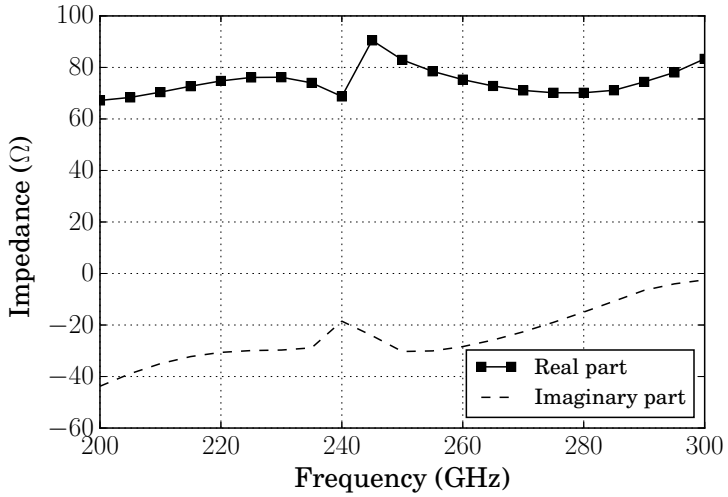


Figure 4.20: Simulated differential input impedance for a 50 Ω load termination at the single-ended output of the Marchand-balun. From 200-300 GHz, the input impedance is complex and the real part varies from 75-80 Ω.

Table 4.1: Summary of the on-wafer and free-space characterization of the 240 GHz Tx and Rx chipset

Tx	On-chip	Free-space
P_{sat}/P_{rad} (dBm)	6@240 GHz	8.5@238 GHz
EIRP (dBm)	-	34.8
3-dB BW (GHz)	223-263 (40 GHz)	214-252 (38 GHz)
OP_{1dB} (dBm)	3@240 GHz	-
PDC (W)	1.28	1.28
Antenna directivity (dBi)	-	26.4@240 GHz
Rx	**On-chip**	**Free-space**
peak CG (dB)	13.5@228 GHz	17.5@223 GHz
3-dB RF bandwidth (GHz)	218-246 GHz (28)[1]	214-242 GHz (28)[2]
minimum SSB NF (dB)	15	13.5
IP_{1dB} (dBm)	-17@240 GHz	-
DC power consumption (W)	1.105	1.105
Antenna directivity (dBi)	-	26.4@240 GHz
	On-chip	**Free-space**
IF-bandwidth (GHz)	-	13^{+} (measured at the RF carrier frequency of 240 GHz)

[1] Average peak gain of 11 dB from 220-240 GHz
[2] Average peak gain of 15 dB from 220-240 GHz
$^{+}$ 6 dB back-to-back IF bandwidth

4.4 240 GHz ultra-high data-rate wireless communication

The RF and IF bandwidth characterization results from the fully-integrated wideband 240 GHz quadrature Tx and Rx chipset were presented in the previous sections. In this section, the results from a high data-rate communication system at 240 GHz is presented.

4.4.1 Link-budget and modulation scheme

The modulation schemes with higher spectral efficiency allow a larger number of bits to be transmitted for a given RF bandwidth. However, the linearity requirements on the RF front-end for complex and efficient modulation schemes are stringent. Hence, the Tx needs to be operated in the backed-off mode. The back-off levels depend on the modulation scheme and the required EVM [187]. The back-off operation results in the reduction of the maximum range particularly when the peak output power is limited (typically the case at sub-mmWave frequencies). In contrast, simple modulation schemes like OOK, BPSK and other constant envelope schemes allow the Tx to be operated in saturation. Hence, the choice of an appropriate modulation scheme is a trade-off between the maximum data-rate and range.

The minimum detectable signal in dBm (MDS_{dBm}) at the Rx can be calculated using the equation 4.3 [164].

$$MDS_{dBm} = -174 + 10 \times log(Bandwidth) + NF + SNR_{min} \tag{4.3}$$

Here, SNR_{min} is the minimum signal-to-noise ratio and depends on the bit-error-rate (BER) requirements for a given modulation scheme. For establishing a communication link, the received power P_{RX} must be greater than MDS_{dBm}. As discussed in [136], the respective Tx output power back-off levels for 16-QAM and 64-QAM modulation schemes are 6.5 dB and 7.6 dB. These assumptions are based on root-raised-cosine (RRC) filtering with a roll-off factor of 0.35. The required SNR_{min} for a BER of 10^{-6} for QPSK, 16-QAM and QPSK modulation schemes are 14 dB, 20 dB and 25 dB respectively. The P_{RX} in dBm can be calculated using the Friis equation [186].

$$P_{Rx} = P_{Tx} + G_{TX} + G_{Rx} + 20 \times log10(\frac{\lambda}{4\pi R}) \tag{4.4}$$

Based on the parameters of the 240 GHz Tx and Rx chipset in Table 4.1, the maximum estimated range for the different modulation schemes is shown in Figure 4.21. For QPSK modulation, the maximum range is 6.2 m. For 16-QAM and 64-QAM modulation scheme, the maximum range is 1.4 m and 0.8 m respectively. For QPSK modulation scheme, the Tx

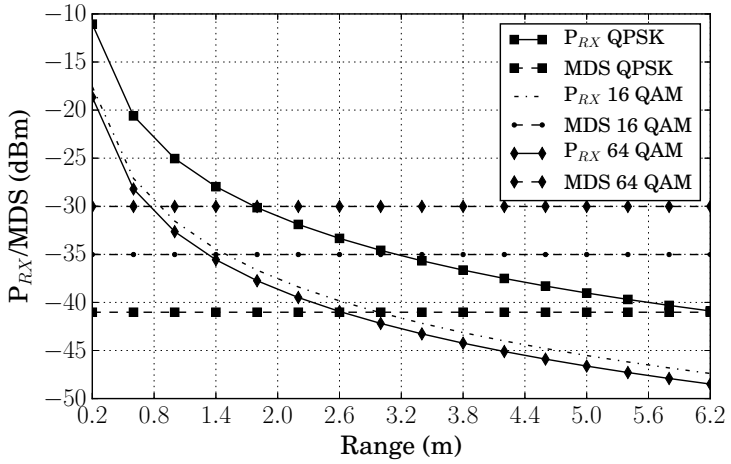


Figure 4.21: Simulated maximum range for a high data-rate communication system using the 240 GHz packaged-Tx and Rx chipset for different modulation schemes. For a BER of 10^{-6}, the maximum estimated range for QPSK modulation is 6.2 m, for 16-QAM it is 1.4 m, and for 64-QAM it is 0.8 m.

output power is assumed to be 3 dBm (corresponding to OP_{1dB}). For high directive point to point links, the link performance is sensitive to misalignment between the Tx and Rx. In this estimation, it is assumed that the Tx and Rx are perfectly aligned and no loss-margin is considered. Also, the back-off levels are conservative numbers. In reality, the back-off levels can be relaxed further based on the EVM requirements and error-correction methodology used in signal processing.

4.4.2 240 GHz wireless communication data-rate measurements

Figure 4.22 shows the measurement setup for the high data-rate communication system using the fully-integrated 240 GHz quadrature Tx and Rx chipset for a wireless link of 70 cm. The differential IF inputs of the Tx are connected to an arbitrary-wave-generator (AWG), and IF outputs of the Rx are connected to a real-time oscilloscope using phase-matched cables. The IF inputs are ac-coupled using precision dc-blocks operating from 0-65 GHz. The dc-blocks have flat group-delay characteristics up to 40 GHz. The external LO input for the Tx and Rx is driven by the same external synthesizer using a power splitter. For this measurement, PRBS9 data is used as the input data stream at the IF input of the Tx and the IF power level is -5 dBm. At the transmit and the receive side, root-raised-cosine (RRC) filtering with a roll-off factor of 0.35 is used for pulse shaping.

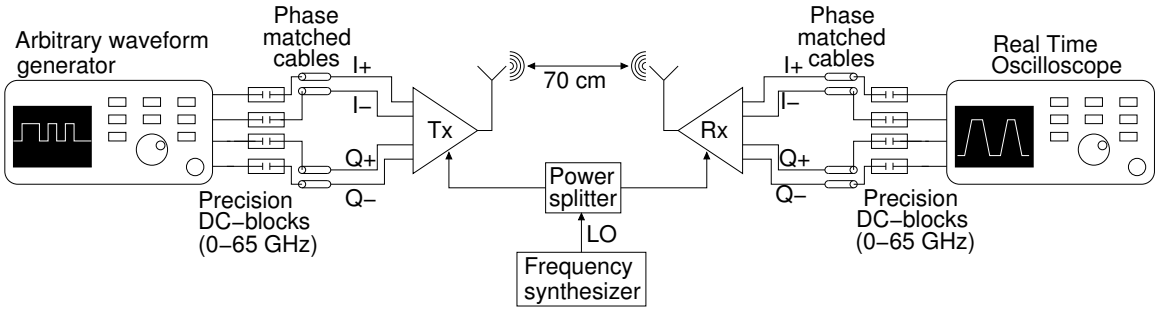


Figure 4.22: Measurement setup for the 240 GHz high data-rate communication system for a wireless link of 70 cm. An AWG is used to feed the Tx IF input with PRBS9 data, and the IF outputs of the Rx are connected to a real-time oscilloscope.

4.4.2.1 Measurement results for BPSK modulation scheme

Figure 4.23 shows the eye-diagram for BPSK modulation scheme at different data-rates. The measured rms EVM is 16% at 10 Gbps, 17.8% at 15 Gbps, 24% at 20 Gbps and 30% at 25 Gbps. As data-rate increases from 15 to 25 Gbps, EVM drops sharply from 17.8% to 30% since the IF bandwidth of the PCB is limited to 13 GHz. These results are raw-data without any IF cable compensation, channel equalization and pre-distortion.

4.4.2.2 Measurement results for QPSK modulation scheme

Figure 4.24 shows the eye-diagram for QPSK modulation scheme at different data-rates. The measured rms EVM is 15% at 17 Gbps, 17% at 20 Gbps and 24% at 24 Gbps. The 240 GHz Tx and Rx chipset do not have clock recovery circuitry, which makes it prone to the effects of phase misalignment between the Tx and Rx LO. The LO phase misalignment results in cross-talk between the I and Q channels. For this measurement, the limitation due to LO phase misalignment is tackled by manually changing the LO-feed path length from the splitter to the Tx and Rx LO. However, this is not a precise approach and repeatability is challenging especially at high data-rates. This is one of the bottlenecks in measuring data-rates beyond 24 Gbps for QPSK modulation scheme.

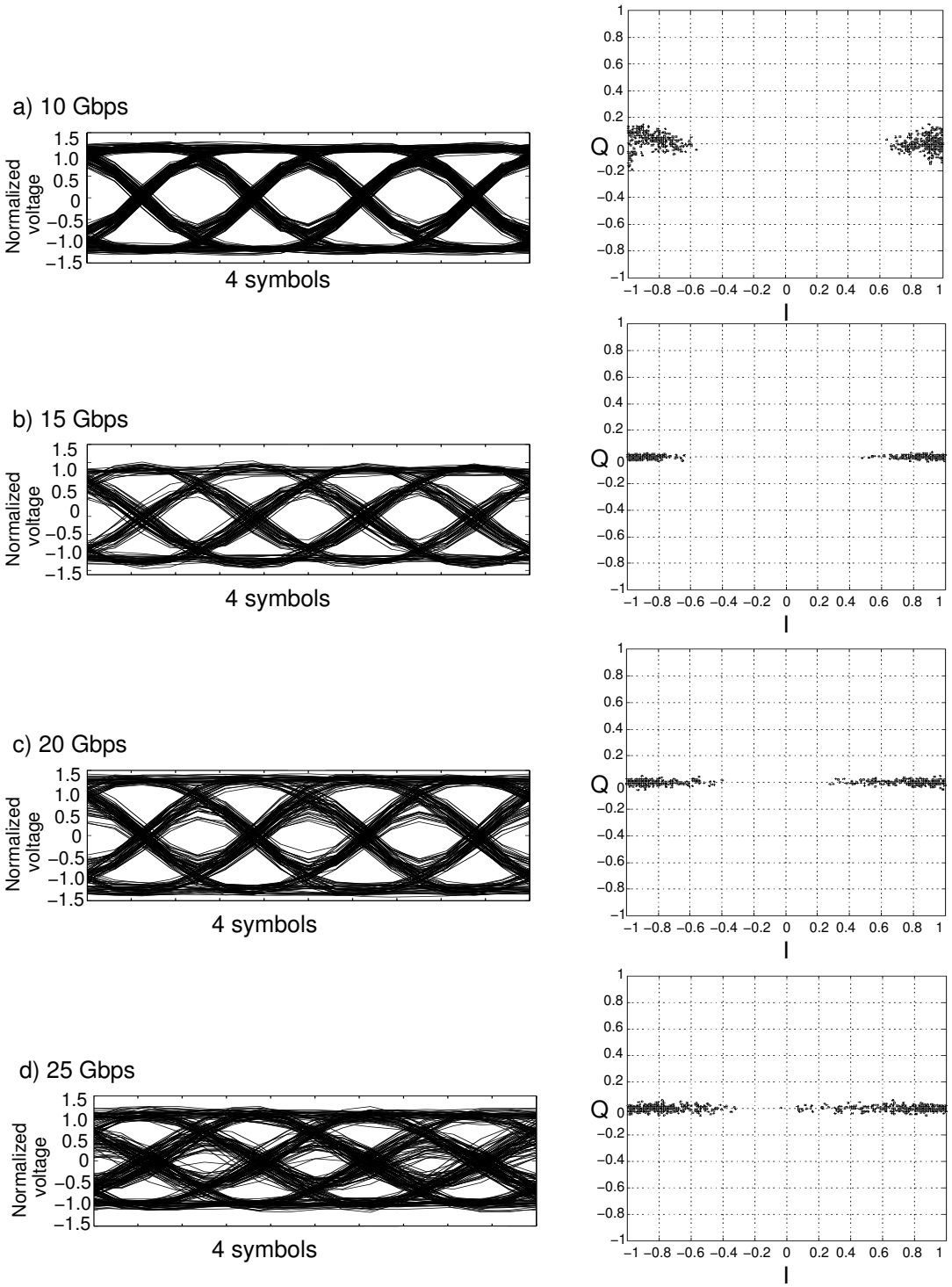


Figure 4.23: Eye-diagram and constellation for BPSK modulation scheme at a carrier frequency of 240 GHz. The measured rms EVM is a) 16% at 10 Gbps, b) 17.8% at 15 Gbps, c) 24% at 20 Gbps and d) 30% at 25 Gbps.

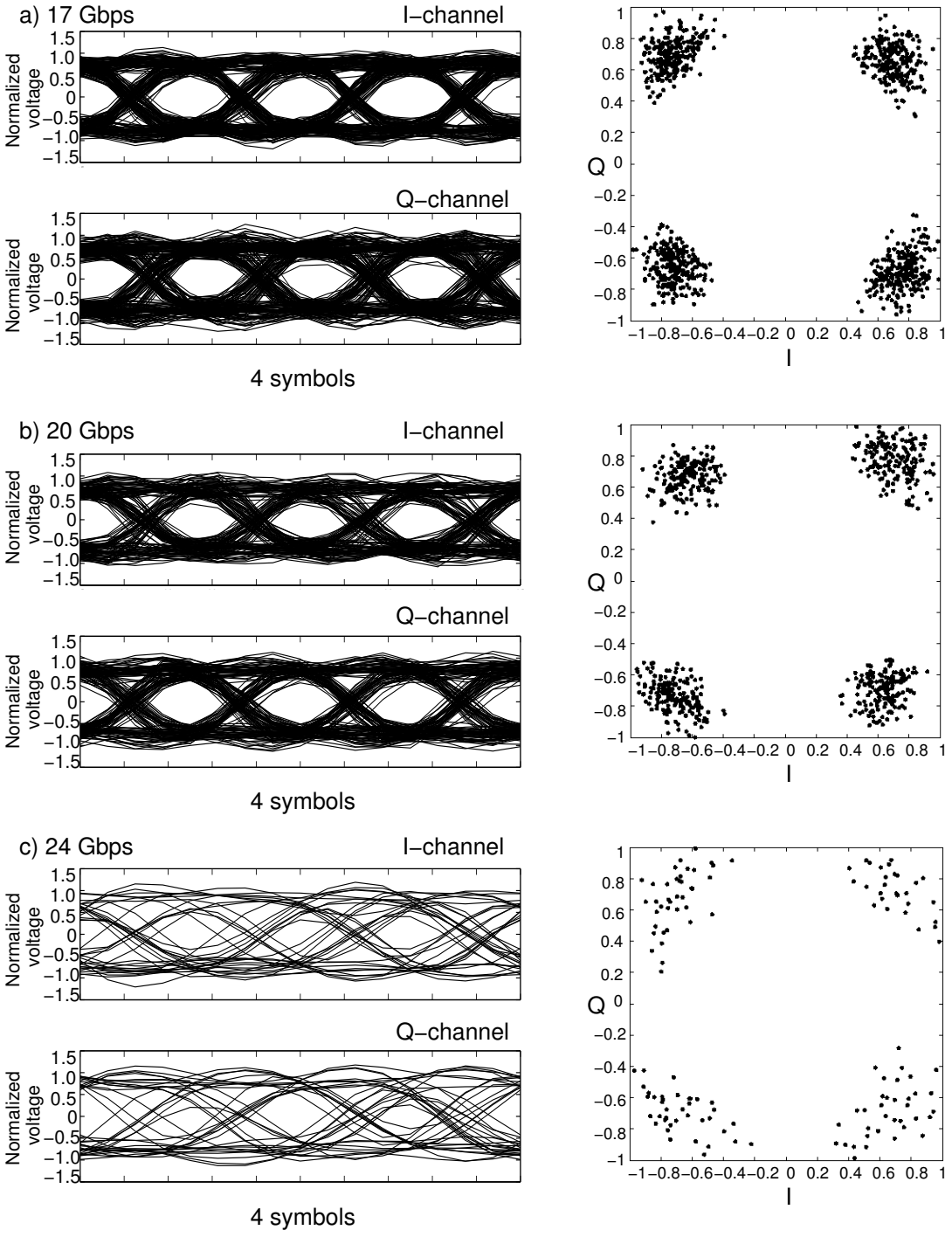


Figure 4.24: Eye-diagram and constellation diagram for QPSK modulation scheme at a carrier frequency of 240 GHz. The measured rms EVM is a) 15.7% at 17 Gbps, b) 17% at 20 Gbps and c) 24% at 24 Gbps.

4.4.2.3 Summary of the data-rate measurements

Table 4.2 summarizes the results of the 240 GHz high data-rate communication system presented in this thesis. These results are without any IF cable compensation, channel equalization and pre-distortion.

For the estimation of BER, SNR can be calculated from EVM using the expression $SNR \approx (\frac{1}{EVM})^2$ [188]. From the SNR, BER can be estimated based on the standard E_b/N_o curve with the assumption of additive white Gaussian channel noise [187]. Based on this consideration, SNR greater than 10 dB is required for an estimated BER less than 10^{-8} for BPSK modulation scheme. For the 240 GHz communication system presented in this thesis, this condition is satisfied up to a data-rate of 25 Gbps for BPSK modulation scheme. For QPSK modulation scheme, SNR greater than 15 dB is required for an estimated BER less than 10^{-8}. For the 240 GHz communication system presented in this thesis, this condition is satisfied up to a data-rate of 20 Gbps for QPSK modulation scheme. The measured SNR at a data-rate of 24 Gbps for QPSK modulation scheme is 12.4 dB, and hence the estimated BER is lower than 10^{-5} in this case.

The estimation of BER above is based only on the assumption of additive white Gaussian channel noise. In practice, BER would increase further due to the different other non-idealities. By using forward-error-correction (FEC), BER can be significantly reduced. For applying 3^{rd} order FEC, the required minimum BER threshold is 4.5×10^{-3} towards achieving a corrected BER lower than 10^{-15} with an overhead of 7% [189].

Table 4.2: Summary of the 240 GHz communication system

Modulation scheme	Data-rate (Gbps)	Baud-rate (Gbaud/s)	EVM (rms in %)	SNR (dB)	Estimated BER
BPSK	10	10	16	15.9	$<10^{-8}$
	15	15	17.8	15	$<10^{-8}$
	20	20	24	12.4	$<10^{-8}$
	25	25	30	10.4	$<10^{-8}$
QPSK	17	8.5	15.7	16.1	$<10^{-8}$
	20	10	17	15.4	$<10^{-8}$
	24	12	24	12.4	$<10^{-5}$

4.4.3 Conclusion

In this chapter, the RF and IF characterization results from a wideband fully-integrated 240 GHz quadrature Tx and Rx chipset are presented. A high data-rate communication system using this chipset is demonstrated. Table 4.3 compares the result from this work with others reported in the literature from 200-325 GHz. In [6, 8–10], Tx and Rx chipsets with integrated on-chip antennas for high data-rate communication have been demonstrated. However, the maximum range is limited to a distance of 1-3 cm. This mostly limits their usability for chip-to-chip communication or near-field communication. Recently, a Tx chip at 300 GHz is reported in [71] which is capable of supporting 32-QAM, but the output power is only -14.5 dBm. Moreover, it is only a Tx implementation with no on-chip antennas, and no real wireless link is demonstrated.

The chipset presented in this work has the highest output power and RF bandwidth among all the other Tx and Rx implementations in the 200-325 GHz frequency range in silicon technologies. Also, record data-rates were demonstrated over a wireless link of 70 cm (limited by measurement setup). The estimated maximum range for QPSK modulation scheme using this chipset is 6.2 m. The data rates reported in this work are raw-data. The maximum data-rate can be significantly increased by compensating for the IF cables, channel equalization, pre-distortion and other error-correction techniques. For III-V technology based Tx and Rx implementations reported in the literature, data rates up to 64 Gbps have been reported at 240 GHz over a wireless link of 850 m in [13]. However, it is based on the bulky split-block waveguide modules, and the maximum output power is only -4.5 dBm and external antennas with 50 dBi gain are used. Also, the f_{max} for the III-V technology used for this implementation is 1 THz, and the frequency of operation is close to $f_{max}/4$. In comparison, the frequency of operation for the 240 GHz Tx and Rx chipset presented in this thesis is close to $f_{max}/2$, and yet the performance is significantly better.

Table 4.3: Tx and Rx chips in the 220-325 GHz range reported in the literature

Tech	Freq, BW (GHz)	LO arch	Tx P_{rad}, EIRP, OP_{1dB} (dBm)	Rx CG, NF (dB)	App Data rate (Gbps)	Ref	On-chip antenna	Note
130-nm SiGe	240, Tx 40 Rx 28	x16	8.5, 35.8, 3	15, 15	Comm 24, QPSK 25, BPSK	This work [11]	yes	0.7 m link
40-nm CMOS	275-305, -	x3	-14.5, -, -	-	Comm 17.5×6^3 32-QAM	[71]	no	Tx only, on-wafer
65-nm CMOS	240	VCO +x3	0, 1, -	25, 15	Comm 16, QPSK	[9, 10]	yes	1-2 cm link
65-nm CMOS	254	push-push VCO	-4.8, -, -	- -	10, OOK	[190]	no	Tx only on-wafer
32-nm CMOS	210, >14	Fund VCO	-, 5.13, -	18, 11	10, OOK	[6]	yes	3.2 cm link
65-nm CMOS	260	VCO +x4	-, 5, -	17, 19	Comm 10, OOK	[8]	yes	40 mm range
130-nm SiGe	220, 30 320, 13	sub-harmonic (x9)	-	16, 18 -14, 36	Imaging Comm	[180]	no	Rx only
130-nm SiGe	240, 40	External LO	-	18, 18	Comm	[191]	no	Rx only
130-nm SiGe	314	push-push VCO	-8, -, -	-22.5, 19.5	-	[85]	yes	-
III-V implementations								
250-nm InP HBT	300, Tx 18 Rx 20	Fund VCO	-2.3, -, -	26, 16	-	[192]	no	-
mHEMT	240, 64	x6	-4.5, -, -	-,11	Comm 64, QPSK	[13]	no	850m link

Chapter 5

Conclusion and future outlook

This thesis addressed the various circuit design challenges and system level considerations for the realization of fully-integrated wideband Tx and Rx chipset towards sub-mmWave frequencies in SiGe BiCMOS technologies. In the first part of the thesis, the focus was on the challenges at the individual circuit building-blocks of the RF front-end. The particular emphases are on the aspects of wideband operation, and high RF power generation. At frequencies of operation close to $f_{max}/2$, the limited MAG does not leave enough room for gain-bandwidth trade off. Hence, the implementation of wideband high gain amplifiers requires optimum interstage matching networks. Another significant impediment is the limited output power of PAs, which severely limits the maximum range of wireless links towards sub-mmWave frequencies. The output power is limited due to the low output impedance (at resonance), which makes it challenging to couple the output power to the load. In this thesis, the special considerations for loadline matching of PAs towards sub-mmWave frequencies are presented for the first time. Additionally, power combination techniques for PAs were explored. Based on these considerations, a 4-stage wideband PA at 240 GHz was implemented with a small-signal gain of 26 dB, a 3-dB bandwidth of 28 GHz, and a record peak output power of 7.5 dBm (without power combination). This PA has the best FoM among all the other silicon-based implementations above 200 GHz at the time of writing this thesis. In this design, the capacitor-coupled LC resonator based bandwidth enhancement technique is used. Also, power combination for PAs above 200 GHz was demonstrated for the first time in a silicon technology with a peak output power of 9.6 dBm (record number) at 215 GHz. Another key challenge addressed in this thesis was the implementation of a high-power wideband tunable LO source. A wideband tunable LO gives the chipset a generic attribute, which makes it suited for applications requiring a fixed (communication) or a wideband tunable LO (FMCW RADAR, imaging, and material characterization). A 240 GHz LO signal source based on a frequency multiplier-based topology ($\times$16) with a peak output power of 6 dBm, and a 3-dB RF bandwidth of 50 GHz

was presented. This circuit was optimized to operate from low input RF power (-10 dBm), and dc-power consumption was minimized to 0.74 W. The LO signal source can be used as a high-power standalone source, and also it can be used to drive sub-harmonic receivers at 480 GHz with an overall bandwidth of 100 GHz. This source can also be used for wideband power generation at sub-mmWave frequencies by cascading non-linear stages at the output. Furthermore, the design of 240 GHz up-conversion and down-conversion mixers optimized for high RF and IF bandwidth were presented.

In the second part of this thesis, the system level and packaging aspects for the implementation of a fully integrated direct-conversion 240 GHz quadrature Tx and Rx chipset in a compact form-factor were presented. The Tx and Rx chipset were integrated with wideband on-chip antennas designed to be used with an external replaceable silicon lens for backside radiation. The ability to mount external silicon lens in the case of backside radiation gave the ability to have flexible application specific directivities by varying the lens size. Also, it reduced the size of the on-chip antenna due to the high dielectric constant of silicon. The chip-lens assembly was integrated into a low-cost PCB based on the Rogers 4350B material. For wideband IF matching, stepped impedance microstrip-line based low-pass filters were implemented on the PCB, and the overall IF bandwidth is 13 GHz. The packaged chipset was used to demonstrate a high data-rate communication system at 240 GHz over a wireless link of 70 cm. For QPSK and BPSK modulation schemes, the maximum measured data-rates using this chipset are 24 Gbps and 25 Gbps respectively. At the time of writing this thesis, this is the highest data-rate reported in the literature for fully-integrated wireless systems operating above 200 GHz in silicon technologies.

Hence, the results presented in this work contribute further in establishing silicon-based wideband, fully-integrated, compact and low-cost systems as a viable alternative to the existing III-V based systems towards sub-mmWave frequencies.

5.1 Recommendations for future work

In this section, some recommendations for further performance enhancement and frequency upscaling of the 240 GHz fully-integrated quadrature Tx and Rx chipset (presented in this thesis) are briefly summarized.

- For future versions of the 240 GHz Tx and Rx chipset, on-chip integration of a 12.5-18.75 GHz frequency synthesizer should be considered to circumvent the need for external synthesizers, and make the implementation completely independent.
- For making the 240 GHz Tx and Rx chipset well-suited for robust and real-time communication links, RF carrier recovery techniques like Costas-loop should be incorporated on-chip.
- For the direct-conversion topology, LO leakage and I/Q imbalance results in the deterioration of the signal constellation, and consequently it degrades the EVM further. For future versions of the 240 GHz Tx and Rx chipset, on-chip integration of analog and digital calibration techniques should be investigated to circumvent these limitations.
- The mismatch in the wire-bond used to connect the chip to the PCB introduces asymetry in the differential IF inputs of the chip. Hence, for future versions of the 240 GHz Tx and Rx chipset, on-chip active baluns should be integrated for a single-ended IF interface from the chip to the PCB.
- A QPSK transmitter at 720 GHz can be implemented by just adding a frequency tripler ($\times 3$) at the output of the 240 GHz PA in the Tx, and by frequency upscaling of the on-chip 240 GHz antenna. Although, a $\times 3$ frequency multiplication of a QPSK signal results in some amount of signal corruption due to the increased PM distortion, the overall constellation is still preserved. At the Rx side, the wideband 240 GHz LO signal source can be used to pump a sub-harmonic mixer for heterodyne detection. Hence, a 720 GHz Tx and Rx chipset with more than 100 GHz RF bandwidth can be implemented by making these modifications.

References

[1] T. H. Lee, "Terahertz electronics: The last frontier," *European Solid State Device Research Conference*, pp. 30–34, 2014.

[2] U. R. Pfeiffer, and E. Oejefors, "A 600-GHz CMOS focal-plane array for terahertz imaging applications," *European Solid-State Circuits Conf.*, pp. 110–113, 2008.

[3] M. J. Fitch, and R. Osiander, "Terahertz waves for communications and sensing," *Johns Hopkins APL technical digest*, vol. 25, no. 4, pp. 348–355, 2004.

[4] S. P. Voinigescu, A. Tomkins, E. Dacquay, P. Chevalier, J. Hasch, A. Chantre, and B. Sautreuil, "A Study of SiGe HBT Signal Sources in the 220-330 GHz Range," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2011–2021, 2013.

[5] Y. Kawano, H. Matsumura, S. Shiba, M. Sato, T. Suzuki, Y. Nakasha, T. Takahashi, K. Makiyama, and N. Hara, "230-240 GHz, 30 dB Gain Amplifier in INP-HEMT for Multi-10 Gb/s Data Communication Systems," *IEEE Compound Semicond. IC Symp.*, pp. 1–4, Oct 2013.

[6] Z. Wang, P. Chiang, P. Nazari, C. Wang, Z. Chen, and P. Heydari, "A CMOS 210-GHz fundamental transceiver with OOK modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, 2014.

[7] N. Sarmah, J. Grzyb, K. Statnikov, S. Malz, P. R. Vazquez, W. Foerster, B. Heinemann, and U. R. Pfeiffer, "A Fully Integrated 240-GHz Direct-Conversion Quadrature Transmitter and Receiver Chipset in SiGe Technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 562–574, Feb 2016.

[8] J. Park, S. Kang, S. V. Thyagarajan, E. Alon, and A. M. Niknejad, "A 260 GHz fully integrated CMOS transceiver for wireless chip-to-chip communication," *Symposium on VLSI Circuits (VLSIC)*, vol. 2, pp. 48–49, Jun. 2012.

[9] S. Kang, S. V. Thyagarajan, and A. M. Niknejad, "A 240 GHz Fully Integrated Wideband QPSK Transmitter in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2256–2267, Oct 2015.

[10] S. V. Thyagarajan, S. Kang, and A. M. Niknejad, "A 240 GHz Fully Integrated Wideband QPSK Receiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2268–2280, Oct 2015.

[11] N. Sarmah, P. R. Vazquez, J. Grzyb, W. Foerster, B. Heinemann, and U. R. Pfeiffer, "A Wideband Fully Integrated SiGe Chipset for High Data Rate Communication at 240 GHz," *"European Microwave Integr. Circuits Conf."*, October 2016.

[12] D. Lopez-Diaz, A. Tessmann, A. Leuther, S. Wagner, M. Schlechtweg, O. Ambacher, S. Koenig, J. Antes, F. Boes, F. Kurz, R. Henneberger, and I. Kallfass, "A 240 GHz quadrature receiver and transmitter for data transmission up to 40 Gbit/s," *"European Microwave Integr. Circuits Conf."*, pp. 440–443, Oct 2013.

[13] I. Kallfass, F. Boes, T. Messinger, A. Tobias, J. Antes, A. Inam, U. Lewark, A. Tessmann, H. Axel, and R. Henneberger, "64 Gbit/s Transmission over 850 m Fixed Wireless Link at 240 GHz Carrier Frequency," *Int. Conf. on Infrared, Millimeter, and Terahertz Waves*, vol. 36, no. 2, pp. 221–233, 2015.

[14] J. Grzyb, K. Statnikov, N. Sarmah, and U. R. Pfeiffer, "A wideband 240 GHz lens-integrated circularly polarized on-chip annular slot antenna for a FMCW radar transceiver module in SiGe technology," *Microwave and Optoelectronics Conference (IMOC)*, pp. 1–4, Nov 2015.

[15] K. Statnikov, J. Grzyb, N. Sarmah, S. Malz, B. Heinemann, and U. R. Pfeiffer, "A 240-GHz circularly polarized FMCW radar based on a SiGe transceiver with a lens-coupled on-chip antenna," *International Journal of Microwave and Wireless Technologies*, vol. FirstView, pp. 1–9, 7 2015.

[16] K. Statnikov, E. Oejefors, J. Grzyb, P. Chevalier, and U. R. Pfeiffer, "A 0.32 THz FMCW radar system based on low-cost lens-integrated SiGe HBT front-ends," *European Solid-State Circuits Conf.*, pp. 81–84, 2013.

[17] T. Jaeschke, C. Bredendiek, and N. Pohl, "3D FMCW SAR Imaging based on a 240 GHz SiGe Transceiver Chip with Integrated Antennas," *German Microwave Conference*, pp. 1–4, March 2014.

[18] T. Jaeschke, M. Vogt, C. Baer, C. Bredendiek, and N. Pohl, "Improvements in distance measurement and SAR-imaging applications by using ultra-high resolution mm-wave FMCW radar systems," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1–3, Jun. 2012.

[19] R. Al Hadi, H. Sherry, J. Grzyb, Y. Zhao, W. Forster, H. M. Keller, A. Cathelin, A. Kaiser, and U. R. Pfeiffer, "A 1 k−pixel video camera for 0.7−1.1 terahertz imaging applications in 65-nm cmos," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2999–3012, 2012.

[20] K. Statnikov, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "160-GHz to 1-THz Multi-Color Active Imaging With a Lens-Coupled SiGe HBT Chip-Set," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 520–532, 2015.

[21] U. R. Pfeiffer, Y. Zhao, J. Grzyb, R. A. Hadi, N. Sarmah, W. Foerster, H. Ruecker, and B. Heinemann, "A 0.53 THz reconfigurable source module with up to 1 mW radiated power for diffuse illumination in terahertz imaging applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2938–2950, 2014.

[22] J.-S. Rieh, S. Jeon, and M. Kim, "An overview of integrated THz electronics for communication applications," *IEEE International Midwest Symposium on Circuits and Systems*, pp. 1–4, 2011.

[23] R. Lachner, "Towards 0.7 Terahertz Silicon Germanium Heterojunction Bipolar Technology–The DOTSEVEN Project," *ECS Transactions*, vol. 64, no. 6, pp. 21–37, 2014.

[24] H. Rucker, B. Heinemann, and A. Fox, "Half-Terahertz SiGe BiCMOS technology," *IEEE SiRF Tech. Dig.*, pp. 133–136, Jan 2012.

[25] M. Xiaobing, W. Yoshida, M. Lange, J. Lee, J. Zhou, L. Po−Hsin, K. Leong, A. Zamora, J. Padilla, S. Sarkozy, R. Lai, and W.R. Deal, "First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process," *IEEE Electron Device Letters*, vol. 36, no. 4, pp. 327–329, April 2015.

[26] P. Molchanov, S. Gupta, K. Kim, and K. Pulli, "Short−range FMCW monopulse radar for hand-gesture sensing," *IEEE Radar Conference (RadarCon)*, pp. 1491–1496, 2015.

[27] R. Lachner, "Industrialization of mmWave SiGe technologies: Status, future requirements and challenges," *IEEE SiRF Tech. Dig.*, pp. 105–107, Jan 2013.

[28] R. Hartley, "Transmission of information," *Bell System technical journal*, vol. 7, no. 3, pp. 535–563, 1928.

[29] E. Oejefors, J. Grzyb, Y. Zhao, B. Heinemann, B. Tillack, and U. R. Pfeiffer, "A 820GHz SiGe chipset for terahertz active imaging applications," *IEEE Int. Solid-State Circuits Conf.*, pp. 224–226, Feb 2011.

[30] O. Momeni, "A 260GHz amplifier with 9.2dB gain and -3.9dBm saturated power in 65nm CMOS," *IEEE Int. Solid-State Circuits Conf.*, pp. 140–141, Feb 2013.

[31] A. Tang, N. Chahat, and E. Decrossas, "CMOS THz communication links for wireless applications: Where do they fit into mobile access and fixed access?" *Int. Conf. on Infrared, Millimeter, and Terahertz Waves*, pp. 1–2, Sept 2014.

[32] I. F. Akyildiz, J. M. Jornet, and C. Han, "Terahertz band: Next frontier for wireless communications," *Physical Communication*, vol. 12, pp. 16–32, 2014.

[33] I. F. Akyildiz, D. M. Gutierrez-Estevez, R. Balakrishnan, and E. Chavarria-Reyes, "LTE-Advanced and the Evolution to Beyond 4G (B4G) Systems," *Physical Communication*, vol. 10, pp. 31–60, Mar. 2014.

[34] D. A. Kirkpatrick, "The Deep Sub-micron Signal Integrity Challenge," *Proceedings of the 1999 International Symposium on Physical Design*, pp. 4–7, 1999.

[35] S. Abadal, E. Alarcon, A. Cabellos-Aparicio, M. Lemme, and M. Nemirovsky, "Graphene-enabled wireless communication for massive multicore architectures," *IEEE Communications Magazine*, vol. 51, no. 11, pp. 137–143, November 2013.

[36] I. Akyildiz and J. M. Jornet, "The Internet of nano-things," *IEEE Wireless Communications*, vol. 17, no. 6, pp. 58–63, December 2010.

[37] I. Sarkas, J. Hasch, A. Balteanu, and S. P. Voinigescu, "A Fundamental Frequency 120-GHz SiGe BiCMOS Distance Sensor With Integrated Antenna," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 795–812, March 2012.

[38] L. Maurer, G. Haider, and H. Knapp, "77 GHz SiGe based bipolar transceivers for automotive radar applications – An industrial perspective," *New Circuits and Systems Conference*, pp. 257–260, June 2011.

[39] F. Dielacher, M. Tiebout, R. Lachner, H. Knapp, K. Aufinger, and W. Sansen, "SiGe BiCMOS technology and circuits for active safety systems," *International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, pp. 1–4, April 2014.

[40] A. Stelzer, E. Kolmhofer, and S. Scheiblhofer, "Fast 77 GHz chirps with direct digital synthesis and phase locked loop," *Asia Pacific Microwave Conf.*, vol. 3, Dec 2005.

[41] Dietmar Kissinger, *Millimeter-wave receiver concepts for 77 GHz automotive radar in silicon-germanium technology*. Springer Science & Business Media, 2012.

[42] M. Skolnik, *Radar Handbook*, ser. Electronics electrical engineering. McGraw-Hill Education, 2008.

[43] I. V. Komarov, and S. M. Smolskiy , *Fundamentals of Short-range FM Radar*, ser. Artech House radar library. Artech House, 2003.

[44] P. Siegel *et al.*, "Terahertz technology," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 910–928, 2002.

[45] A. K. Huhn, E. Saenz, P. de Maagt, and P. H. Bolivar, "Broadband terahertz analysis of energetic materials−influence of crystal structure and additives," *IEEE Trans. on Terahertz Science and Technology*, vol. 3, no. 5, pp. 649–655, 2013.

[46] M. Tonouchi, "Cutting-edge terahertz technology," *Nature photonics*, vol. 1, no. 2, pp. 97–105, 2007.

[47] K. H. Jin, Y-G. Kim, S. H. Cho, J. C. Ye, C. Jong, and Dae-Su. Yee, "High-speed terahertz reflection three-dimensional imaging for nondestructive evaluation," *Optics express*, vol. 20, no. 23, pp. 25 432–25 440, 2012.

[48] L. Gilreath, V. Jain, Y. Hsin−Cheng, L. Zheng, and P. Heydari, "A 94-GHz passive imaging receiver using a balanced LNA with embedded Dicke switch," *IEEE Radio Freq. Integr. Circuits Symp.*, pp. 79–82, May 2010.

[49] S. Koch, M. Guthoerl, I. Kallfass, P. Leuther, and S. Saito, "A 120−145 GHz Heterodyne Receiver Chipset Utilizing the 140 GHz Atmospheric Window for Passive Millimeter-Wave Imaging Applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 1961–1967, Oct 2010.

[50] B. Ferguson, and X.C. Zhang, "Materials for terahertz science and technology," *Nature materials*, vol. 1, no. 1, pp. 26–33, 2002.

[51] D. H. Auston, "Picosecond optoelectronic switching and gating in silicon," *Applied Physics Letters*, vol. 26, no. 3, pp. 101–103, 1975.

[52] F. Hindle, A. Cuisset, R. Bocquet, and G. Mouret, "Continuous-wave terahertz by photomixing: applications to gas phase pollutant detection and quantification," *Comptes Rendus Physique*, vol. 9, no. 2, pp. 262 – 275, 2008.

[53] B. S. Williams, "Terahertz quantum-cascade lasers," *Nature photonics*, vol. 1, no. 9, pp. 517–525, 2007.

[54] T. Anbinderis, P. Anbinderis, A. V. Usoris, P. Bagdonaite, E. Prusakova, I. Kasalynas, E. Sirmulis, D. Seliuta, and G. Valusis, "Waveguide-based calorimeter for terahertz frequency range," *Electronics Letters*, vol. 43, no. 14, July 2007.

[55] G. N. Goltsman, and D. N. Loudkov, "Terahertz Superconducting Hot-Electron Bolometer Mixers and Their Application in Radio Astronomy," *Radiophysics and Quantum Electronics*, vol. 46, no. 8, pp. 604–617.

[56] X. Galiano, A.J. Kreisler, V.S. Jagtap, and A.F. Degardin, "Fast pyroelectric response of semiconducting Y-Ba-Cu-O detectors with high IR sensitivity," *Int. Conf. on Infrared, Millimeter, and Terahertz Waves*, pp. 1–3, Sept 2013.

[57] L. O. T. Fernandes, P. Kaufmann, R. Marcon, A. S. Kudaka, A. Marun, R. Godoy, E.C. Bortolucci, M. B. Zakia, and J. A. Diniz, "Photometry of THz radiation using Golay cell detector," *General Assembly and Scientific Symposium*, pp. 1–4, Aug 2011.

[58] S. Kohjiro, K. Kikuchi, M. Maezawa, T. Furuta, A. Wakatsuki, N. Shimizu, T. Nagatsuma, Y. Kado, H. Ito, and A. Shoji, "A $0.2-0.5$ THz heterodyne receiver based on a photonic local oscillator and a superconductor-insulator-superconductor mixer," *Int. Conf. on Infrared, Millimeter, and Terahertz Waves*, pp. 1–2, Sept 2008.

[59] Jia Du, "HTS Josephson junction devices for microwave and terahertz applications," *International Conference on Applied Superconductivity and Electromagnetic Devices (ASEMD)*, pp. 113–117, Dec 2011.

[60] J. H. Booske, R. J. Dobbs, C. D. Joye, C. L. Kory, G. R. Neil, P. Gun−Sik, P. Jaehun, and R. J. Temkin, "Vacuum Electronic High Power Terahertz Sources," *IEEE Trans. on Terahertz Science and Technology*, vol. 1, no. 1, pp. 54–75, Sept 2011.

[61] L. A. Samoska, "An Overview of Solid-State Integrated Circuit Amplifiers in the Submillimeter-Wave and THz Regime," *IEEE Trans. on Terahertz Science and Technology*, vol. 1, no. 1, pp. 9–24, Sept 2011.

[62] J. Tucek, D. Gallagher, K. Kreischer, and R. Mihailovich, "A compact, high power, 0.65 THz source," *International Vacuum Electronics Conference*, pp. 16–17, April 2008.

[63] A.A. Borisov, U.A. Budzinsky, S.V. Bykovsky, A.V. Galdetskiy, A.N. Korolev, M.I. Lopin, A.A. Negirev, V.I. Pugnin, and G.V. Ruvinsky, "The development of vacuum microwave devices in Istok," *International Vacuum Electronics Conference*, pp. 437–438, Feb 2011.

[64] QL Liu, ZC Wang, PK Liu, CH Du, HQ Li, and AY Xu, "A THz Backward-Wave Oscillator Based on a Double-Grating Rectangular Waveguide," *IEEE Int. Electron Devices Meeting*, vol. 60, no. 4, pp. 1463–1468, April 2013.

[65] T. Watanabe, K. Akagawa, Y. Tanimoto, D. Coquillat, W. Knap, and T. Otsuji, "Terahertz imaging with InP high-electron-mobility transistors," *Proc. SPIE*, vol. 8023, 2011.

[66] S. Koenig, D. Hillerkuss, and J. Leuthold, "Wireless sub-THz communication system with high data rate enabled by RF photonics and active MMIC technology," *IEEE Photonics Conference (IPC)*, pp. 414–415, 2014.

[67] P. S. Chakraborty, A. S. Cardoso, B. R. Wier, A. P. Omprakash, J. D. Cressler, M. Kaynak, and B. Tillack, "A 0.8 THz f_{max} SiGe HBT Operating at 4.3 K," *IEEE Electron Device Letters*, vol. 35, no. 2, pp. 151–153, Feb 2014.

[68] E. Johnson, "Physical limitations on frequency and power parameters of transistors," *IRE International Convention Record*, vol. 13, pp. 27–34, 1966.

[69] J. Scholvin, D. R. Greenberg, and A. del Alamo Jesus, "Performance and limitations of 65 nm CMOS for integrated RF power applications," *IEEE Int. Electron Devices Meeting*, pp. 369–372, 2005.

[70] S. Hu, Y. Z. Xiong, B. Zhang, L. Wang, T. G. Lim, M. Je, and M. Madihian, "A SiGe BiCMOS Transmitter/Receiver Chipset With On-Chip SIW Antennas for Terahertz Applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2654–2664, Nov 2012.

[71] K. Katayama, K. Takano, S. Amakawa, S. Hara, A. Kasamatsu, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "A 300 GHz 40nm CMOS transmitter with 32-QAM 17.5Gb/s/ch capability over 6 channels," *IEEE Int. Solid-State Circuits Conf.*, pp. 342–343, Jan 2016.

[72] K. Statnikov, J. Grzyb, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A lens-coupled 210-270 GHz circularly polarized FMCW radar transceiver module in SiGe technology," *European Microw. Conf.*, pp. 550–553, Sept 2015.

[73] T. Jaeschke, C. Bredendiek, and N. Pohl, "A 240 GHz ultra-wideband FMCW radar system with on-chip antennas for high resolution radar imaging," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1–4, 2013.

[74] E. Oejefors, and U. R. Pfeiffer, "A 650 GHz SiGe receiver front-end for terahertz imaging arrays," *IEEE Int. Solid-State Circuits Conf.*, pp. 430–431, Feb 2010.

[75] N. Sarmah, B. Heinemann, and U.R. Pfeiffer, "A 246 GHz fundamental source with a peak output power of 2.8 dBm," *"European Microwave Integr. Circuits Conf."*, pp. 184–187, Sept 2015.

[76] J. Grzyb, Y. Zhao, and U. R. Pfeiffer, "A 288-GHz Lens-Integrated Balanced Triple-Push Source in a 65-nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1751–1761, July 2013.

[77] K. Schmalz, J. Borngraeber, W. Debski, P. Neumaier, R. Wang and, H.W. Huebers, "Tunable 500 GHz transmitter array in SiGe technology for gas spectroscopy," *Electronics Letters*, vol. 51, no. 3, pp. 257–259, 2015.

[78] K. Schmalz, J. Borngraeber, W. Debski, P. Neumaier, R. Wang, D. Kissinger, and H. W. Huebers, "Tunable 500 GHz sensor system in SiGe technology for gas spectroscopy," *Electronics Letters*, vol. 51, no. 17, pp. 1345–1347, 2015.

[79] P. D. L. Beasley, "The Influence of Transmitter Phase Noise on FMCW Radar Performance," *European Microw. Conf.*, pp. 1810–1813, Sept 2006.

[80] Y. M. Tousi, O. Momeni, and E. Afshari, "A novel CMOS high-power terahertz VCO based on coupled oscillators: Theory and implementation," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3032–3042, 2012.

[81] R. H. Derksen and H.-M. Rein, "7.3-GHz dynamic frequency dividers monolithically integrated in a standard bipolar technology," *IEEE Trans. Microw. Theory Techn.*, vol. 36, no. 3, pp. 537–541, Mar 1988.

[82] H. Knapp, T. Meister, W. Liebl, D. Claeys, T. Popp, K. Aufinger, H. Schaefer, J. Bock, S. Boguth, and R. Lachner, "Static frequency dividers up to 133 GHz in SiGe:C bipolar technology," *IEEE Bipolar/BiCMOS Circuits and Tech. Meeting*, pp. 29–32, Oct 2010.

[83] J. Al-Eryani, H. Knapp, H. Li, K. Aufinger, J. Wursthorn, S. Majied, and L. Maurer, "A 47−217 GHz dynamic frequency divider in SiGe technology," *IEEE Bipolar/BiCMOS Circuits and Tech. Meeting*, pp. 125–128, Oct 2015.

[84] B. Razavi, "A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 894–903, April 2011.

[85] S. Zeinolabedinzadeh, M. Kaynak, W. Khan, M. Kamarei, B. Tillack, J. Papapolymerou, and J. D. Cressler, "A 314 GHz, Fully-Integrated SiGe Transmitter and Receiver with Integrated Antenna," *IEEE Radio Freq. Integr. Circuits Symp.*, pp. 361–364, 2014.

[86] O. Momeni and E. Afshari, "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 583–597, March 2011.

[87] S. Shopov, J. Hasch, P. Chevalier, A. Cathelin, and S. P. Voinigescu, "A 240 GHz Synthesizer in 55nm SiGe BiCMOS," *IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 1–4, Oct 2015.

[88] N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "235−275 GHz (x16) frequency multiplier chains with up to 0 dBm peak output power and low DC power consumption," *IEEE Radio Freq. Integr. Circuits Symp.*, pp. 181–184, June 2014.

[89] K. Yuk and G. Branner, "Advances in active microwave frequency multipliers," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1–4, Aug 2011.

[90] E. Oejefors, B. Heinemann, and U. R. Pfeiffer, "Active 220− and 325− GHz Frequency Multiplier Chains in an SiGe HBT Technology," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1311–1318, 2011.

[91] H. C. Lin, and G. M. Rebeiz, "A 135-160 GHz balanced frequency doubler in 45 nm CMOS with 3.5 dBm peak power," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1–4, June 2014.

[92] J.-J. Hung, T. Hancock, and G. Rebeiz, "High-power high-efficiency sige ku- and ka-band balanced frequency doublers," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 754–761, Feb 2005.

[93] N. Sharma, W. Choi, and K. O. Kenneth, "160-310 GHz frequency doubler in 65-nm CMOS with 3-dBm peak output power for rotational spectroscopy," *IEEE Radio Freq. Integr. Circuits Symp.*, pp. 186–189, May 2016.

[94] M. Abbasi, and D. S. Ricketts, "A high−power, broadband 245−285 GHz balanced frequency doubler in 45 nm SOI CMOS," *Microwave and Optical Technology Letters*, vol. 58, no. 2, pp. 423–426, 2016.

[95] K. Nai-Chung, T. Zuo-Min, K. Schmalz, C. J. Scheytt, and H. Wang, "A 52−75 GHz frequency quadrupler in 0.25 μm SiGe BiCMOS process," *"European Microwave Integr. Circuits Conf."*, pp. 365–368, Sept 2010.

[96] Y. Wang, W. Goh, L. Wang, and Yong-Zhong Xiong, "A 9% power efficiency 121-to-137GHz phase-controlled push-push frequency quadrupler in 0.13μm SiGe BiCMOS," *IEEE Int. Solid-State Circuits Conf.*, pp. 262–264, 2012.

[97] S. Yuan and H. Schumacher, "Novel frequency quadrupler design covering the entire V-Band in 0.13 μm SiGe process," *IEEE SiRF Tech. Dig.*, pp. 101–103, Jan 2014.

[98] M. Adnan, and E. Afshari, "Efficient Microwave and Millimeter-Wave Frequency Multipliers Using Nonlinear Transmission Lines in CMOS Technology," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2889–2896, Sept 2015.

[99] H. Jia, L. Kuang, Z. Wang, and B. Chi, "A W-Band Injection-Locked Frequency Doubler Based on Top-Injected Coupled Resonator," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 1, pp. 210–218, Jan 2016.

[100] E. Monaco, M. Pozzoni, F. Svelto, and A. Mazzanti, "Injection-Locked CMOS Frequency Doublers for μ-Wave and mm-Wave Applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1565–1574, Aug 2010.

[101] S. Hara, T. Sato, R. Murakami, K. Okada, and A. Matsuzawa, "60 GHz injection locked frequency quadrupler with quadrature outputs in 65 nm CMOS process," *Asia Pacific Microwave Conf.*, pp. 2268–2271, Dec 2009.

[102] Y. Shuai, and H. Schumacher, "Compact V band frequency doubler with true balanced differential output," *IEEE Bipolar/BiCMOS Circuits and Tech. Meeting*, pp. 191–194, Sept 2013.

[103] J. Thornton, C.M. Mann, and P. de Maagt, "Optimization of a 250-GHz Schottky tripler using novel fabrication and design techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 46, no. 8, pp. 1055–1061, Aug 1998.

[104] R.J. Hwu, L.P. Sadwick, N.C. Luhmann, D.B. Rutledge, and M. Sokolich, "Highly efficient frequency triplers in the millimeter wave region incorporating a back-to-back configuration of two varactor diodes," *International Conference on Millimeter Wave and Far-Infrared Technology*, pp. 100–106, 1989.

[105] U. R. Pfeiffer, E. Oejefors, and Y. Zhao, "A SiGe quadrature transmitter and receiver chipset for emerging high-frequency applications at 160GHz," *IEEE Int. Solid-State Circuits Conf.*, pp. 416–417, Feb 2010.

[106] W. L. Chan, and J. R. Long, "A 56−65 GHz Injection-Locked Frequency Tripler With Quadrature Outputs in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2739–2746, Dec 2008.

[107] Z. Chen and P. Heydari, "An 85−95.2 GHz transformer-based injection-locked frequency tripler in 65nm CMOS," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1–1, May 2010.

[108] Y. L. Yeh, and H. Y. Chang, "A W-Band Wide Locking Range and Low DC Power Injection-Locked Frequency Tripler Using Transformer Coupled Technique," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 860–870, Feb 2013.

[109] F. Vecchi, S. Bozzola, E. Temporiti, D. Guermandi, M. Pozzoni, M. Repossi, M. Cusmai, U. Decanis, A. Mazzanti, and F. Svelto, "A Wideband Receiver for Multi-Gbit/s Communications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 551–561, March 2011.

[110] S. Shekhar, J. S. Walling, and D. J. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2424–2439, 2006.

[111] B. Analui, and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, Aug 2004.

[112] J. R. Nelson, "A Theoretical Comparison of Coupled Amplifiers with Staggered Circuits," *Proceedings of the Institute of Radio Engineers*, vol. 20, no. 7, pp. 1203–1220, July 1932.

[113] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave filters, impedance-matching networks, and coupling structures*, ser. Artech House microwave library. McGraw-Hill, 1964, no. Bd. 1.

[114] N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 135-170 GHz power amplifier in an advanced SiGe HBT technology," *IEEE Radio Freq. Integr. Circuits Symp.*, pp. 287–290, June 2013.

[115] M. Motoyoshi, R. Fujimoto, K. Takano, and M. Fujishima, "140GHz CMOS amplifier with group delay variation of 10.2 ps and 0.1 dB bandwidth of 12GHz," *IEICE Electronics Express*, vol. 8, no. 14, pp. 1192–1197, 2011.

[116] S. William, "Thermionic valve circuit," Dec 1940, US Patent 2,226,255.

[117] E. Ginzton, W. Hewlett, J. Jasberg, and J. Noe, "Distributed amplification," *Proceedings of the IRE*, vol. 36, no. 8, pp. 956–969, Aug 1948.

[118] A. Hajimiri, "Distributed integrated circuits: an alternative approach to high-frequency design," *IEEE Communications Magazine*, vol. 40, no. 2, pp. 168–173, Feb 2002.

[119] T. H. Lee, *Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits*. Cambridge University Press, 2004.

[120] H. Wu and A. Hajimiri, "Silicon-based distributed voltage-controlled oscillators," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 493–502, Mar 2001.

[121] K. Fang, C. Levy, and J. Buckwalter, "A 105-GHz, supply-scaled distributed amplifier in 90-nm SiGe BiCMOS," *IEEE Bipolar/BiCMOS Circuits and Tech. Meeting*, pp. 182–185, Oct 2015.

[122] A. Arbabian and A. M. Niknejad, "A three-stage cascaded distributed amplifier with GBW exceeding 1.5THz," *IEEE Radio Freq. Integr. Circuits Symp.*, pp. 211–214, June 2012.

[123] J. Chen and A. Niknejad, "Design and Analysis of a Stage-Scaled Distributed Power Amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1274–1283, May 2011.

[124] O. Momeni, and E. Afshari, "A Broadband mm-Wave and Terahertz Traveling-Wave Frequency Multiplier on CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2966–2976, Dec 2011.

[125] G. Gonzalez, *Microwave transistor amplifiers: analysis and design*. Prentice-Hall, 1984.

[126] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Artech House, Inc., 2006.

[127] E. Kerherve and D. Belot, *Linearization and Efficiency Enhancement Techniques for Silicon Power Amplifiers: From RF to mmW*. Elsevier, 2015.

[128] P. Song, M. A. Oakley, A. C Ulusoy, M. Kaynak, B. Tillack, G. A. Sadowy, and J. D. Cressler, "A Class-E Tuned W-Band SiGe Power Amplifier With 40.4% Power-Added

Efficiency at 93 GHz," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 10, pp. 663–665, Oct 2015.

[129] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M. T. Yang, P. Schvan, and S. P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.

[130] N. Sarmah, P. Chevalier, and U. R. Pfeiffer, "160-GHz power amplifier design in advanced SiGe HBT technologies With Psat in Excess of 10 dBm," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 939–947, 2013.

[131] P. Chevalier, F. Pourchon, T. Lacave, G. Avenier, Y. Campidelli, L. Depoyan, G. Troillard, M. Buczko, D. Gloria, D. Celi *et al.*, "A conventional double-polysilicon FSA-SEG Si/SiGe: C HBT reaching 400 GHz f_{max}," *IEEE Bipolar/BiCMOS Circuits and Tech. Meeting*, 2009.

[132] Jeffrey Lee, Chung-Chun Chen, Jen-Han Tsai, Kun-You Lin, and Huei Wang, "A 68-83 GHz power amplifier in 90 nm CMOS," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 437–440, 2009.

[133] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed active transformer-a new power-combining and impedance-transformation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 316–331, 2002.

[134] U. R. Pfeiffer, and D. Goren, "A 23-dBm 60-GHz Distributed Active Transformer in a Silicon Process Technology," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 5, pp. 857–865, May 2007.

[135] Y. Zhao, and J. R. Long, "A wideband, dual-path, millimeter-wave power amplifier with 20 dBm output power and PAE above 15% in 130 nm SiGe-BiCMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 1981–1997, 2012.

[136] D. Zhao, and P. Reynaert, "An E-band power amplifier with broadband parallel-series power combiner in 40-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 683–690, 2015.

[137] Qun Jane Gu, Zhiwei Xu, and Mau-Chung Frank Chang, "Two-way current-combining W-band power amplifier in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1365–1374, 2012.

[138] Kyu Hwan An, Ockgoo Lee, Hyungwook Kim, Dong Ho Lee, Jeonghu Han, Ki Seok Yang, Younsuk Kim, Jae Chang, Wangmyong Woo, Chang-Ho Lee, and others, "Power-combining transformer techniques for fully-integrated CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1064–1075, 2008.

[139] W. Tai, and D. S. Ricketts, "A W-band 21.1 dBm power amplifier with an 8-way zero-degree combiner in 45 nm SOI CMOS," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1–3, June 2014.

[140] W. Tai, L. R. Carley, and D. S. Ricketts, "A 0.7W fully integrated 42GHz power amplifier with 10% PAE in 0.13 μm SiGe BiCMOS," *IEEE Int. Solid-State Circuits Conf.*, pp. 142–143, Feb 2013.

[141] K. Schmalz, J. Borngraeber, W. Debski, M. Elkhouly, R. Wang, P. F. X. Neumaier, D. Kissinger, and H. W. Huebers, "245-GHz Transmitter Array in SiGe BiCMOS for Gas Spectroscopy," *IEEE Transactions on Terahertz Science and Technology*, vol. 6, no. 2, pp. 318–327, March 2016.

[142] D. M. Pozar, *Microwave Engineering, 4th Edition*. Wiley, 2011.

[143] A.M. Niknejad, M. Bohsali, E. Adabi, and B. Heydari, "Integrated circuit transmission-line transformer power combiner for millimetre-wave applications," *Electronics Letters*, vol. 43, no. 5, p. 1, 2007.

[144] A. D. Pye, and M. M. Hella, "Analysis and optimization of transformer-based series power combining for reconfigurable power amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 37–50, 2011.

[145] J. Kim, W. Kim, H. Jeon, Y. Y. Huang, Y. Yoon, H. Kim, C. H. Lee, and K. T. Kornegay, "A Fully-Integrated High-Power Linear CMOS Power Amplifier With a Parallel-Series Combining Transformer," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 599–614, March 2012.

[146] N Sarmah, K Aufinger, R Lachner, and Ullrich R. Pfeiffer, "A 200-225 GHz SiGe Power Amplifier with peak P_{sat} of 9.6 dBm using wideband power combination," *European Solid-State Circuits Conf.*, 2016.

[147] D. Chowdhury, P. Reynaert, and A. M. Niknejad, "Design Considerations for 60 GHz Transformer-Coupled CMOS Power Amplifiers," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2733–2744, Oct 2009.

[148] W. L. Chan, and J. R. Long, "A 60-GHz Band 2×2 Phased-Array Transmitter in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2682–2695, Dec 2010.

[149] S. Voinigescu, *High-Frequency Integrated Circuits*, ser. High-frequency Integrated Circuits. Cambridge University Press, 2013.

[150] M. Schroeter, and A. Chakravorty, *Compact Hierarchical Bipolar Transistor Modeling with Hicum*, ser. International series on advances in solid state electronics and technology. World Scientific, 2010.

[151] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2004.

[152] S. Malz, B. Heinemann, R. Lachner, and U. R. Pfeiffer, "J-band amplifier design using gain-enhanced cascodes in 0.13 μm SiGe," *International Journal of Microwave and Wireless Technologies*, vol. 7, no. 3-4, pp. 339–347, 2015.

[153] V. Radisic, W. R. Deal, K. Leong, X. B. Mei, W. Yoshida, P. H. Liu, J. Uyeda, A. Fung, L. Samoska, T. Gaier, and R. Lai, "A 10-mW Submillimeter-Wave Solid-State Power-Amplifier Module," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 7, pp. 1903–1909, July 2010.

[154] W. Deal, X. Mei, V. Radisic, B. Bayuk, A. Fung, W. Yoshida, P. Liu, J. Uyeda, L. Samoska, T. Gaier *et al.*, "A new sub-millimeter wave power amplifier topology using large transistors," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 8, pp. 542–544, 2008.

[155] D. Fritsche, C. Carta, and F. Ellinger, "A Broadband 200 GHz Amplifier with 17 dB Gain and 18 mW DC-Power Consumption in 0.13 μm SiGe BiCMOS," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 11, pp. 790–792, Nov 2014.

[156] K. Schmalz, J. Borngraber, Y. Mao, H. Rucker, and R. Weber, "A 245 GHz LNA in SiGe Technology," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 10, pp. 533–535, Oct 2012.

[157] S. Malz, P. Hillger, B. Heinemann, and U.R. Pfeiffer, "A 275 GHz Amplifier in 0.13μm SiGe," *"European Microwave Integr. Circuits Conf."*, October 2016.

[158] Z. Xu, Q. J. Gu, and M. C. F. Chang, "200 GHz CMOS amplifier working close to device f_T," *Electronics Letters*, vol. 47, no. 11, pp. 639–641, May 2011.

[159] D. Parveg, D. Karaca, M. Varonen, A. Vahdati, and K. A. I. Halonen, "Demonstration of a 0.325-THz CMOS amplifier," *Global Symposium on Millimeter Waves (GSMM) ESA Workshop on Millimetre-Wave Technology and Applications*, pp. 1–3, June 2016.

[160] A. Tessmann, A. Leuther, H. Massler, M. Kuri, and R. Loesch, "A Metamorphic 220-320 GHz HEMT Amplifier MMIC," *IEEE Compound Semicond. IC Symp.*, pp. 1–4, Oct 2008.

[161] V. Radisic, K. Leong, S. Sarkozy, X. Mei, W. Yoshida, PH. Liu, and R. Lai, "A 75 mW 210 GHz power amplifier module," *IEEE Compound Semicond. IC Symp.*, pp. 1–4, 2011.

[162] V. Radisic, K. Leong, S. Sarkozy, X. Mei, W. Yoshida, PH. Liu, W. R. Deal, and R. Lai, "220-GHz solid-state power amplifier modules," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2291–2297, 2012.

[163] A. Tessmann, A. Leuther, H. Massler, and M. Seelmann-Eggebert, "A high gain 600 GHz amplifier TMIC using 35 nm metamorphic HEMT technology," *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pp. 1–4, 2012.

[164] B. Razavi, *RF Microelectronics*, ser. Prentice Hall Communications Engineering and Emerging Technologies. Prentice Hall, 1998.

[165] Q. Xiao, J. L. Hesler, T. W. Crowe, B. S. Deaver, and R. M. Weikle, "A 270-GHz Tuner-Less Heterostructure Barrier Varactor Frequency Tripler," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 4, pp. 241–243, April 2007.

[166] A. Zamora, G. Mei, K. Leong, M. Lange, J. Lee, W. Yoshida, B. S. Gorospe, J. G. Padilla, and W. R. Deal, "A Submillimeter Wave InP HEMT Multiplier Chain," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 9, pp. 591–593, Sept 2015.

[167] A. Zamora, X. B. Mei, K. Leong, M. Lange, J. Lee, W. Yoshida, B. S. Gorospe, and W. R. Deal, "A $\times$18 340 GHz InP HEMT multiplier chain," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1–3, May 2015.

[168] S. Jameson, and E. Socher, "A 0.3 THz Radiating Active x27 Frequency Multiplier Chain With 1 mW Radiated Power in CMOS 65-nm," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 4, pp. 645–648, July 2015.

[169] F. Golcuk, O. D. Gurbuz, and G. M. Rebeiz, "A 0.39–0.44 THz 2x4 Amplifier-Quadrupler Array With Peak EIRP of 3–4 dBm," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4483–4491, 2013.

[170] K. Schmalz, J. Borngraeber, B. Heinemann, H. Ruecker, and C. J. Scheytt, "A 245 GHz Transmitter in SiGe Technology," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 195–198, 2012.

[171] R. Han, and E. Afshari, "A CMOS High-Power Broadband 260-GHz Radiator Array for Spectroscopy," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3090–3104, Dec 2013.

[172] S. Jameson, and E. Socher, "High Efficiency 293 GHz Radiating Source in 65 nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 7, pp. 463–465, July 2014.

[173] K. Sengupta, and A. Hajimiri, "A 0.28 THz Power-Generation and Beam-Steering Array in CMOS Based on Distributed Active Radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, Dec 2012.

[174] M. Adnan, and E. Afshari, "A 247-to-263.5GHz VCO with 2.6mW peak output power and 1.14% DC-to-RF efficiency in 65nm Bulk CMOS," *IEEE Int. Solid-State Circuits Conf.*, pp. 262–263, Feb 2014.

[175] J. Yun, D. Yoon, S. Jung, M. Kaynak, B. Tillack, and JS. Rieh, "Two 320 GHz signal sources based on SiGe HBT technology," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 3, pp. 178–180, 2015.

[176] M. Hossain, N. Weimann, B. Janke, M. Lisker, C. Meliani, B. Tillack, O. Krueger, V. Krozer, and W. Heinrich, "A 250 GHz hetero-integrated VCO with 0.7 mW output power in InP-on-BiCMOS technology," *European Microw. Conf.*, pp. 391–394, Sept 2015.

[177] M. Seo, M. Urteaga, A. Young, V. Jain, Z. Griffith, J. Hacker, P. Rowell, R. Pierson, and M. Rodwell, "$>$300GHz fixed-frequency and voltage-controlled fundamental oscillators in an InP DHBT process," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 272–275, May 2010.

[178] J. Yun, D. Yoon, H. Kim, and JS. Rieh, "300-GHz InP HBT oscillators based on common-base cross-coupled topology," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3053–3064, 2014.

[179] M. Seo, M. Urteaga, J. Hacker, A. Young, Z. Griffith, V. Jain, R. Pierson, P. Rowell, A. Skalare, A. Peralta, R. Lin, D. Lin, and M. Rodwell, "InP HBT IC Technology for

Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2203–2214, Oct 2011.

[180] E. Oejefors, B. Heinemann, and U. R. Pfeiffer, "Subharmonic 220- and 320-GHz SiGe HBT Receiver Front-Ends," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1397–1404, 2012.

[181] Behzad Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 6, pp. 428–435, 1997.

[182] J. Grzyb, H. Sherry, A. Cathelin, A. Kaiser, and U. R. Pfeiffer, "On the co-design between on-chip antennas and THz MOSFET direct detectors in CMOS technology," *Int. Conf. on Infrared, Millimeter, and Terahertz Waves*, pp. 1–3, 2012.

[183] J. Grzyb, R. A. Hadi, Y. Zhao, and U. R. Pfeiffer, "Towards room-temperature all-silicon integrated THz active imaging," *IEEE European Conference on Antennas and Propagation*, pp. 1740–1744, 2013.

[184] D. F. Filipovic, S. Member, S. S. Gearhart, S. Member, G. M. Rebeiz, and S. Member, "Double-slot antennas on extended hemispherical and elliptical silicon dielectric lenses," *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 10, pp. 1738–1749, 1993.

[185] D. F. Filipovic, G. P. Gauthier, S. Raman, and G. M. Rebeiz, "Off-axis properties of silicon and quartz dielectric lens antennas," *IEEE Transactions on Antennas and Propagation*, vol. 45, no. 5, pp. 760–766, May 1997.

[186] C. Balanis, *Antenna Theory: Analysis and Design*. John Wiley & Sons, 2005.

[187] D. Zhao and P. Reynaert, *CMOS 60-GHz and E-band Power Amplifiers and Transmitters*, ser. Analog Circuits and Signal Processing. Springer International Publishing, 2015.

[188] R. A. Shafik, M. S. Rahman, and A. R. Islam, "On the extended relationships among EVM, BER and SNR as performance metrics," *International Conference on Electrical and Computer Engineering*, pp. 408–411, 2006.

[189] F. Chang, K. Onohara, and T. Mizuochi, "Forward error correction for 100 G transport networks," *IEEE Communications Magazine*, vol. 48, no. 3, pp. S48–S55, March 2010.

[190] H. Koo, C. Y. Kim, and S. Hong, "A 254 GHz CMOS Transmitter With VCO-Q Modulation," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 6, pp. 458–460, June 2016.

[191] M. Elkhouly, Y. Mao, S. Glisic, C. Meliani, F. Ellinger, and C. J. Scheytt, "A 240 GHz Direct Conversion IQ Receiver in 0.13 μm SiGe BiCMOS Technology," *IEEE Radio Freq. Integr. Circuits Symp.*, pp. 305–308, 2013.

[192] S. Kim, J. Yun, D. Yoon, M. Kim, J. S. Rieh, M. Urteaga, and S. Jeon, "300 GHz Integrated Heterodyne Receiver and Transmitter With On-Chip Fundamental Local Oscillator and Mixers," *IEEE Trans. on Terahertz Science and Technology*, vol. 5, no. 1, pp. 92–101, Jan 2015.