Fachbereich Mathematik und Naturwissenschaften
Fachgruppe Physik
Bergische Universität Wuppertal

Development of a Detector Control System for the serially powered ATLAS pixel detector at the HL-LHC

PhD Thesis

of

Lukas Püllen

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Introduction

The ultimate goal, which scientists from all around the world are working on for several hundreds of years now, is a theory of everything. Unfortunately, this goal is far from being accomplished. Nowadays, physicists have managed to explain three of the four elemental forces, which describe the laws of physics in our universe. The understandings of these three forces, as we have it today, have mainly been contributed in the second half of the 20th century:

In 1960, for the first time, a way to unify two elemental forces (the weak- and the electromagnetic force) into one theory, was found by Sheldon Glashow. A few years later, in 1967, Steven Weinberg and Abdus Salam expanded this electroweak theory with the Higgs mechanism, forming the theory that was about to develop to the Standard Model of particle physics as we know it today. The first prediction of this theory was the existence of a neutral partner for the already discovered massive $W^{\pm}$- bosons. Several years later, this neutral partner, called the Z^0 boson, was at first discovered at CERN in 1983 in a bubble chamber experiment. With this discovery the huge triumphal procession of the Standard Model began, induced by the Nobel Price for physics in 1979 for Salam, Glashow and Weinberg. In parallel to the electroweak theory, the theory of strong interactions formed, predicting a new type of particle composing the hadrons. The large amount of particles, known to particle physics, was thereby being broken down to only a hand full of elemental bricks of matter called leptons and quarks.

Almost all of the particles, postulated by the theories mentioned above, were discovered in the following years by CERN and other laboratories. The most recently discovered particle, the Higgs particle, was detected by the experiments ATLAS and CMS at the Large Hadron Collider (LHC) located at CERN in 2012 [1, 2].

To produce and observe Higgs bosons, collider experiments with high luminosity and high energy are necessary. Hence, prior to the construction of the LHC, the Higgs boson could not be discovered, even decades after its prediction. The search for the Higgs boson was one of the main reasons for the LHC to be built (see chapter 2). The LHC is the largest ever build particle accelerator combining state of the art technology from various fields of science. With its circumference of 27 km and a magnetic field of 8 T, the LHC is able to accelerate particles to almost the speed of light and colliding them with a center of mass energy of $\sqrt{s} = 8\,\text{TeV}$. Due to the previous experiments, the mass range, in which the Higgs could be found, was limited to be above $m_H > 114.4\,\text{GeV}$[3]. Indirect searches from precision electroweak measurements excluded a Higgs-mass above $m_H > 154\,\text{GeV}$[4]. The LHC was constructed to cover

the entire range with sufficient luminosity, in order to find the Higgs boson, if it existed. In July 2012, two of the experiments at CERN announced the discovery of a particle candidate for the Higgs boson with a mass of $m_H = 126.0\,\text{GeV}$ (ATLAS) and $m_H = 125.3\,\text{GeV}$ (CMS) respectively [1, 5]. In 2013, further analysis confirmed the candidate to be the Higgs boson[2].

With the last missing part of the Standard Model being found, the LHC now focuses on studies with high energy boson-boson scattering to study electro-weak symmetry breaking mechanism and the examination of theories that go beyond the Standard Model. One of these theories is the supersymmetric Standard Model, also called SUSY. In SUSY, each known particle has a more massive super symmetric twin. The lightest of these twin particles is a hot candidate for the dark matter. The chance to find new physics in sub atomic interactions is a question of statistics. To improve the chances and increase the probability of new discoveries, there are plans to upgrade the accelerator and the experiments. These plans started already prior to the assembly of the machine itself and are executed in multiple phases. The phase 0 upgrade is currently ongoing. As part of this upgrade, the LHC will be made suitable to reach its design center of mass energy of $\sqrt{s} = 14\,\text{TeV}$ and luminosity of $L = 5 \cdot 10^{34} \frac{1}{cm^2 s}$.

In further upgrades in the years 2018 and 2024, the luminosity and energy will be increased even further. Besides the upgrades of the accelerator, the detectors are also enhanced and/or partly renewed. Due to the high radiation in the experiments, electronics age a lot faster than under normal conditions. This, and the increased luminosity of the upgraded LHC, will make a replacement of the entire inner tracker of the ATLAS experiment necessary. This thesis will focus on developments for the phase II upgrade of the innermost sub-detector of the ATLAS experiment, the pixel detector. In particular, the development of a detector control system (DCS).

Chapter 1

The Standard Model of Particle Physics

The Standard Model (SM) of particle physics describes three of four known forces in the universe. The fourth force, the gravitational force, is not covered by the Standard Model. The gravitational attraction between electron and proton in atoms, for example, is 10^{39} times weaker than the electromagnetic attraction. Therefore gravitation is commonly neglected in high energy physics.

The Standard Model is a quantum field theory. Its fundamental fields are only changeable in quantized packets, which are commonly interpreted as the particles observed in experiments. The theory of the SM has been very successful through the years since its modeling. All of the predictions made by the Standard Model could be confirmed. All predicted particles have been found, without exception. Vice versa, no particle has been found up to now, that is not part of the Standard Model.

Although the SM was able to predict particles prior to their discovery, it cannot make any assumptions about their masses. The rest mass of each particle has to be measured by experiments in high energy physics. There are also extensions of the Standard Model, which try to explain phenomena, the Standard Model cannot. Examples for these phenomena are the hierarchy problem, the question what dark matter is and the matter/anti matter asymmetry. These extensions are summarized under the term 'Beyond the Standard Model' (BSM). One famous example is the Supersymmetry, in which every particle of the Standard Model has a super symmetric twin. Though none of the super symmetric partners could be discovered, yet.

1.1 Matter

The universe, as we know it today, is made of four different fundamental particles, two leptons and two quarks. The most famous of these four is the electron, a lepton that was first discovered in 1897 by J. J. Thomson. It creates the atomic shell. The electron carries a negative electrical elemental charge ($e = -1.602 \cdot 10^{-19}\,\mathrm{As}$). The other fundamental particles are the up- and the down-quark. When combined, up and down quarks can form protons and neutrons, which make the counterpart of the electron

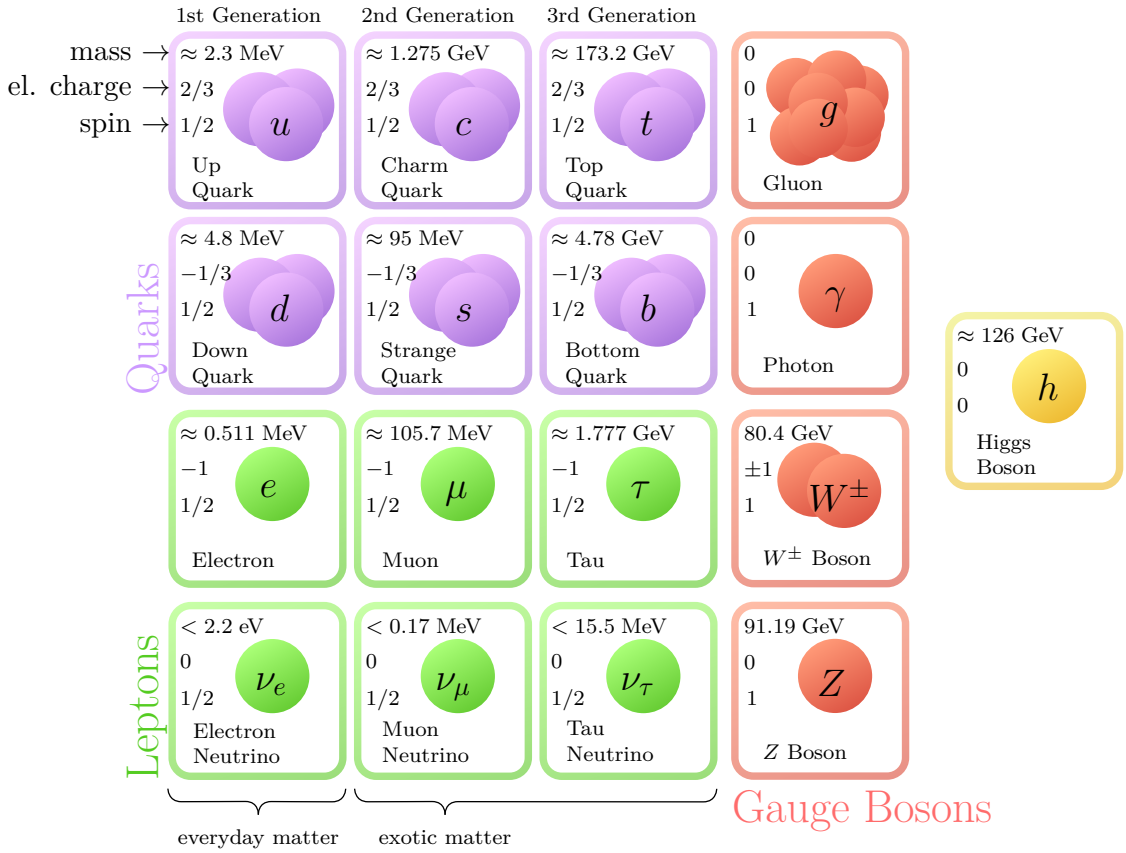


Figure 1.1: *The Standard Model of particle physics.*

inside the atoms, the nucleus. Quarks also have electrical charge, similar to the electron. The up-quark carries $\frac{2}{3}e$ and the down quark $-\frac{1}{3}e$. When summarized, this leads to one elemental charge for the proton and no electrical charge for the neutron. Together with the charge of the electron, this makes the atom electrically neutral. The last of the four fundamental particles, that make up today's universe is the electron neutrino. Neutrinos are very light particles, which hardly interact with other particles. Due to the very rare interaction of neutrinos with other matter, they cannot be experienced in everyday life. The neutrino was postulated by W. Pauli, who tried to explain the β^--decay, where electrons are emitted from unstable nuclei. The electrons have a broad spectrum of energies, when they leave the nucleus. This is only possible, when, besides the electron, a second particle is emitted. As the particle had to be electrically neutral, it was called neutrino[1]. It took 23 years from its prediction to the first discovery. The neutrino belongs to the group of leptons and has no electric charge.

The two quarks and two leptons described above, make the first generation of particles in the Standard Model. However, there are two more generations, which can exist, though these particles have very short life times and rapidly decay into particles of lower generations, leaving only the first (stable) generation that can be found in

[1] the name was introduced by E. Fermi standing for small neutron

everyday life. The particles of the second and third generation are almost identical to their siblings in the first generation. Only the masses of the particles increase with every generation. The second generation consists of the charm- and the strange-quarks and the muon with its corresponding neutrino, the muon-neutrino. While the charm and the strange quarks are hardly found outside of large high energy physics experiments, the muon (and due to conservation laws also the muon neutrino) plays a significant role in the analysis of cosmic radiation. The third generation contains the bottom and the top-quarks and the tau and the tau-neutrino. All of these particles from the third generation only exist in high energy interactions, either in space or in large experiments[2]. A list of all matter particles, their generation affiliation in the Standard Model and the masses of the individual particles is shown in Figure 1.1. Between the generations, the masses of the particles increase a lot. The mass difference of the top-quark (the heaviest observed quark, approximately as heavy as a gold atom) compared to the mass of the up-quark, for example is in the order of 10^6. It is still a mystery in today's physics, why there are such huge mass differences.

For each of these particles shown in Figure 1.1, there is also an antimatter representative. The antimatter particles are identical to the normal particles, except their charge type quantum numbers being negative. All of the 12 particles (and 12 anti-particles) described above belong to a group called fermions[3]. Fermions have half integer spin and are thus subjects to the Pauli principle; two identical fermions cannot have the same quantum state when their wave functions overlap.

1.2 Force

In the Standard Model, interactions between particles are mediated by the exchange of energy packets, called quanta. These quanta are interpreted as exchange particles, or Gauge Bosons[4]. The boson carries the energy and the momentum, that is propagated from one particle to another. Each interaction has thereby its own set of gauge bosons. And each particle is only affected by a certain interaction, if it carries the corresponding charge (see Figure 1.2 on the following page). To comply with the conservation laws, the exchange process has to take place over a time or range, limited by Heisenberg's Uncertainty Principle. Like all particles, which are part of the Bose-Einstein-statistics, the spin of bosons is integer.

1.2.1 Electromagnetic Interaction

The electromagnetic interaction is the best observable of the three interactions of the Standard Model, as it is part of the everyday life. It binds the atomic shell to its nucleus and is responsible for many common phenomena like electricity, magnetism and light.

The propagator of the electromagnetic interaction is the photon, also known as γ boson. Photons are mass- and chargeless. Thus the range of the electromagnetic

[2]Due to the neutrino oscillation, it is possible to observe also neutrinos from higher generations, although lower generation neutrinos are expected.

[3]after the Italian physicist Enrico Fermi

[4]Named after the Indian physicist S. Bose

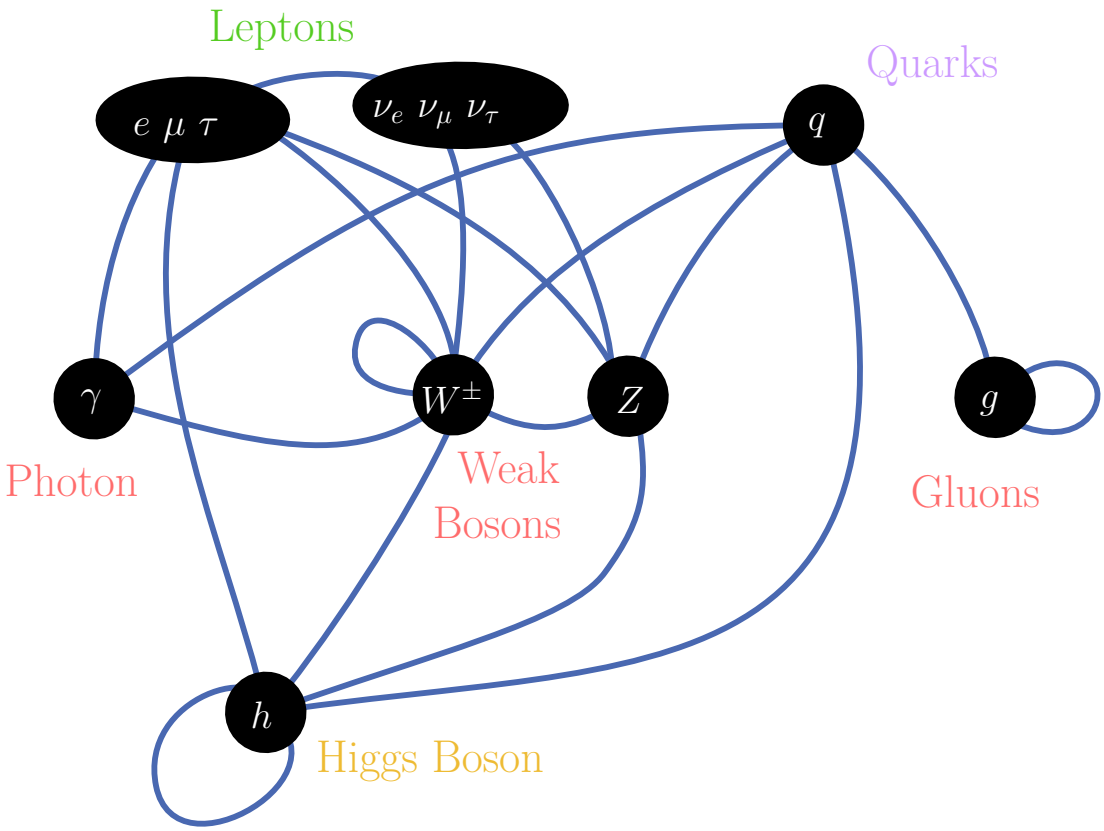


Figure 1.2: *Schematic of the interactions between elementary particles.*

force is infinite, due to the uncertainty principle. Accordingly, the photon is a stable particle. The photon itself has no charge of any kind, thus it couples to none of the interactions. All fermions, except neutrinos, have electric charge, making them subject to the electromagnetic interaction.

1.2.2 Weak Interaction

The weak interaction has no macroscopic occurrence. Two examples of processes, where the weak interaction is involved in the β-decay, which is already mentioned in Section 1.1 and the fusion of hydrogen to helium in stars. The name 'weak' comes from the limited range of the interaction.

The propagator particles of the weak interaction are the $W^\pm$ and the Z^0 bosons. As these particles are quite massive ($m_{W^\pm} = 80.4\,\text{GeV}$, $m_{Z^0} = 91.19\,\text{GeV}$[6]), the uncertainty principle limits their lifetime. A virtual gauge boson with a mass of 90 GeV can only exist for $\approx 2 \cdot 10^{-26}$ s, limiting its reach to $\approx 10^{-18}$ m. This short range of the weak interaction (1/10 of the diameter of atoms) suppresses the weak interactions.

The weak interaction is the only interaction, all fermions participate in. It is also the only interaction, allowing flavor changes, which means that fermions transform into other fermions. The conversion of quarks into other quarks, or leptons into other leptons respectively, only occurs with $W^\pm$-bosons as propagator. Flavor changes with Z^0 as

propagator have not been observed, yet. The transformation of quarks is described by the unitary quark mixing matrix, also called CKM-Matrix[5], which describes the probability $|V_{ij}|^2$ for a quark q_i to decay into another quark q_j [6]:

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \cdot \begin{pmatrix} d \\ s \\ b \end{pmatrix}$$

$$|\mathrm{V}| = \begin{pmatrix} 0.974 & 0.225 & 0.003 \\ 0.225 & 0.973 & 0.04 \\ 0.008 & 0.04 & 0.9991 \end{pmatrix}$$

Due to the unitarity of the matrix, its free parameters can be reduced to three mixing angles and a complex phase. The numerical parameters of the matrix are, similar to the particle masses, not determined by the theory of the Standard Model and have to be measured by the experiments.

Similar to the quarks, the neutrino eigenstates are also not equal to their mass eigenstates to the weak interaction. Thus, analogously to the CKM-matrix, a Pontecorvo-Maki-Nakagawa-Sakata (PMNS)-Matrix can be defined, which describes the transition between neutrino flavors:

$$\begin{pmatrix} |\nu_e\rangle \\ |\nu_\mu\rangle \\ |\nu_\tau\rangle \end{pmatrix} = \mathrm{U} \cdot \begin{pmatrix} |\nu_1\rangle \\ |\nu_2\rangle \\ |\nu_3\rangle \end{pmatrix}$$

$$|\mathrm{U}|^2 = \begin{pmatrix} 0.68 & 0.30 & 0.024 \\ 0.13 & 0.49 & 0.38 \\ 0.20 & 0.21 & 0.59 \end{pmatrix}$$

The off orthogonal elements of the PNMS-matrix[7], are much larger than in the CKM-matrix. This leads to a significant mixing of neutrino flavors.

Unlike all other interactions, the weak interaction does not create bound states, as its range is too short.

1.2.3 Strong Interaction

The mediator of the strong interaction is the massless gluon (g). Gluons couple to the so called color charge. The name color charge is abbreviated from the charge's nature, as there are three different types of charge creating the strong interaction, similar to the three basic colors red, blue and green. Each quark carries one of the three colors, while anti-quarks carry anti-color.

What makes the strong interaction different from the other interactions, is that besides quarks, the gluons also carry color charge. Thereby a gluon carries a combination

[5] named after the three physicists, who developed the matrix: N. Cabibbo, M. Kobayashi and T. Maskawa.

of one color and a different anti-color. A combination of a color and its corresponding anti-color would be color-neutral, and thus not be subject to the strong interaction. Due to their color charge, gluons couple not only to quarks, but also to other gluons. This however leads to a constant attractive force between two quarks, as the distance increases. If the distance, and thus the energy between two quarks rises above a certain level, a new quark anti-quark pair is created. These new quarks complement the departing quarks to new hadrons with regained neutral color. This process is called hadronization. The only exception is the top-quark. Due to its large mass, its lifetime is shorter than the time necessary for hadronization and it decays prior to that.

Bound states of the strong interaction

The strong interaction allows the creation of free bound states, called hadrons. There are two kinds of hadrons, baryons and mesons. Mesons are made of one quark and one anti-quark. The quarks in mesons always carry one color charge and the corresponding anti-color charge. Thus they appear color neutral or white. The spin of mesons is either 0 or 1, depending if the spins of the constituents are anti-parallel or parallel, respectively. All mesons are unstable.

Constitutions of three quarks are called baryons. Each of the quarks inside a baryon carries a different color charge, what makes baryons color neutral, similar to mesons. The spin of baryons is half integer, thus they are fermions. The only free stable baryon is the proton (two up- and one down-quark). When bound in an atomic nucleus, neutrons (two down- and one up-quark) are also stable.

The strong interaction is also responsible for the binding of the nucleons in atomic nuclei.

1.3 Mass

The theory of the Standard Model is based on gauge theories, not foreseeing any masses for gauge bosons and fermions[6]. However, most of the particles described above do have mass, which is in most cases measured very precisely. To explain the massive gauge bosons $W^{\pm}$ and Z^0, the theory of the Standard Model can be extended by the Higgs sector. The Higgs sector uses spontaneous symmetry breaking to augment the theory of the electro-weak interaction[7], with its four gauge bosons, the photon, the Z-boson and the two W-bosons. The electro-weak theory is thereby separated into the weak and electromagnetic interaction. The Higgs mechanism also predicts a massive particle with a spin of 0, the Higgs boson. This boson is generated by a quantum field with a vacuum expectation value greater than zero and thereby gives mass to the $W^{\pm}$ and Z^0 bosons as they couple to the Higgs field. The photon does not couple to the Higgs field, so it remains mass-less. The mass of Fermions is generated by the Yukawa coupling of the Fermions to the Higgs field[8].

[6] In this case, rest masses of fundamental fermions are addressed. The mass generated by binding energy is not part of the Higgs mechanism

[7] The electro-weak interaction describes a mathematical unification of the weak and the electromagnetic interaction.

Chapter 2

The Experimental Setup at the HL-LHC

2.1 The Large Hadron Collider

2.1.1 Accellerator

The Large Hardron Collider (LHC)[9] is a superconducting hadron accelerator and collider, operated by the European Organization for Nuclear Research (CERN). It was installed into the existing 26.7 km long tunnel from the former LEP[1] accelerator. The tunnel is located between 45 m and 170 m below the surface and is inclined by 1.4% sloping towards lake *Lèman*. The LHC accelerates protons and heavy ions in two counter rotating beams. There are eight points along the beam line, where the beams are crossed. At four of these points, large experiments have been constructed in order to study the reactions of the colliding particles. In its design phase, the LHC was supposed to accelerate the two particle beams up to a center-of-mass energy of 14 TeV. To bend the beams onto a circular trajectory, strong magnetic fields up to 8 T are necessary. These fields are generated by state of the art superconducting magnets. These magnets are cooled by superfluid helium to a temperature below 2 K and therefore are cooler than space. Due to a defective magnet, which caused heavy damage shortly after start-up, leading to a down time of approximately one year, the design energy could not be reached from the beginning of operation. After the repairs, the LHC started operation again with a center-of-mass energy of 3 TeV, which was then stepwise increased up to 8 TeV. To finally reach the design center-of-mass energy of 14 TeV, further upgrades of the machine are necessary which will not only increase the beam energy but also the luminosity significantly. These upgrades are part of a long shutdown in 2018. A further upgrade is planned in the years of 2023 to 2024. After this upgrade, the LHC changes its name to the High Luminosity LHC (HL-LHC). The HL-LHC is designed to provide an instantaneous luminosity of $5 \cdot 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ over 10 years, delivering $2500\,\mathrm{fb}^{-1}$ of data. [10]

[1] Large Electron-Positron Collider, former particle accelerator at CERN

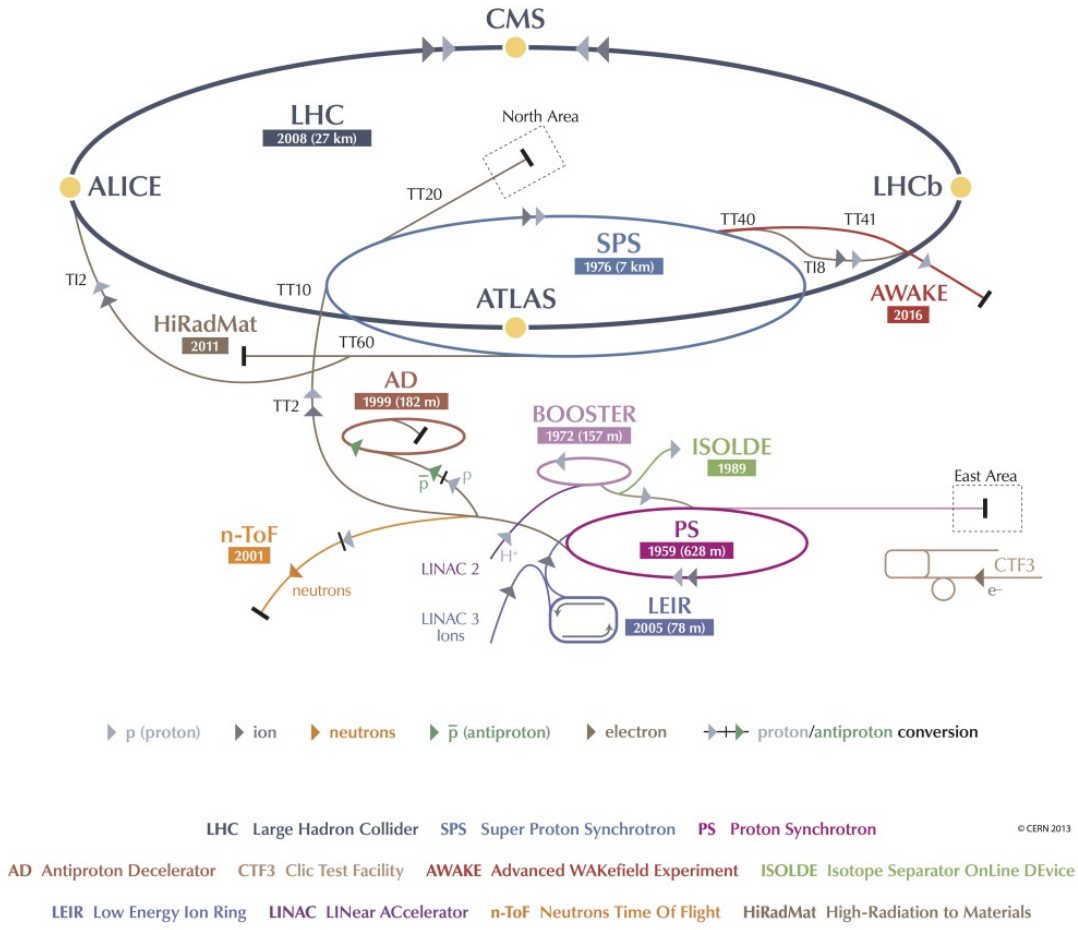


Figure 2.1: *Accelerator chain providing the preaccellerated particles for the HL-LHC. [9]*

Figure 2.1 shows the accellerating chain of the protons for the LHC, as it is used now. During the upgrade to the HL-LHC components of the individual preaccellerators will be replaced, but the chain itself will not change.

2.1.2 Experiments

The HL-LHC provides several experiments in order to observe particle collisions. The most important experiments and their purpose will be described briefly.

The HL-LHC has two high luminosity experiments, ATLAS [11] and CMS [12], which are aiming to fully use the provided luminosity of the accelerator. There is also an experiment with reduced luminosity at the HL-LHC: LHCb[13], which is investigating in b-quark physics and the cp-violation. Besides the proton-proton beams, the HL-LHC will also collide heavy ions (lead nuclei), which are studied by the ALICE[2] [14] experiment.

[2] **A** **L**arge **I**on **C**ollider **E**xperiment

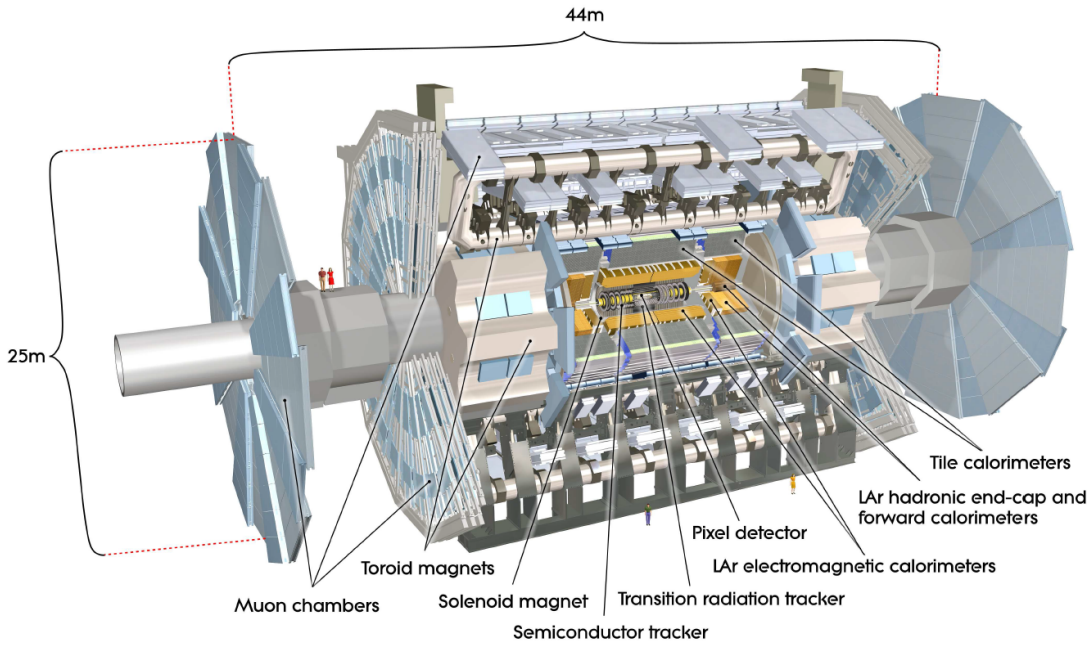


Figure 2.2: *Sketch of the ATLAS detector as it was at first launch. [15]*

Similar to the ATLAS experiment, which is described in the next section, the Compact Muon Solenoid (CMS) is a multipurpose detector. The CMS detector has a high magnetic field of 4 T in its core, generated by a large superconducting solenoid magnet. Inside the magnet a silicon pixel tracker, a silicon strip tracker, a lead-tungsten scintillating crystals electromagnetic calorimeter and a brass-scintillator sampling hadronic calorimeter are located. Outside of the solenoid the iron yoke of the flux-return is mounted. Integrated into the yoke are four stations of muon detectors, covering most of the 4π solid angle. The overall dimensions of CMS are 14.6 m diameter, 21.6 m length and 12600 t of weight.

2.2 The ATLAS Experiment

The ATLAS[3] experiment (further referred to as ATLAS) is a multipurpose detector, operated at the LHC at CERN. It is located at Point 1, 100 m below the ground in the largest man made cavern on earth. ATLAS studies the physics in the tera scale by observing the proton-proton and ion-ion[4]-collisions, which are provided by the LHC. Figure 2.2 shows a sketch of ATLAS at the time of the first launch. ATLAS is the largest experiment at the LHC with a length of 46 m and a diameter of 25 m. It weights ~7000 t and is thus lighter than the smaller CMS. Like CMS, ATLAS is being build as a barrel shaped detector, constructed in layers around the beam pipe. The

[3] **A** **T**oroidal **L**HC **A**pparatu**S**, which is btw. the most special abbreviation ever! Even thinking about it is so embarrassing, that nowadays ATLAS is commonly used as a name and its origin as abbriviation is usually denied.

[4] lead nuclei

detector is symmetric in forward-backward direction from the interaction point and in angular direction around the beam pipe. During the design phase of the detector, the search of the Higgs boson was used as an orientation for the classification of several sub-detector performance requirements. For momentum measurements, there are two strong magnetic fields in ATLAS, a solenoidal field of 2 T in the inner detector and a toroidal field between 0.5 and 1 T in the outer regions.

With the upgrade of the LHC to the HL-LHC, the provided instantaneous luminosity for ATLAS and the other experiments will increase to $L = 5 \cdot 10^{34}\,\mathrm{cm^{-2}s^{-1}}$, allowing to aim for an integrated luminosity of $2500\,\mathrm{fb^{-1}}$ over 10 years of operation [10]. The high luminosity and the high center-of-mass energy of up to $\sqrt{s} = 14\,\mathrm{TeV}$ opens the door to new physics, that could not be studied prior to the upgrade. With this new opportunities, and the recently discovered Higgs boson [1, 5], the physics goals of ATLAS are extended by several fields. There is still a lot of investigation necessary to fully classify the Higgs boson in all its facets, for example self coupling, spin, parity, and as many final states as possible. Besides that, ATLAS will also investigate in weak boson scattering and the discovery (or exclusion) of weak scale super-symmetry (SUSY) just to name a few.

Along with the continuous increase of luminosity of the HL-LHC comes an increase in the number of particle interactions per bunch crossing up to ~140 at $5 \cdot 10^{34}\,\mathrm{cm^{-2}s^{-1}}$. The current ATLAS detector will not be able to process the increased number of particle tracks, that originate from this amount of interactions for various reasons. The read out bandwidth of the inner detector is not high enough to reliably transmit the increased number of hits in the pixel and the strip system to the DAQ[5]. The occupancy of the straw tube radiation tracker (TRT) will reach the 100% limit. At the time of the upgrade to the HL-LHC, the components of ATLAS will be 15-20 years old and exceeding their intended life times due to the harsh radiation environment. Accordingly, to ensure a sufficient performance of ATLAS, the detector will also be upgraded several times during the shutdown phases of the LHC. In this sub-chapter, the specifications of the ATLAS detector after the upgrade to the HL-LHC are outlined. During this upgrade several detectors will be either enhanced or replaced. The inner tracker (ITK), consisting today of 3 sub-detectors, will be replaced entirely by an all silicon tracker, combining pixel sensors in the layers around the beam pipe and strip sensors in the more outer radii. The emphasis of this thesis will thereby lie on the pixel detector (as part of the inner detector), as the R&D for this thesis is mainly on this topic.

2.2.1 Inner Detector

Prior to the HL-LHC upgrade, the inner detector (ID) consists of 3+1 layers[6] of pixels, four layers of silicon micro-strips (SCT) and a straw tube tracker, which uses radiators to generate transition radiation (TRT). After the upgrade to the HL-LHC, the performance requirements of the inner tracking system of ATLAS will exceed its capabilities entirely for various reasons. Therefore, the ID will be replaced entirely. Detailed information on performance requirements and possible layouts can be found in Section 2.3.

[5] **D**ata **A**c**Q**uisition

[6] Three primal layers and a fourth inserted B-layer (IBL)[16]

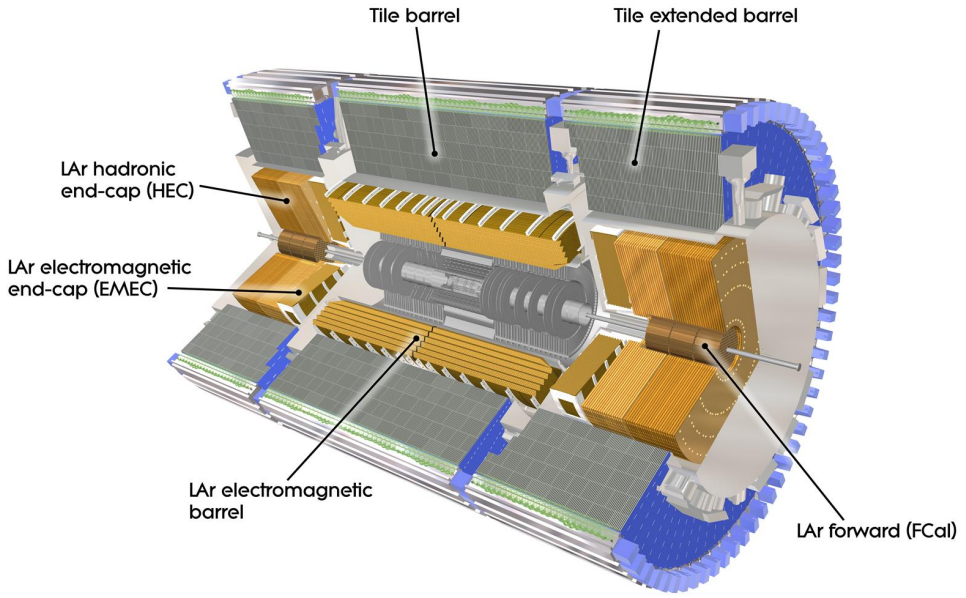


Figure 2.3: *Sketch of the ATLAS calorimeter system at first launch. [17]*

	Radius [m]	Length [m]	Pseudorapidity η
EM barrel	$1.4 \leq R \leq 2.0$	$0 \leq \|z\| \leq 3.2$	$\|\eta\| \leq 1.475$
EM end cap inner wheel	$0.3 \leq R \leq 0.6$	$3.7 \leq \|z\| \leq 4.3$	$2.5 \leq \|\eta\| \leq 3.2$
EM end cap outer wheel	$0.6 \leq R \leq 2.0$	$3.7 \leq \|z\| \leq 4.3$	$1.375 \leq \|\eta\| \leq 2.5$
FCal1	$0.07 \leq R \leq 0.46$	$4.7 \leq \|z\| \leq 5.15$	$3.1 \leq \|\eta\| \leq 4.9$
Tile calorimeter	$2.28 \leq R \leq 4.25$	$0 \leq \|z\| \leq 6.1$	$\|\eta\| \leq 1.7$
Hadronic end-cap	$0.475 \leq R \leq 2.03$ $(0.372 \leq R \leq 2.03)$[7]	$4.3 \leq \|z\| \leq 6.1$	$1.5 \leq \|\eta\| \leq 3.2$
FCal2, FCal3	$0.07 \leq R \leq 0.46$	$5.1 \leq \|z\| \leq 6.05$	$3.1 \leq \|\eta\| \leq 4.9$

Table 2.1: *Dimensions and coverings of the individual calorimeter sections. [18]*

2.2.2 Calorimetry in ATLAS

Two types of calorimeters, both designed as sampling calorimeters, are used in ATLAS. In detector regions, that are exposed to high radiation, liquid argon (LAr) is used as active material. This applies to the entire electromagnetic (EM) calorimeter (barrel and end-cap section), the hadronic end-cap calorimeter and the forward calorimeters. The barrel section of the hadronic calorimeter uses scintillating tiles to detect passing particles. The dimensions and coverings of the individual calorimeter sections are shown in Table 2.1, the alignment can be seen in Figure 2.3. Figure 2.4 on the next page shows the thicknesses of the calorimeter sections in terms of radiation length.

[7] first nine plates of the upstream wheel

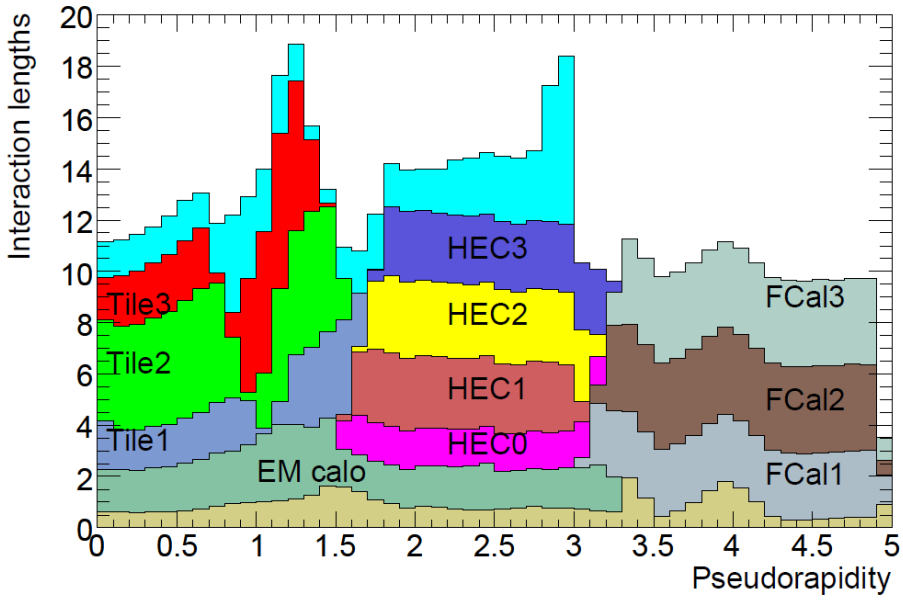


Figure 2.4: *Cumulative amount of material, in units of interaction length, as a function of η, in front of the electromagnetic calorimeters, in the electromagnetic calorimeters themselves, in each hadronic layer, and the total amount at the end of the active calorimetry. Also shown, for completeness, is the total amount of material in front of the first active layer of the muon spectrometer (up to $|\eta| < 3.0$). [18]*

Liquid Argon Calorimeters

The innermost of the LAr calorimeters is the barrel section of EM calorimeter, contained in a barrel cryostat, that surrounds the inner detector. It is divided into two identical half barrels, which are abutted in the middle of the detector at $z = 0$. Each of the half barrels covers thereby a region of $0 < |\eta| < 1.475$ on its corresponding side. Inside the half barrels an accordion shaped lead structure shown in Figure 2.5 is used as absorber, which covers the entire ϕ range without any gaps. The space between the lead plates is filled with LAr. Inside this LAr, readout electrodes (three-layer Kapton-copper boards) are located. While the LAr gaps between the lead plates have a constant thickness throughout the whole barrel, the thickness of the lead plates varies with η according to Table 2.2 to improve the energy resolution of the calorimeter. To maintain a constant sampling fraction of the calorimeter as a function of radius and ϕ, the bending angles and the length of the folds between the bends increase with the radius. For further details about the shape of the EM barrel calorimeter, refer to [19].

Section	Rapidity	Lead	LAr gap
Barrel	$\|\eta\| < 0.8$	1.5	2.1
	$0.8 < \|\eta\| < 1.475$	1.1	2.1
End-cap	$1.375 < \|\eta\| < 2.5$	1.7	2.8-0.9
	$2.5 < \|\eta\| < 3.2$	2.2	3.1-1.8

Table 2.2: *Lead- and LAr gap thickness in mm in the EM calorimeter as a function of η. [18]*

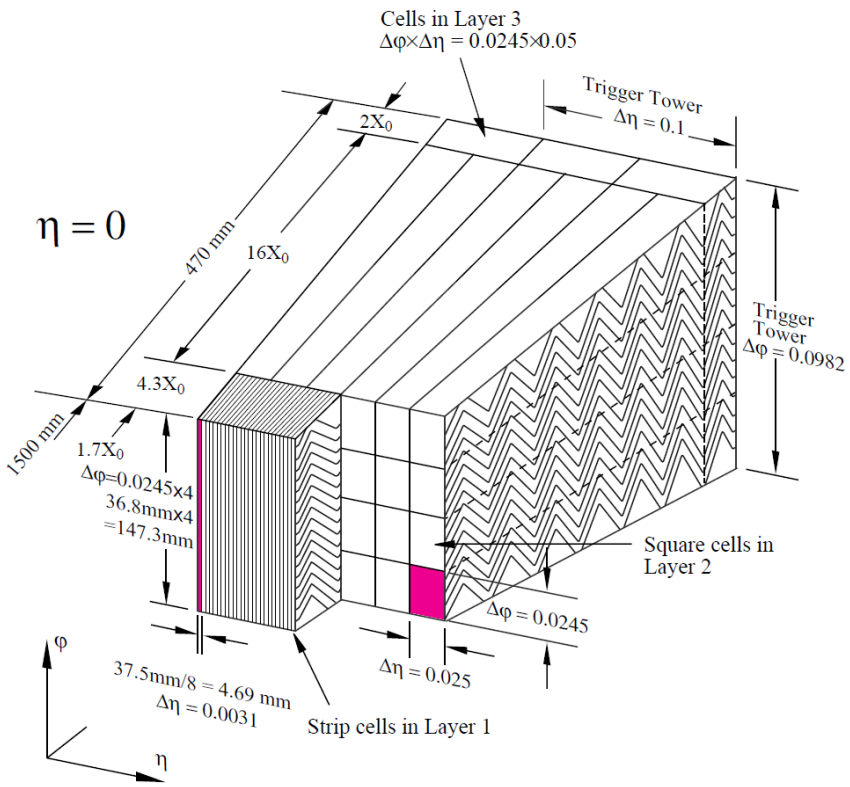


Figure 2.5: *Schematic of the accordion shaped absorber structure of the electromagnetic barrel calorimeter. [18]*

The end-cap section of the EM calorimeter shares a cryostat with the hadronic end-cap calorimeters and the forward calorimeters on each side of the detector. In the EM end-caps, the same accordeon structure as in the barrel section is used. Similar to the barrel section, the bending angles and the fold lengths need to increase with the radius. But the end-caps cover a much larger range of radii, compared to the barrel section. So to keep the folding angles within a feasible range, the end-cap wheels are divided into an inner and an outer wheel. Both wheels together cover a region of $1.375 < |\eta| < 3.2$.

When a particle traverses the calorimeter, it ionizes the LAr. The generated charge is collected on the outer layers of the read out electrodes, which are at high voltage. This produces a voltage spike, which is capacitively coupled into the inner layers of the electrodes. A segmentation of the inner layers defines the granularity of the calorimeter to $\Delta\eta \times \Delta\phi = 0.025 \times 0.025$ in the barrel region, and 0.1×0.1 in the end-cap region. Together with the barrel part, the EM calorimeter has ~190 000 channels. The energy resolution of the EM calorimeter is $\sigma_E/E = 10\%/\sqrt{E} \oplus \%$.

The hadronic end-cap calorimeter also uses LAr as active material, but unlike to the EM calorimeters flat copper plates as absorbers. It consists of two independent wheels on each detector side, located behind the EM end-cap wheels. The first wheel (upstream) uses 25 mm copper plates as absorber material, while the second one uses copper plates of 50 mm thickness. Each wheel consists of 32 identical wedge modules and a cen-

tral ring for assembly. The gap for the active material between the plates is 8.5 mm wide in both cases. Between the absorbers, three parallel electrodes split the active area into four drift spaces, ~1.8 mm wide, building an electrostatic transformer (EST) shown in Figure 2.6. With the EST the high voltage can be reduced by a factor of two to ~2 kV. The central electrode is the readout electrode, similar to the readout of the EM calorimeter. The remaining two electrodes supply the high voltage. To keep the distances between the electrodes constant, a honeycomb sheet in the gaps is used for stabilization. Similar to the EM readout, the granularity is defined by the geometry of the readout cells on the readout electrode to $\Delta\eta \times \Delta\phi$=0.1×0.1 for $\eta < 2.5$ and 0.2×0.2 for larger η. The number of channels for the whole hadronic end-cap calorimeter is 5632, the energy resolution will be at σ_E/E=50%/$\sqrt{E}\oplus$3%.

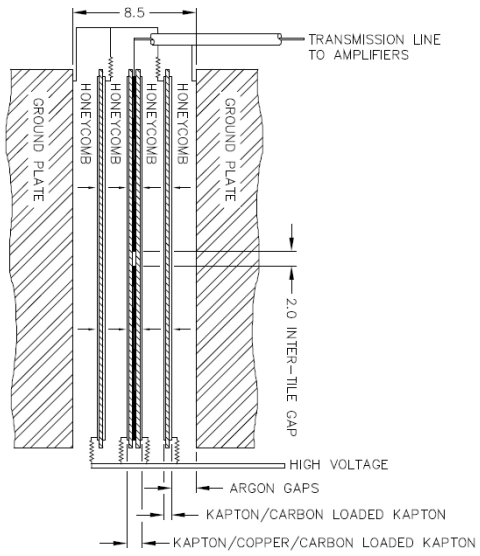


Figure 2.6: *Schematic of the LAr gap in the hadronic end-cap calorimeter. [18]*

The forward calorimeter (FCal), as it is used prior to the HL-LHC, is divided into three parts. The electromagnetic part (FCal1) and the two hadronic parts (FCal2 and FCal3). For the FCal1 copper is used as absorber, while FCal2 and FCal3 mainly use tungsten. The copper absorber plates in FCal1 are stacked behind each other. In these copper plates, 12260 holes hold the electrode structures, that are made of coaxial rods and tubes made from copper. The gap between the rods and tubes is separated by a radiation-hard plastic fiber, wound between them. The gap between rod and tube contains LAr (see Figure 2.7). In FCal1 the thickness of the fiber is 269 µm, resulting in a gap of similar dimension. FCal2 and FCal3 have two copper end plates each, between which electrode structures similar to those in FCal1 are spanned (10200 in FCal2 and 8224 in FCal3). These electrode nodes use tungsten rods instead of copper rods, to reach higher absorption lengths and have larger LAr gaps (FCal2 376 µm and FCal3 508 µm). The space between the end plates and the tubes is filled with small tungsten slugs, that are arranged in a hexagonal pattern. The readout electrodes are organized in hardwired groups of four (FCal1), six (FCal2) or nine (FCal3) via small boards on the faceplate of each forward calorimeter resulting in 1008 channels for each FCal1, 500 channels for each FCal2 and 254 channels for each FCal3. The readout boards are placed in regions with least radiation. This is at the inner end of FCal1 and the outer end of FCal2 respectively. Behind the forward calorimeter a shielding block made of a copper alloy is placed to reduce the background particle flux to the muon end cap systems. To reduce the neutron albedo, the forward calorimeter block is moved by 1.2 m away from the EM end-cap calorimeter in |z| direction (see Figure 2.8). The energy resolution of the FCal is $\sigma_E/E = 100\%/\sqrt{E} \oplus 10\%$.

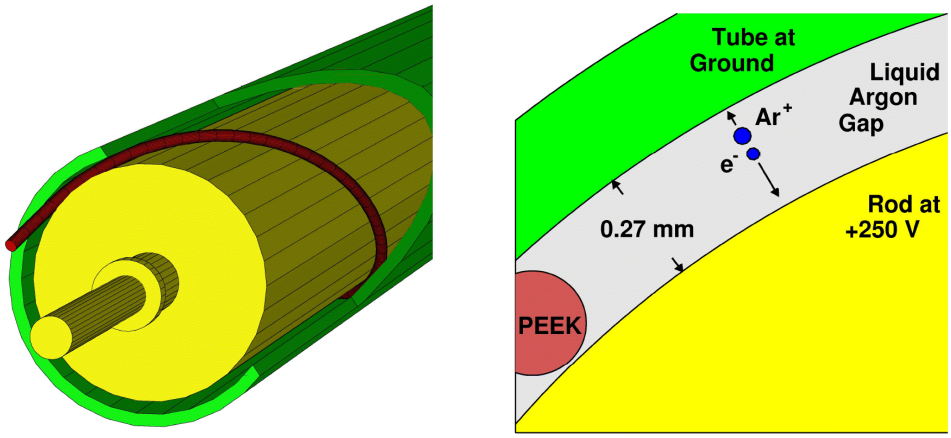


Figure 2.7: *Left: Cut-away drawing of an FCal electrode tube. Right: Close up view of a cross section of a FCal1 electrode tube. [20]*

After the upgrade to the HL-LHC, the increased luminosity will drive the forward calorimeter (FCal) to its limits. Therefore currently there are discussions ongoing how the FCal can be upgraded to cope with the luminosities of the HL-LHC. Two options are being developed, which yet have to be fully evaluated. The first option is the sFCal, which would replace the current FCal. In sFCal the LAr gaps are smaller (100 µm in sFCal1) and the signal processing electronics are optimized for higher luminosity. Due to additional space needed for the sFCal, the envelope of the ATLAS calorimetry would have to change. The second option is to add another small calorimeter, the Mini-FCal, in front of the existing FCal1 to reduce the particle flux entering the FCal. There are three sensor technologies in discussion for the Mini-FCal: diamond detectors, high pressure Xe gas and LAr. The LAr option would comply with sFCal1. The diamond and Xe option would be standard sampling calorimeters with parallel absorber plates and active sensors in between.

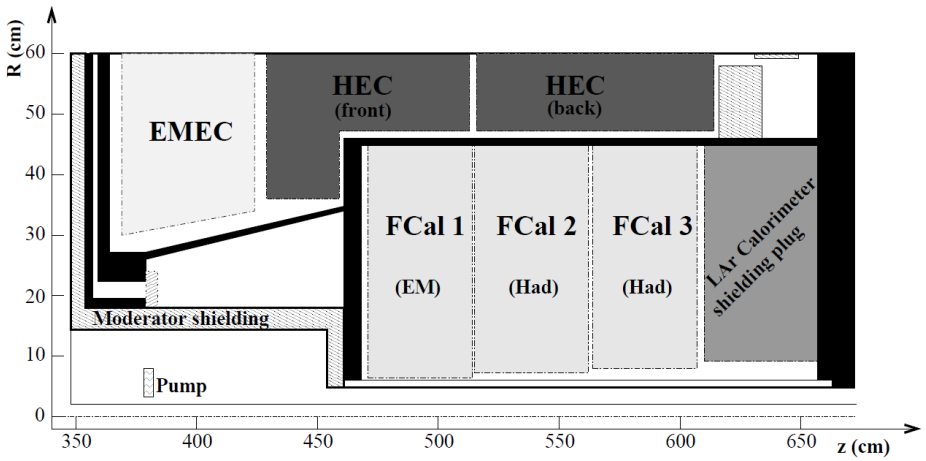


Figure 2.8: *Location of the FCal in ATLAS. [18]*

Due to the updated trigger system of ATLAS used at the HL-LHC and the heavy radiation damage that the components of the LAr calorimeter will have suffered, the front- and back-end electronics of the LAr calorimeter will have to be replaced. All readout data after the upgrade to the HL-LHC is digitalized in situ and transmitted off-detector. This will provide as much flexibility as possible to the trigger system, as full granularity data will be available.

To correct for the energy that is lost in the material upstream of the calorimeter (ITK, solenoid magnet and cryostat), a presampler calorimeter (not shown in Figure 2.3 on page 17) is installed outside the cryostat cold wall, covering a pseudorapidity range of $|\eta| < 1.8$. The presampler consists of an active LAr layer, 1.1 cm thickness in the barrel region and 0.5 cm thickness in the end-caps.

Tile Calorimeter

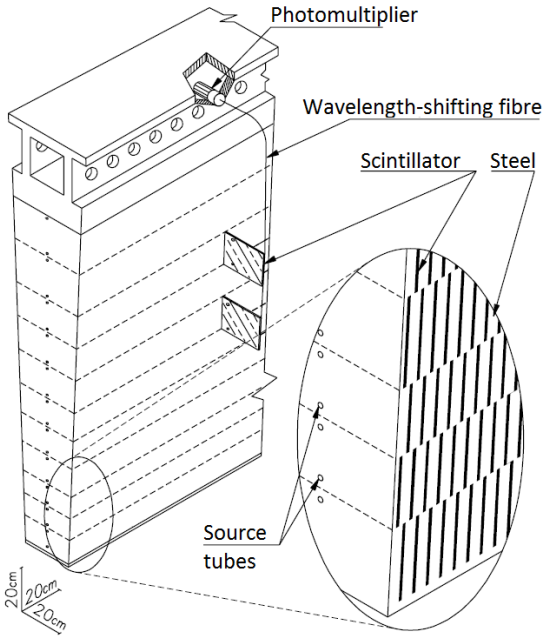


Figure 2.9: *Schematic showing one module of the TileCal and its components. [18]*

The barrel section of the hadronic calorimeter makes the outermost part of the calorimetry in ATLAS. Unlike the rest of the calorimeters, this sub-detector is not realized with LAr and copper/tungsten/lead, but with scintillating tiles as an active material and steel used as an absorber. Therefore it will further be addressed as TileCal. The TileCal is subdivided into three parts: the central barrel part, which is 5.8 m long and the two extended barrels, 2.6 m long each. Each barrel itself is made up of 64 identical wedge shaped modules, that cover an angle of $\phi = 5.625°$ with a gap of 1.5 mm between two modules. The resulting cylinder (the barrel) has an inner radius of 2.28 m and an outer radius of 4.25 m. Overall, the TileCal has an absorber/sensor ratio of 4.7:1. In the gaps between the central barrel and the extended barrels, additional scintillation counters are used to recover some of the energy, that is lost there. The schematic of a wedge module is shown in Figure 2.9. The absorber structure consists of a 5 mm thick steel plate, of which 4 mm thick plates are glued in a staggered way, leaving gaps for the scintillation tiles. While the thickness of the tiles is constant, the length and height vary between 97 mm and 187 mm and 200 mm and 400 mm respectively, to match the wedge shape.

Ionizing particles passing through the tiles induce the emission of ultraviolet light, which is converted and transported to the photomultiplier tubes (PMT) by two wavelength shifting fibers each. By coupling the fibers to the PMTs in groups, a three

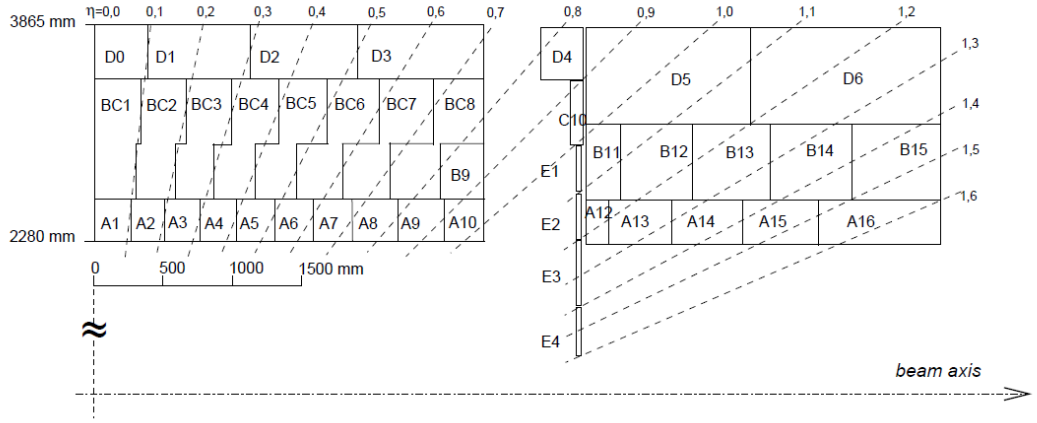


Figure 2.10: *Segmentation of the readout clusters in the TileCal, that are formed by the bundling of the optical fibers. The picture shows the central part (left) and one extended part (right) of the TileCal. The TileCal is symmetric in z and ϕ. [18]*

dimensional cell structure is created (see Figure 2.10). At $\eta = 0$ these structures define three layers with different sampling depths of 1.5, 4.1 and 1.8λ. Depending on the location, the cells form a granularity of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ in the two inner layers and 0.1×0.2 in the outer layer. On top of each module, a steel girder supports the absorber structure and houses the read out electronics as well as the PMTs. The girder also works as return joke for the magnetic field of the solenoid (see Section 2.2.4).

For the calibration of the TileCal, three systems are foreseen: charge injection, lasers and a ^{137}Cs source. With these systems, uniformity of each PMT gain can be tuned to $\pm 3\%$. The total number of channels is in the order of 10 000.

As for the LAr calorimeter, the readout electronics of the TileCal have to be replaced when the LHC is upgraded to the HL-LHC. The new readout concept of the TileCal is also based in the idea to continuously digitize all readout data and transmit it entirely to the back-end electronics, for further processing. This concept also includes a fully redundant optical transmission of the data, as both gain ranges of the front-end electronics are transmitted.

The energy resolution of the TileCal is $\sigma_E/E = 50\%/\sqrt{E} \oplus 3\%$.

2.2.3 The Muon System

The Muon System in ATLAS makes up the largest sub-detector in terms of space with its maximum diameter of 22 m and maximum distance of 21.5 m in z from the interaction point. A cut-away drawing of the muon systems can be seen in Figure 2.11 on the next page. It is used to detect charged particles, that traverse the calorimeters and to measure their momentum (via tracking of the particle trajectory through the toroidal magnetic field) over a pseudorapidity range of $|\eta| \leq 2.7$. Besides that, the muon system also provides trigger information for particles with $|\eta| \leq 2.4$. To be able to reach a momentum resolution of $\sigma_{p_T}/p_T = 10\%$ (at $p_T = 1$ TeV) together with the provision of the fast trigger signals, the muon system relies on four different detector

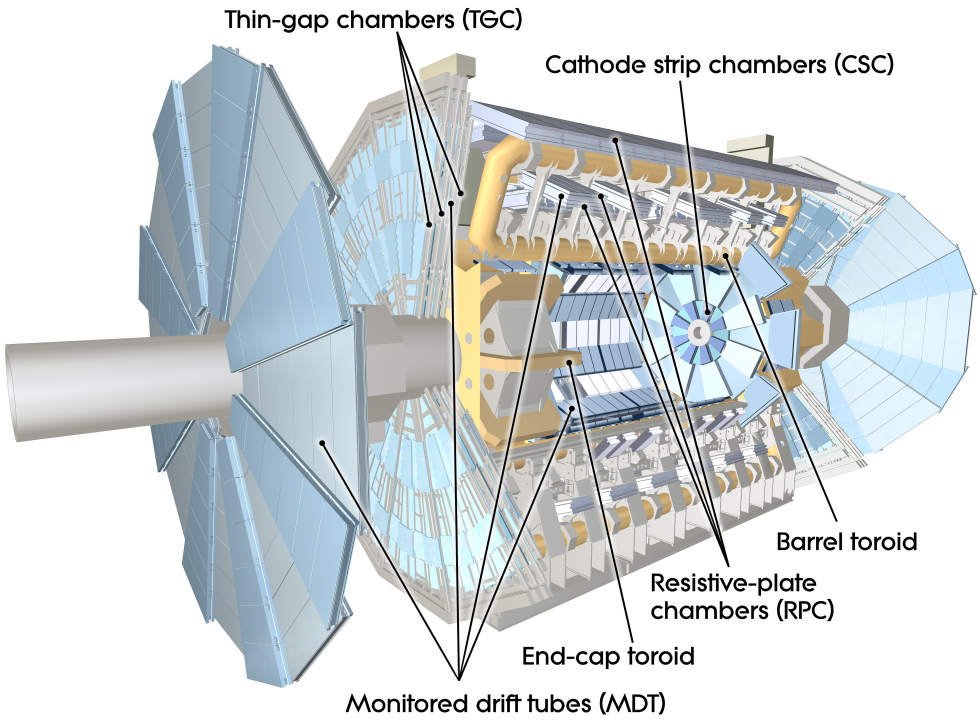


Figure 2.11: *Cut-away drawing of the ATLAS muon system. [21]*

types. For the precision measurements Monitored Drift Tubes (MDT) are used in the outer wheels, as well as in the central barrel sections around the hadronic calorimeter. They cover a pseudorapidity range of $|\eta| < 2.7$, except for the innermost layer in the barrel section, which only covers $|\eta| < 2$. Due to the higher particle flux in the forward region, Cathode-Strip Chambers (CSC) are used in as the innermost layer of the muon system for the coverage of $2 < |\eta| < 2.7$. The drift time though is with ~700 µs rather low. Thus for trigger information faster detectors with response times < 25 ns are necessary. In the barrel section, Resistive Plate Chambers (RPC) are used to cover pseudorapidities up to $|\eta| < 1.05$, while for the end-cap regions with $1.05 < |\eta| < 2.4$, Thin Gap Chambers (TGC) are used. Table 2.3 shows the parameters of all subsystems of the muon system.

		Chamber resolution			Measurements/track		Number of	
Name	Function	z/R	ϕ	time	barrel	end-cap	chambers	channels
MDT	tracking	35 µm	—	—	20	20	1150	354k
CSC	tracking	40 µm	35 µm	7 ns	—	4	32	30.7k
RPC	trigger	10 mm	35 µm	1.5 ns	6	—	606	373k
TGC	trigger	2-6 mm	35 µm	4 ns	—	9	3588	318k

Table 2.3: *Parameters of the four muon subsystems. The spacial resolutions in z and ϕ do not consider the alignment uncertanties and the time resolution does not consider the signal-propagation and electronic delays. [18]*

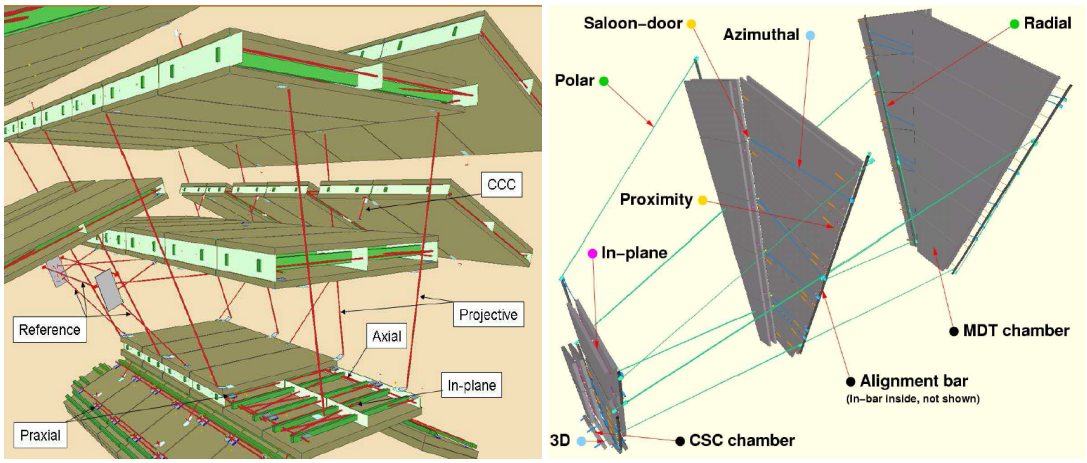


Figure 2.12: *Layout of the optical alignment monitoring system. The red lines show light beams simulating infinite momentum muons in the barrel (left) and the end-cap section (right). [18]*

Monitored Drift Tubes

For the drift tubes in the MDT system, aluminum tubes with an outer diameter of 29.97 mm and a wall thickness of 0.4 mm are used. Ar/CO_2 (93/7) gas with a pressure of 3 bar and a gas gain of $2 \cdot 10^4$ fills the tubes as active material. Inside the tubes, gold-plated tungsten-rhenium wires with diameters of 50 µm and a potential of 3080 V collect the electrons, which are produced by ionizing particles in the Ar/CO_2 gas. The wires are held in place by cylindrical end plugs, which guarantee a concentric position accuracy of the wire of $\sigma < 10$ µm. The signal readout and the HV supply to the central wire are on opposite ends.

To minimize the effect of misalignment in the muon system, it is continuously monitored for potential deformations. Light beams are sent from one end of each chamber onto CCD sensors on the other end to detect contortions and sagging of the chambers. For alignment monitoring, light beams and simulate the trajectory of an infinite momentum muon. These measurements are used to detect deformations of a few µm in the frame structure, supporting the chambers, and the chambers itself (see Figure 2.12). Besides the alignment, the thermal deformation of each chamber is also monitored by 3 to 28 temperature sensors in each chamber. The local magnetic field strength is also measured by two to four B-field sensors in each chamber.

Using the monitoring of position and temperature, the tracking resolution is only limited by the single tube resolution of about 80 µm. Combining the signals of all tubes in a chamber, the resolution increases to 35 or 30 µm for six or eight layers of tubes in a chamber. Overall there are 191568 tubes in the barrel and 162816 tubes in the two end-caps resulting in 354384 channels for the MDT system.

In terms with the upgrade to the HL-LHC, most of the tubes can continue operation within acceptable occupancy levels. Only the innermost end-cap wheels need replacement. To cope with the increased data rate, generated by the MDTs, and the new triggering concepts, the readout electronics will be replaced by more modern technolo-

gies. The most significant improvement in performance will come from the HPTDC[8] [22], which provides more timing flexibility for the L1 trigger and less data to be transferred from the detector.

Cathode-strip chambers

In the very forward region ($|\eta| > 2$) the counting rates exceed the acceptable limit for safe operation of the MDTs. Therefore the first layer of the MDTs in this region is replaced by cathode-strip chambers (CSC), which cope with hit-rates up to 1 kHz/cm^2. The CSC wheels are shaped like the ones in the MDT. The CSCs work as multi-wire proportional chambers with anode wires and cathode strips. For the operating parameters of the CSC, see Table 2.4. All wires in one chamber are spanned in parallel to each other and the central wire pointing in radial direction. Perpendicular to the wires, the cathode strips are arranged, providing the transverse coordinate. By interpolation between the collected charges of adjacent cathode strips, a track resolution of 60 µm can be reached in radial direction. In the second cathode plane, the strip pitch is larger, resulting in a resolution of 5 mm. The timing resolution is determined by the average drift velocity (60 µm/ns) and the maximum drift distance (1.27 mm) to about 20 ns for each chamber. Combing the measurements of all hits of a track, the resolution can be increased to an RMS value of 3.6 ns, which is enough for reliable tagging of the beam-crossing. The overall number of channels of the CSCs is 24 567.

Parameter	Value
Operating Voltage	1900 V
Anode wire diameter	30 µm
Gas Gain	$6 \cdot 10^4$
Gas mixture	Ar/CO_2 (80/20)
Total ionization (normal track)	90 ion pairs

Table 2.4: *Operating parameters of the CSC. [18]*

For the alignment monitoring, the same system as in the MDTs is used for the CSCs.

Resistive Plate Chambers

In the Resistive Plate Chambers (RPCs) parallel plates with gas gaps in between are used as detector. These plates are made of phenolic-melaminic plastic laminate, which is conductive, but with a high ohmic resistance ($10^{10}\,\Omega$/cm). A high voltage of 9.8 kV is applied to the plates, by a thin coating with a resistive graphite paint (100 kΩ/□[9]). A detailed setup is shown in Figure 2.13. When charged particles ionize the gas mixture ($C_2H_2F_4$/Iso-C_4H_{10}/SF_6 (94.7/5/0.3))

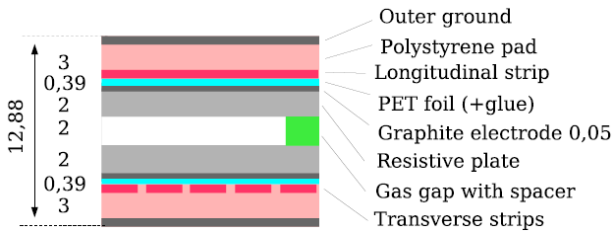


Figure 2.13: *Cross-section of a RPC. Measurements are in mm. [18]*

[8] **H**igh **P**erformance **T**ime to **D**igital **C**onverter
[9] kiloohms per square

by traversing it, the produced electrons immediately form avalanches simultaneously, due to the strong homogenous electric field. This produces one single signal instantaneously after the particle passed the gas, without any time of electrons drifting to regions of amplification.

Due to the high resistance of the plates and the graphite coating, the shielding of the electric field generated by the avalanches is neglectable. Thus the signal is capacitivly coupled into the pickup-strips leading to an intrinsic time jitter of $\leq 1.5\,\text{ns}$ ($\leq 10\,\text{ns}$ with strip propagation time). This qualifies the RPCs for the provision of trigger signals in the barrel section. From the pickup-strips, the signal is amplified and sent to readout. The pickup-strips have a width of 25-35 mm. Between the strips is a gap of 2 mm with a 0.3 mm wide ground strip to improve decoupling. By combining all hits of a unit, a track resolution of ~10 mm is reached in Z and ϕ.

For readout after the upgrade to the HL-LHC, the new Data Collector and Transmitter (DCT) trigger box will be used. This DCT will be located on top of the previous readout, avoiding complex reworking of the on-chamber-cabling. It receives the data from the RPC front-end, splits it and sends it to the DAQ.

Thin Gap Chambers

Thin Gap Chambers (TGCs) are multi-wire proportional chambers with a gas mixture of CO_2 and n-C_5H_{12} (55/45). Figure 2.14 shows the structure of the TGCs. The cathodes are formed by a thin graphite coating ($0.5 - 1\,\text{M}\Omega/\square$) on the inside (facing the wires) made of 1.6 mm thick FR4[10] plates. On the outside of these plates, a copper film perpendicular to the wires is used as pickup-strips or grounding. Similar to the RPC, the high electric field (wires are at 2900 V) produces fast signals (time resolution 4 ns), that are capacitively coupled into the pickup-strips. Unlike to the CSCs, in the TGCs the anode wire signals are also read out. The final track resolution is 7 mm in ϕ and 6 mm in R. With the second, azimuthal coordinate, the TGCs complements the measurements of the MDT wheels. The TGCs also provide the end-cap trigger signals of the muon system.

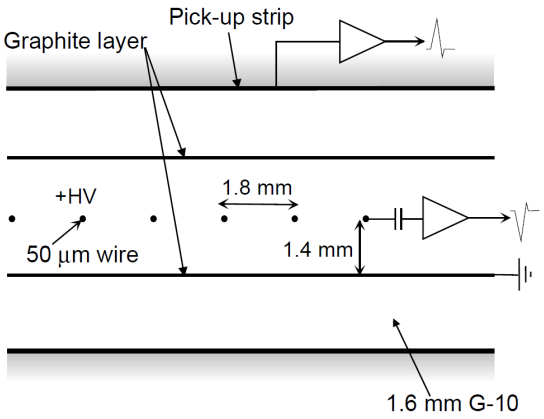


Figure 2.14: *Schematic of the TGC structure. [18]*

Prior to the upgrade to the HL-LHC, the small (inner) wheel of the inner TGC wheel will already be replaced by the new Small Wheel (nSW) project to reduce the number of fake triggers. Due to the increased particle flux and hitrates in the TGC, the readout electronics will have to be replaced for HL-LHC operation. This allows to

[10] **F**lame **R**etardant **4**, a common carrier material for circuit boards.

Property	Feature	Unit	Solenoid	Barrel toroid	End-cap toroids
Size	Inner diameter	m	2.46	9.4	1.65
	Outer diameter	m	2.56	20.1	10.7
	Axial length	m	5.8	25.3	5.0
	Number of coils		1	8	2×8
Mass	Conductor	t	3.8	118	2×20.5
	Cold mass	t	5.4	370	2×140
	Total assembly	t	5.7	830	2×239
Coil	Turns per coil		1154	120	116
	Nominal current	kA	7.73	20.5	20.5
	Stored energy	GJ	0.04	1.08	2×0.25
	Field range (in bore)	T	0.9-2.0	0.2-2.5	0.2-3.5
	Critical current (5 T, 4.2 K)	kA	20.4	58	60
	Temperature margin	K	2.7	1.9	1.9
Heat load	At 4.5 K	W	130	990	330
	At 60-80 K	kW	0.5	7.4	1.7
	Liquid helium mass flow	g/s	7	410	280

Table 2.5: *Main parameters of the ATLAS magnet system (summary, for full Table see [18])*

place as much of the signal processing electronics to the radiation-free zones as possible, therefore allowing the use of FPGAs to process the L0 trigger information.

2.2.4 Magnets

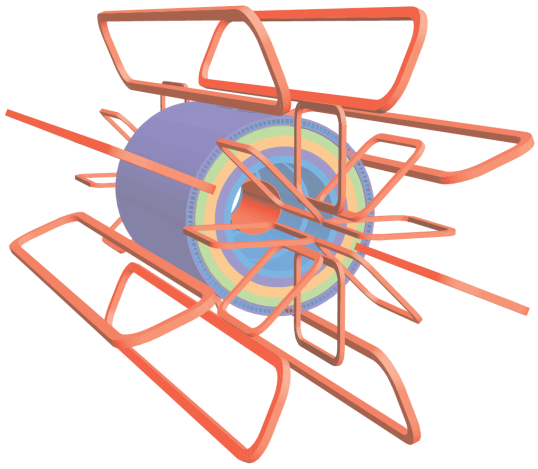


Figure 2.15: *Coil arrangement of the ATLAS magnet system. Shown are the barrel and the end-cap coils of the toroid magnet and the solenoid magnet (both orange). The solenoid winding lies inside the calorimeter volume. The tile calorimeter with the return yoke of the solenoid is also shown (outer blue cylinder). [18]*

The ATLAS magnet system is a hybrid system of four large superconducting magnets, which main parameters are given in Table 2.5. It measures 22 m in diameter and 26 m in length and stores a total energy of 1.6 GJ when powered. The generated field by the magnetic system covers a volume of approximately 12 000 m^3 (in which the field exceeds 50 mT). The magnet system consists of two fields: a solenoidal field covering the inner detector and the calorimeters and a toroidal field surrounding the muon detectors. The location of the magnets can be seen in Figure 2.2 on page 15. A schematic of the coil arrangement is shown in Figure 2.15.

The central solenoid generates a field of 1.998 T at its center with a nominal current of 7.730 A. It surrounds the inner detector and because of that had to be optimized to keep the material

thickness at a minimum, to allow a satisfying calorimeter performance, resulting in a material thickness of ~0.66 X_0 at normal incidence. In order to accomplish this, the solenoid magnet is located in the vacuum vessel of the liquid argon barrel calorimeter (also sharing the cryostat, see Section 2.2.2), saving two vacuum walls. The coil is made of a single layer winding of high-strength Al-stabilized NbTi conductor and stores an energy of 40 MJ. As the return yoke for the field, the outer steel support girders of the tile calorimeter are used (see Section 2.2.2). Charging (and discharging) of the magnet takes about 30 min. In the event of a quench, the released energy is absorbed by the cold mass of the magnet, heating it up to a safe maximum value of 120 K. Re-cooling it to 4.5 K takes about one day.

The toroidal field is generated by three magnet systems: the barrel and two end-cap toroids. Each system consists of eight coils. The coil windings of the toroid magnet are made of Al-stabilized Nb/Ti/Cu superconducting material. While in the two end-caps the eight coils are housed within a single cold mass each, in the barrel each coil is encased in an individual vacuum vessel. With a weight of 240 t each, the end-cap toroid magnets are the most heavy objects, that had to be lowered into the cavern. To generate the magnetic field in the barrel (0.5 T) and in the end-caps (1 T) a current of 20.5 kA is necessary. In case of a quench in the system, the stored energy of 1.1 GJ is, similar to the solenoid, absorbed by the cold mass, heating it up to a maximum spot temperature of 85 K. To distribute the energy over the entire system, four heaters in each coil bring the system from super conducting to normal conducting state within less than two seconds. After a heat-up, the systems needs about 50 hours to re-cool.

The power for the barrel section is supplied by a single 20.5 kA/16 V power supply, that powers the three magnets in series. For the solenoid, a smaller supply with 8 kA/8 V is used. The ramping is done with a speed of 3 A/s, leading to a maximum charge up time of two hours.

2.2.5 Trigger System

The amount of data, that ATLAS produces, is too large to be handled. Therefore the events, that are read out from the detector and stored are filtered. This is done in three trigger levels and an event builder. The first level is the level 0 trigger (L0). The L0 trigger stage uses a limited amount of the data from the detector, that is fast accessible. This data is analysed in less than 6 µs to make a decision, whether the data is to be analyzed further or discarded. It uses a feature extractor based on calorimeter, electromagnetic, and jet triggers and the fast trigger chambers in the muon system to search for high-p_T muons. With this information the L0 trigger accepts events at a rate of at least 500 kHz. The L0 decision is made in the central trigger system, incorporating topological triggering capability. In the next stage, the L1 system further reduces the acceptance rate to 200 kHz with a decision time of 14 µs. The L1 system involves track information within a Region-of-Interest (RoI), the entire calorimeter granularity in that region and a refined muon selection based on data from the MDT. In the L2 system, the full granularity of all detector subsystems inside the RoI is used, reducing the trigger rate to 3.5 kHz. The examination of this data takes up to 40 ms. In the last stage, the event filter, offline analysis procedures process the L1 data and create events with a

rate of 200 Hz. The event building process takes time in the order of magnitude of four seconds.

2.3 The ATLAS Inner Tracker

The Inner Tracker (ITK) is the innermost subdetector of the ATLAS experiment. It plays a fundamental role in the identification and reconstruction of electrons, photons, muons or tau-leptons emerging from the proton-proton and heavy ion collisions in tagging b-jets and in fully reconstructing certain hadronic decays.

To do so, the Inner Tracker needs to have the highest possible vertex resolution. This is achieved by providing a very high tracking resolution and measuring tracks as often and close to the interaction point as possible. In 2013 and 2014, during a long shutdown, an update of the inner detector has already been performed, in which an additional innermost layer, the Insertable B-Layer, was inserted into the inner detector to improve the vertex resolution. The close proximity of the inner detector electronics to the interaction point leads to very high radiation levels, though.

The electronics in the original pixel detector were designed to survive a radiation fluence of 10^{15} 1MeV n_{eq}/cm^2 (1 MeV neutron equivalent per cm^2), which is estimated to correspond to an integrated luminosity of 400 fb^{-1} [23, 24, 25, 26]. The radiation tolerance of the Insertable B-Layer (IBL) corresponds to 850 fb^{-1}. Simulations of the background radiation in the inner tracker at the HL-LHC have shown, that the fluence in the region of the pixel detector is in the order of magnitude of $2 \cdot 10^{16}\, n_{eq}/\mathrm{cm}^2$, which is way more than the pixel detector or the IBL can handle. In the regions of the SCT detector, the expected fluence is $\sim 10^{15}\, n_{eq}/\mathrm{cm}^2$. This is also significantly higher than the design tolerance of $2 \cdot 10^{14}\, n_{eq}/\mathrm{cm}^2$ [27].

Besides the exceeded radiation tolerances, bandwidth saturation is an issue during HL-LHC operation. Both the pixel and the SCT detectors are capable of handling occupancies of up to 50 pile-up events per bunch crossing. For operation at the LHC (~23 pile-ups), this bandwidth includes a safety factor of ~ 2. Due to limitations in the buffering and in the readout, the efficiency of the pixel detector drops, if a pixel hit rate of $0.2 \sim 0.4$ hits / 25 ns bunch crossing is exceeded, leading to major data losses. This is expected for luminosities larger than $3 \times 10^{34}\, cm^{-2}s^{-1}$. Similar effects are expected for the SCT. For the TRT detector, the high pile-up would lead to an occupancy approaching 100%, leaving no room for a safety margin.

To allow satisfying operation in the environment of the HL-LHC, with much harsher radiation and occupancy conditions, the entire inner detector is being redesigned in the Inner Tracker project (ITK). The guiding principle in designing the new ITK is the anticipated physics program at the HL-LHC. Its main task is the reconstruction of primary vertices and the identification of jets to hard scattering events of interest. To to this, the new ID needs sensors with finer granularity than the old ones, because it has to cope with the very high pile-up and it has to be able to reconstruct tracks in the cores of multi-TeV jets. Currently there are more than one possible layouts, being studied for the ITK, which share certain design requirements regarding layout and capabilities:

- measuring of the transverse momentum and direction of isolated particles
- reconstruction of vertices of pile-up events
- identification of secondary vertices in b-jets with high efficiency
- measuring of tracks in the cores of high energy jets with good double-track resolution
- identification of the decay of tau leptons, including impact parameter information
- reconstruction of tracks associated with converted photons

A layout requirement for the upgraded tracker is the replaceability of the first two pixel layers in a standard opening of the experiment without removing the beam pipe. It should also be possible to replace the outer pixel layers and discs without any impact on the strips during a longer opening. For further details of the requirements for the ID after the HL-LHC upgrade, see [28].

Currently there are four possible layouts for the new inner tracker under discussion: the baseline layout and three alternative layouts. The baseline layout is used as a reference for the comparison with the other alternatives, the conical, the alpine, and the five pixel layers layout. In these layouts, position, support and orientation of the pixel sensors are varied to find the best possible detector performance.

2.3.1 Baseline Layout

The sensor arrangement of the baseline layout is shown in Figure 2.16 on the next page. The layout reflects the classical barrel and disc structure, as it is already used in the previous silicon trackers. In the barrel part, the layout consists of four pixel layers starting at a radius of 39 mm, followed by three short-strip layers and two long-strip layers. The forward region is covered with six pixel and seven strip layers. At radii of 110 mm and 345 mm, the tracker will be supported by an inner support tube (IST) and a pixel support tube (PST), respectively. The active area and number of channels is shown in Table 2.6. Outside of the tracker, a polythylene moderator reduces the energies of neutrons entering from the calorimeters and absorbs them, to decrease the 1 MeV neutron equivalent silicon damage in the tracker.

Detector	Si area [m^2]	Chan. [10^6]
Pixel barrel	5.1	445
Pixel end-cap	3.1	193
Pixel total	**8.2**	**638**
Strip barrel	122	47
Strip end-cap	71	27
Strip total	**193**	**74**

Table 2.6: *Active area and number of channels of the ITK. [29]*

To keep the tracking inefficiencies at a minimum and to provide better precision, the layout is optimized to minimize the overall detector material. In the inner two pixel layers, this is achieved by the usage of lightweight carbon foam structures.

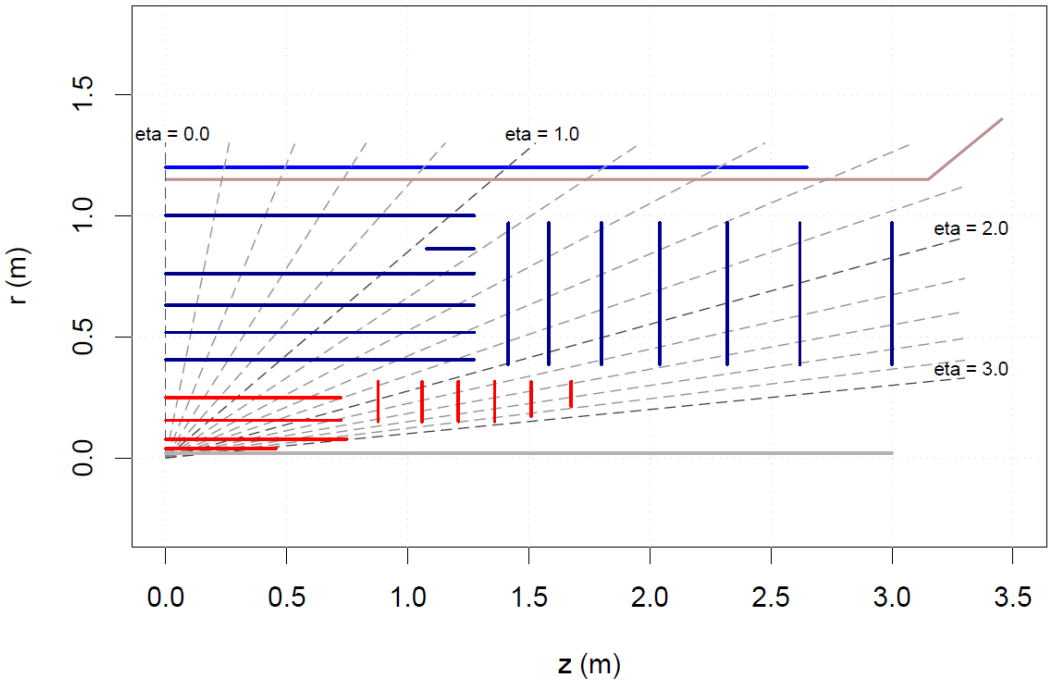


Figure 2.16: *The baseline layout for the new inner tracker. Shown are the beam pipe (gray) pixel layers and discs (red), the strip layers and discs (dark blue) and a polythylene moderator (blue). [29]*

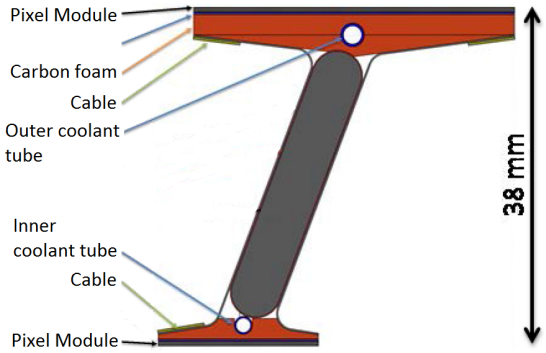


Figure 2.17: *Cross-section of the I-beam support structure. [29]*

These I-beam called structures (see Figure 2.17) carry the detector modules of both layers and provide sufficient stiffness to allow precise spacial resolution, without the need for additional support structures. Inside the I-beam, close to the module layers, two titanium pipes cool the structure with evaporating CO_2. The outer pixel layers also are carried by carbon foam, that encloses a titanium pipe. The stiffness is provided by an omega shaped carbon fiber laminate. Additional reduction of the detector material is accomplished by moving services of pixel inwards to small radii and then out of the detector along the z axis. This way, service material is removed from the tracking region as fast as possible. The overall material contribution of the pixel detector is shown in Figure 2.18. Except some small regions, it stays below $0.7\,X_0$ up to $|\eta| = 2.7$.

The current detector has shown that at high pile-ups, at least 11 hits per track are required to minimize the number of fake tracks. The baseline layout aims to have

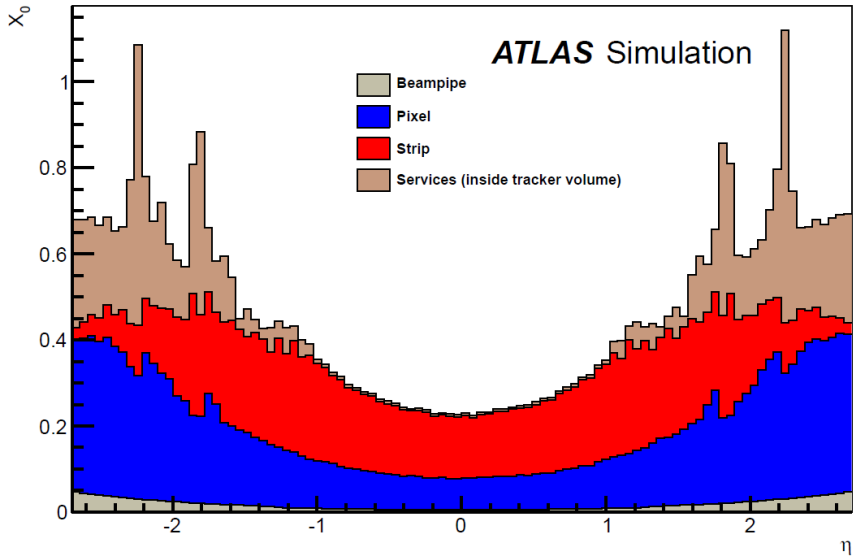


Figure 2.18: *Material contribution of the inner tracker in X_0 as function of η. [29]*

at least 14 silicon hits per track (including possible dead readout channels and each strip layer providing two hits). To close a gap in the strip coverage, which allowed only 12 hits for tracks in the region around $\eta = 1.1$, a shorter ("stub") strip barrel is foreseen. Figure 2.19 shows that the number of hits for primary vertices within a region of $z \pm 15\,\text{cm}$ up to a pseudorapidity of $|\eta| = 2.5$ is not smaller than 14.

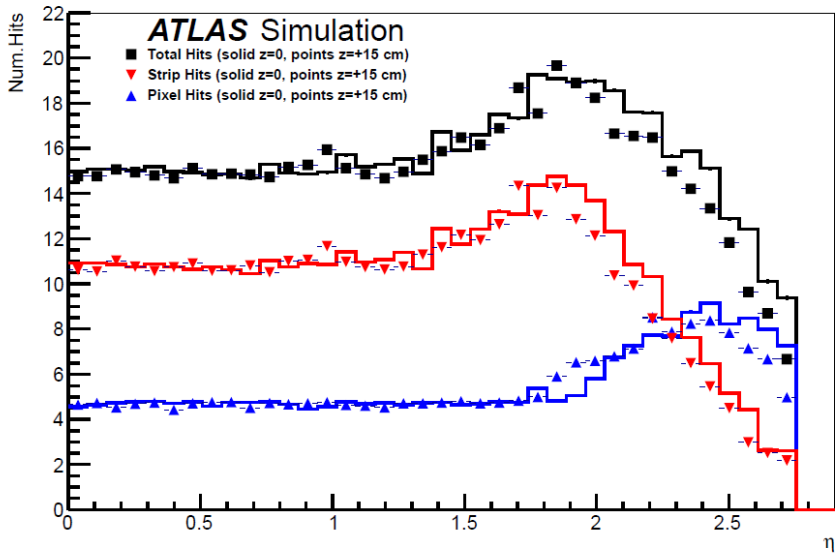


Figure 2.19: *The simulated number of hits in the baseline layout, which are produced by muon tracks originating from the center of the detector (solid) and from $z = 150\,\text{mm}$ (points) with $p_T > 5\,\text{GeV}$ as a function of η. [29]*

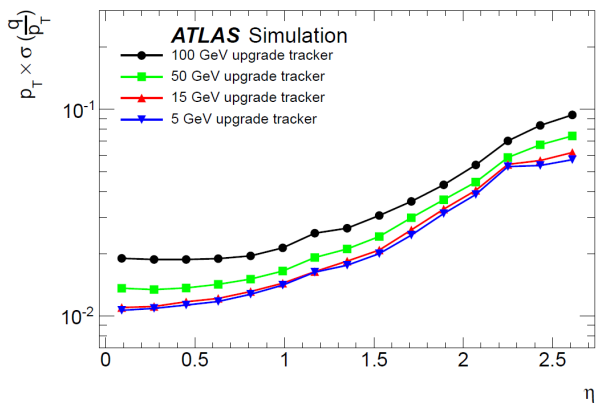


Figure 2.20: *Momentum resolution of the baseline tracker layout. [30]*

For the best possible momentum resolution, the layout maximizes the trajectory lengths of particles inside the solenoid and measurements are made in locations, where the variations of resolutions are minimal. The outermost strip barrel layer is placed at the largest radius as mechanically possible (with respect to the moderator and other services) as well as the last disc is placed at the largest possible z coordinate. The expected momentum resolution has been simulated with muon tracks with p_T>5 GeV as a function of η and is shown in Figure 2.20. The simulations have also shown, that the momentum resolution is largely independent of the level of pile-up [29].

2.3.2 Alternative Layouts

Conical Layout

Due to necessary service boards at the end of each stave (EoS-cards), the gap between the end of the barrel cylinder and the first disc cannot be removed (see "stub"-barrel in the baseline layout on page 32). The conical approach to solve this problem is to use staves with bent ends. This geometry was inspired by the Babar vertex detector. The construction of bent staves is no more complicated than the construction of straight staves, it only requires different tooling. In Figure 2.21 a prototype of an end section of a bent stave is shown. This prototype has taken the same mechanical testing as the straight staves and showed equal performance.

Figure 2.21: *Prototype of a bent stave. [31]*

The conical layout has three advantages. The first is, that the radius of the end-cap discs can be reduced to match the barrel, as the EoS services move to smaller radii. This simplifies the mechanical support structures. Moving the EoS cards to lower radii implies moving them to higher η, shifting the dead material to less critical areas. The third advantage is the decreased crossing angle of high η tracks passing the bent areas of the stave, reducing the material seen by the particle in the critical η ranges.

For comparison reasons, the studied conical layout was designed with the baseline layout as basis. This means that only the outer two pixel layers have bent staves, while the inner layers were not changed. As the conical layout offers a lot of flexibility to the placement and the length of the staves, two approaches are studied. In the first approach, the barrel layers are placed equidistant between the inner pixel layers and the

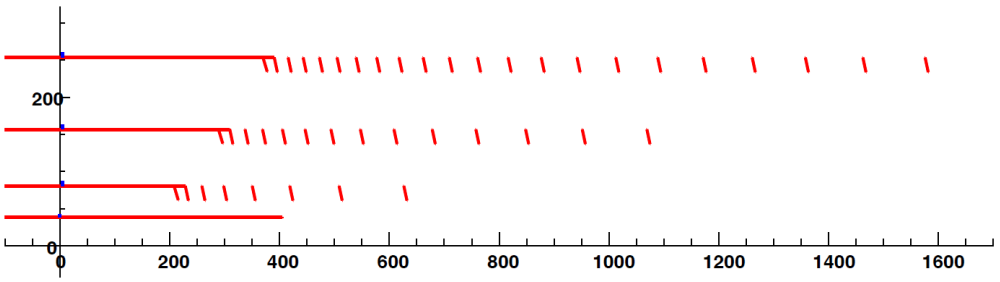


Figure 2.22: *Arrangement of the pixel sensors in the alpine layout. [32]*

strip layers. The second approach does not change the radii of the staves, but shortens the lengths to reduce the silicon area and the cost of the detector. In both cases, the hermecity of the detector has not changed. The total active area of the conical layout can be estimated to $7.68\,\mathrm{m}^2$ for the first approach and $6.85\,\mathrm{m}^2$ for the second.

In general, the performance of the conical layout is, in terms of material budget, number of hits/track and momentum resolution either equal to the baseline layout, or better. For detailed information about the performance of the conical layout, see [31].

Alpine Layout

The alpine layout is inspired by an ideal geometry of a tracker for a hadronic collider where all tracks cross the sensors perpendicularly. In practice, this is not easily realizable with rectangular sensors. Therefore the alpine staves combine the classical barrel layout in the central section with modules mounted with increasing inclination at high η (see Figure 2.22). As the innermost layer is as close to the beam as possible, it remains unchanged. With this module geometry, the barrel section (where the sensors are arranged in parallel to the beam pipe) is shorter than in the baseline layout and the use of discs becomes obsolete. This leads to a reduction of active area to $4.6\,\mathrm{m}^2$ and thus lower cost.

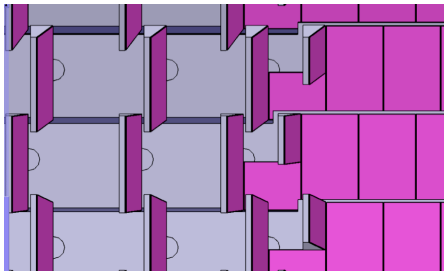


Figure 2.23: *Transition from the barrel to the end-cap region in the alpine layout. [32]*

To realize the cylindrical arrangement of the alpine staves with a sufficient coverage, while avoiding mechanical conflicts is not straight forward. A sketch of cylindrically arranged staves is shown in Figure 2.23. To avoid conflicts between the standing modules, neighboring staves are shifted by about 10.3 mm to each other. Conflicts between the standing modules and the neighboring stave core are avoided by reducing the stave width on one side in the end-cap region. In the transition region, the stave is equipped with a barrel module and a standing module of half size to ensure hermecity, as there the stave width cannot be reduced.

The performance of the alpine layout still needs to be thoroughly tested to compare it to the other concepts. [32]

Five Pixel Layers

Another layout concept adds a fifth pixel layer to the tracker. This additional pixel layer allows better two-particle separation and more robust pattern recognition. This layout shortens the outer pixel barrel layers and removes the stub barrel from the strips. For further details, see [33].

2.3.3 Pixel Modules

The smallest electrically controllable unit of the pixel detector is the pixel module. The module is a composition of a sensor chip and between two to six readout chips. The readout chips and the sensors are connected via bump bonding in case of passive sensors or by gluing in case of active sensors (see 2.3.4). The number of readout chips, and thus the size of a module depends on its location in the detector. In the innermost layer, 2-chip-modules (two readout chips connected to a sensor of $4 \times 2\,\mathrm{cm}^2$) are used to accommodate the limited space. In three remaining outer barrel layers quad-modules are used (four readout chips cover a sensor of $4 \times 4\,\mathrm{cm}^2$). Hex-modules (modules with six readout chips covering a sensor of $6 \times 4\,\mathrm{cm}^2$) are used on the discs (together with smaller module types).

Two generations of Front End (FE) readout chips will be implemented in the new pixel detector. For the outer two layers, a C revision of the FE-I4 readout chip, which is also used in the IBL, is foreseen. This new revision will add compatibility with multi-chip modules and the new trigger system. For the inner layers, R&D for a new FE-5 chip using a 65 nm technology is ongoing. The FE-5 chip has similar characteristics as the FE-I4 chip in size, power and IO capability, but provides a smaller pixel size.

In the current pixel detector (without the IBL), a module consists of a sensor chip, which is bump-bonded to the readout chips. Onto the other side of the sensor, a thin Kapton flex (called module flex) is glued, which carries passive analog and active digital electronics for decoupling and signal readout, respectively. The connection of the readout chip to the module flex is done via wire bonding, while the connection of the module itself to the stave flex (see Section 2.3.5) is done with a Kapton flex cable, connected to the module flex. This Kapton flex cable supplies power and data lines. [34] The module concept foreseen for the HL-LHC pixel detector adopts the current concept in most, but not all aspects. All digital readout electronics move into the readout chips, leaving only passive circuitry on the module flex.

An alternative to the wire-bond connection of the readout chip to the module flex is currently under investigation. Here the connection of the readout chip to the module flex is done with Through Silicon VIAs (TSV), which makes the bond-wires obsolete and therefore allows further material reduction and higher reliability, as wire-bonds are a common cause of defects in the detector [35].

2.3.4 Pixel Sensors

The choice of a sensor type for the pixel detector is mainly a choice of durability and radiation tolerance, as the sensors will have to withstand an expected fluence of $1.4 \cdot 10^{16}\, n_{eq}/\mathrm{cm}^2$ in the innermost and $1.7 \cdot 10^{15}\, n_{eq}/\mathrm{cm}^2$ in the outermost layer

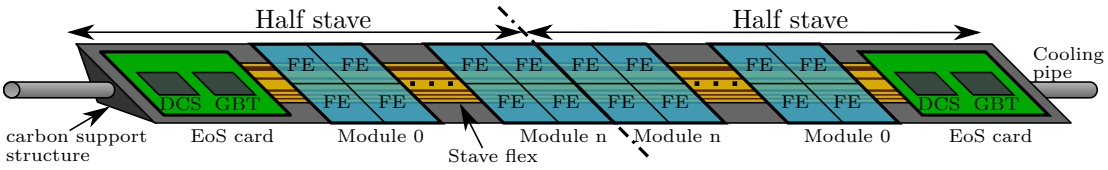


Figure 2.24: *Schematic of a stave creating the barrel section of ITK.*

over the scheduled 3000 fb^{-1} of data taking. These numbers do not include any safety factors, yet. To enhance the radiation tolerance and lower the material budget, the pixel sensors will most likely be thinned down to 150 µm. For the outer two layers, n-in-p planar sensors are assumed, as these types of sensors have proven their radiation tolerance for fluences of $5 \cdot 10^{15}\, n_{eq}/\text{cm}^2$ and 1 kV bias voltage. To reduce the inactive regions at the edges of the sensor chips to 100 µm, longer pixels are used here. For the innermost two layers, n-in-n sensors are assumed, as this type of sensors has proven its reliability at fluences up to $10^{16}\, n_{eq}/\text{cm}^2$. [32]

For the inner layers the R&D for a sensor choice is still ongoing. Currently four types of senors are under discussion:

- planar sensors [36, 37]
- 3D sensors [38]
- diamond sensors [39]
- monolithic active sensors [40, 41]

For a decision for one of these technologies, further R&D is necessary. The main R&D focuses on sensor thinning, reducing the depletion voltage for planar sensors and cost reduction for the 3D and the diamond sensors. The R&D for the monolithic sensors, which combines sensors and preamplification in one chip in HV-CMOS technology is still in the early stages. A massive reduction of cost (no bump-bonding necessary) can be expected, but the ability of fast sensor readout in high radiation environments has yet to be shown.

The size of the pixels in mainly determined by the readout chips. The pixel size for the FE-I4 rev. C is assumed to be $50 \times 250\,\mu\text{m}^2$, for the FE-5 chips a pixel size of $25 \times 150\,\mu\text{m}^2$ is targeted. [32]

2.3.5 Pixel Staves and Discs

The construction of the barrel part and the forward discs (if there are some) is similar in all possible layouts, described above. This section describes the structure of the barrel and the disc sections in the baseline layout. The barrel part of the pixel detector consist of a cylinder shaped assembly of long carrier structures, the staves, which are slightly tilted (by 14°) and shingled to avoid gaps (similar to a radial fan). A stave consists of a long carbon foam support structure, housing the cooling pipe(s), the detector modules, a flex cable and an electronics boards at both ends, the so called End-of-Stave card (EoS). A sketch of a stave is shown in Figure 2.24. The flex cables connect each module

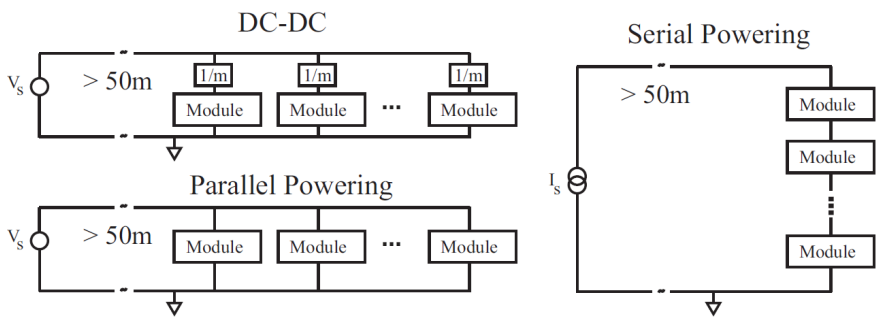


Figure 2.25: *Schematics illustrating the parallel and serial powering schemes. [29]*

to an EoS-card. Thereby the stave is electrically organized in two half-staves, as each module is only connected to that EoS-card, to which it is closer. On the EoS-card, a data multiplexer is located, which serializes the module data coming from the flex cable, and transmits it to the optical link. The current candidate for the data multiplexer is the GBT[11] chipset [42]. The heat generated by the electronics is dissipated through the cooling pipes, located in the stave, by a CO_2 cooling system.

The discs are also made of carbon foam core with an embedded cooling pipe. The electrical organization is similar to the staves, as all electrical connections are passed through an EoS-card. In this case, the term end-of-stave, does not really fit and can be generalized by end-of-substructure. The location on the EoS-card is not yet decided, as well as the exact module arrangement.

2.3.6 Powering

The powering of the ATLAS tracker is a challenge, due to the increased sensor granularity of the tracker and the need of low material budget. In the pixel detector, the reuse of the existing low voltage cables is planned, which limits the intrinsic supply granularity by the power supplies. As the current powering scheme, where each module has its own power lines, is not suitable, for both, the pixel and the strip system, two options of powering exist and are currently in R&D: parallel powering with DC-DC converters and serial powering. A comparison scheme is shown in Figure 2.25.

In the parallel powering scheme, DC-DC converters are used to reduce able diameter, by lowering the supplied current and provide voltage regulation for each module. The DC-DC converters being developed for the strip system have been tested on a four module stave without a noise increase compared to a single module powered by a low noise supply. Rudimentary DC-DC converters have been implemented and tested in the FE-I4-A chip, but this development has not been continued as of today.

The serial powering scheme is currently the baseline for the pixel detector. In this scheme, a constant current is supplied for a chain of modules. Each module in this chain has its own shunt regulator, providing the regulated supply voltage for the front end electronics. In the strip system, a Serial Power Protection ASIC (SPP) in combination with pass transistors built into the readout chips forms the shunt regulator. The SPP

[11] GigaBit Transceiver

chip can also be controlled by the detector control system and shunt the complete current to switch off the readout electronics if necessary [43]. In the pixel system, the shunt regulators are completely included into each FE chip. The FE-I4 chip used for the IBL already contains the necessary regulators. Prototyping of a serial powered stave with FE-I4B chips is currently ongoing [44].

The control of the high voltage supply of the pixel sensors is foreseen to take place in the power supplies, including control and monitoring of the current and the voltage. In the strip system, there is not enough space to provide individual HV supply for each sensor. To avoid losses through shared lines, an approach is investigated where the high voltage of a sensor can be switched inside the detector by the detector control system.

2.3.7 Optical link

The data communication between the pixel modules and the off-detector electronics at the HL-LHC is realized as a combination of electrical and fibre optic data transmission. A detailed plan of the pixel detector readout has not been made, yet. Thus, this section will only outline a likely implementation of the data path from the pixel modules to the off-detector electronics for the case of a serially powered pixel detector.

Data generated by the detector modules is transmitted electrically via LVDS[12] lines on the stave flexes to the EoS-cards. On the EoS-cards, the lines from each module or readout chip are connected to a serializer and multiplexer. The multiplexed and serialized data is transmitted via Micro Twinax cables to the optoboards, which are located outside of the tracker, to limit radiation exposure and to allow easier access. The optoboards make the opto-electrical interfaces, which connect the electrical lines to optical fibres. The optical fibres transmit the module data to off-detector electronics, where the data is converted back into electrical signals and then transfered to the DAQ system for processing. [29]

[12] **L**ow **V**oltage **D**ifferential **S**ignaling

Chapter 3

Controlling a detector

To operate an experiment like ATLAS efficiently, a continuous acquisition of data with best possible quality is mandatory. The quality of the data taken is significantly determined by the operating conditions of the detector. Reliable physics data can only be measured, when the detector works under optimal operating conditions. If the optimal case cannot be guaranteed, the exact operating conditions of the detector must to be known, to judge the quality of the aquired data. To ensure the best possible detector operating conditions, the ATLAS detector has a Detector Control System, or DCS. This DCS monitors and steers the detector on different levels to perform three main tasks.

The first task of the DCS is controlling the detector. The ATLAS detector consists of a huge amount of individually controllable parameters to configure the detector operation. Operating all units of the detector by hand is simply impossible. Therefore the DCS provides a user interface, which organizes the detector parameters and assists the user in the operation of the detector. To minimize the dead time in case of a detector incident, the user interface is optimized to minimize the time, a user needs to perform certain tasks. This is done by assisting scripts, e. g. for the start-up procedure or preparing the detector for data taking.

A further task of the DCS is the protection of the detector. The DCS monitors the environmental conditions in the detector volume and the operating conditions of detector sub-units. This includes humidity, temperature, voltages and currents. In the case of one or more of these parameters exceeding certain thresholds and becoming dangerous to the detector health, the DCS tries autonomously to prevent any damage to the detector. In most cases, this is done by switching off the affected detector parts. This section of the DCS is known as the interlock system and will be described in more detail in the safety path in Section 3.1.1.

Another of the DCS' tasks is the provision of a DCS-data-quality flag. This flag shows the data quality management, that the detector is working under known conditions. This kind of flag is necessary, to recognize corrupted data, which could originate from i.e. malfunctioning detector modules.

In this chapter, a possible implementation of a DCS for the ATLAS pixel detector at the HL-LHC is described. Thereby the serial powering concept is taken as the baseline powering concept. Possible modifications necessary for a detector operation

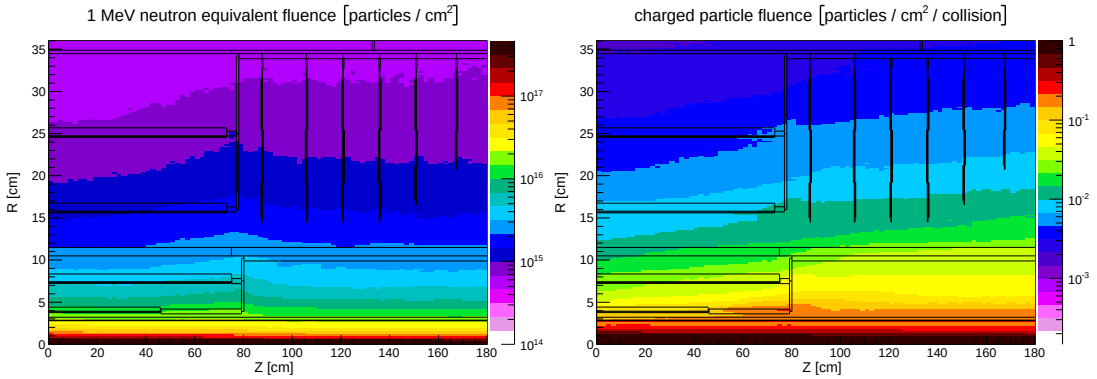


Figure 3.1: *Simulated background radiation for the pixel region in the inner tracker. Shown are the neutron equivalent fluence (left) and the charged particle fluence (right) [27]*

with parallel powering will also be given.

3.1 DCS Requirements

The requirements for the ATLAS pixel DCS after the upgrade to the HL-LHC will change significantly, due to the replacement of the inner tracker. The number of detector modules, which have to be controlled will increase approximately by a factor of four. The DCS cables, going from the detector cavern to the counting rooms, where the DCS crates and computers are located however, are currently not supposed to be exchanged. Thus the number of data lines per detector element available for DCS data of the new pixel detector will be fairly low and new concept of data multiplexing is mandatory, as a decrease in the monitoring granularity is not an option.

Due to the increasing instantaneous luminosity, the radiation exposure of the electronics in the pixel detector volume will also rapidly increase. FLUKA[1] simulations of the inner tracker region have shown, that fluences of up to $2 \cdot 10^{16}\, n_{eq}/\mathrm{cm}^2$ have to be expected in regions close to the beam pipe. As most of the background radiation comes from the beam halo and not from the p-p-collisions in the interaction point, there is no safe spot for the location of DCS components for the innermost layer which is shown in Figure 3.1 in the left plot. The right plot of Figure 3.1 shows the charged particle fluences, which contribute significantly to the chance of single event effects (SEE) in integrated electronics[46]. A high chance of SEE, and thus a high number of radiation induced bit-flips during operation, makes the design of reliable electronics challenging. For details about the impact of radiation to circuits and consequence-limiting measures, see Sections 4.4 and 4.5. However, reliability is not only an issue on short time scale. All components used in the tracker volume have to have a high level of long time reliability, as once installed, access is not possible for many years.

Another requirement for the DCS is the low material budget. The increased density of sensors and electronics in the inner detector and the demanded high precision of the detector leave only little space and material for a control system. The high electronics

[1] FLUKA (**FLU**ktuierende **KA**skade) is a fully integrated Monte Carlo simulation package[45].

Detector element	Parameter	Type of supervision
Detector modules	Low voltage	Switching on and off Monitoring of voltage and current Adjustment of supply voltage/current (depending on the powering scheme)
	High voltage	Switching on and off Monitoring of voltage and current Adjustment of supply voltage
	Temperature	Monitoring of module temperature Protection against overheating
EoS-card	Low voltage	Switching on and off Monitoring of voltage and current Adjustment of supply voltage
	Temperature	Monitoring of EoS-card temperature
	Reset	Provision of reset signals to the GBT
Optical interface	Low voltage	Switching on and off Monitoring of voltage and current Adjustment of supply voltage
	Temperature	Monitoring of optical interface temperature
	Reset	Provision of reset signals to data transceivers
Environment	Temperature	Monitoring of environmental temperature
	Humidity	Monitoring of environmental humidity

Table 3.1: *DCS relevant detector elements and their status of supervision.*

density also demands for a DCS with very low power consumption. In case of a failure of the cooling system, the DCS still needs to be operational, without generating too much heat in the detector.

Hence all these requirements, a completely new DCS concept is being developed. In this concept, the decreased amount of space and material budget and the high radiation is remedied by the use of Application Specific Integrated Circuits (ASICs) for DCS components inside the detector volume.

Detector elements, which require supervision by the DCS are the detector modules, the EoS-cards, the optical interface and the environment in the detector volume. Thereby, the high and low supply voltages and the currents of all electrical components are monitored and controlled. For some components, like the EoS-cards and the oprtical interfaces, additional reset signals are provided. As in most cases, overheating is the direct cause of damage in the detector, the temperatures of all detector components is monitored. Table 3.1 shows all parameters of the detector, which are relevant to the DCS and their type of supervision. The term GBT in Table 3.1 and all following Figures and Tables is thereby stating the GigaBit Transceiver [42] as a candidate for a data multiplexer (see Section 2.3.5).

3.1.1 Three Paths

The DCS concept for the ATLAS pixel detector at the HL-LHC is grouped into three paths, which differ in granularity, precision, availability and reliability. An overview of the DCS paths is given in Figure 3.2 on the next page. As detector safety has

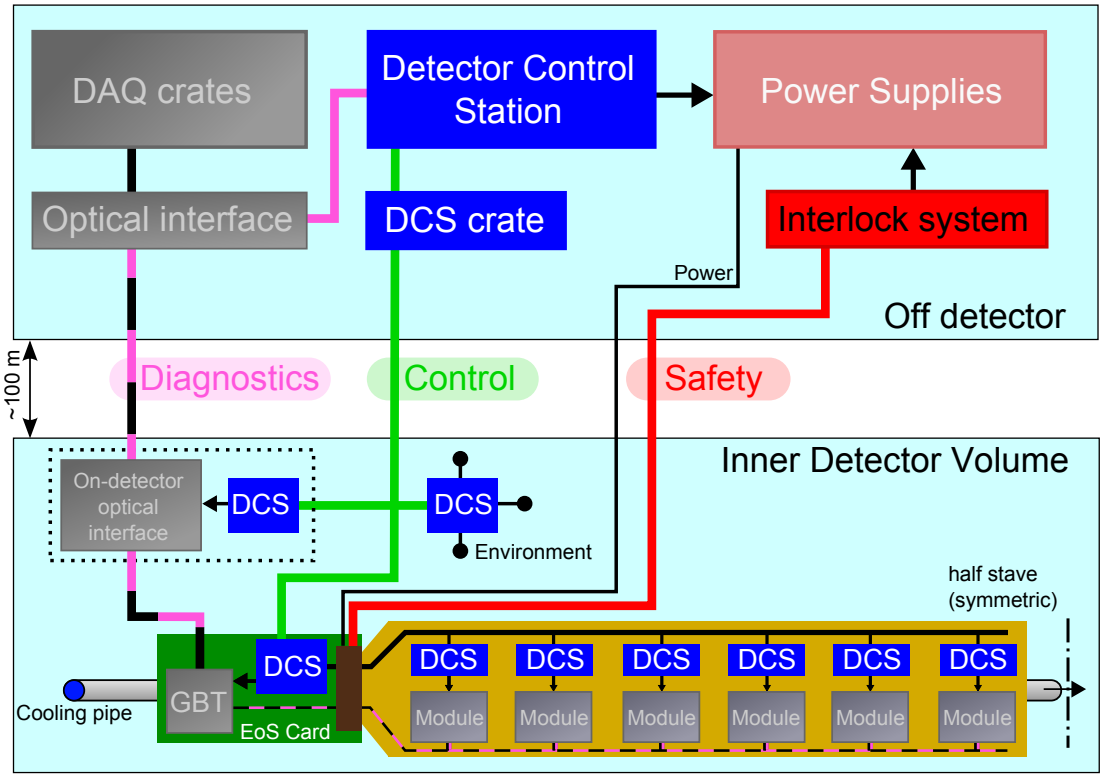


Figure 3.2: *Diagnostics, Control and Safety paths in the ATLAS pixel DCS.*

to be ensured at all times, items of the *Safety* category require the highest level of reliability. *Control* manages the user interaction with the detector. This includes operation, start-up and the commissioning phases. Components of the Control path need a high reliability, to ensure stable operation. The *Diagnostics* path allows to tune the detector performance. Information from this path should be available on request.

Safety

The safety of human beings and the detector has the highest priority. Therefore the *Safety* system is completely independent from any other system. The highest possible level of reliability is achieved by avoiding the placement of active components in inaccessible areas. Placing the equipment further outside of the tracker allows access for possible repairs. To be independent of any kind of initialization procedure or software loading, the *Safety* path is realized as a completely hardwired system, the so called interlock system.

Over-temperature poses the highest risk of permanent damage to the detector modules. Therefore, the temperature of the detector modules has to be monitored all the time, and a fast response to overheating is mandatory. This is achieved by passive temperature sensors, which measure the temperature of the cooling pipes. Each sensor has its own lines, connecting it directly to the interlock system. In case of modules overheating, the interlock system immediately inhibits the power supply of the corre-

sponding detector parts, avoiding further heat up. Due to the lack of active components inside the detector, this kind of system is able to run at all times, independent of the detector state. Neither high granularity nor precision is required.

This kind of interlock concept has also been used to protect the current detector, in which case it has proven its reliability.

Control

The Control path supervises the entire detector, including the hardware of the Data Acquisition system. It provides an intelligent user interface to the detector. The Control path supervises all powering units for the pixel detector, and therefore has to operate very reliably. Actions are partly taken directly at the power supply and partly on individual detector modules. The segmentation thereby depends on the type of power, being supervised. The Control path is supposed to have its own data lines, independent from the optical link.

The high voltage supply for the pixel sensors is supervised directly at the power supplies. This includes switching the high voltage on and off, modifying the voltage set and the current compliance as well as monitoring both values. A signal from the interlock (safety) system always has higher priority and can overwrite any control commands.

Concerning the low voltage supply for the read out electronics, control and monitoring just on power supply level is only sufficient for the interlock signal, inhibiting any power output. Depending on the powering scheme (serially or parallel) different concepts for the supervision of the detector modules are necessary. In case of parallel powering, the switching of a module and the current monitoring can take place at the DC-DC converters, while the voltage monitoring should take place as close to the module as possible, using sense wires. In case of serially powered modules, only the current monitoring can take place at the power supply level, while for switching individual modules on and off, and for the voltage monitoring, a local DCS entity close to the module itself is necessary. A concept for the supervision of serially powered modules is described in Section 3.2.1.

Diagnostics

Information from the Diagnostics system is used to tune the detector to its optimum performance. Thus the granularity should be very fine, and the precision high. However high granularity and precision also means a high amount of data. As the diagnostics data is only required on demand, and not all the time compared to the other paths, it can be embedded into the optical link. This way, no further material is added to the detector in form of data lines.

The segmentation of the diagnostics system is per readout chip. Each readout chip has thereby an ADC and an analogue multiplexer to measure various voltages, currents and temperatures on sub module level. To receive the information of the diagnostics system, a mechanism is needed, which separates the physics data and the DCS data from the optical link on off-detector level.

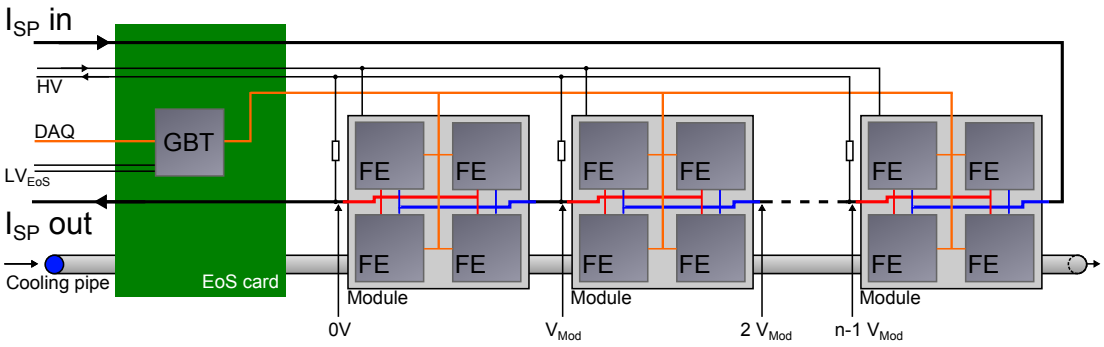


Figure 3.3: *Schematic of a serial powering chain of a half stave (without DCS). Shown are four-chip modules. The thick black lines show the power line, thin black lines show the high voltage supply. The orange lines (and the GBT) belong to the DAQ.*

3.2 Controlling a serially powered stave

The actual baseline for the powering of the pixel detector in the HL-LHC is a serial powering scheme. The serial powering has a lot of advantages in terms of cost and material budget. Compared to the direct powering of each module, where each module needs an own set of cables and a power supply, a serial powering chain of n modules needs only two cables and one power supply. This reduction of cables also bears a great risk. In case of a broken wire or a malfunctioning module, an entire powering chain may fail. Due to the shared power supply of the modules, noisy modules can easily influence other modules in the chain.

In Figure 3.3, a schematic of a serial powering chain is depicted. A constant current I_{SP} is flowing through a serial powering chain. The current source needs to be capable of generating voltages of n times the supply voltage of a module plus the voltage drop on the cables. Each module has its own set of regulators, generating the supply voltage of the module from the constant current. In the actual concept, these regulators are implemented into the readout chips. The current itself has to be high enough, to supply the analog and digital circuits in each readout chip in a module and the current, which the regulators need to work. More information about the operation of a serially powered pixel detector can be found in [47].

Each module in the chain has a different ground level. To be more precise, the supply voltage level of the n^{th} module is the ground of the $n-1^{th}$ module and only the 1^{st} module shares its ground level with the EoS card. The DCS requirements demand, that each module can be switched and monitored individually. To switch off a module in a serial powering chain, it needs to be bypassed. This requires a switch next to the module, which can shunt the entire current of the chain. The location of the switch should be as close to the module as possible, to keep the powering lines as short as possible. To monitor the module voltage precisely, it has to be measured as close to the regulators as possible, as well. The use of sense wires for each module would add significant material to the detector.

To keep the material budget at a minimum, the switching and the monitoring of each module will be prformed by an external ASIC. These ASICs are located on the

stave flex, as close as possible to the corresponding modules. The next sub section describes a concept to monitor and control the detector modules remotely from DCS computers. In this concept, the mentioned ASIC is called DCS chip.

3.2.1 A Control Path for serial powering

According to the demands and restrictions described above, a possible implementation of the Control path has been developed in terms of this thesis. For this, the following considerations have been made.

Commands generated by the detector control station must be distributed to individual modules, groups of modules or all modules in the detector. Vice versa, locally generated feedback data must be sent back. To collect and transmit these kinds of data, the so called DCS Network is spanned in the detector. This network is the key component of the *Control* system inside the detector volume. It uses two types of nodes in form of two ASICs, the DCS Controller and the DCS Chip. Between these two nodes and the DCS crates in the detector control station, two types of data buses transmit commands and data. For the transmission between the DCS computers and the DCS controller, the CAN[2] protocol is used. The CAN bus, originally developed by the Robert Bosch GmbH for automotive industries, is a very fault-tolerant serial bus[48]. Its reliability and suitability for experiments in high energy physics has been proven in the current detectors at the LHC as well, and thus will also be used in the HL-LHC detectors. Between the DCS Controller and the DCS Chip, a modified version of the Inter-Integrated Circuit (I^2C) protocol, I2C-HC[3], is used. The I2C-HC protocol extends the I^2C-Protocol by a four bit Hamming code, to allow error detection. I2C-HC originates from a previous concept for a control system for a detector with individually powered detector modules.

The network was split into two bus protocols for different reasons: The CAN bus was chosen to benefit from the robustness of the bus, the capability of spanning long distances and to be compatible with the rest of the ATLAS control system, which uses CAN as a quasi standard. Though, the CAN protocol is very complex and requires a lot of logic, as well as a continuous and precise clock inside each node. Hence, to reduce the required chip area and the energy consumption of the DCS chips, the I2C-HC bus was chosen for communication on stave level. The I2C-HC protocol is much more simple than the CAN bus and requires less logic, giving the possibility to produce smaller DCS chips. Besides that the I2C-HC bus allows to clock the DCS chips only during active communication, reducing the power consumption. A more detailed discussion about the searching and the suitability of buses for that concept can be found in [49].

Although the general conditions have changed with the swap from individually powered modules to serially powered modules, the I2C-HC will also be used in the current DCS concept, as it has proven its reliability in previous tests [50, 51]. An option to reduce the number of lines even further could be a one wire bus (see 5.2.1). The reliability of such a bus has to be evaluated in the future, though.

[2] **C**ontroller **A**rea **N**etwork

[3] **I**nter-**I**ntegrated **C**ircuit with **H**amming **C**ode

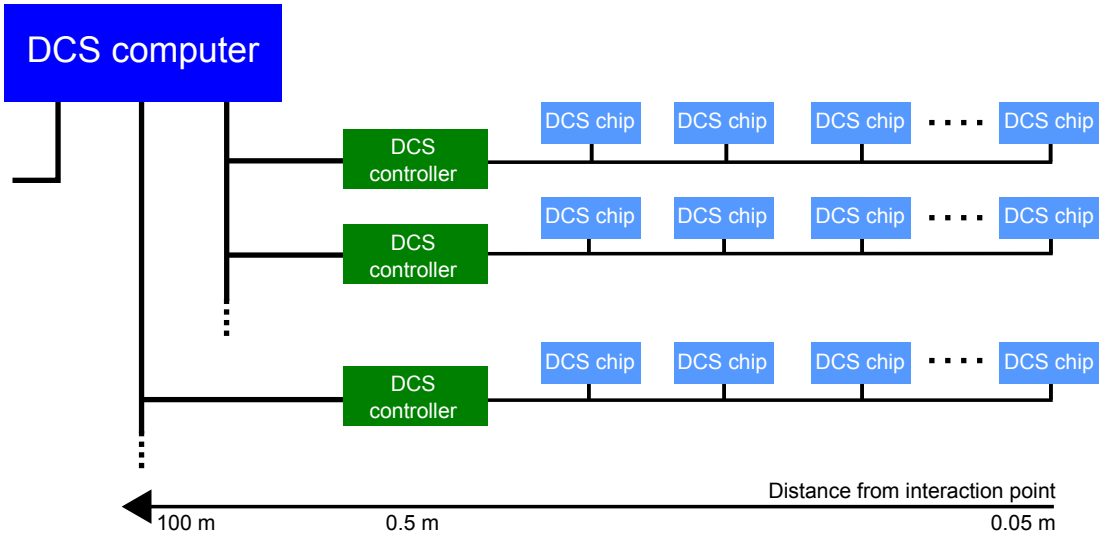


Figure 3.4: *Schematic of the DCS network. The thick lines on the left side of the picture symbolize the CAN busses, the thin lines on the right side symbolize the I2C-HC busses.*

Figure 3.4 shows a schematic of the DCS network with its two buses and two devices. Each powering chain has its own I2C-HC bus and DCS controller. The exact number of DCS controllers connected to one CAN bus is not yet decided, as of the writing of this thesis.

I2C-HC bus

The common I^2C-bus, developed by the Phillips company in 1982 is a bidirectional two-wire-bus as shown in Figure 3.5. Its original purpose was to allow communication between ICs with a minimum number of lines and reasonable effort. The two lines of the bus are a clock line and a data line. At least the data line is bidirectional. In the specification of the I^2C bus, the clock line is also bidirectional[52], but this feature is not necessary in this application and therefore not implemented. The data line ports are usually open collector (output drivers can tie the line to ground, but not to the supply voltage). Pullup resistors in the order of $2\,k\Omega$ pull the bus lines to the supply voltage, when the output drivers are off. This driver structure creates a wired OR assignment and makes shorts between two drivers impossible. As there is no driver to

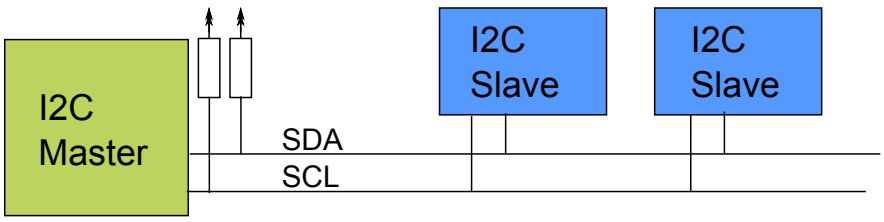


Figure 3.5: *Schematic of a standard I^2C bus.*

force the HIGH state of a bus line, the rise time of the bus voltage, and thereby the data rate, is limited by the cable capacitance and the pullup resistor.

The I^2C protocol is based on a master-slave concept. All communication is controlled by the bus master and each slave has a unique address on the bus. A communication sequence is encapsulated by a start and a stop condition. The start and stop condition are the only occasions, in which the state of the data line is allowed to change while the clock line is high. Regularly, the data line changes only when the clock line is low. After the start condition, the master sends a seven bit address onto the bus, followed by an eighth direction bit. The direction bit determines whether the master reads or writes the following data bytes from or to the addressed slave respectively. Sequentially, data bytes are transmitted. Thereby all byte transmissions, have to be acknowledged by either the master or the slave, depending on the data direction.

During physics data taking, approximately one bit flip per chip and per hour can be expected in the detector control system[4]. This makes error detection, on each bus used in the detector, necessary. The native I^2C protocol is not able to detect false transmissions at all. In order to compensate for false transmissions, an extension for the I^2C bus has been developed at Wuppertal University, the so called I2C-HC protocol[49]. In I2C-HC four additional bits, generated by a cyclic Hamming code, have been appended to the native I^2C data. The redundancy generated by the additional bits allow automatic correction of false data transmissions in which one bit has flipped. False transmissions with two bit flips can also be detected, but a correction is not possible and the data has to be retransmitted. Transmissions with three or more bits flipped cannot be recognized.

The physical implementation of the I2C-HC bus in the HL-LHC pixel detector presents a challenge. As each slave has a different potential (see Figure 3.3), no common ground is available, on which the I^2C specification relies. The missing common potential makes a capacitive coupling between the master and the slaves necessary to avoid overvoltages in the individual chips. A concept of a physical layer for capacitivly coupled I2C-HC has been developed for the first prototype of the DCS chip and will be described in Chapter 5.

For the communication between DCS chip and DCS controller, a data rate of 100 kHz is envisaged.

CAN bus in ATLAS DCS

In most cases, the CAN bus used for DCS communication in ATLAS is implemented with commercial hardware. Hence, no explanation of the CAN bus is given at this point. For more detailed information about the CAN specification, refer to [48]. The only occasion, where a standard CANbus implementation does not fit, is the connection between the DCS computers and the DCS controller. The physical layer for the CAN bus is implemented into the DCS controller chip, thus the voltage levels on the bus lines must not exceed the supply voltage of the chip (which is limited due to the fabrication process). The standard voltage levels of the CAN bus (up to 5 V) exceed the proposed voltage tolerances of the DCS controller chip (max 1.6 V) by far. Hence the voltage

[4] assuming the conditions stated in Section 4.5

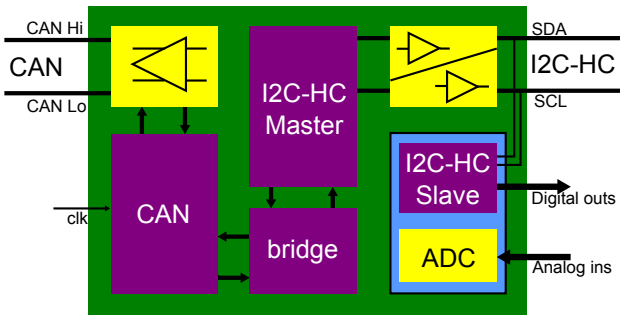


Figure 3.6: *Schematic of the components of the DCS controller*

levels on the bus lines have to be lowered. A design for a physical layer, suitable for a CAN bus with lowered voltages as described above, has already been developed and tested [50].

Whether to use commercial CAN interfaces with level shifters or custom designed CAN interfaces on the off detector site has not been discussed, yet. The data rate of the CAN bus between the DCS computers and the DCS controller, however, has been constrained to 125 kbps or 250 kbps.

DCS controller

The DCS controller is the first of the two chips in the DCS network. It is located on the EoS cards. There it links the long range CAN bus coming from the DCS PCs with the short range I2C-HC bus connected to the DCS chips. Therefore the DCS controller contains logic for a CAN node, an I2C-HC master and a bridge module as shown in Figure 3.6. The bridge module translates the incoming CAN messages into I2C-HC data and vice versa. In order to connect the bus lines directly to the chips and spare additional drivers on the EoS cards, the physical layers for the CAN bus and the I2C-HC are also implemented into the chip (including the pullup resistors for the I2H-HC bus). More details about the CAN and the I2C-HC bus implementation into the DCS controller along with tested prototypes can be found in [49].

For stable operation of the CAN node, the DCS controller needs a precise external clock signal. For reliability reasons, this clock signal should be provided by an independent oscillating crystal.

The physical implementation of the DCS controller will be realized as an IC, most likely in a 130 nm[5] CMOS[6] technology. To ensure the radiation tolerance, the registers of the DCS controller are implemented in triple modular redundancy (TMR, see Section 4.5). This chip will also contain full DCS chip functionality, except for the over voltage and shunting protection. The DCS chip blocks in the DCS controller are internally connected to the data and clock lines of the I2H-HC bus, creating the first DCS chip on an I2C-HC bus of each half stave. The analog inputs will be used to monitor voltages on the EoS card, while the digital outputs can be used e. g. as reset signals for parts of the DAQ.

[5] Standard IBM process, see Chapter 4.5

[6] **C**omplementary **M**etal **O**xide **S**emiconductor

DCS chip

The other type of node in the DCS network is the DCS chip. A schematic is shown in Figure 3.7. There is a DCS chip for each module, located on the stave flex close to the module's power lines. Its main task is the switching of individual detector modules in a serial powering chain. Therefore it has a shunting transistor build in, which is capable of bypassing the current of a module (up to 2.4 A). Thereby the voltage drop on the shunting transistor has to be small enough to switch a module completely off. The shunting can be initiated in two ways: either a command to shunt is sent over the DCS network, or the module voltage exceeds a certain threshold. In both cases, the shunting can be disabled via DCS commands. To get feedback of the module switching and to monitor the operating voltage of a module, there is an ADC implemented in the DCS chip. An analog multiplexer allows also temperature measurements using thermistors. The digital block of the DCS chip provides a number of digital in- or outputs, although the use of these ports on module level is not foreseen, yet.

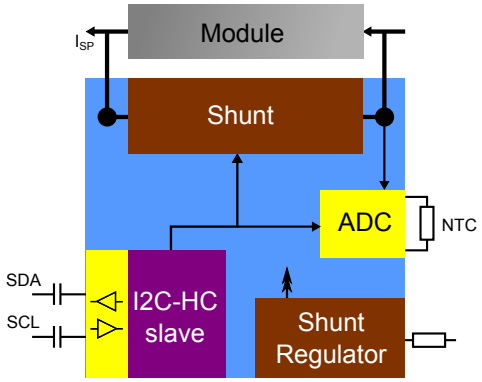


Figure 3.7: *Schematic of the components of the DCS chip*

As each module in a serial powering chain is operated at a different voltage level, the DCS chips also need to operate at different voltage levels. To be rather independent of the input voltage, the DCS chip contains its own shunt regulator[7]. This regulator generates the supply voltage for the DCS chip from a current. The current line is shared by all DCS chips on one half stave. A separate return line is not necessary, as the return of the DCS chip is linked to the serial powering line. In total, the shared power line and the two bus lines of this concept give three additional lines per serial powering chain for DCS.

Similar to the DCS controller, TMR is foreseen for the DCS chip's registers.

For more details of the individual components of the DCS chip, please refer to Chapter 5, where the first prototype of a DCS chip in a 130 nm technology, the PSPP chip, is explained.

DCS network

Figure 3.8 on the next page shows the DCS network covering the serial powering chain of a half stave. Three lines are needed in the critical area in the pixel detector: a power line and two data lines. Each DCS chip (light blue in Figure 3.8) has an individual resistor between its shunt regulator and the power line, transforming the supply voltage into a current. Thereby the voltage of the power line needs to be high enough to supply the DCS chip with the highest ground (most right DCS chip in Figure 3.8). The different

[7] A shunt regulator generates a constant voltage from a variable current, as long as this current is high enough

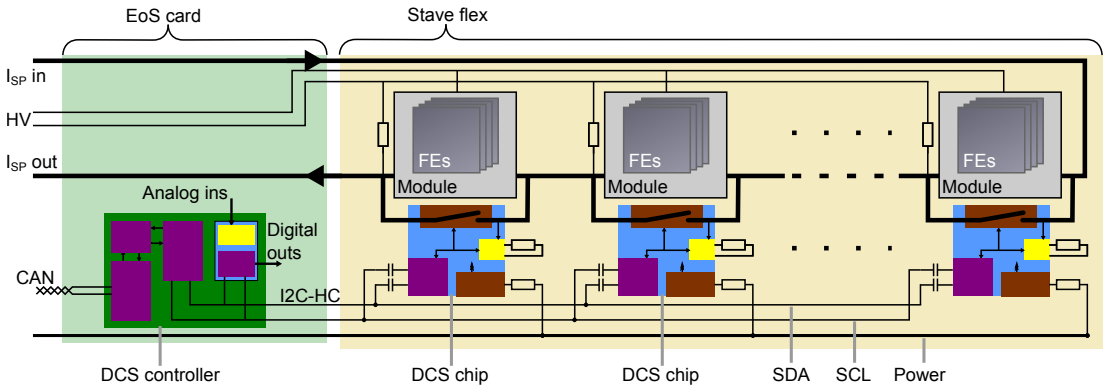


Figure 3.8: *Schematic of the DCS network on one half stave. Three additional lines are needed to cover the full DCS functionality.*

ground potentials of the DCS chips also demand individual capacitive decoupling of the data lines, as these data lines remain at the EoS card's ground potential. Hence, each DCS chip is connected to the I2C-HC data lines of the half staves via two capacitors.

The exact design of the stave flex, as well as all details in the grounding of the serial powering chains are not decided, yet. Assuming that the ground potentials of the two half staves of a stave can be tied together, redundancy for the lines in the tracker volume can easily be achieved. To add redundancy to the power supply of the DCS chips, the power lines of two opposing half staves could be connected between the stave flexes of each powering chain as shown in Figure 3.9. In case of a broken DCS power line (red line) on one half stave, the DCS power line of the other half stave still provides the necessary power to the DCS chips. Though, the serial powering chains of both half staves have to share the same ground potential, for this redundancy to work. These two connected power lines can then share one power supply. Redundancy for the

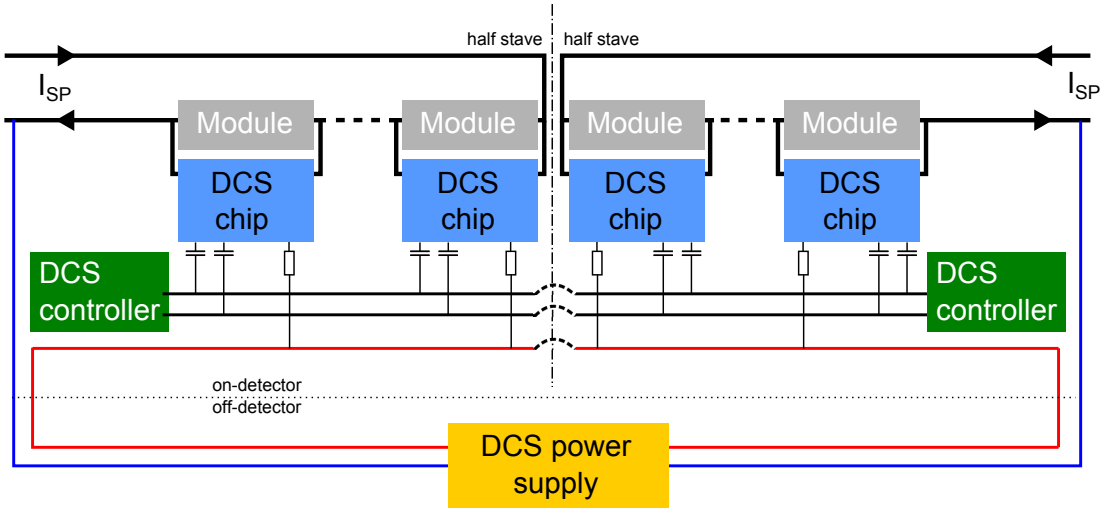


Figure 3.9: *Two half staves with connected power and data lines to redundancy to the system.*

data lines can be achieved in the same manner, if a protection against data collisions on the I2C-HC bus is implemented into the I2C-HC master[8]. This concept of adding redundancy to the DCS network is very attractive, as it enhances the reliability of the Control path at almost no material cost.

3.3 Modifications for parallel powering

To control a directly powered detector, where each module has individual power lines, the concept described above needs modification. The voltage monitoring directly on the module is unnecessary, as all the power lines for the modules pass through the EoS card. There the DCS controller chip can monitor voltages directly on the power lines. The only modification necessary on the DCS controller is an enhanced number of analog inputs, provided by a larger analog multiplexer. The switching of modules is supposed to happen at the DC-DC converters. An additional DCS controller chip with multiple digital outputs can be used to switch the DC-DC converters on and off.

The entire removal of DCS chips, and thus the I2C-HC bus, makes the I2C-HC master and the bridge module in the DCS controller design obsolete. To conserve the ability to measure analog signals with the DCS controller, an enhancement of the CAN module to control the ADC (previously conntrolled by the I2C-HC master) is necessary.

[8] In existing prototypes, this has not been the case, yet.

Chapter 4

Designing an ASIC for a Detector Control System

This chapter describes the necessary knowledge and the design steps, which were taken into account designing the PSPP chip (see Chapter 5). In the first sub-chapter, the basic module of a complementary metal-oxide semiconductor integrated circuit (CMOS IC), the field effect transistor, or (MOS)FET[1] is described. The knowledge described in this sub-chapter is taken from the books [53, 54, 55]. The further sub-chapters will describe the design flow, used to develop the PSPP chip, and discuss several methods to enhance the radiation tolerance of integrated circuits.

4.1 The MOSFET

The MOSFET, as implemented in the ICs described in this thesis, can occur in two types: the n-type and the p-type MOSFET. The difference between the two types is in the doping of the crystal. In the n-type MOSFET (or NMOS) the intrinsic silicon crystal is doped with donors (elements from Group V) and charge is conducted in form of free electrons. Contrary, in a p-type MOSFET (or PMOS) the crystal is doped with acceptors (elements from Group III) and charge is conducted in form of holes[2]. Here, only the NMOS shall be described. The PMOS operation is identical to the NMOS operation, with the exception that all the doping and signs on the terminal voltages and currents are inverted and that the charge mobility of electrons is by a factor of $\approx 2-4$ higher than of holes.

Figure 4.1 shows the structure of a NMOS device, fabricated on a p-type substrate, as it was used for all chips described in this thesis. The device has four terminals: Drain (D), Source (S), Gate (G) and Bulk (B). The D and the S terminals, are formed by heavily n-doped regions. These two terminals are symmetric, and can be interchanged. The G terminal is formed by a conductive piece of poly silicon, deposited onto an insulating layer of silicon dioxide (SiO_2). The B terminal is a heavily p-doped region, which forms a resistive contact to the p-doped substrate. To implement a PMOS device into a

[1] (**M**etal **O**xide **S**emiconductor) **F**ield **E**ffect **T**ransistor

[2] lack of an electron in the atomic lattice

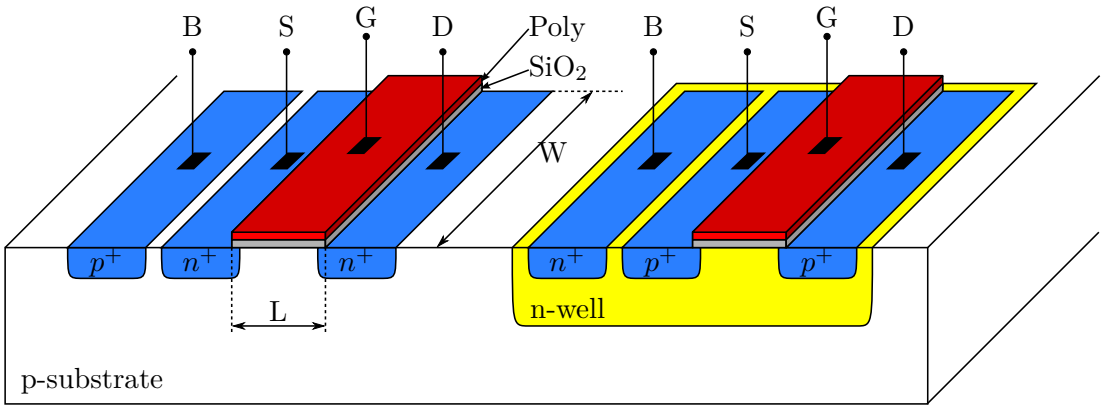
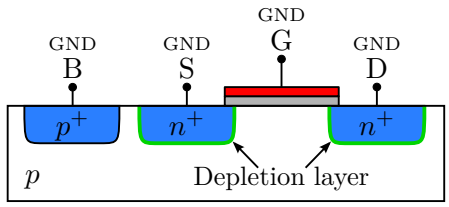
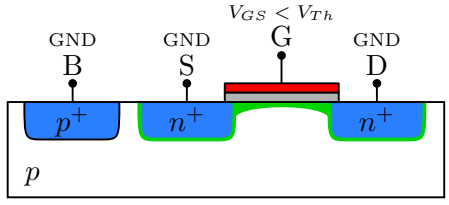


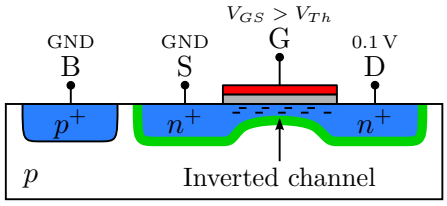
Figure 4.1: *Structures of an NMOS device (left) and a PMOS device (right).*



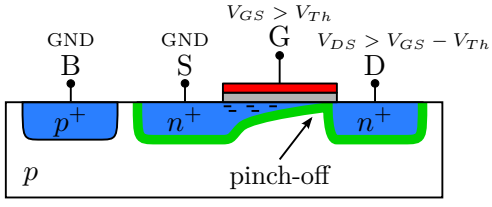
(a) No biasing



(b) Voltage applied to the Gate



(c) An inversion channel is formed



(d) The inversion channel is pinched-off

Figure 4.2: *Cross-sections of an NFET with different terminal voltages.*

p-type substrate, the substrate doping needs to be changed to n-type locally. This island of n-type doping in the p-type wafer substrate is called a 'well', in this case an 'n-well'. While the levels of doping are defined by the fabrication process, the parameters which can be influenced by the designer are the width (W) and the length (L) of the each transistor.

The Gate-Source-Voltage, V_{GS}, and the Drain-Source-Voltage, V_{DS}, determine the current, I_D, flowing through the device from Drain to Source (electrons traveling from Source to Drain). The areas between the n-doped regions and the p-doped substrate form depletion layers due to recombination of the free charge carriers (as shown in Figure 4.2a). When a positive voltage is applied to the Gate ($V_{GS} > 0$), free electrons from the substrate are attracted to the terminal below the gate oxide. These electrons recombine with the holes in this area and create another depletion region (Figure 4.2b). When the Gate voltage exceeds a certain threshold voltage, V_{Th}, electrons from the Source are attracted to the depleted region below the gate oxide, forming a conducting channel between the S- and D-electrodes (as shown in Figure 4.2c). A potential difference between Drain and Source ($V_{DS} > 0$) causes the local voltage difference between

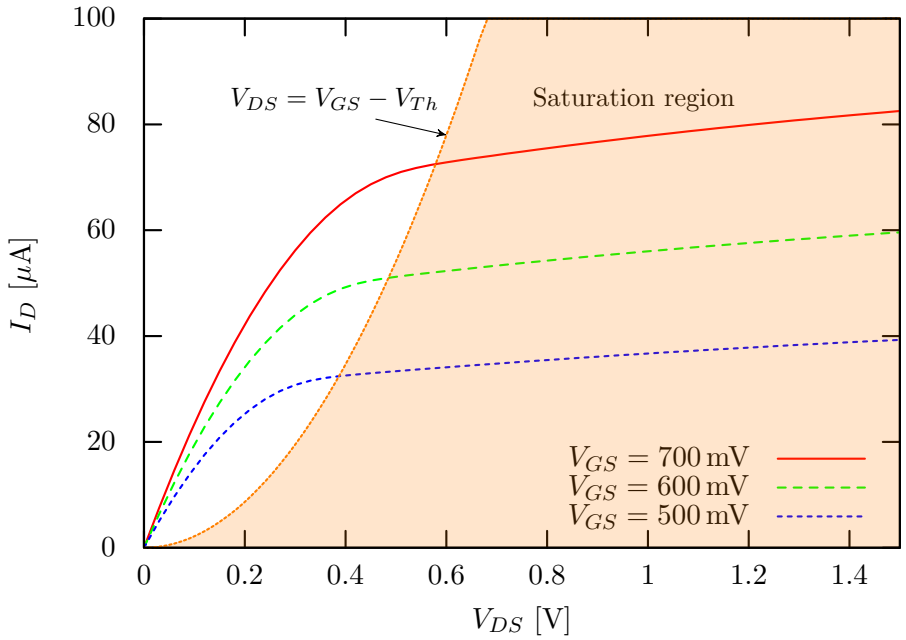


Figure 4.3: *I-V characteristics of an NMOS device with $W = 10\,\mu m$ and $L = 10\,\mu m$.*

Gate electrode and the inversion channel to vary between V_{GS} at the Source and $V_{GS} - V_{Th}$ at the Drain. Hence, the inversion channel has a non-homogeneous charge density in the L direction. At a certain point, where $V_{GS} = V_{DS}$, the local voltage difference at the Drain drops to zero and thus does the local charge density of the inversion layer. A further increase of V_{DS} causes the inverted channel to become shorter as the end of the channel moves to the Source. The channel is then "pinched-off", as seen in Figure 4.2d.

As shown in Figure 4.3, the I/V characteristics of the MOSFET can be divided into two regions: a linear region ($V_{DS} < V_{GS} - V_{Th}$) and a saturation region ($V_{DS} > V_{GS}$-V_{Th}). In the linear region, the current flowing through the device for Gate voltages larger than the threshold voltage ($V_{GS} - V_{Th} > 0$) can be described by the following equation:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{Th})\, V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

with μ_n the electron mobility, C_{ox} the gate oxide capacitance, W and L the channel dimensions, V_{Th} the threshold voltage, V_{GS} the Gate voltage and V_{DS} the Drain voltage, both with respect to the Source. μ_n and C_{ox} are constants defined by the design process technology. In this equation, μ_n and V_{Th} are assumed to be independent of the position under the Gate electrode.

For small V_{DS}, the Drain current is a linear function of V_{DS} and the MOSFET behaves like a resistor. The so called on-resistance is controlled by the Gate voltage according to the following equation:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})} \text{ with } V_{DS} \ll 2(V_{GS} - V_{Th}).$$

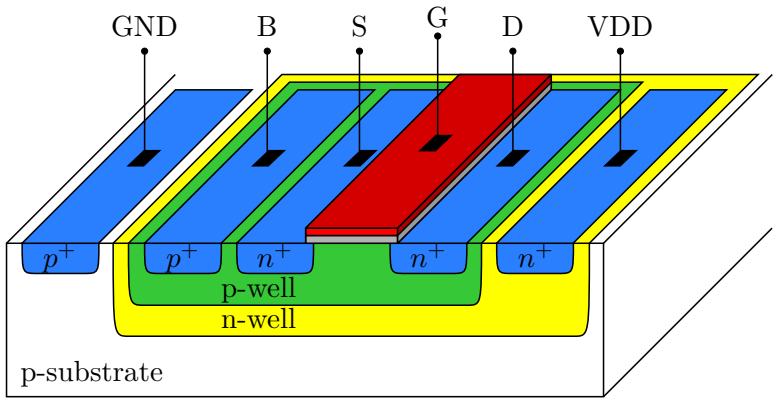


Figure 4.4: *Structure of a triple-well NMOS device.*

In the saturation region, the channel length is not constant any more, due to the pinch-off (see Figure 4.2d). This effect is called channel length modulation. Therefore the channel length L needs to be replaced by a modified length L' with $0 \leq L' \leq L$. With the assumption of a linear relationship between $\frac{\Delta L}{L}$ and V_{DS} with $\Delta L = L - L'$, the Drain current in the saturation region can be approximated to:

$$I_D \approx \frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS})$$

with $\lambda = \frac{\Delta L}{L}$.

For large channel lengths, the influence of V_{DS} cancels out, and the MOSFET behaves like a current source, when operated in the saturation region.

4.1.1 Body Effect

In the description of the MOSFET, given above, the voltage difference between the Bulk and the Source was assumed to be zero. As the Bulk terminals of all NFET devices on a wafer are connected by the substrate, this ideal condition cannot be met, when i.e. two transistors are cascaded. In this case, the Source-Bulk voltage of the upper transistor matches the Drain-Source voltage of the lower transistor. This is called the 'Body-Effect'. The voltage difference between the Bulk and the Source of the upper transistor causes the depletion layer (Figure 4.2a) to increase in thickness and leads to an increased Threshold voltage, V_{Th}.

To avoid this inconvenience, the Bulk potentials of two neighboring transistors need to be decoupled. This can be done with a triple-well structure, shown in Figure 4.4. In this structure, an additional n-well (yellow) is added. Inside this n-well lies a p-well, which works as substrate for the NMOS device. The n-well is biased with a voltage, higher than the voltage of the p-well (green) and the substrate. Usually the n-well is tied to the chip's VDD, while the substrate is tied to GND. The pn-junctions between the substrate and the n-well, as well and between the p-well and the n-well, are both reverse biased and thus work as isolation layers.

Triple-well NMOS devices have been used in the shunt transistor described in Chapter 5.2.3 to get rid of the Body Effect.

4.1.2 Sub-threshold Conduction

The description, given above, assumes that the Gate voltage needs to be larger than the Threshold voltage, to allow a Drain current greater than zero. In reality, there is a third region, the sub-threshold region, in which a MOSFET can be operated ($V_{GS} < V_{Th}$). Though there is no inversion channel formed below the Gate oxide, a small current can still flow through the device. Charge flows thereby due to drift instead of diffusion.

This drift current is a major part of the leakage current of modern integration technologies.

4.2 Cadence Analog Design-flow

To develop and design the ASICs, created in the frame of this thesis, the Cadence Custom IC Design suite [56] was used together with the Mentor Graphics Calibre Physical Verification tool-set [57]. These ASICs are mostly analog designs, which contain only a few small digital blocks. Therefore the chips are almost entirely designed in the Cadence Virtuoso tool-suite for analog design, including the top cell. Only the digital blocks were synthesized with the digital design-flow, provided by the CERN Microelectronics group. For the analog circuit blocks, the design flow was as follows:

1. Design of the schematics of a sub-circuit with the Cadence Virtuoso Schematics editor
2. Simulation and tuning of the created schematic with the Virtuoso Analog Design Environment, which invokes the Cadence Spectre Circuit Simulator
3. Creation of the layout block for the designed and tuned schematic with the Virtuoso Layout Editor
    - During and after the layout process: Design Rule Checks (DRC) with the Cadence Assura Physical Verification and the Calibre Physical Verification tools
4. When the layout is DRC clean: Verifying the layout by performing a Layout Versus Schematic (LVS) check with the Assura Physical Verification tool
5. When the layout passes the LVS check: Extraction of the circuit, which lies in the layout design, including parasitic resistances and capacitances
6. Simulation of the extracted circuit
    - If necessary, adjusting the schematic and/or the layout, followed by the steps 4. - 6.

The steps listed above were executed for every block included in a chip. After all blocks behave as expected in the simulation, including corner simulations[3], the top cell of a

[3] A corner simulation simulates the tolerances of the fabrication process to estimate the yield of the produced chips.

chip can be designed. The top cell creates the highest level in the design hierarchy of a chip design and contains all sub-circuit blocks (including digital blocks), as well as the IO-Pads and the bevel of the chip. The creation of the top cell also follows the six points stated above, but in a more complex manner, as the design is much larger and the simulation now also contains digital blocks.

4.3 CERN Digital Design-flow

To create a digital block, which can be included into the design-flow described above, a different tool-set is necessary. The logic for the digital blocks has been developed with the Xilinx ISE Design Suite in the Verilog hardware description language. After the logic code has passed all simulation tests, the Verilog files are used as input for the synthesis scripts, written by the CERN Microelectronics group. These scripts automate the Cadence digital design-flow. This includes the following steps:

1. Translation of the high level Verilog code into a net-list with the Cadence Encounter RTL Compiler [58]
2. The synthesis of the net-list into a layout with the SoC[4] Encounter RTL-to-GDSII System [59] (including optimization)
3. Automated physical verification (DRC and LVS) with the Assura Physical Verification tool

4.4 Impact of Ionizing Radiation onto Integrated Circuits

The effects, which ionizing radiation has onto integrated MOS circuits, can be divided into two groups: Cumulative effects and Single Event Effects (SEE).

Cumulative effects take place during the entire time, a circuit is exposed to radiation. The major cumulative effect for MOS technologies is the damage caused by the Total Ionizing Dose (TID) deposited in the device. Once the accumulated TID has exceeded the tolerance limits of the device, it fails. The TID deposited in a device is commonly measured in Rad by the radiation community, despite of the Gray being the SI unit for energy deposited by radiation ($1\,\mathrm{Gy} = 100\,\mathrm{Rad}$).

Single event effects, on the contrary, are triggered by the energy deposition of a single particle traversing the device. Therefore, these effects can occur at any time, the device is exposed to radiation and have to be treated statistically. The probability of an SEE is most commonly expressed as a cross-section in square meters or in barn ($1\,\mathrm{b} = 10^{-28}\,\mathrm{m}^2$).

4.4.1 TID effects

In the environment of the ATLAS pixel detector, the deposited ionization energy is delivered by charged hadrons, electrons, gammas and neutrons (indirectly by the latter

[4] **S**ystem **o**n **C**hip

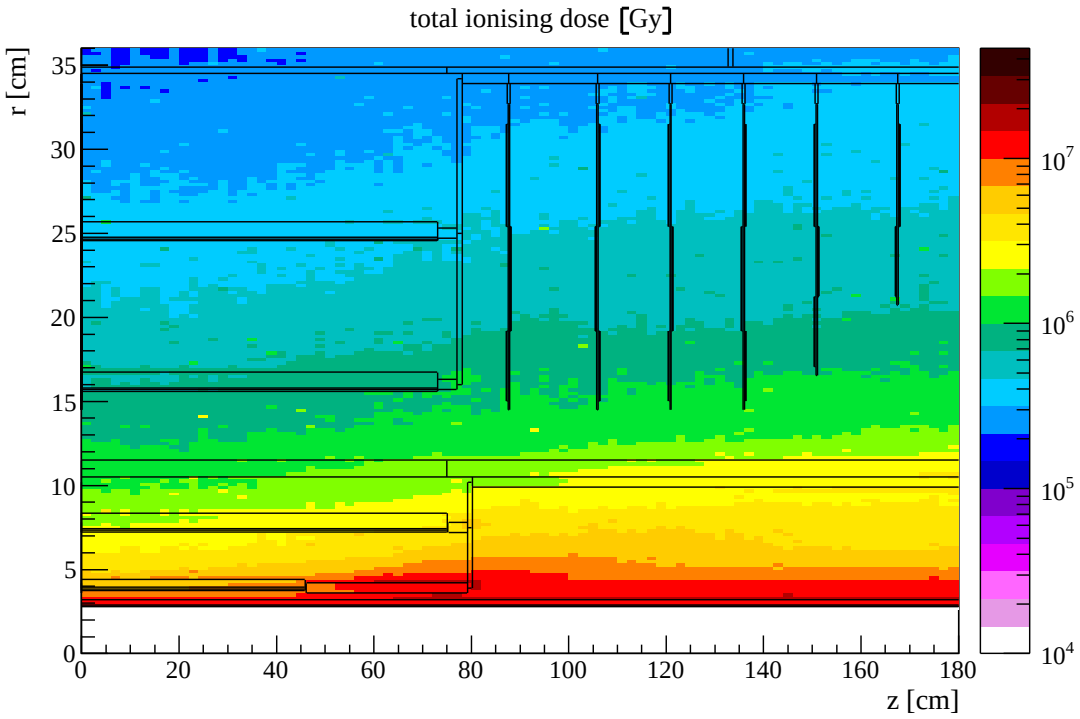


Figure 4.5: *Simulated total ionizing dose, expected for the electronics in the ATLAS pixel detector volume. [27]*

two). Figure 4.5 shows a simulation of the radiation dose to be expected in the volume of the pixel detector accumulated over the expected run-time of $3000\,\mathrm{fb}^{-1}$. For the innermost layer of the pixel detector, a TID of 2 GRad has to be expected. The deposition of this ionizing energy can have two different effects, depending on the material in the device, in which the energy is deposited.

In the SiO_2, which has an amorphous structure, the ionizing radiation can activate the intrinsic defects, which then become traps for positive charges. Ionizing radiation traversing a MOSFET generates electron-hole pairs. The Gate and the Substrate materials have rather low resistance, so the electric field gradient in these materials is low and the electron-hole pairs recombine quickly. In the silicon dioxide on the other hand, the resistance is high and therefore is the electric field gradient, if the device is biased. Due to this field, some of the electron-hole pairs are separated, as electrons and holes start to drift in opposite directions. While the generated electrons have a rather high mobility, and thus are able to leave the SiO_2, the holes can be trapped by the defect centers of the silicon dioxide and remain as a fixed local positive charge. Those holes, which have not been trapped by the defects, drift to the $SiO_2 - Si$ interface and recombine with electrons from the silicon.

The fixed charges in the SiO_2 are not permanent, though. If the energy of the electrons in the vicinity of the trapped holes is high enough, the electrons can anneal the trapped holes. Thereby the annealing electrons can have two origins: Either the

electrons tunnel from the silicon lattice to the holes, if the bias voltage is high enough (tunnel annealing), or electrons from the valence band in the SiO_2 jump to the traps, if the band gap is small enough (thermal annealing). This takes place already during the irradiation[5]. Therefore, at a certain point, the number of radiation induced charge traps is high enough, so that the rate of annealing equals the rate of trap generation, causing the number of traps to saturate.

The other effect of the ionizing radiation occurs in the silicon close to the Si-SiO_2 interfaces. These regions contain a lot of defects in the crystal lattice, due to the abrupt transition from amorphous to crystalline structure. These defects, located up to a few Å from the interface, are called interface states and give origin to the interface traps. By a complicated process, described in [60, 61, 62, 63], the ionizing radiation can increase the number of interface traps by several orders of magnitude. In contrast to the traps in the SiO_2, which trap only positive charges, the interface traps can trap both positive and negative charge. There is also, contrary to the traps in the SiO_2 no significant annealing of interface states at room temperature.

These effects can change the characteristics of a MOSFET device in several ways: A shift of the Threshold voltage, V_{Th}, an increase of the leakage current and a decrease of the charge carrier mobility and the transconductance. The type of characteristic, which is changed, depends thereby on the location of the traps inside the MOSFET device.

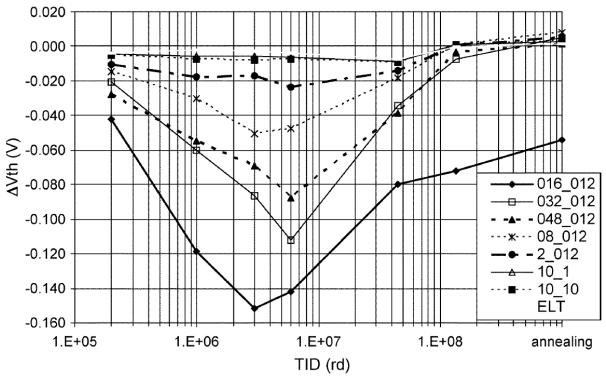


Figure 4.6: *V_{Th} shift with TID for different NMOS transistor sizes, up to 136 Mrd. The last point refers to full annealing at* 100 °C. *[64]*

In the gate-oxide, the trapped positive charges can either enhance (NMOS transistors) or shield (PMOS transistors) the electric field induced by the charge on the gate electrode. Hence, the (absolute) threshold voltage is increased or decreased for PMOS or NMOS transistors, respectively. The interface traps below the gate oxide can trap charge from the inversion channel. This causes an increase of the (absolute) threshold voltage for both, NMOS and PMOS transistors and decreases the mobility of the charge carriers in the channel and thus the transconductance of the device.

Both effects the charge trapping and the activation of interface states, have thereby a different dynamic. The trapped holes accumulate faster and thus are dominant at low TID. At higher TID, the interface states gain significance in the threshold voltage shift and, due to the annealing of the trapped holes, become the dominant effect. This means that for NMOS transistors, the total threshold voltage drift is negative for small TID and positive for large TID (see Figure 4.6). PMOS transistors always have a negative threshold voltage shift, as both effects increase the absolute threshold voltage.

[5]The rate of annealing depends on the temperature and the fabrication technology of the ASIC.

Modern fabrication processes of integrated circuits (250 nm and smaller) also implement a silicon dioxide insulation layer at the outer interfaces between the terminal implants and the substrate, called Shallow Trench Isolation[65] or STI, as shown in Figure 4.7. This insulation layer, made of SiO_2, reduces the inter transistor leakage current. Ionizing radiation though, can induce trapped holes in the silicon dioxide of the STI. These trapped positive charges attract image charges in the substrate material. In the area between the Source and the Drain implants of NMOS transistors, these image charges can form an inversion channel, which increases the leakage current in the transistor. Figure 4.8 shows measurments from another group, which confirms this. In narrow channel transistors, the trapped charges at the edges of the transistor can have a significant effect on the electric field, generated by the charge on the transistor gate. Hence, in transistors with a very small width, the positive charge trapped in the STI can decrease or increase the absolute threshold voltage of NMOS and PMOS transistors, respectively. This effect is called Radiation-Induced Narrow Channel Effect (RINCE) according to the group, which discovered it [64]. The interface states induced by the SiO_2 of the STI though, increase the threshold voltage of the parasitic lateral transistor and decrease the leakage current.

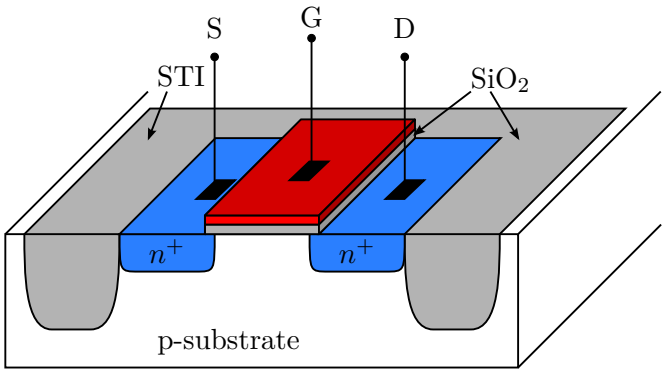


Figure 4.7: *Schematic showing an NMOS transistor with the surrounding Shallow Trench Isolation (STI), which reduces the inter transistor leakage current.*

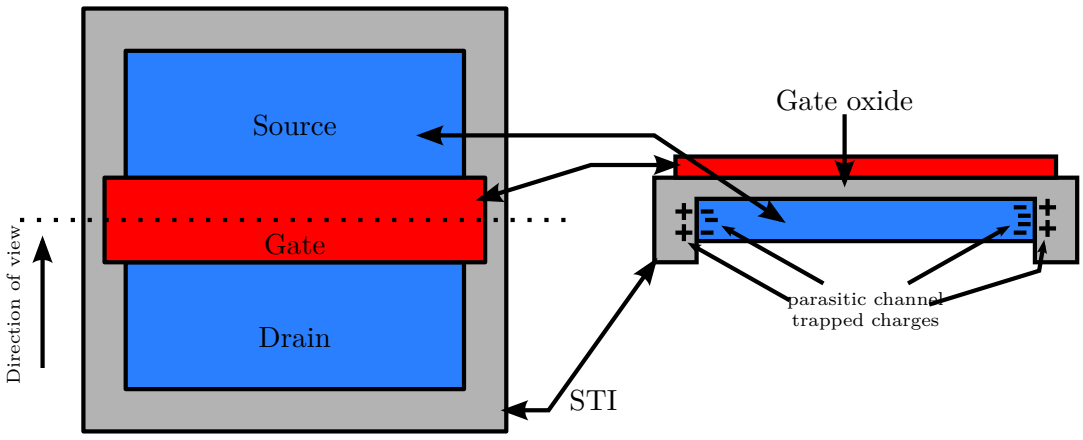


Figure 4.8: *Right: Schematic top view of an NMOS transistor. Left: Schematic showing the same transistor along the dashed line. The gate oxide and the STI are formed by the same piece of silicon dioxide here. The trapped charge in the STI generates an electric field, which can form an inversion channel between the Source and the Drain islands.*

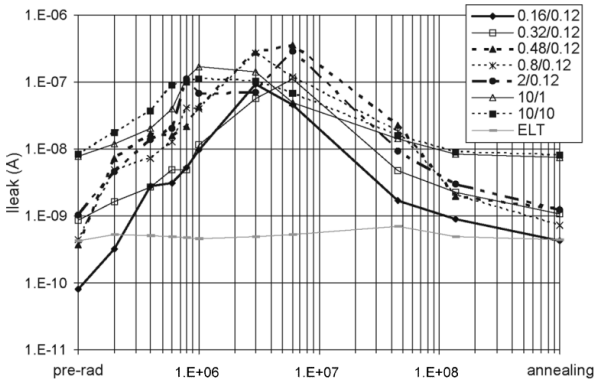


Figure 4.9: *Evolution of the leakage current with TID for different NMOS transistor size, up to 136 Mrd. The last point refers to full annealing at 100 °C.[64]*

Again, due to the different dynamics of the activated defects and the interface states, as described above, the leakage current does not rise monotonous. For NMOS transistors the leakage rises fast for low TID and then rises slower or decreases again for higher TID. Measurements from other groups confirm this, as seen in Figure 4.9. Due to the polarity of PMOS transistors, the trapped charges in the STI cannot induce a parasitic lateral channel there.

For more information about TID effects in MOSFET devices, see [66] and [67].

4.4.2 Single Event Effects

Contrary to the TID effects, single event effects (or SEE) are not triggered by an accumulated dose of deposited energy, but can be triggered by single particle interactions. Thereby charged particles traverse the die and generate a certain amount of charge. This charge may cause transient, static or permanent errors, if generated close to a sensitive node. A simulation of the flux of charged particles, to be expected in the volume of the pixel detector for an instantaneous luminosity of $L = 5 \cdot 10^{34} \frac{1}{cm^2 s}$, is shown in Figure 3.1 on page 42.

If, due to a particle interaction, charge is induced into a circuit, it causes a transient which can falsify measurements. These transients occur asynchronous and are found mostly in analog circuits or combinatorial logic. Usually the deposited amount of charge is small and the generated errors are corrected within the next clock cycle. When a transient is propagated onto a latch register, it can become static. Then it is called a Singe Event Upset (or SEU). Static errors can only be corrected from the outside, when the data is rewritten or by a power cycle. A very dangerous form or error is the permanent or hard error induced by a latch-up (also called Single Event Latch-up or SEL). These errors can, if not detected immediately, destroy the entire chip due to over current.

The SEU and the SEL are the most important SEE for ASICs produced with the chosen technology and hence will be described further. For more information about Single Event Effects in MOSFET devices, see 67.

SEU

Ionizing particles lose energy through Rutherford scattering, when traversing an ASIC. The energy is deposited in form of electron-hole pairs. While in the substrate these pairs recombine without any further effect, in proximity to the p-n junctions the charges are separated and induce a current spike. Besides causing transients, the generated charge

can also corrupt the stored information in a memory cell. In the synthesized logic cores, this kind of SEU is the most probable.

Figure 4.10 shows the schematic of a memory cell as an example for an SEU. In the beginning, the output of the memory cell is low, storing the value '0'. In this schematic, the NMOS transistor's Drain of the input inverter is traversed by an ionizing particle. The generated electron-hole pairs induce charge into the lines of node 1. When this charge is drained off by the connected PMOS transistor, the voltage of node 1 drops towards GND. Should the amount of charge induced to node 1 be sufficient, to lower its voltage below the threshold voltage of the output inverter, node 2 also changes its state from '0' to '1' and the stored information is falsified.

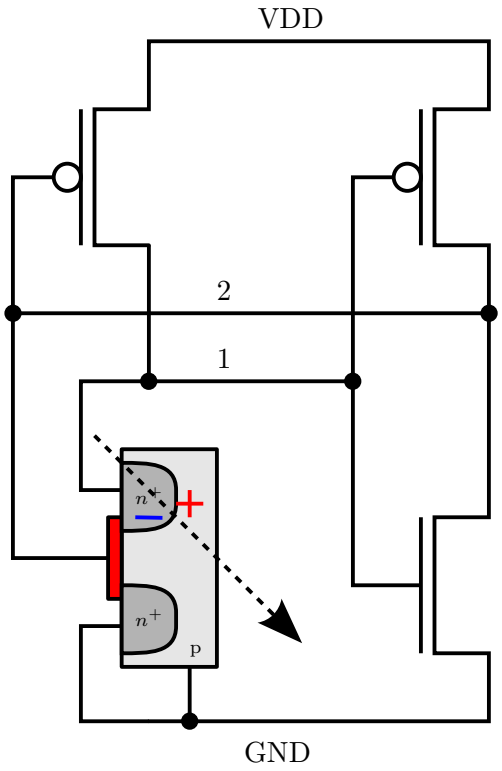


Figure 4.10: *Schematic showing the impact of an ionizing particle, which traverses the sensitive volume of an NMOS transistor of a memory cell.*

To induce an SEU, the trace of the traversing particle needs to contain a sufficient amount of charge close enough to the sensitive node. In the environment of the ATLAS pixel detector, hadrons as protons, pions and neutrons are dominating the radiation environment. These particles cannot induce SEU directly, as the deposited charge is too small. Nevertheless, these particles can interact (elastically or inelastically) with the nuclei in the sensitive volume. The recoils from these interactions can provide enough energy loss to induce SEU.

SEL

Usually, modern integration technologies are protected against electrical latch-up, initiated by improper voltage sequences on the power supply or input/output lines, with trench isolation [68]. Nevertheless, a latch-up can also be initiated by an ionizing particle. These radiation induced latch-ups are called Single Event Latch-up (SEL).

Figure 4.11 shows the simplest model for a latch-up: The p^+-implant in the n-well, the n-well itself and the p-doped substrate form a bipolar junction transistor (pnp). Another bipolar junction transistor (npn) is formed by an n^+-implant in the substrate, the substrate itself and the n-well. Due to the structure of the two transistors, they form a pnpn-thyristor[6], a device with an internal positive feedback loop: An increase

[6] A thyristor is a device which can be switched on (conducting) by a small gate current. Once switched on, the thyristor continues to conduct until the conducted current drops below a certain

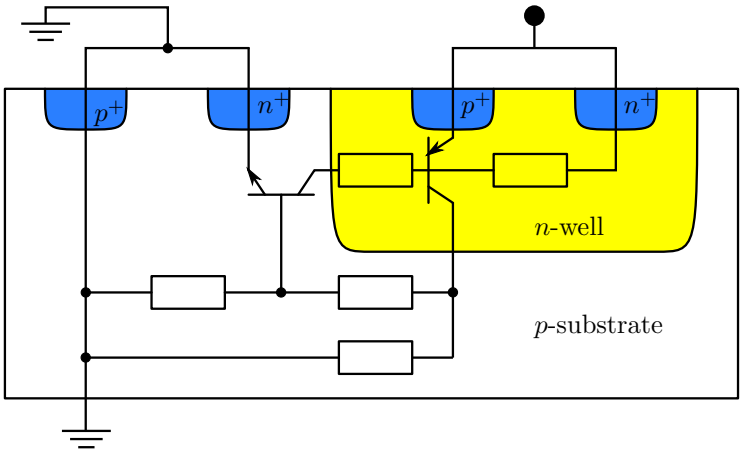


Figure 4.11: *Schematic of the parasitic thyristor structure which can cause a destructive latch-up.*

in the collector current of one transistor also increases the base current of the other transistor. This in turn increases the collector current of the other transistor, which again increases the base current of the first transistor. The increased base current of transistor one increases also its collector current. If the overall gain of this feedback loop is high enough, any induced charge or current, which switches one of the two transistors conducting, will switch on the thyristor. Once this thyristor is switched on, it creates a conducting path between the power supply terminals of the device. If not cut-off immediately, the device will break due to over current. The necessary current to trigger a latch-up can e. g. be generated by an ionizing particle traversing the device. The generated electron-hole pairs in or in proximity to the pn-junction between n-well and substrate will be separated due to the electric field and flow to the power supplies through the well- and substrate contacts. If the resistance along this path is high enough, the consequent voltage drop can produce the necessary base current to one of the two transistors and the thyristor will switch on.

4.5 Principles for Radiation Hard Electronics

To make an integrated circuit tolerant against the radiation effects described above, several actions can be taken. At first, the choice of the fabrication process plays an important role in the development of a radiation tolerant design. High substrate resistivity, e. g. increases the probability for SEL. In high energy physics, especially for the experiments at the (HL-)LHC, a commercial 130 nm process was established due to its intrinsic radiation hardness [64, 46]. During the writings of this thesis, there is also research ongoing to evaluate the applicability of 65 nm process in high energy physics. Up to now, the results of this research are promising, as the 65 nm process shows increased radiation tolerance and allows for smaller design sizes [69]. Unfortunately, this process was not available during the development of the ASICs described within this thesis.

threshold.

4.5.1 Thin Gates of the 130 nm Process

As described above, in Section 4.4.1, the deposition of charge in the silicon dioxide, located under the gate terminal, can change the threshold voltage of a transistor. Due to the very thin gate oxides of modern fabrication processes, the intrinsic radiation tolerance of these processes is already very high, in terms of threshold voltage drifts. This has also been proven for the commercial 130 nm process, as it is used to design ASICs for the detector control system, for a TID of 136 MRad. The measurements have shown that the threshold voltage of the core transistors with gate thicknesses of 2.2 nm changes only by $\approx 20\,\text{mV}$, as long as the transistor is wide enough ($W > 2\,\mu\text{m}$) [64], which can be neglected for most applications. In contrary, the I/O-type transistors with gate thicknesses of 5.2 nm do not show negligible parameter variations and should be avoided [46, 64]. The RINCE effect described in Section 4.4.1 could also be measured showing, that the threshold voltage shift for NMOS transistors and the leakage current peak at TIDs of $\approx 1 - 6\,\text{MRad}$. PMOS transistors always have a negative threshold voltage shift, as both effects increase the absolute threshold voltage, and no peak can be observed. [64]

As these measurements include only doses up to several hundrets of MRad, it is advisable to perform further measurements with very high doses of up to 1 GRad for the ASICs, which are part of the detector control system.

4.5.2 Enclosed Layout Transistor

While the thin gates of the core transistors of the used 130 nm process suppress the accumulation of charge in the gate oxide, charge can still be collected in the STI. As described above, deposited charge in the STI can induce parasitic lateral channels, which increase the leakage current of an NMOS transistor. To prevent the creation of these lateral channels, the geometry of the transistor can be modified in a certain way, so that there is no boundary surface touching the STI. An example for such a transistor geometry is shown in Figure 4.12. Due to the shape, these kind of transistors are called Enclosed Layout Transistors or ELT. There are drawbacks for ELT though. One is, that the ratio of W to L is limited due to the geometry. Another one is the reduced integration density. Measurements confirm the enhanced radiation tolerance of ELT compared to standard transistors, by measuring almost no increase in the leakage currents after irradiation. [64, 46]

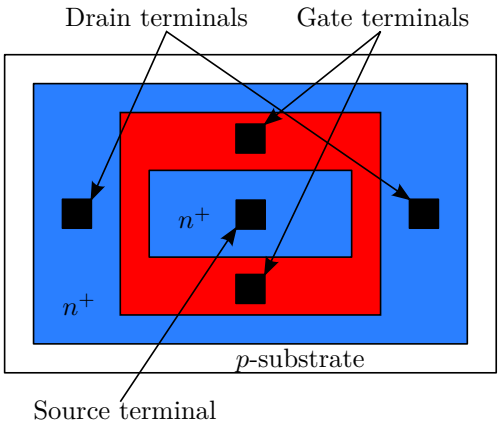


Figure 4.12: *Schematic showing the top-view of an Enclosed Layout Transistor*

Unfortunately, a library of ELT was not available for the chips, which were designed by our group at their time of design. Thus all transistors implemented in the PSPP

chip and the Cofee 1 and 2 [7][50, 51, 49] chips use standard transistors for digital and analog circuits.

4.5.3 DICE Latches

There are several ways to increase the tolerance of an integrated circuit against the corruption of stored data due to radiation (or SEU). Two will be described here, as these were taken into account for a possible implementation into ASICs for the detector control system described in Chapter 3. The first one is the use of Dual Interlocked storage Cells (or DICE) as memory cells in the chip. These memory cells contain a redundant latch structure, which can detect single bit flips in the cell. Figure 4.13 shows the schematic of a DICE latch structure. When, for example, the stored data in the cell is '0', then the nodes S1 to S4 are S1-S2-S3-S4 = '0101'. If an SEU is assumed in one of the four latches, w.l.o.g.[8] a positive transition of S1, the transistor MP2 is switched off and thus blocks the propagation of the transient to node S2. Simultaneously, transistor MN4 will propagates a negative pulse to S4 which switches off transistor MN3, so that node S3 remains unchanged. After the SEU induced charge has drained, the cell returns to the initial state, as nodes S2 and S3 have conserved the true information.

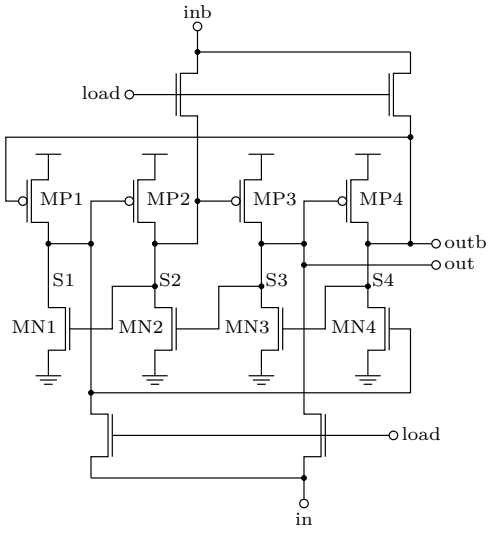


Figure 4.13: *Schematic of a DICE latch structure.*

So due to the inverting feedback inside the cell, single bit flips are corrected automatically after the radiation induced charge has drained and the error will not be persistent. Nevertheless, a simultaneous bit flip in two latches of one DICE structure leads inevitably to the corruption of the stored data. In highly integrated processes, a single incident of a traversing particle can lead to a bit flip in multiple latches, due to charge sharing. Hence, the redundancy in the DICE structure is most effective, if the distance between the individual latches is as large as possible. Measurements performed by other groups have shown, that the cross section for an SEU can be lowered by a factor of 3, only by applying a reorganization of the layout of the DICE structure. The final SEU cross section for an interleaved layout of the DICE structure, created with the 130 nm process also used by our group, was thereby measured to be $\sigma_{DICE} = 2.4 \cdot 10^{-16}\,\mathrm{cm}^2$ for an equal distribution of '1' and '0' in the registers. [70]

[7] The Cofee 1 and the Cofee 2 chips were digital prototype designs, containing the logic to span a DCS Network with CAN and I2C-HC bus. The chips were created in parallel to this thesis by our group.

[8] without loss of generality

4.5.4 Triple Modular Redundancy

Another way to increase the tolerance of logic cells against SEU is to add pure redundancy. Bringing the minimal number of duplications, to recognize and correct a single error is three. This technique is called Triple Modular redundancy, or TMR. Besides the three redundant logic cells, a majority voter is needed. This increases the layout size approximately by a factor of four. As long as only one of the three cells is corrupted, the remaining two cells hold the correct value and the majority voter determines the correct value by evaluating, which value occurs most often. After the next clock cycle, the voted data is then written back into all three logic cells to correct for the corrupted ones. Hence, the output is inevitably wrong, if two or more cells are being corrupted during one clock cycle. Similar to the DICE Latches described above, charge sharing can also induce dual SEUs in the TMR structure. So the hardness against dual SEUs can be improved by making the distance between the three redundant logic cells as large as possible.

Assuming, that the redundant logic cells are sufficiently separated and charge sharing cannot induce a dual bit flip, the probability for an undetected data corruption (for each clock cycle) can be calculated as:

$$P_{SEU(TMR)} = \binom{3}{2} \cdot P_{SEU}^2 \cdot (1 - P_{SEU}) + \binom{3}{3} \cdot P_{SEU}^3$$

with $P_{SEU(TMR)}$ being the probability of an undetected data corruption in the TMR structure and $P_{SEU} = \sigma_{SEU} \cdot \phi \cdot T_{clk}$ being the probability of a bit flip in one of the redundant logic cells during one clock cycle. The probability of a bit flipping twice and falling back to its true value can be neglected. As the effectiveness of TMR depends on the ratio between the clock frequency and the particle flux, a general value for the cross-section cannot be given.

Though, with the relation $N_{SEU} = \sigma_{SEU} \cdot F$, number of SEUs equals the cross-section multiplied with the Fluence, a cross-section for a data corruption in a TMR structure can be estimated for the conditions in the pixel detector, by using the following assumptions:

- The cross-section for an SEU in a common memory cell lies between σ=(2.78±0.38) $\cdot$ $10^{-14}\,\frac{\mathrm{cm}^2}{\mathrm{bit}}$[51] and $\sigma \approx 6 \cdot 10^{-14}\,\frac{cm^2}{bit}$[46],
- the clock cycle will be at 100 kHz (envisaged clock frequency for the I2C-HC bus),
- SEU relevant particle flux is $\phi = 3.3 \cdot 10^8 \mathrm{cm}^{-2}\mathrm{s}^{-1}$ in the pixel detector volume at the HL-LHC [49],
- the number of clock cycles is $\approx 6 \cdot 10^{12}$ over a run-time of $L = 3000\,\mathrm{fb}^{-1}$ at an instantaneous luminosity of $\mathcal{L} = 5 \cdot 10^{34}\,\frac{1}{\mathrm{cm}^2\mathrm{s}}$,
- and the Fluence of SEU relevant particles is $F = 2 \cdot 10^{16}\,\frac{1}{\mathrm{cm}^2}$ (calculated from the values above).

With the assumptions above, the cross-section for a data corruption in a TMR structure is between

$$\sigma_{SEU(TMR)} = 3,54 \cdot 10^{-23}\,\mathrm{cm}^2 \text{ and } \sigma_{SEU(TMR)} = 7,57 \cdot 10^{-24}\,\mathrm{cm}^2.$$

Irradiation measurements with the Cofee 1 and 2 chips have also proven the effectiveness of TMR [50, 51].

4.6 Hardness By Design Techniques for DCS Electronics in the ITK

Fortunately, the accumulating radiation effects on the threshold voltage can be lessened very effectively, by the use of a modern fabrication process with thin gate oxides as described in Section 4.5.1.

Irradiation measurements using the CoFee 2 chip have shown, that during the irradiation the current consumption of the chip can peak at very high values (due to the increased leakage current). Even though the high current consumption is only temporary, it should be avoided. A combined peak of all chips can deposit a significant amount of heat, which the detector has to cope with especially if the cooling fails. Thus, the use of ELT is advised for all transistors, where it is possible. Should the chips be manufactured in a 65 nm technology, the need of ELT in the logic part no longer applies [69].

Protection against SEE is more complicated. To ensure a faultless operation of the detector control system and the pixel detector, the envisaged number of undetected errors due to Single Event Effects is less than one. Considering the harsh environmental conditions in the pixel detector, meeting this constraint is no trivial task and requires a thoughtful use of the techniques described above. In the DCS concept (Chapter 3), both used types of ASICs are located in areas with similar radiation levels, which implies, that the same protection mechanisms should be used for both ASICs. To estimate the number of undetected bit flips in the entire detector control system, the number of susceptible registers needs to be known. The baseline layout of the pixel detector foresees 3833 modules[49]. Each one of these modules is supervised by a DCS chip. In the PSPP prototype of the DCS chip, the logic core contains 77 registers. So, there are $\approx 300,000$ registers in the DCS chips alone. The last prototype of the DCS controller, the CoFee 2 chip, contained 1492 registers. As there are 684 End-of-Stave cards planned[49], further $\approx 1,000,000$ registers contribute to the detector control system. The number of undetected bit flips can then be calculated according to

$$N_{SEU} = \sigma_{SEU} \cdot F \cdot N_{Reg}$$

with N_{SEU} the estimated number of undetected bit flips, σ the cross section for an SEU, F the particle fluence and N_{Reg} the number of registers. Table 4.1 shows the number of SEUs expected in the DCS chips and DCS controllers. The stated values represent the worst case scenario in terms of cross sections. The values in Table 4.1 show clearly, that neither the unprotected memory cells nor the DICE latch structures provide sufficient tolerance against SEU induced memory corruption.

To estimate the number of memory corruptions in case of TMR protected chips is more complicated. The level, on which TMR is implemented into an ASIC is variable

Technology	σ_{SEU}	N_{SEU} DCS chips	DCS controller	$\sum$
no protection	$6 \cdot 10^{-14}\text{cm}^2$	$3.54 \cdot 10^8$	$1.22 \cdot 10^9$	$1.58 \cdot 10^9$
DICE latches	$5.90 \cdot 10^{-16}\text{cm}^2$	$3.48 \cdot 10^6$	$1.20 \cdot 10^7$	$1.55 \cdot 10^7$

Table 4.1: *Estimated number of undetected bit flips in the registers of the Detector control system. The cross sections are the worst case values for a charged particle fluence of $F = 2 \cdot 10^{16} \frac{1}{cm^2}$ (see Section 4.5.4).*

and should be chosen according to the tasks of the ASIC. As the DCS controller is provided with a permanent clock signal of 4 MHz, an implementation of TMR on register level is advisable. This means that each register of the chip contains three flip-flops and a majority voter. This kind of implementation was also used for the Cofee 2 chip[50]. One advantage is, that the implementation can take place at a rather late point in the design synthesis and be performed by scripts. Due to the high clock speed, the cross section for a data corruption in a TMR structure reduces $\sigma_{SEU(TMR)}$ to $8.91 \cdot 10^{-25}\,\text{cm}^2$ (worst case value).

The DCS chip is clocked only by the SCL line of the I2C-HC bus. This clock is envisaged to be not permanent to reduce the power consumption of the chip. To guarantee that the time window for two corrupting SEUs in one register is only as short as 10^{-5} s, the clock would have to be applied permanently as a trade-off between safety and heat deposition. Should this implementation be chosen, the cross section described above (in Section 4.5.4) is valid. Another possibility to provide a permanent clock signal, independent of the SCL line, is to derive it by delaying the error output of the majority voter. This error output generates a transition, if the majority voter detects an SEU in one of the three memory cells. Assuming this signal is delayed, it can be used to correct the corrupted memory cells. This kind of TMR clock generation was implemented in the Cofee 1 chip, which contained the first prototype logic block for an I2C-HC slave[51]. The delay can be variable at will, so for a better comparison it shall be assumed to 250 ns (4 MHz), similar to the DCS controller. Table 4.2 shows the expected number of SEUs in the entire detector control system for the different TMR

Technology	σ_{SEU} [cm^2] DCS chip	DCS contr.	N_{SEU} DCS chips	DCS contr.	$\sum$
TMR (SCL clocked)	$3.53 \cdot 10^{-23}$	$8.91 \cdot 10^{-25}$	$2.08 \cdot 10^{-1}$	$1.82 \cdot 10^{-2}$	$2.26 \cdot 10^{-1}$
TMR (delay clocked)	$8.91 \cdot 10^{-25}$	$8.91 \cdot 10^{-25}$	$5.62 \cdot 10^{-3}$	$1.82 \cdot 10^{-2}$	$2.34 \cdot 10^{-2}$
TMR w. DICE l. (SCL clocked)	$3.41 \cdot 10^{-27}$	$8.62 \cdot 10^{-29}$	$2.01 \cdot 10^{-5}$	$1,76 \cdot 10^{-6}$	$2.19 \cdot 10^{-5}$
TMR w. DICE l. (delay clocked)	$8.62 \cdot 10^{-29}$	$8.62 \cdot 10^{-29}$	$5.09 \cdot 10^{-7}$	$1,76 \cdot 10^{-6}$	$2.27 \cdot 10^{-6}$

Table 4.2: *Estimated number of undetected bit flips in the TMR protected registers of the Detector control system. The cross sections are the worst case valuesfor a charged particle fluence of $F = 2 \cdot 10^{16} \frac{1}{cm^2}$ (see Section 4.5.4).*

implementations in the DCS chip. All implementation methods produce less than one undetected error during the run-time of the HL-LHC. Though, in case the exact number of modules and EoS-cards increase, a TMR implementation with a clock frequency of 100 kHz might not be sufficient. The implementation of a combination of TMR and the DICE latch structures described in [70] (three DICE latches and a majority voter form a TMR structure), should not be necessary though, and the additional chip area can be saved.

One problem, which cannot be investigated yet, is the probability of an SEU in the analog circuits. A transient induced into the comparator by an SEU could lead to an activation of the shunting mode in the affected DCS chip. This needs to be prevented by limiting the impedance of the sensitive analog circuits, even though this would increase the current consumption of the chip.

Chapter 5

The Pixel Serial Powering & Protection Chip

As part of this thesis, a concept for a detector control system for the ATLAS pixel detector at the HL-LHC was developed, which is presented in Chapter 3. This concept is designed for the supervision of a detector with serially powered detector modules. A similar concept of a serially powered detector has also been under investigation by the strip detector. It turned out, that some of the results of these investigations can be used in the development of the pixel detector control system. Furthermore the concept introduced in Chapter 3 foresees a bidirectional and AC coupled communication with the I2C-HC protocol. To evaluate the applicability of this concept, especially the AC coupled data transmission, several studies were made. With the results of these studies it was possible to the design a first prototype of one component of the new detector control system, the **P**ixel **S**erial **P**owering and **P**rotection chip, or PSPP chip. The performed studies, as well as the first prototype are described in this chapter.

5.1 Inspired by the SPP

Similar to the pixel detector, for the strip detector system of the ITK, the serial powering of the detector modules is also an option as a powering scheme [71]. As part of the research done for the serial powering of the strip systems, an ASIC was developed at the University of Pennsylvania which should control and protect the serially powered detector modules. This ASIC is called SPP (Serial Powering and Protection) chip. The SPP chip was designed in the same 130 nm process as the strip detector read out ASICs. The tasks of the SPP chip include an autonomous fault detection including the shutdown of the faulty module as well as an addressable power control to switch a module on and off. There is one SPP chip for each module located as close to the module as possible. Due to the proximity to the interaction point of the ATLAS detector, the chip was designed and tested to withstand radiation doses up to 30 MRad [43]. To reduce the amount of material in the detector, all SPP chips on a serially powered stave share the same power line. This single power line is also used to send commands to the SPP chip.

The concept of a control chip close to a detector module has been under discussion for some time in the ATLAS pixel DCS group but never been further investigated. Although the needs for a control chip for the ATLAS pixel detector differ from the ones in the strip system, the concept of the SPP chip was used as an inspiration to elaborate the concept for detector control system described in Chapter 3.

5.1.1 SPP Functionality

The SPP chip contains a large number of features, especially designed for the use in the strip detector. As not all of these features are suited for the use in the pixel detector, only those of intereset were examined in terms of this thesis and are described here.

Voltage regulator

The SPP chip generates its operating voltage with a shunt regulator from a variable input current[1]. This input current supplies all circuits in the SPP, which generates a voltage drop over the SPP, the operating voltage. Hence, the input current must not go below a minimum value to allow all parts of the SPP to work. To keep the operating voltage constant, even with a varying input current, excess current has to be bypassed around the chip's circuits with a shunting transistor. The gate voltage of the shunting transistor is generated by constantly comparing the operating voltage to a fixed voltage generated using a band gap voltage reference.

Comparator

To monitor and regulate the operating voltage of the detector modules, the SPP chip contains two comparators comparing the module voltage (over voltage dividers) to the output voltage of the band gap reference. Should the module voltage exceed a certain value, the shunting comparator can generate a shunting command and switch off the supervised detector module. The other comparator works as a differential amplifier and amplifies the voltage difference between the module voltage (scaled by a voltage divider) and the output voltage of the band gap reference. This analog signal can in combination with a shunting transistor be used as a shunt regulator to regulate the module voltage.

Shunting and addressing logic

The output of the shunting comparator is fed into a flip-flop to keep the shunting command active even when the module voltage drops (due to shunting). To shunt the detector module, the output of the flip-flop can be routed to the gates of the shunting transistors.

Besides by an over-voltage tripping, the flip-flop can also be switched by an external signal from the user. Therefore the SPP chip holds a data in port, in which a serial signal can be fed. A data packet fed into the data port contains 4 address bits and one

[1] The current is generated from a constant high voltage (~20 V) and a resistor in series to the SPP chip.

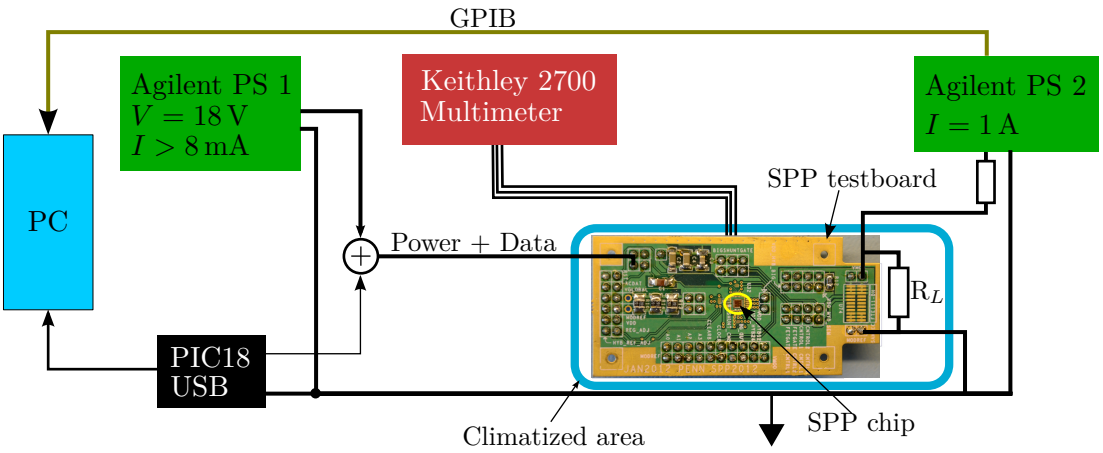


Figure 5.1: *Test assembly for the functionality tests of the SPP. Outgoing connections are going to a computer, which handles the automated measurements.*

data bit. The data is pulse-width-encoded, which means a pulse shorter than 0.4 µs is interpreted as 0 and a pulse wider than 0.4 µs is interpreted as 1. When the four address bits match the individual SPP's address (applied via IOs) the fifth bit is written into the flip-flop.

The data in signal can be transmitted AC coupled, so that the data signal can also be modulated onto the supply voltage line of the SPP.

Shunting transistors

The SPP contains two transistors to shunt the module current, a small one (w_{eff}=6,000 µm) and a big one (w_{eff} ≈60,000 µm).

5.1.2 Functionality-tests with the SPP

To fully verify the functionality of the SPP, its components were tested under laboratory conditions, where one SPP chip was operated individually without any further electronics, except the power supplies and multimeters necessary for the measurements, attached to it. The SPP chip itself was bonded onto a test board, designed by the University of Pennsylvania, on which the operation of the SPP could be configured with jumpers. The test assembly is depicted in Figure 5.1. The data communication coming from the PIC micro-controller is modulated onto the power line (from Agilent PS 1) going to the SPP test board. On the board a resistor limits the current of the supply voltage, which flows into the power input of the SPP. A capacitor on the board separates the data from the power line, which is then routed into the data input of the SPP. The load resistor, R_L, mimics a detector module by transforming the serial power current from Agilent PS 2 into the module voltage.

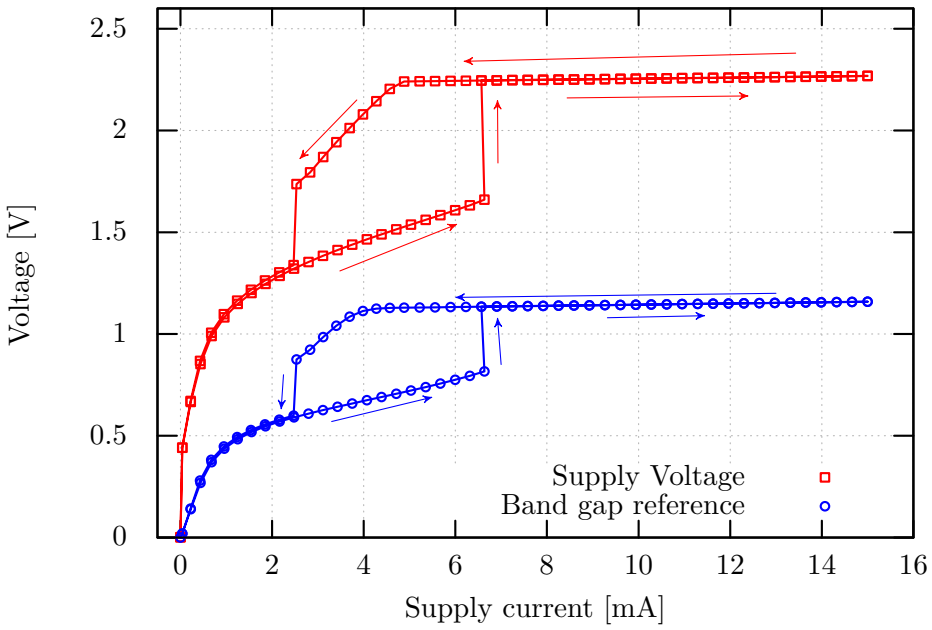


Figure 5.2: *Characteristics of the SPP shunt regulator and the band gap reference. To cover the hysteresis, the input current has been swept from 0 mA to 15 mA and then vice versa.*

Voltage regulator

The function of the voltage regulator and the band gap voltage reference was tested by applying a voltage (Agilent PS 1 in Figure 5.1 on the previous page) to the regulator input of the SPP with a resistor in series. The supply current and voltage were measured as well as the output voltage of the bang gap reference. As shown in Figure 5.2, the regulator begins to work at a current of approximately 6.9 mA and the supply voltage of the SPP stabilizes to 2.24 V. A further increase of the input current changes the supply voltage of the SPP only slightly by about $\Delta V_{DD}(I_{Supply}) = (2.668 \pm 0.017)\,\frac{\mathrm{mV}}{\mathrm{mA}}$. The measurements have also shown, that once the regulator is running, the input current can drop to approximately 5 mA before the supply voltage drops significantly. The output voltage of the band gap reference shows a similar behavior. Once the regulator started to work, the change in the reference voltage output depending on the supply current is $\Delta V_{BG}(I_{Supply}) = (2.898 \pm 0.005)\,\frac{\mathrm{mV}}{\mathrm{mA}}$. If during detector operation a possible supply current variation of $I_{PWR} = 10\,\mathrm{mA} \pm 5\,\mathrm{mA}$ is assumed, the output precision of the reference voltage is limited to a variance of $\approx 2.5\%$, with respect to the average value. While the regulator is working, the output voltage of the band gap reference is $1.144\,\mathrm{V} \pm 0.030\,\mathrm{V}$.

To test the reliability of the voltage regulator of the SPP chip, the chip has been operated in a climatized environment simulating the detector volume, with and without active cooling. During the test, the temperature of the chip was varied between -20°C (lowest temperature when cooling is active) and +50°C (highest temperature before the interlock system cuts all power from the detector). Measured voltages were again the output of the band gap reference and the operating voltage. As seen in Figure 5.3, the

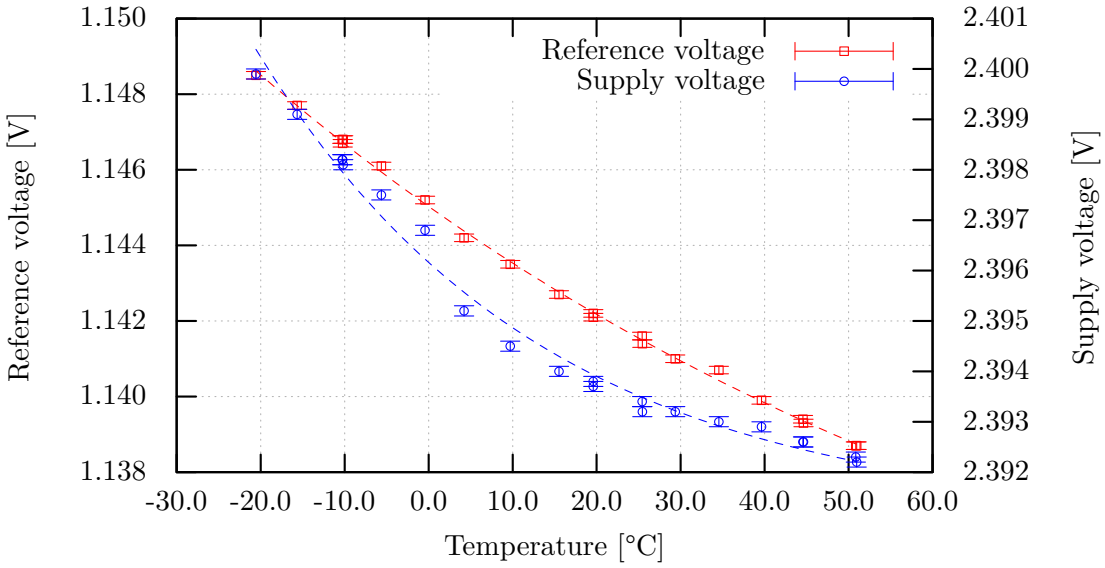


Figure 5.3: *Dependance of the reference voltage output of the SPP depending on the environmental temperature. Supply current of the SPP chip is 10 mA.*

output voltage of the band gap reference degrades exponentially with higher temperature (fitted function: V(T)=10 mV · exp(-15 · 10^{-3} $\frac{1}{°C}$ · T)+1.13 V, χ^2_{ndf}=1.2). Over the entire temperature range, the reference voltage shows an variance of ≈0.9 %, with respect to the average value. As the supply voltage is directly depending on the band gap voltage, it also shows an exponential degradation (fitted function: V(T)=5.0 mV · exp(-29 · 10^{-3} $\frac{1}{°C}$ · T)+2.39 V, $\chi^2_{ndf} = 8.6$).

Comparator

As the voltage regulation of the module's supply voltage in the ATLAS pixel detector is handled by the shunt regulators implemented in the readout chips, the comparator for shunt regulation in the SPP was disabled during the tests. For the tests of the other comparator of the SPP, which generates the shunting command to switch modules off, the tripping voltage was configured to be at 2.11 V. This was done by adding an additional resistor of 8.2 kΩ (5%) in front of the built in voltage divider (14 kΩ to 10 kΩ), which divides the module voltage inside the SPP, to match the output voltage of the band gap reference at the desired tripping point. It is not possible, to measure the output of the comparator directly as it is routed into the flip-flop inside the chip. Hence, the output voltage of the flip-flop was measured, while the module voltage was swept from 0 V to 2.3 V. At a module voltage of 2.100 V ± 0.002 V, the output of the flip-flop went to a high state. A reset of the flip-flop was not possible by changing the module voltage. Only a chip reset or data communication could change the flip-flop state after it went to high.

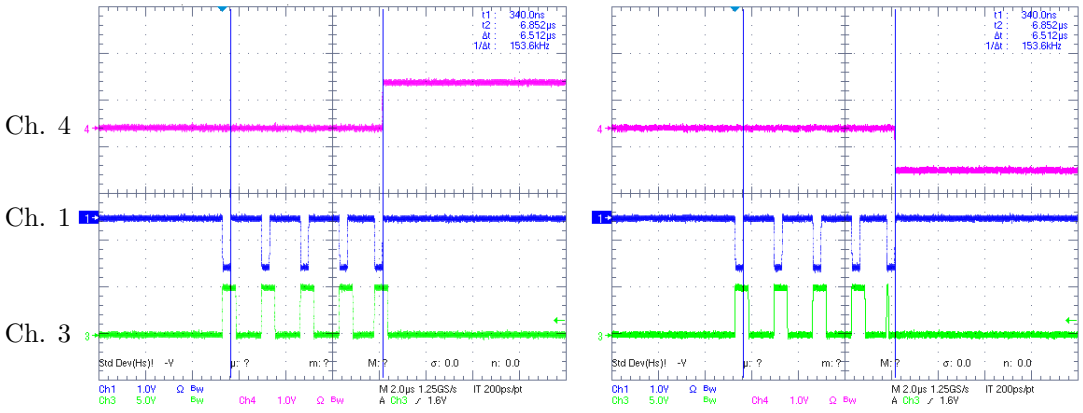


Figure 5.4: *Snapshots of data communication with the SPP. Left: A 11111_2 signal is transmitted to the SPP. Right: A 11110_2 signal is transmitted to the SPP. Channel 1: Sampling timer. Ch. 3: Data input. Ch. 4: Output (AC coupled).*

Shunting and addressing logic

The digital signal to address the SPP chip was generated by a PIC18F4550 microcontroller, which was controlled by a computer via USB. The address IOs of the SPP chip were tied to VDD with 10 kΩ resistors (address 1111_2). Figure 5.4 left and right show a screen shot from an oscilloscope recording data transmission to the SPP and how the SPP responses. Channel 1 (blue signal) measures the sampling timer signal of the SPP, channel 3 (green signal) measures the data input signal and channel 4 (purple signal) measures the output of the shunting flip-flop.

Every time, the SPP recognizes a positive edge on its data input, an internal timer is started and the sampling timer output is pulled to chip ground. After 400 ns, the timer expires and the reference clock is set to VDD again. At this time the SPP samples the signal on the data input. Should the data input fall back to ground before the timer finishes, the bit is read as '0', should it fall back after the timer expires the bit is read as '1'. The first four bits identify the chip address, the fifth bit holds the new value for the shunting flip-flop. Figure 5.4 left shows a signal of five ones being transmitted to the SPP. After the fifth bit has been sampled, the flip-flop output is switched to '1'. In Figure 5.4 right, the opposite case is shown, where a zero is written into the flip-flop.

Shunting transistors

At the beginning of the SPP testing, it turned out that the small shunting transistor in the SPP is not suited for the need in ATLAS pixel. The remaining voltage drop on the shunting transistor is with 650 mV at a serial powering current of 1 A too high. Hence, no further tests were performed with the small transistor.

The large transistor however, is capable of shunting a module with a supply current of 1 A with a remaining module voltage of approximately 130 mV. Figure 5.5 shows a combined test of the over voltage protection, the switching by command and the shunting. In this measurement, the tripping voltage was 2.1 V. The current supplied by

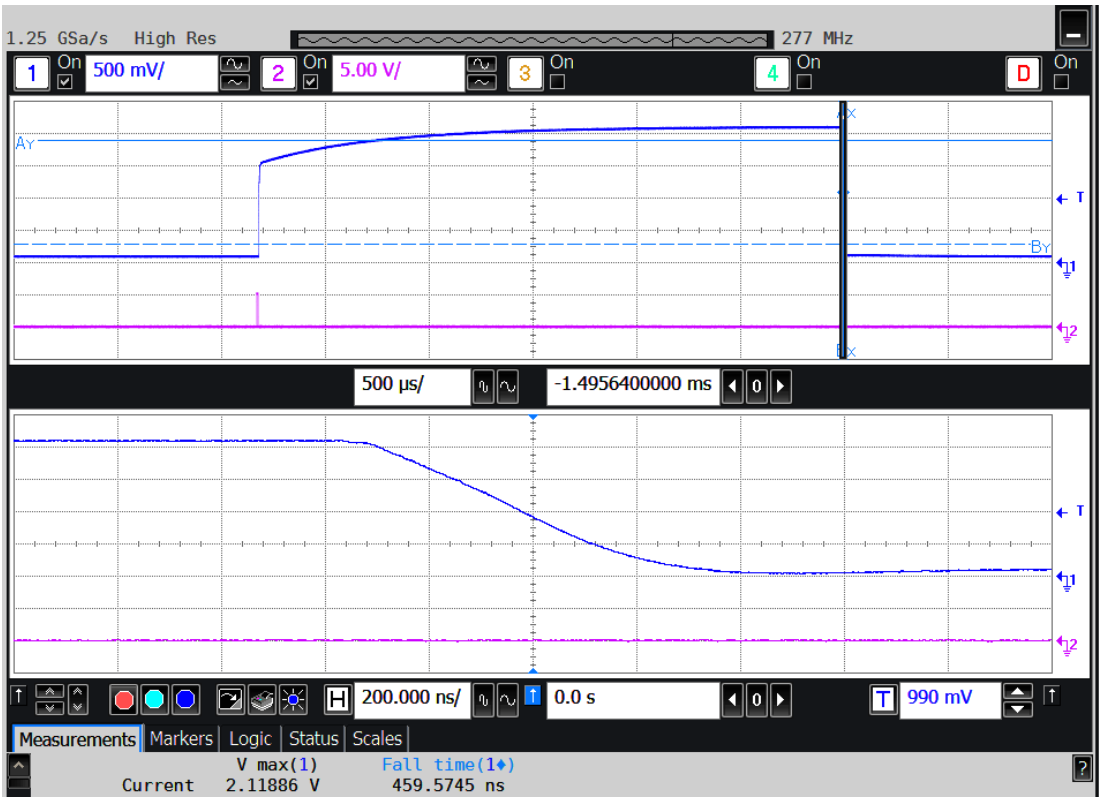


Figure 5.5: *Snapshot of the module voltage (Channel 1, blue) while the SPP received a command (Channel 2, purple) to stop the shunting. The upper diagram shows the entire measurement with a moderate time resolution. The lower diagram gives a detailed view of the time span under the thin gray rectangle in the upper window (at 1.5 ms).*

the Agilent PS 2 was slightly above 1 A so that the voltage drop over the load resistor R_L exceeded the tripping voltage. In the beginning, the SPP is shunting the module and the module voltage (Channel 1, blue curve) is low (130 mV). After $\sim$ 1.2 ms a command to switch the module back on is sent to the SPP. Channel 2 (purple curve) shows the data input line of the SPP chip. The spike on channel 2 are the five bits sent to the SPP (similar to Figure 5.4 left). Immediately after the SPP read the command, the module voltage rises, until it reaches the tripping voltage. The slow rise of the module voltage originates from the regulating characteristics of the Agilent power supplies, which is a voltage source operating in current compliance. At the point, where the module voltage exceeds the tripping voltage, the SPP starts to shunt again and the module voltage drops back to 130 mV within $\sim$ 460 ns.

Compatibility tests

After the SPP has been investigated intensively, the load resistor R_L was removed, and the SPP was connected to a real detector module from the Bonn University. A threshold scan performed on the module with and without the SPP attached showed,

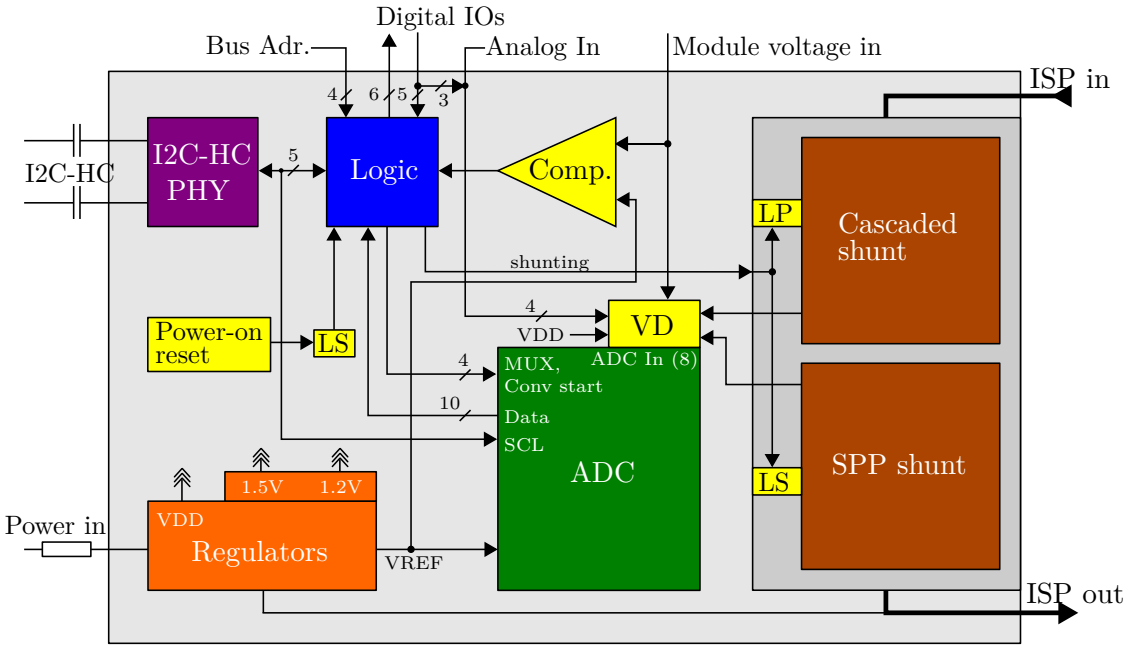


Figure 5.6: *Schematic of the PSPP and its components. Debug signals not shown (see Table 5.3 on page 94 for all I/O signals). The colors indicate the classification of the particular block. Yellow: Analog blocks. Brown: High power transistors (shunts). Blue: Synthesized logic. Green: Mixed signal. Purple: Communication. Orange: Power supply of the chip. The abbreviations LS, LP, and VD stand for 'level shifter', 'low pass filter', and 'voltage divider' respectively.*

that the impact of the SPP onto the module is negligible. The noise of the module has not change.

The tests performed with the SPP show, that the concept of a bypass chip next to a detector module is feasible. It is possible to switch detector modules with a bypass chip and the chip's impact on the detector is negligible. However, the specifications and needs for a bypass chip for the pixel detector differ from those in the strip system. Hence, a modified and enhanced version of the SPP chip is needed to set up a control system for a serially powered pixel detector.

5.2 PSPP, a prototype for the DCS chip

In the frame of this thesis, the first prototype for the DCS chip (see Section 3.2.1) was designed for the IBM 130 nm process with the corresponding CERN design kit[2]. Due to the affinity to the SPP chip, this prototype is called Pixel Serial Powering and Protection (PSPP) chip. Although the PSPP was designed to be a proof-of-principle study for the bidirectional AC coupled communication, it was designed to fully supply the functionality of a DCS chip. This includes the following features (see also Figure 5.6):

- Module switching

[2] version 1.8

- Module protection
- Module status monitoring
  - Temperature monitoring
  - Voltage monitoring
- Floating GND operation

Only the harsh radiation tolerance requirements of the DCS chip, as described in Section 4.6, cannot be met for various reasons. One reason is, that the logic blocks of the PSPP are synthesized without the implementation of TMR due to development time issues. This reduces the tolerance against single event upsets (SEU) of the PSPP chip. Another reason is that some of the SPP's analog blocks, which were tested as described in Section 5.1.2 were adopted for the PSPP design with some minor modifications. This includes the voltage regulators for VDD and VREF, the comparator, the power-on reset, and the big shunt. These blocks contain FETs with thick gate oxides (thickness 5.2 nm), which have a lower tolerance against total ionizing dose (TID) effects than the thin gate oxide transistors (thickness 2.2 nm) [46, 64] and thus are not suitable for radiation environments such as the inner tracker in ATLAS. This does not include the voltage generators deriving the 1.2 V and 1.5 V, as these were designed especially for the PSPP chip. Nevertheless, the PSPP contains all functional blocks to provide the full functionality of the DCS chip and thus can be used to control a chain of serially powered modules under laboratory conditions.

5.2.1 AC coupled I2C-HC

To receive commands to control a detector module, each DCS chip needs a link to the outside of the detector. A modulation of the data link onto the power line, similar to the SPP chip was in discussion during the design phase of the PSPP, but then rejected, because the DCS concept requires bidirectional communication. Due to the lack of an evaluated and tested alternative one wire bus, the implementation of the well known two wire bus I2C-HC was chosen with the DCS controller as the master and the DCS chips as the slaves. One advantage of a synchronous bus like the I2C-HC bus is the omitted need of an oscillator inside the chip. This leads to a reduced power consumption, as the chip is only clocked during data transmission.

The DCS concept requires floating data transmission, as each module in a serial powering chain and thus each slave on the I2C-HC bus (DCS chip), has an individual ground potential (see Section 3.2). A capacitive decoupling is necessary for the bus lines. As each module / DCS chip is on a different voltage level, the decoupling has to be on chip level, which means that each chip needs a decoupling capacitor on each bus line as shown in Figure 5.7 left. The bus line itself is directly connected to the bus line drivers of the I2C-HC master (DCS controller), which shares the ground potential of the EoS card. The implementation of such a decoupling creates some issues, though. When the system is active, the decoupling capacitors charge up to the voltage difference between the individual slave and the master plus the mean voltage of the bus line. When the

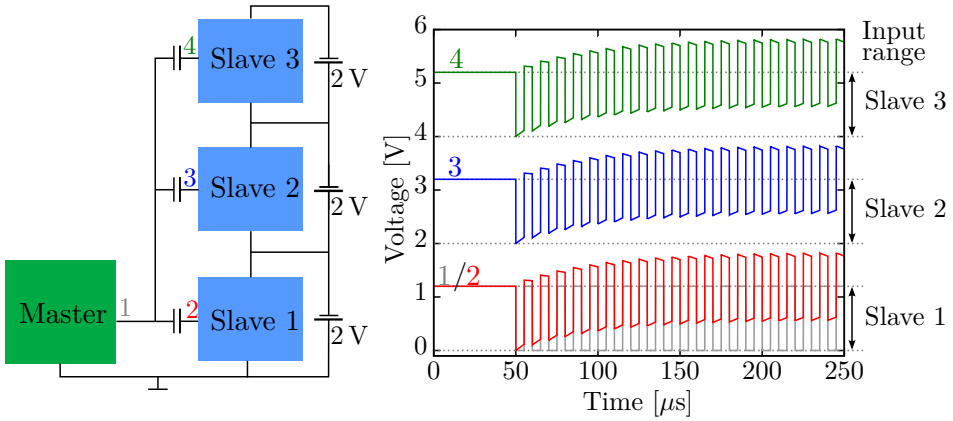


Figure 5.7: *Left: Schematic of the capacitive decoupling of the I2C-HC bus on a serially powered stave. Right: Signal drift due to charge up of the decoupling capacitors (1 nF). After 50 µs the master starts transmitting a 100 kHz clock with 50 % duty cycle. Simulated with Cadence Spectre. Both: Supply voltage of the detector modules is 2 V, the supply voltage for the bus drivers is 1.2 V.*

bus is idle, the mean voltage on the bus line is 0 V. When the bus is active and data is transmitted, the mean voltage can be assumed to be half of the dynamic range of the bus driver, a MSR[3] of 1. This charge up quickly moves the signal out of the dynamic range of the data inputs of the slaves as seen in Figure 5.7 right. The signal drift could be reduced by increasing the decoupling capacitance and reducing the occupancy on the bus. But larger capacitors would require larger line drivers and add more material for the capacitors and the chips. A limitation of the bus occupancy could increase the response time of the control system.

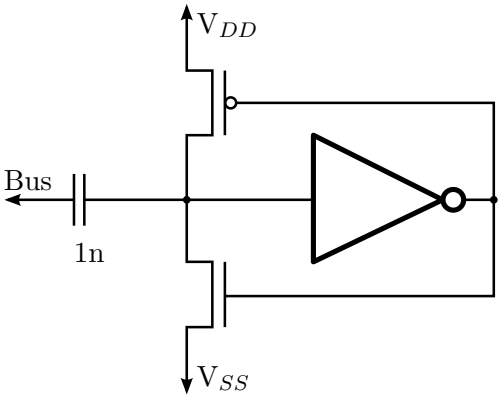


Figure 5.8: *Schematic of the Keeper structure behind the decoupling capacitor. The width to length ratios for the FETs are 3/2 (P-FET) and 1/2 (N-FET).*

To keep the voltage levels of the incoming bus signals in valid ranges, the principle of encoding data in voltage levels and constant currents has been discarded. A new physical layer was developed which should require as few modifications on the existing I2C-HC slave logic as possible. This new physical layer transmits charge to or from the gate capacitances of the data inputs. Thereby the transmitted charge rises or lowers the input voltage on the data inputs by charging or discharging the gates. The absolute voltage level behind each decoupling capacitor (on slave side) is set by a keeper structure (bistable multivibrator), which weakly pulls the input voltage either to

[3] **M**ark to **S**pace **R**atio

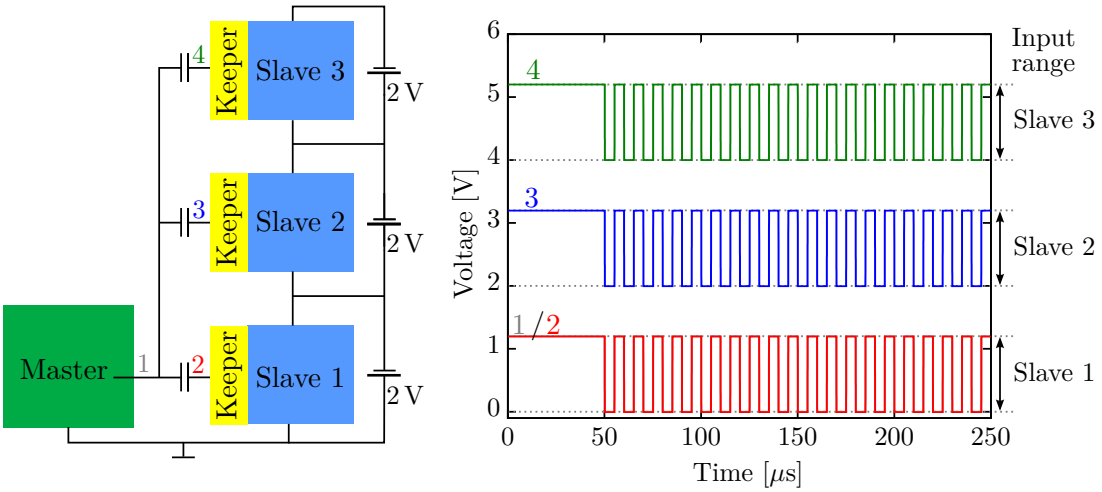


Figure 5.9: *Left: Schematic of the capacitive decoupling of the I2C-HC bus with a keeper structure on the slave's inputs. Right: The signal transmitted by the master reaches the slaves without any drift and covers the full dynamic range of the data inputs. After 50 µs the master starts transmitting a 100 kHz clock with 50 % duty cycle. Simulated with Cadence Spectre. Both: Supply voltage of the detector modules is 2 V, the supply voltage for the bus drivers is 1.2 V. The decoupling capacitances are 1 nF.*

the chips V_{DD}[4] or V_{SS}[5] as seen in Figure 5.8. A current pulse high enough can push the gate voltages under or over the threshold of the keeper and switch the value of the data input. Thereby the current needs to be high enough to charge the gates and to produce a voltage drop on all keeper outputs on the bus. This requires a strong output driver on the side of the master. Once the threshold of the keeper is exceeded, the keeper switches its state and pulls the input voltage to the corresponding new value. Figure 5.9 shows a simulation of a transmitted 100 kHz signal with an implemented keeper structure. The input signal of each slave fully retains in the dynamic range of the corresponding slave.

In the PSPP chip, the keeper is realized as a weak pull up resistor (50 kΩ) and a small pull down transistor[6] for both the data and the clock line of the I2C-HC bus. The pull up resistor is a residue of the typical I^2C PHY[7] design and was chosen due to limited development time. A replacement of the resistor with a pull up FET would reduce the current consumption, while the input is in low state. The pull down FET is controlled by a standard cell inverter, which defines the switching threshold. To reduce the current, necessary to switch the state of the bus line, the keeper in the data input of the PSPP is only enabled while the clock line is high.

To read a signal back from a slave to the master, the responding slave needs to control the bus line, as the master does while writing. Therefore the writing slave needs to have the strongest line driver on the bus, as it needs to switch the inputs (and the keepers) of all other nodes on the bus. This can only be achieved, if the data output

[4] Positive supply voltage
[5] Negative supply voltage
[6] Overall width/length ratio = 2 µm / 2 µm.
[7] **Phy**sical layer

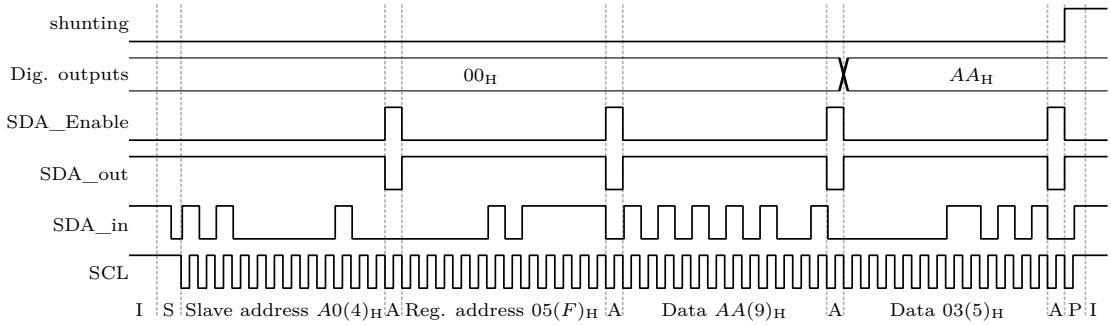


Figure 5.10: *Simulated writing sequence with the I2C-HC slave. The bus master addresses the slave with address $A0_H$ and writes to the registers 05_H (Digital outputs) and 06_H (shunting status) subsequently (see Table 5.1). Digits in braces indicate the 4-bit Hamming checksum. After each byte written by the master, the slave answers with an ACK bit. Letters in the bottom line indicate the I2C-HC message conditions: I: Bus idle; S: Start condition; A: ACK bit; P: Stop condition.*

stage of the master is deactivated, while it reads. The output stage of the clock line is never deactivated. Additionally, the writing slave needs an output driver on the data line which is strong enough to switch the keepers of all other slaves. This output stage must only be active while the slave is writing, as it blocks the bus. To switch on the strong output stages of the master and the slaves, at the correct time (and only then), the I2C-HC master and -slave logic needs to provide an output-enable signal.

In the PSPP the output line driver consists of strong transistors forming a push-pull stage with an overall W/L[8] ratio of 200 µm / 0.4 µm (PMOS) and 64 µm / 0.4 µm (NMOS). These values produced the best results in communication simulation with up to 10 slaves per bus. Both, the output stage and the keeper transistors are switched by synthesized logic, which generates the gate signals from the data signals coming from the I2C-HC slave.

5.2.2 PSPP Logic core

The logic core of the PSPP is a standard cell logic block, synthesized from Verilog code. This code is a combination of two modules, which provide the functionality of the PSPP. The first module is the I2C-HC slave, which handles the communication with the DCS controller and controls most of the periphery of the chip. The second block is the shunting logic, which controls the shunting transistors of the PSPP. The shunting logic was not implemented into the I2C-HC slave and handled individually in order to keep the necessary changes to the I2C-HC slave at a minimum.

I2C-HC slave

The Verilog code of the PSPP I2C-HC slave is an adapted version of the I2C-HC slave code used in the Cofee1 chip[50]. As the code of the I2C-HC slave was not developed in terms of this thesis, only the modifications made to the code will be described.

[8] **W**idth to **L**ength

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
00	Chip ID [15:8]								R
01	Chip ID [7:0]								R
02	0	0	0	0	0	0	ADC data [9:8]		R
03	ADC data [7:0]								R
04	Digital In [7:0]								R
05	Digital Out [7:0]								R/W
06	0	0	0	0	0	0	shunting	shunt CMD	R/W
07						ADC MUX [2:0]			R/W
08	ADC data [9:2]								R
09							ADC data [1:0]		R

Table 5.1: *Register map of the PSPP I2C-HC slave.*

The I2C-HC slave module for the Cofee1 chip was developed to be used with an open collector output, commonly used with standard I²C. Thus it is not fully compatible to the physical layer described above. Therefore, code was added to the top level of the I2C-HC slave module, which generates an enable signal to be used by the physical layer after the following conditions: Depending on the direction of transmission of the bus the enable signal depends on two other signals. While the master is in control of the bus, the output stage is activated for the ACK bit (13th bit), if the sent bus address and the slave address match. With the activated output stage (SDA_Enable = 1), the addressed slave can give an ACK or a NACK by setting the data line of the bus to '0' or '1' respectively. An example of a writing sequence in I2C-HC communication, where the SDA_Enable signal is shown, can be found in Figure 5.10. Vice versa, if the addressed slave takes control of the bus, the conditions for the enable signal change. While the slaves controls the bus, the output stage is enabled except during the 13th bit, while the slave reads ACK signal from the master. Should the master transmit a NACK signal (or no ACK signal) the slave releases the bus and output stage is disabled.

Another major change in the code was the adaptation of the ADC control logic. Almost all of the ADC related registers of the original I2C-HC slave have been removed and replaced with a logic fitted to the ADC implemented in the PSPP. To control and read the implemented ADC, the new code holds two registers, which can be read or written via the I2C-HC bus. The first register holds the results of the ADC. This register is 10 bits wide (resolution of the ADC) and therefore has to be accessed as two register addresses from the I2C-HC bus. This result register is read-only. The other register holds the address for the analog input multiplexer of the ADC. The multiplexer address is three bits wide, as the ADC can sample 8 different input channels. This register can be read and written. The clock for the ADC is just an inverted clock signal coming from the clock line of the I2C-HC bus. The clock is permanently fed into the ADC. The control signal for the ADC triggers the conversion. It is pulsed every time, the multiplexer address is written. After the ADC received the trigger signal, it converts the input channel set in the multiplexer in the next eleven clock cycles coming from the bus. As each transmitted data byte needs 13 clock cycles (8 cycles for the data byte, 4 for the check sum and one for the ACK bit), the result of the conversion can be read after the next data transmission.

The rest of the code remained unchanged. Only the register mapping was modified (see Table 5.1). Besides the described ADC control, the I2C-HC slave provides 8 digital inputs, 8 digital outputs and a 16 bit chip address, which are directly mapped into the register bank. The chip address is planned to be a serial number to uniquely identify each DCS chip. However, this feature requires special treatment for each individual chip and was not implemented into the PSPP. Instead the chip ID has a fixed value of $21F4_H$. At register address 06_{H}, the control of the shunting logic is located. The shunting bit indicates the status of the shunting transistors. A '1' indicated that the PSPP is in shunting mode. The shunt command bit controls the shunting logic. When a '1' is written, the PSPP starts shunting. When a '0' is written the PSPP deactivates the shunting.

As seen in Table 5.1, the ADC data is mapped twice in the register map. At register address 02_{H} and 03_{H} the result are read right justified, while at address 08_{H} and 09_{H} the results are read left justified. As the left justified ADC results are stored right behind the multiplexer address, they can be read subsequently after the conversion has been started, as the address register (which points to the register address currently in use) is incremented after each written byte. Only a restart condition[9] and the slave address (in read mode) have to be transmitted after writing the multiplexer address, to directly read the ADC results. This way an additional writing of the address register is superfluous.

Shunting logic

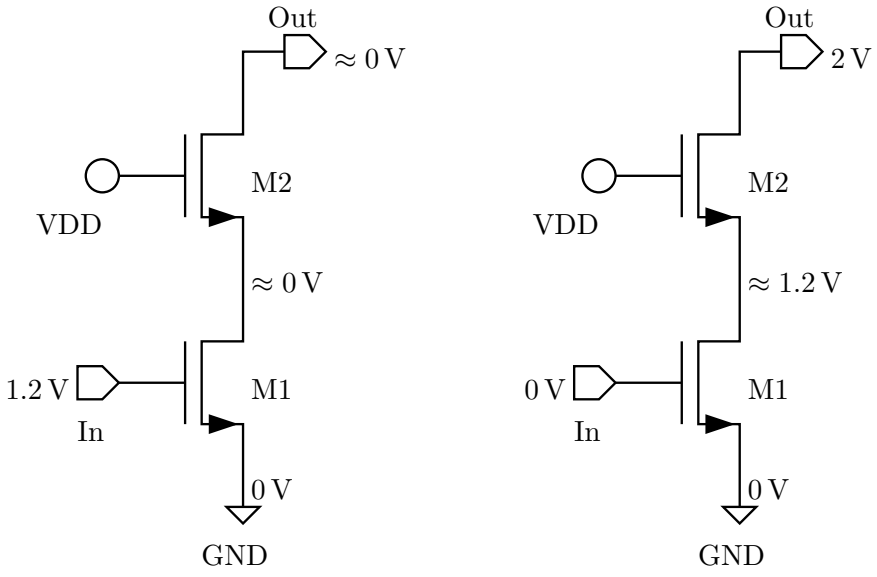
The shunting logic block of the logic core evaluates the comparator output and controls the gates of the shunt transistors. A rising edge of the comparator output (over-voltage detected on the supervised module) activates the shunting transistors. To deactivate the shunting transistors, the correspondent command has to be sent on the I2C-HC bus, as described above. When a command to deactivate the shunt is sent, the transistors are switched off and the module voltage can rise again. If there is a malfunction and the rising module voltage exceeds the over-voltage threshold, the shunt will immediately begin to shunt again. So in case of a malfunction on the serial powering chain, the module voltage will exceed the over-voltage threshold for a time equivalent to the signal propagation delay in the PSPP every time the shunting is switched off. This delay should be in the range of nanoseconds.

Power-on-reset

To start in a defined state, the PSPP is equipped with a power-on-reset, which sets all registers in the chip to '0'. This includes the shunting logic, which means that shunting is deactivated after power up.

The block, generating the reset signal is taken from the SPP design. It generates a pulse, with a width of approximately 40 µs on its output after the chip is powered. As the power-on-reset block output swings between chip VDD and chip GND, the output voltage has to be lowered. The reset pulse is routed into level converters, supplied with 1.2 V, which generate a lower reset pulse for the synthesized logic block.

[9] see I²C specification [52]



a) shunting b) not shunting

Figure 5.11: *Schematic of a cascaded shunt transistor with the expected terminal voltages for both, the shunting (a) and the idle (b) case.*

5.2.3 Shunting with the PSPP

The PSPP chip contains two large shunting transistors. The first transistor is taken from the SPP chip. This transistor contains thick gate oxides, thus the radiation tolerance required for a DCS chip is not given and it is not suited for use in the detector. Nevertheless, it was still included as a fail safe solution for testing in the laboratory, as it has been tested to successfully shunt a module current of 2.4 A. The SPP shunt transistor is composed of ≈ 600 DGN-FETs[10] with a length of 600 nm and a width of 100 µm, leading to an effective width of $w \approx 60.000$ µm. A Spectre simulation of the extracted layout showed that a shunting current of 2.4 A generates a voltage drop of 99.58 mV between Drain and Source. The Gate was thereby tied to a logic high level (2.3 V, supply voltage). This results in a heat deposition of ≈ 240 mW.

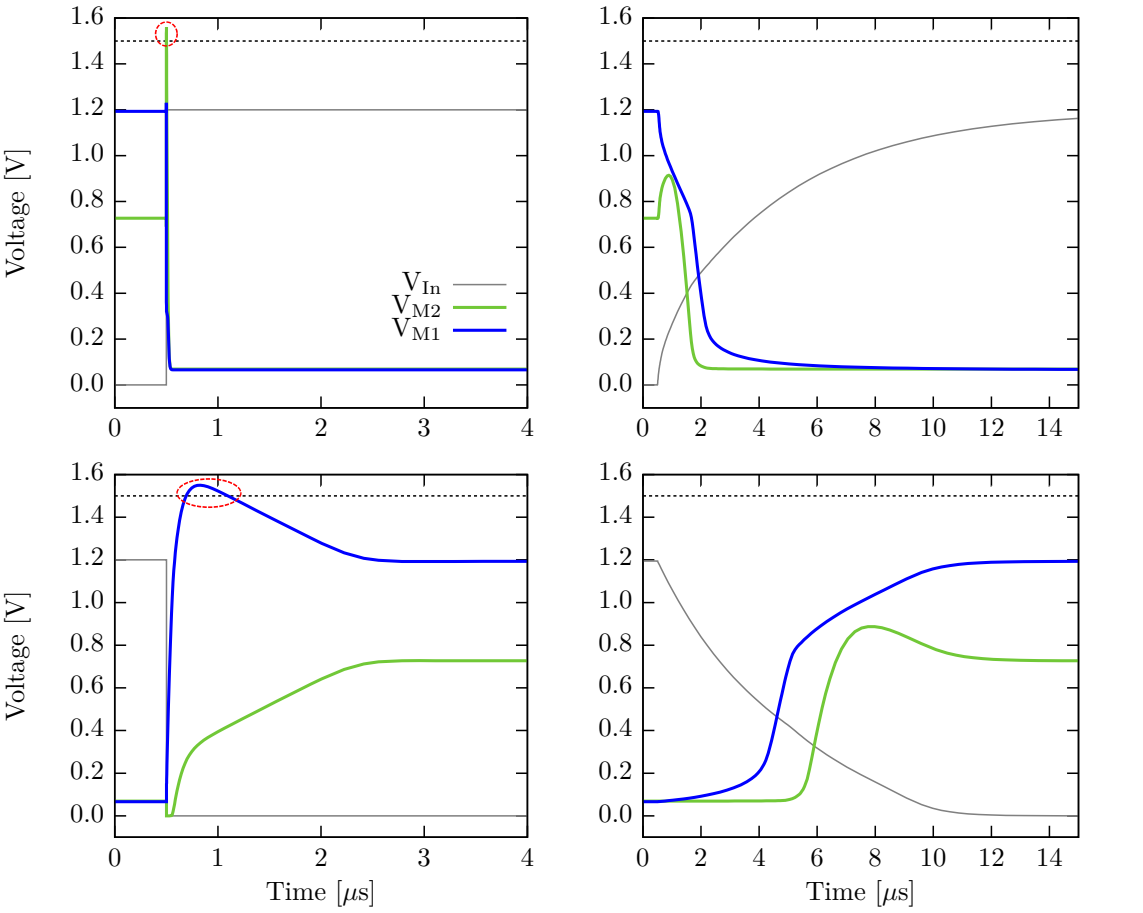
In the final DCS chip, the use of thick gate oxide transistors should be avoided to enhance the radiation tolerance of the chip. The preferable thin gate oxide transistors in the 130 nm process have a maximum Drain-Source-voltage of 1.6 V, though. Thus a simple replacement of the two transistor types is not possible, as the envisaged module voltage can be as high as 2 V. The reliable switching of voltages higher than 1.5 V with transistors with thin gate oxides is possible though, if the transistors are cascaded [72]. Thereby, each transistor in the cascade must only switch voltage differences of up to 1.5 V, between its terminals. For a two fold cascade, as used in the PSPP, this can be achieved by biasing the upper FET with a constant voltage of 1.2 V (supply voltage of digital blocks). Figure 5.11 shows a cascaded shunt in both states, shunting

[10] n-type FET with thick gate oxide

(a) and not shunting (b). The In-terminal of the cascaded shunt is driven by the shunting logic, while the Out-terminal is connected to the power input of the detector module. When the cascade is in shunting state, the Gate of the lower transistor (M1) is at 1.2 V ($V_{Th} \approx 200\,\text{mV}$) and the transistor operates in the linear region. Hence, the node between the two transistors is pulled to GND. With the Gate of the upper transistor (M2) permanently being connected to 1.2 V, this transistor is also in the linear region and pulling the module voltage to GND. The detector module is switched off (shunted), as most of the serial powering current is bypassed through the shunt. In the not-shunting state, the Gate of M2 is connected to GND and the transistor is switched off. As the node between the transistors is not pulled to GND anymore, it is charged up and the voltage increases. At a certain point, when the V_{GS} of M2 decreases to the threshold voltage, it enters the cut-off region. Subthreshold currents through the upper transistor further charge the node between the transistors, until it has reached 1.2 V and M2 is switched off completely. As both transistors are switched off, no current is bypassed and the module can generate its operating voltage. With this type of cascading, a module voltage of up to 2.7 V can be switched (1.2 V Gate voltage of M2 plus 1.5 V maximum Drain-Source voltage). If the Gate voltage of M2 is increased to 1.5 V, module voltages of up to 3 V could be switched.

During the transition from idle to shunting state of the cascade, the node between the transistors is discharged to GND level. If the module voltage is not discharged at the same speed, the Drain-Source voltage of M2 can exceed the maximum value of 1.5 V (see Figure 5.12a, upper plot). The shunting to idle transition, there is a similar problem. When the M1 switches off slower than M2, the voltage on the M1 can exceed its maximum voltage (see Figure 5.12a, lower plot). To avoid this, the node between the transistors has to be charged/discharged slowly. Therefore, a low-pass filter with a time constant of $\tau \approx 13\,\text{ns}$ is implemented in the PSPP, which limits the transition time of the In-terminal of the cascade. Figure 5.12b shows the simulation of both transients with the low pass attached to the In-terminal. In this simulation, the Drain-Source voltage on neither transistor exceeds a voltage of 1.2 V. Yet, the module can still be switched off in less than 5 µs. For all simulations shown in Figure 5.12, the cascaded shunt was switched in parallel to a resistor (R=800 mΩ) and a capacitor (C=100 nF), which simulated the module. A serial powering current of 2.4 A was forced through the assembly.

The two transistors (M1 and M2) used for the cascaded shunt in the PSPP are equal and have both a width of 100 µm and a length of 0.6 µm. To avoid shorts by the substrate, triple well FETs have been used. Thereby the bulk contact of each FET is connected to its Source, while the N-well contacts are connected to the Out-terminal of the cascade. Both transistors share the same N-well, which is surrounded by a guard ring. Together with a repetitive routing structure around the two transistors, a single unit of the cascade consumes a rather large amount of die space. Due to the limited chip size, only three blocks with 200 cascaded transistors, with a width of 100 µm each, could be implemented into the PSPP, leading to an overall effective width of $w = 60,000\,\mu\text{m}$. Both shunting transistors in the PSPP occupy similar amounts of die area, their voltage drop, differs though quite a lot. Figure 5.13 shows a simulation of the voltage drop over both transistors (in shunting mode) depending on the shunting current. Both shunts



a) steep input signal b) low pass ($\tau \approx 13\,\text{ns}$) on the input terminal

Figure 5.12: *Simulation of the rising (upper plots) and falling (lower plots) transients of the cascaded shunt with an unfiltered input signal (a) and with a low pass filter at the input (b). The red dashed markings show where the maximum Drain-Source voltage of certain transistors is exceeded.*

were simulated with extracted parasitics and a module equivalent (see above). The input (Gate-) voltages were set to the expected values during operation. As seen in Figure 5.13, the voltage drop on the cascaded shunt is more than twice as high as on the SPP shunt and generates a heat dissipation of slightly more than 500 mW. Both, the voltage drop and the generated heat are too high for an operation in the detector, but still suitable for proof of principle tests in the lab.

5.2.4 Measuring with the PSPP

To measure the module voltage during detector operation, the PSPP contains an analog to digital converter (ADC). Due to the limited development time, it was decided not to develop a new ADC, but to implement the ADC used in the FE-I4 chip. As this

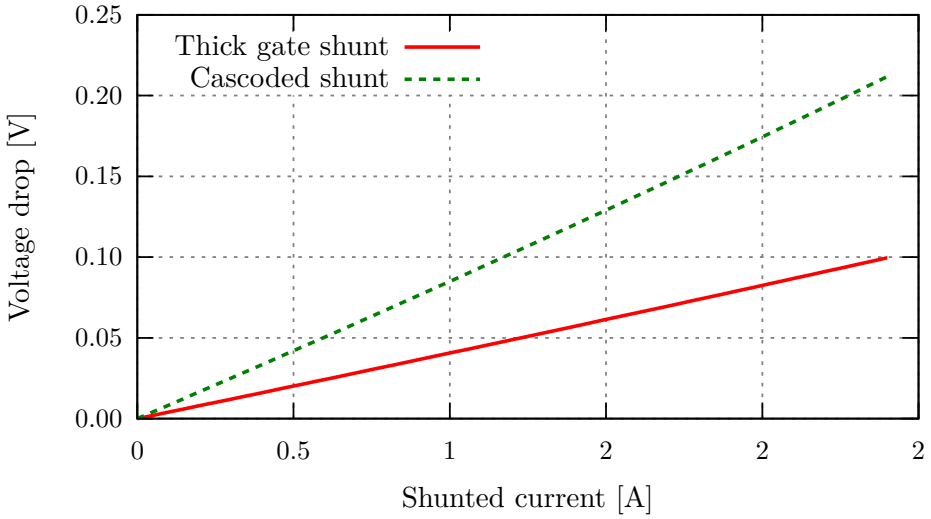


Figure 5.13: *Simulation of the voltage drop generated by the SPP shunt transistor (with thick gate oxides) and the cascaded shunt. Gate/Input voltages of the shunts were 2.3 V for the SPP shunt and 1.2 V for the cascaded shunt.*

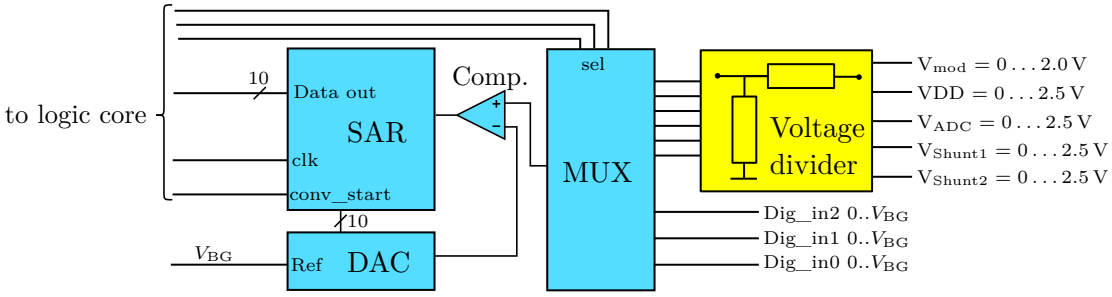


Figure 5.14: *Schematic of the ADC implemented in the PSPP chip. Blue parts (SAR, DAC, MUX, and comparator) are parts of FE-I4 IP.*

IP[11] block was developed within the ATLAS collaboration, it is especially designed for the use in the environment, the PSPP will operate in, and its behavior is well known inside the ATLAS collaboration.

The FE-I4 ADC (depicted in Figure 5.14) is an 8 channel, 10 bit successive approximation converter, designed to operate with the 40 MHz clock signal provided by the LHC. It contains the following major components, which are necessary for the analog to digital conversion:

- An 8:1 analog multiplexer
- the successive approximation register (SAR)
- a 10 bit digital to analog converter (DAC)
- a comparator

[11] **I**ntellectual **P**roperty

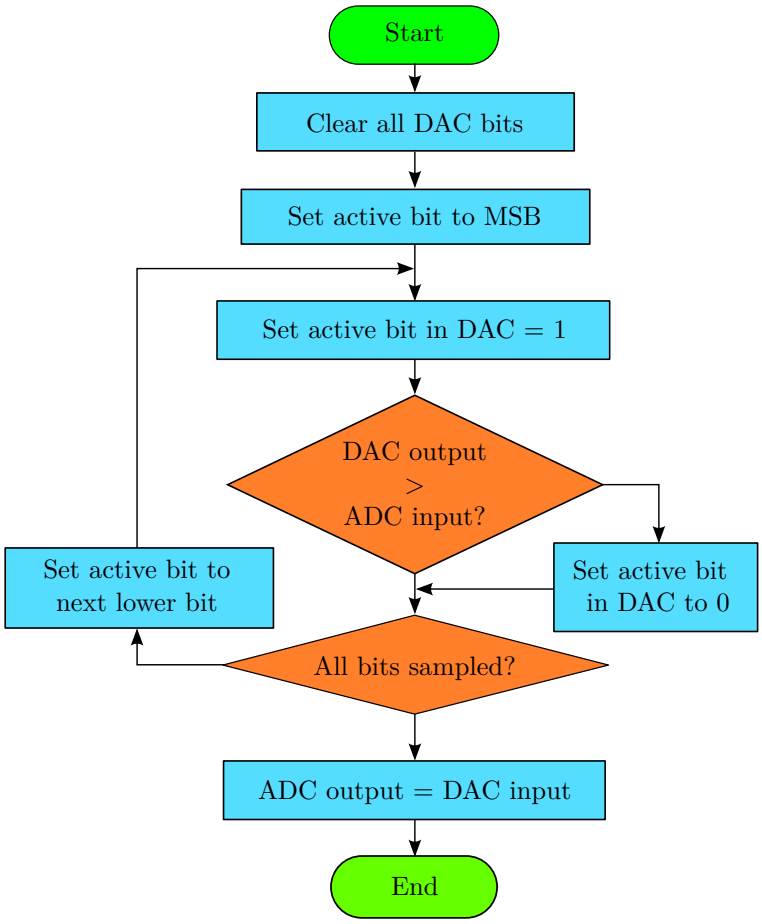


Figure 5.15: *Flowchart of the successive approximation algorithm.*

Besides the components listed above, the FE-I4 ADC also contains a 32:1 frequency divider, which derives an internal clock of 1.25 MHz for the conversion. As the PSPP chip only uses the clock provided by the I2C-HC bus, the frequency divider has been bypassed and the ADC is clocked by the 100 kHz bus clock. Simulations during the design of the PSPP have shown, that the ADC can be operated normally even at these rather low frequencies. A typical sample and hold mechanism, is not implemented. There is no need to freeze the signal during conversion as, in either case (FE-I4 and PSPP implementation), the ADC converts only DC or very slowly changing signals.

The DAC of the FE-I4 ADC uses weighted resistors and pass gates, which are controlled by the DAC input, to form a tunable voltage divider. This voltage divider then generates an output voltage, according to the following equation:

$$V_{\mathrm{DAC}} = V_{Ref} \cdot \frac{DAC_{\mathrm{IN}}}{1024}.$$

The DAC itself is controlled by the SAR, which performs the successive approximation algorithm (see Figure 5.15). This algorithm samples the resulting word of the ADC bit by bit, beginning with the most significant one: At the start of the conversion,

Block	Functionality	Block	Functionality
A	Voltage reference and supply voltage generator	E	Power-On reset
B	Voltage regulator for 1.2 V and 1.5 V	F	Logic block
C	Comparator	G	SPP shunt
D	ADC	H	Cascaded shunt

Table 5.2: *Block functionality of the PSPP chip according to Figure 5.16.*

the SAR clears all input bits of the DAC except the most significant bit. This sets the output voltage of the DAC to $\frac{V_{\text{Ref}}}{2}$. Subsequently, the output of the comparator is evaluated. If the comparator states that the DAC output is higher than the ADC input, the most significant bit of the result word is '0', else it is '1'. The remaining bits are sampled in the same way. In general, to convert the n-th bit, all higher order bits than n (which are already sampled) are written to the DAC input and the n-th bit of the DAC is set to '1'. All lower order bits have to be '0'. After setting the DAC output, the comparator output determines the value of the the n-th bit as described above for the most significant bit. When all bits have been sampled, the result word of the SAR can be read out by the PSPP's logic core.

An analog multiplexer in the ADC allows the conversion of 8 different input signals. The DCS chip concept foresees only two ADC channels (module and NTC voltage), so the remaining six channels were implemented for debugging purposes in the PSPP. As seen in Figure 5.14, the first five channels have voltage dividers at their inputs to enhance the dynamic input range of the ADC, which would otherwise be limited to the band-gap reference voltage of the PSPP. The remaining three channels can be used to sample the input voltage of the digital inputs 0-2.

5.2.5 PSPP Layout

Figure 5.16 shows the layout of the PSPP, extracted from the Virtuoso layout software. The letters in Figure 5.16 indicate functional blocks in the PSPP, which are also listed in table 5.2. The die contains 41 normal sized bond pads (one bond wire/pad) and 4 large bond pads (designed for many bondings). The normal sized pads carry the low current signals into the chip, while the large pads are carrying the shunting current. Only 18 of the implemented pads are essential for the operation as a DCS chip. Of the remaining pads, some are used for debugging purposes, as they are connected to the internal signals of the chip. These signals are decoupled from their sources with 10 kΩ resistors, so that the corresponding pads can be pulled to either voltage, without damaging the internal circuits of the chip. The other additional pads are used for evaluation purposes. Table 5.2 lists the bond pads and their functions. Pads connected to internal signals are marked as (internal).

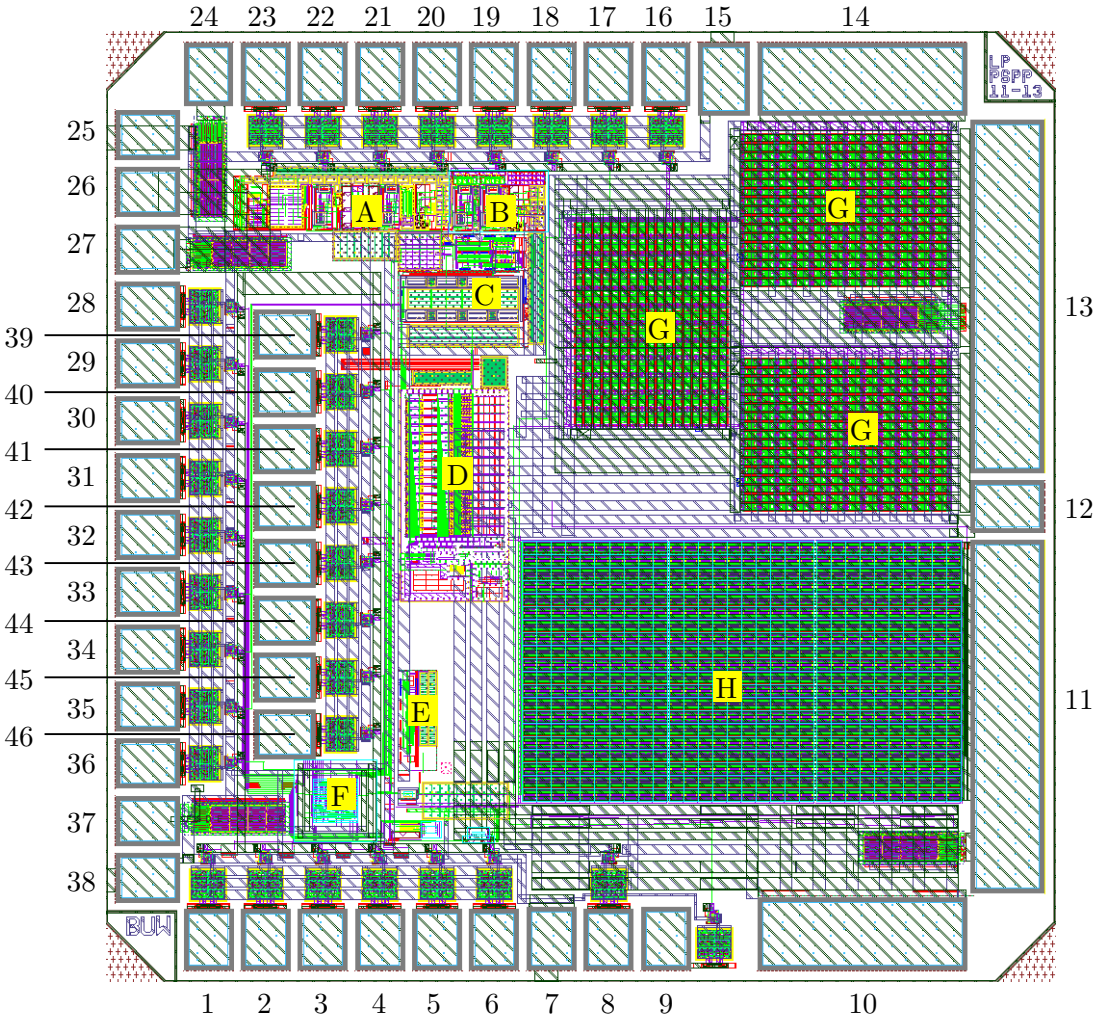


Figure 5.16: *Layout of the PSPP chip, extracted from the layout software. The letters and numbers indicating the block and pad functionality are explained in Table 5.2 and 5.3, respectively.*

Pad #	Functionality	Pad #	Functionality
1	Bus address bit 0	23	Bang gap reference output
2	Bus address bit 1	24	Supply voltage regulator output
3	Bus address bit 2	25	GNDD
4	Bus address bit 3	26	Supply current input
5	SDA (in/out)	27	Supply current input
6	SCL (in)	28	SDA_Enable (internal)
7	GNDD	29	SDA_Out (internal)
8	ADC input	30	Keeper_Enable (internal)
9	Power-On Reset (internal)	31	Digital input bit 4
10	GNDA (Source of the shunting transistors)	32	Digital input bit 3
		33	Digital input bit 2
11	Drain of the cascaded shunt	34	Digital input bit 1
12	GNDD	35	Digital input bit 0
13	Drain of the SPP shunt	36	Shunting state output
14	GNDA (Source of the shunting transistors)	37	Supply voltage regulator output
		38	GNDD
15	GNDD	39	SDA_In (internal)
16	Gate of the cascaded shunt (internal)	40	SCL_In (internal)
17	Gate of the SPP shunt (internal)	41	Digital output bit 5
18	Module voltage input	42	Digital output bit 4
19	Comparator output	43	Digital output bit 3
20	Comparator output (logic level)	44	Digital output bit 2
21	Voltage regulator 1.5 V output	45	Digital output bit 1
22	Voltage regulator 1.2 V output	46	Digital output bit 0

Table 5.3: *Pad functionality of the PSPP according to Figure 5.16.*

Chapter 6

Testing the PSPP

The PSPP design was submitted in November in 2013 to the MOSIS company and got shipped back to Wuppertal in February 2014. During the production period of the chip, a set of printed circuit boards (PCB) was designed to create a test environment for the PSPP. To handle the PSPP die, a carrier board was designed, which is shown in Figure 6.1. The test setup is described in the next sub chapter.

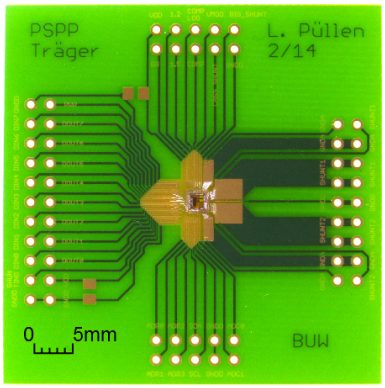


Figure 6.1: *Picture showing the carrier board, holding a PSPP die.*

The carrier board (shown in Figure 6.1) holds the PSPP die in its center and carries the signals from the PSPP bond pads to pin-headers on the brink. Female headers are mounted on the bottom side of the carrier, facing down, and allowing the carrier to be mounted onto the male headers of an evaluation board (Section 6.1). As seen in Figure 6.1, the carrier board also holds pads for two capacitors, which stabilize the supply voltage.

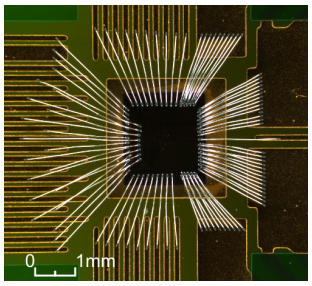


Figure 6.2: *Wire bonding of a PSPP glued onto a carrier board.*

The PSPP die is glued onto a $3 \times 3\,\mathrm{mm}^2$ metal square in the center of the carrier board. This square is surrounded by 150 µm thick wires (100 µm pitch) pointing to the center. These wires make the bond pads on the carrier, which are connected to the bond pads of the PSPP die by wire bonding. To improve the durability of the ultrasonic welding connections between the bond wires and the carrier board, all wires on the board are gold plated. Most of the bond pads of the PSPP and the carrier board are designed to carry one bond wire connection. These wires interface low current signals, like I/O signals and power supply for the chip. For connections which have to withstand high currents, the pads are larger and carry up to 14 bond wires per pad. These large pads interface the serial powering current in and out of the PSPP. Figure 6.2 shows a microscope picture of the wire bond connections of a PSPP die, glued onto a carrier board. The bonding was kindly performed by the Bonn University.

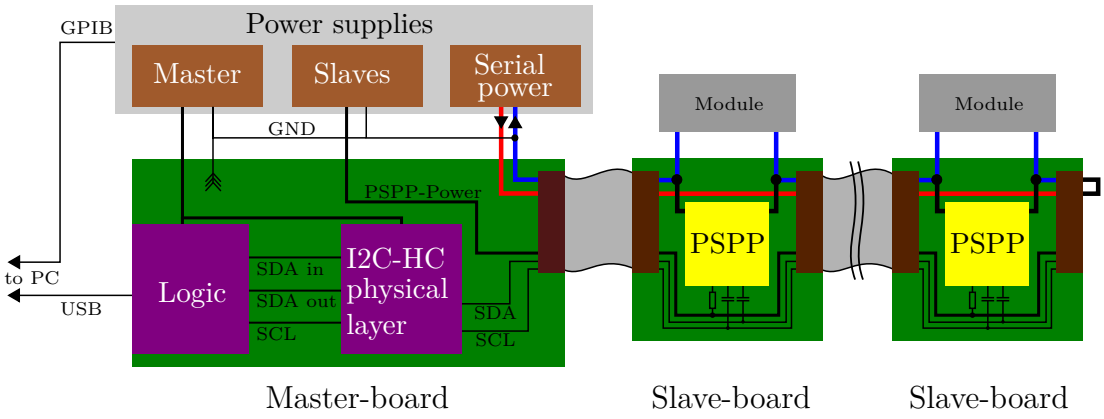


Figure 6.3: *Sketch of the testing setup for the PSPP chip, which simulates a serial powering chain.*

6.1 Test environment

The test setup for the PSPP consists of two kinds of PCBs, a Master-board and the Slave-boards as shown in Figure 6.3. These two board types are used to simulate a serial powering chain, similar to a serially powered stave (see Section 3.2). A simulated serial powering chain thereby contains a single master board (similar to the End-of-Stave card) and one slave board for each module in the chain. Connections between the Master board and the Slave boards are realized with a single 10 wire ribbon cable, to keep the setup clearly arranged. On this cable, the lines for the serial powering current, a supply current line for the slave PSPP chips and the I2C-HC bus lines are combined.

6.1.1 Master-board

The Master-board simulates the End-of-Stave (EoS) card with the DCS controller (see Section 3.2.1). It covers all necessary functions to setup a serial powering chain with Slave-boards in the lab. This includes the following:

- Master for the I2C-HC bus
- Interface to testing PC
- bundle data and serial power into one cable

A separate slave module, as foreseen in the DCS concept for monitoring of the EoS card, is not included.

Figure 6.4 shows a more detailed schematic sketch of the Master-board. As there is no prototype for a DCS controller, the logic part of the Master-board is implemented with a micro-controller (Microchip PIC18F2550). This micro-controller contains a USB interface, which is used to interface I2C-HC bus of the chain with the testing PC. The firmware of the micro-controller emulates an I2C-HC master in software with a bus frequency of 100 kHz. For the physical layer of the I2C-HC data line on the Master-board, a PSPP chip is used. The micro-controller directly interfaces the debug pins of the PSPP chip's physical layer to bypass the logic core. The clock line of the I2C-HC

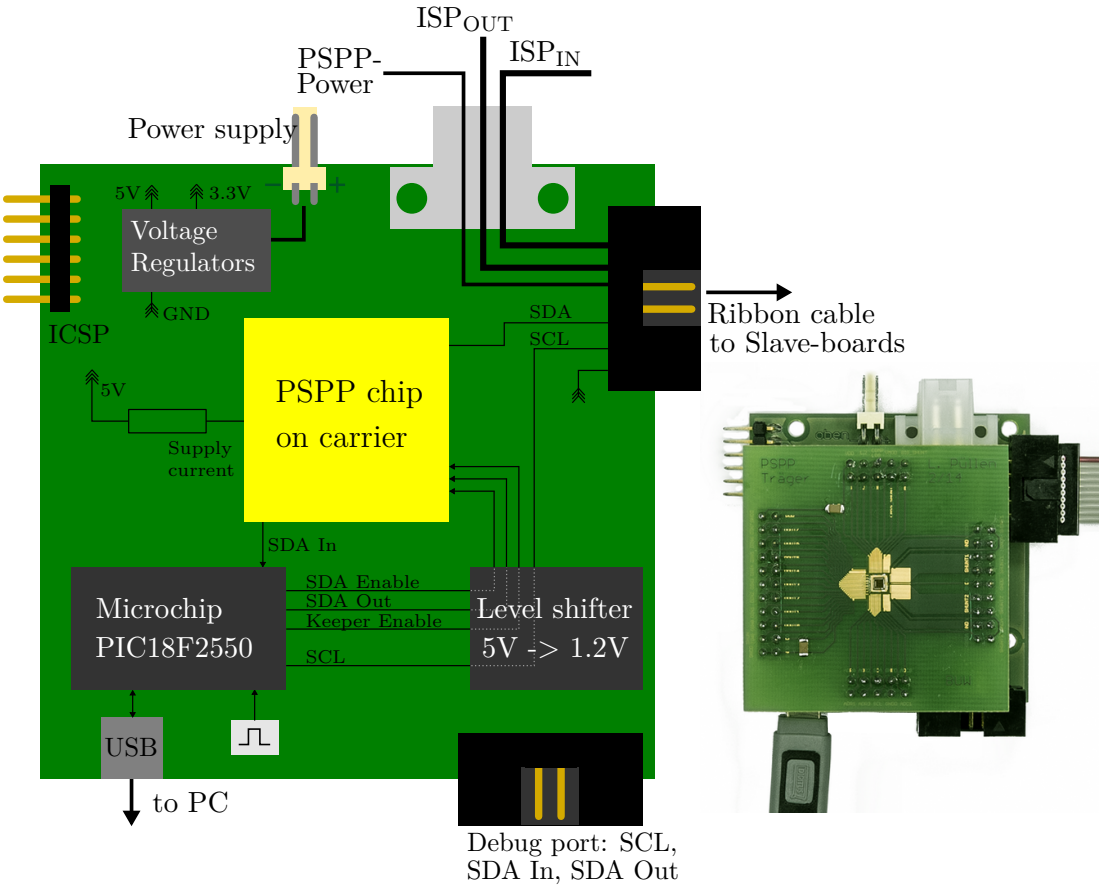


Figure 6.4: *Left :Sketch of the functionality blocks of the Master-board. Right, smaller: Picture of a Master-board with attached carrier board.*

bus is directly driven by the micro-controller. Due to the different supply voltages of the PSPP chip (1.2 V, generated from the supply current inside the chip) and the micro-controller (5 V), level shifters are implemented to interface both components. The SDA-in line from the PSPP chip to the micro-controller can be directly connected to one of the comparator inputs, with a threshold voltage of $\approx 0.6\,\mathrm{V}$. As the debug pins of the physical layer inputs on the PSPP chip are decoupled with $10\,\mathrm{k}\Omega$ resistors, a level shifter with push-pull capability is required to override any voltage level, coming from the logic core. Therefore the output voltage of the micro-controller is lowered by a voltage divider and then buffered by a fast operational amplifier, with high output current capabilities (OPA4354 from Texas Instruments).

To connect the micro-controller with the testing PC, the built-in USB interface is used. The firmware of the micro-controller emulates a serial port over the USB bus, which allows an easy implementation of the Master-board into the testing software. Additionally the Master-board also contains a ribbon cable connector for debugging on the low side and an interface for In-Circuit-Serial-Programming (ICSP), over which the firmware is written into the micro-controller. The schematic of the Master-board can be found in the attachment of this thesis.

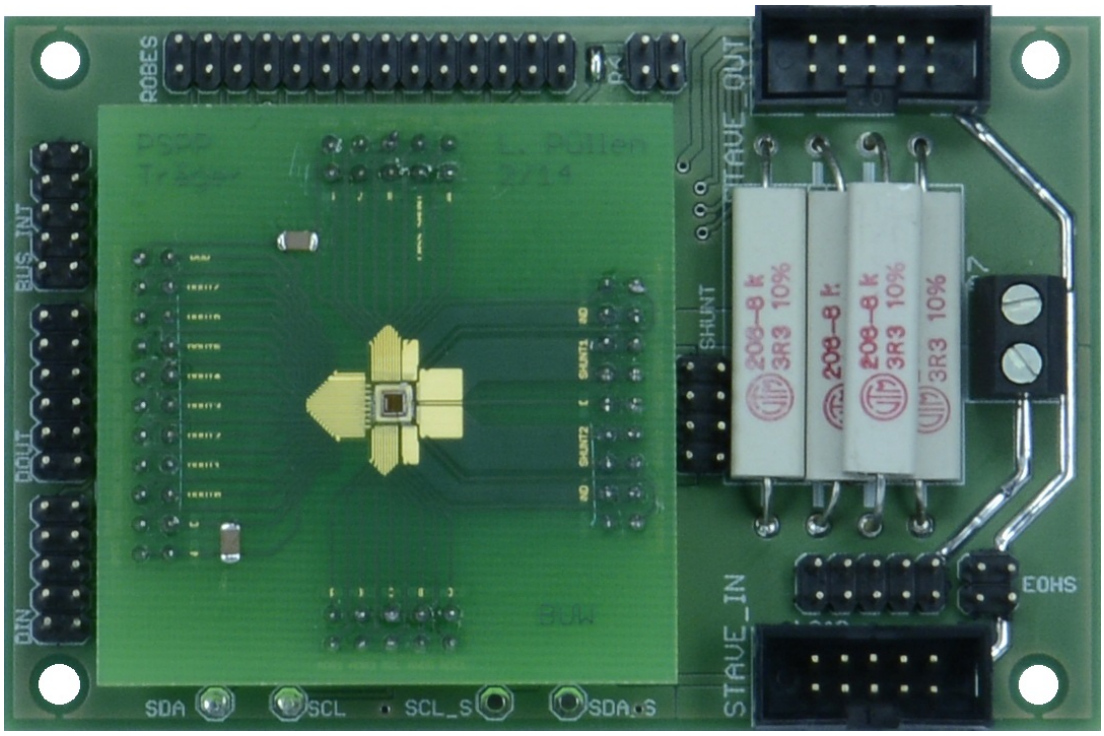


Figure 6.5: *Photo showing the Slave-board with an attached PSPP chip (on a carrier board).*

6.1.2 Slave-board

The Slave-board mainly works as a breakout board for the PSPP chip. It provides all necessary connections between the PSPP chip and the ribbon cable, to test the operation as a current bypass in a serially powered stave (see Figure 6.3). A Picture showing a Slave board with a PSPP chip (on a carrier) attached is shown in Figure 6.5. On the left side of the board, the digital I/O signals of the PSPP chip as well as the debug pins for the physical layer can be accessed via pin-headers. On the top row of pin-headers, right above the carrier board, further internal signals of the chip can be interfaced. This includes the voltage regulator outputs, the comparator outputs and the gates of the shunt transistors. Pads to probe the I2C-HC bus signals (on slave and master side) are located on the bottom side of the Slave-board. Below the carrier board (and thus not seen in Figure 6.5) several passive parts are located, necessary to connect the PSPP chip as a slave to the ribbon cable simulating the stave. This includes the following:

- Capacitors to decouple the SDA and SCL lines,
- a resistor to limit the supply current of the PSPP chip, which is drawn from the PSPP-Power line
- a hex code switch to set the chip address of the PSPP chip on the I2C-HC bus.

On the right side of the Slave-board, between the ribbon cable connectors, a set of high power resistors simulate the voltage drop of a working detector module. There are four resistors with a resistance of 3.3 Ω. This resistance produces a voltage drop slightly below 2 V from a current of 600 mA. These values define the operating point of a FE-I4B chip at normal operation. Using jumpers, each of those resistors can be connected to the serial powering current, simulating any number of readout chips between 0 and 4. On the right edge of the Slave-board, there is also a screw connector, which can be used to add any further electronics to the serial powering chain, or to connect the PSPP chip and the Slave-board to an actual serially powered stave, with real detector modules. The shunt transistor, used to bypass the serial powering current, can also be chosen by connecting either the drain of the SPP shunt or the drain of the cascaded shunt transistor to the current input on the Slave-board. To reduce the voltage drop, these connecting jumpers, located between the carrier board and the resistors, are two-folded. The two by two pin-header tagged with 'EOHS' (End-Of-Half-Stave) can be used to short the ISP_{IN} and ISP_{OUT} lines on the last board in a serial powering chain to close the circuit.

6.2 Testing of the voltage regulator functionality

To test the functionality of the voltage regulators, one Slave-board was connected to the Master-board with the ribbon cable. On the Master-boards only the PSPP-Power line was supplied with power, so that the current of the PSPP-Power line only supplies the tested chip. The current limiting resistor, between the PSPP-Power line and the PSPP chip's power input, was 1.5 kΩ in all tests. When the PSPP chip was powered up for the first time, the voltage of the PSPP-Power line was increased, until the voltage on the VDD output of the PSPP chip stabilized. After the supply voltage on the PSPP-Power line exceeded ≈ 18 V, the VDD voltage changed only very little, which indicated that the voltage regulator in the PSPP had started to work. At this voltage, the PSPP chip consumed a current of 10 mA, and the output voltages shown in Table 6.1 were measured for the PSPP chip with index number 1. The Table also shows the simulated output voltages under the same conditions. The measured voltages differ quite a lot from the simulation. The output voltages $\mathrm{VDD}_{1.5}$ and $\mathrm{VDD}_{1.2}$ are generated by the band-gap voltage by multiplying it with fixed factors of 1.413 and 1.128, respectively. These factors also apply for the measured voltages, so there has to be a fault in the simulation or implementation of the band-gab reference. The layout of the PSPP's voltage reference is identical to the voltage reference implemented into the SPP. As the measured output voltage of the SPP chip's band gap reference is very

Output	Measured	Simulated
VDD	2.2706 V	2.248 V
V_{BG}	1.1353 V	1.068 V
$\mathrm{VDD}_{1.5}$	1.6038 V	1.507 V
$\mathrm{VDD}_{1.2}$	1.2790 V	1.204 V
I_{IN}	10 mA	10.5 mA

Table 6.1: *Measured and simulated output voltages of the PSPP (chip #1) voltage regulator. The uncertainties lie within the last digit. Input voltage: 18.0 V.*

close to the PSPP chip's reference (see Section 5.1.2) there seems to be a fault in the simulation.

As the voltage of the $VDD_{1.5}$ line slightly exceeds the maximum voltage of 1.6 V[1] for the core transistors of the 130 nm design process, a workaround is necessary to prevent the PSPP chips from damage. The output of the band-gap reference has an internal series resistor of 50 Ω implemented. Hence, the output voltage of the band-gap reference can be lowered to the desired voltage from the simulation, when a load of 722.5 Ω is added. To test under uniform conditions, a more common resistor of 1 kΩ (5%) has been added as load for the band-gap output on each PSPP carrier board, if not otherwise noted. This relatively high resistance still produces supply voltages in acceptable ranges, as the absolute values of $VDD_{1.5}$ and $VDD_{1.2}$ have only little impact on the PSPP chip's operation. Only for use of the ADC and the comparator blocks, a reference voltage with small individual variation is important.

6.2.1 Quantitative tests

There were four specimen of the PSPP chip, to which a 1 kΩ (5%) resistor has been added to tune the reference voltage. These chips can give a rough estimate of the regulator precision and the individual variation. The upper plot of Figure 6.6 shows the envelope of the measured regulator hysteresis for the supply voltage and the band-gap reference voltage of the tested PSPP chips. The measurement procedure was identical to the regulator measurements with the SPP chip, described in Section 5.1.2. The 1.2 V and 1.5 V voltages are shown in the lower plot of Figure 6.6. As seen in the plot in Figure 6.6, the supply current, at which the regulator starts to work, is with a minimum of almost 8 mA larger than the starting current measured for the SPP chip. There is also a rather large variation in the starting current of almost 1 mA. This behavior is not suited for a system with high reliability requirements such as the Detector Control System (DCS), and requires improvement. Nevertheless the PSPP can still be used for testing purposes, with the constraint that the DCS system is always switched on prior to the serial powering current. In this case, all PSPP chips on a stave have an input current high enough to switch on the regulators.

The regulator stability has also been tested for the four PSPP chips, tuned with the 1 kΩ resistor. Once the regulator has started to work, the band-gap reference output voltage varied by about 1.43 mV (worst case), a value which is 20 times smaller than the variation of the band-gap reference output of the SPP chip. This limits the regulator output precision to a variance of $\approx 0.14\,\%$, with respect to the average value, legitimating the use of an ADC with a resolution of 9 bits.

[1] Stated in the design manual.

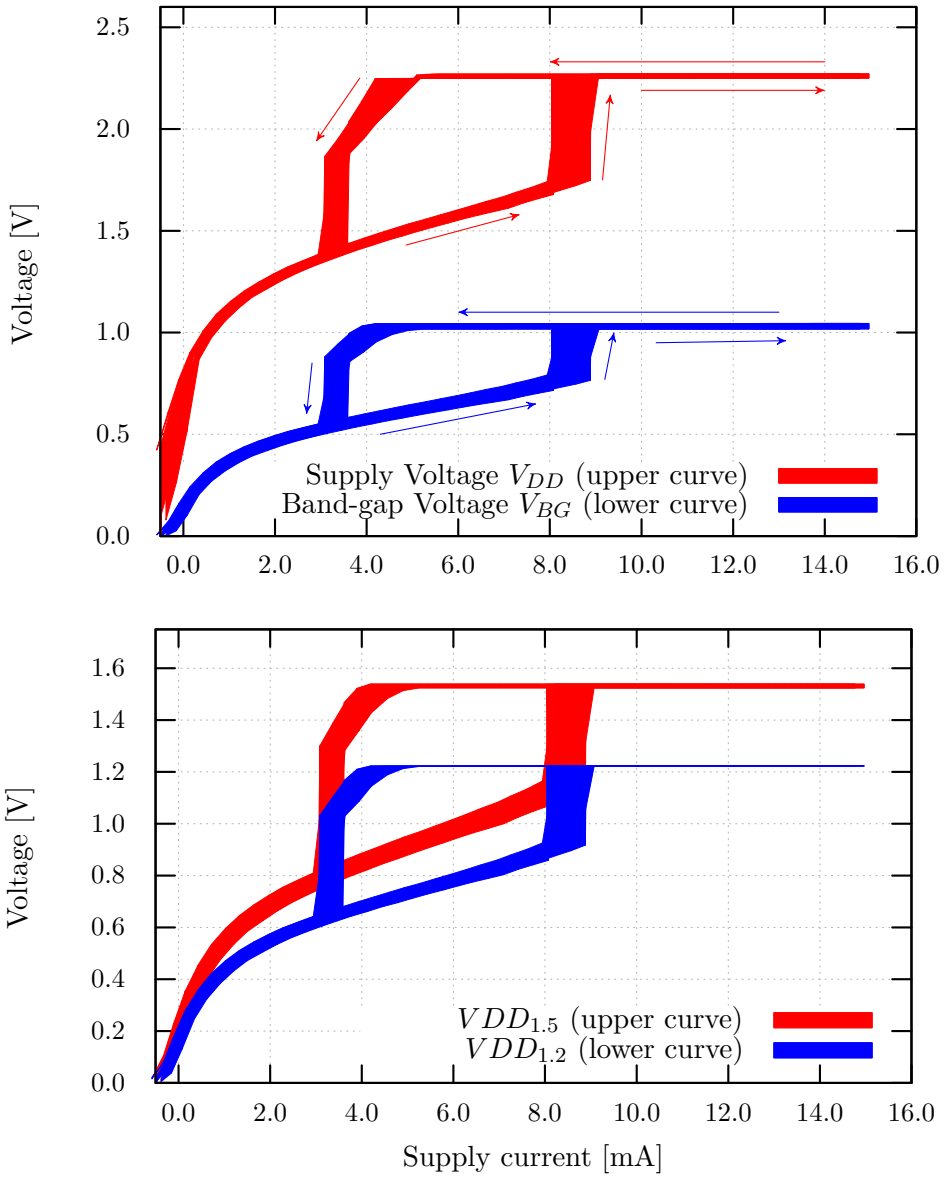


Figure 6.6: *Envelope of the supply voltage and band-gap voltage outputs (top) and the $VDD_{1.5}$ and $VDD_{1.2}$ voltages (bottom) of the measured PSPP chips.*

Further testing conditions
For all further tests, if not otherwise noted, the individual functional blocks of the PSPP chip were exemplarily tested on one chip on a setup similar to the regulator test setup. The tuning resistor, introduced during the regulator tests had a resistance of 1 kΩ (5%). The supply voltage of the tested PSPP chip was thereby always 18 V and the supply current ~10 mA. There was only one Slave-board attached to the Master-board. Measurements including voltage / current sweeps were automated with custom designed Lab-View programs.

6.3 Testing of the Comparator

To test the comparator of the PSPP chip, a voltage was applied directly to the module-voltage input of the PSPP. This voltage was swept from 0 V to 2.5 V, while the comparator output was monitored. Figure 6.7 top shows the measured comparator thresholds, in relation to the reference voltage, V_{Ref}. Each point represents one specimen of the PSPP chip with its individual V_{Ref}. While first five points represent chips with a regulator tuning resistor of 1 kΩ(5%), the rightmost point represents a PSPP chip with no tuning resistor, which explains the high reference voltage.

Inside the chip, the module voltage and the reference voltage are fed into a comparator through voltage dividers. Thereby the reference voltage is scaled by a factor of $\frac{5}{6}$ and the module voltage by a factor of $\frac{5}{11}$. Theoretically, this leads to the linear dependance $V_{Th} = \frac{11}{6} \cdot V_{BGR}$, between the threshold voltage and the reference voltage. This theoretical correlation is also plotted as the dashed blue line in the Figure 6.7 top. The measured threshold voltages do not match the theory very well. This could have various reasons: Besides the possible parts spread, the tuning resistor for the reference voltage could add a non linearity to the comparator. Unfortunately, a statement cannot be given at this point, as the number of measurements is too low. To reliably test the dependance between threshold voltage and reference voltage, more measurements are required.

Due to the voltage divider, which scales the module voltage for the comparator, the threshold voltage of the particular PSPP chip can be increased by adding a resistor into the module voltage sense line. The necessary resistance, R, to set the threshold voltage to the new desired threshold voltage, V_{ThR}, can be calculated using the following equation:

$$R = 18080\,\Omega \cdot \left(\frac{V_{ThR}}{V_{Th}} - 1\right)$$

Figure 6.7 bottom shows measurements of the threshold voltage V_{ThR}, tuned by various resistors R. During the measurements, the reference Voltage, V_{BGR}, was 1.0591 V±0.1 mV and the intrinsic threshold voltage, V_{Th}, was (2.0072±0.0252) V. The calculated values (dashed blue line) show, that the threshold tuning works as expected.

6.4 Testing of the I2C-HC communication

The functionality evaluation of the I2C-HC communication was done with a Master-board connected to a Slave-board, with the address 00_{H}. The concept of the com-

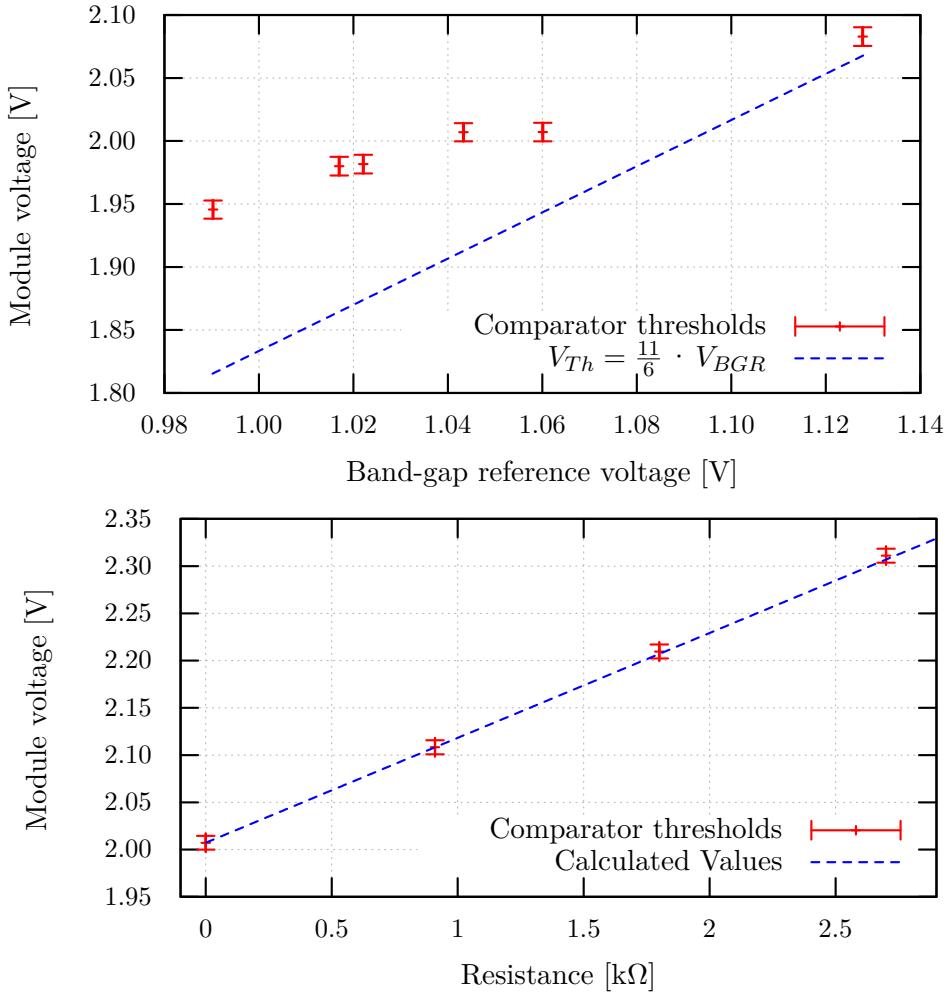


Figure 6.7: *Top: Measurement of the threshold voltage, depending on the reference voltage. Bottom: Measurement of the tuned threshold voltage, depending on the tuning resistor.*

munication with PSPP chips as slaves on the I2C-HC bus foresees, that both lines of the the bus (SDA and SCL) are connected to the corresponding inputs of the slave PSPP chip with 4.7 nF capacitors in series. However, it was not possible to establish a working connection this way due to problems in the SCL input, which could not be fully investigated, yet. To setup a working communication, the physical layer logic of the SCL line in the PSPP chip needs to be bypassed and the decoupled bus line is interfaced directly to the PSPP chip's logic core over the debug pins. To prevent damage to the logic core due to high input voltages, additional protection diodes (BAS40-04-V, Vishay Semiconductors) have been added to the Slave-board. Thereby the SCL input of the PSPP chip is still connected to the SCL line, to sustain the keeper function.

With the modification above, a communication with the I2C-HC-slave logic in the PSPP chip is possible and all registers can be read out and written (if supported). An example read-out sequence of the chip-ID (register address 00_{H} and 01_{H}) of a chip with

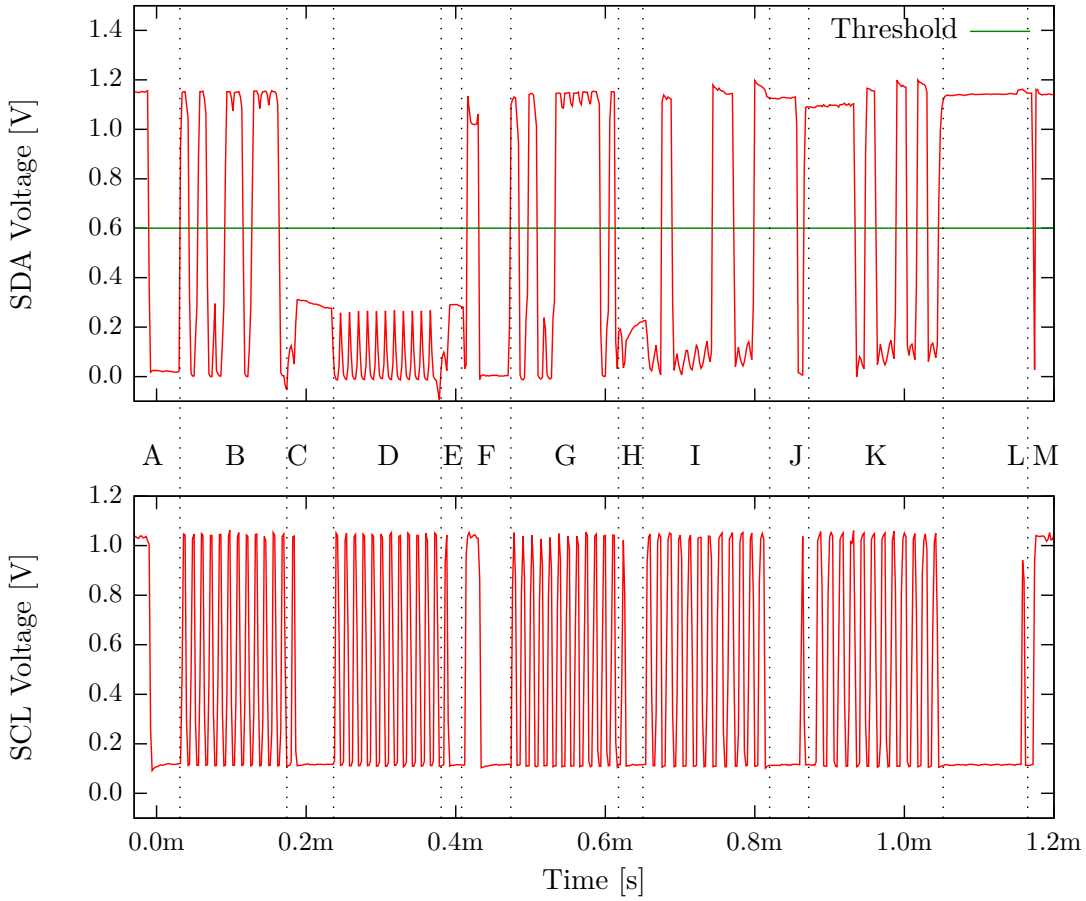


Figure 6.8: *Plot showing an I2C-HC communication sequence. The sequence contains two transmissions: In the first transmission (A - F) the master sets the register address pointer to address 00_H. In the second transmission (F - M), the registers 00_H and 01_H are read from the slave. Table 6.2 gives a detailed listing of all sections.*

Section label	Description
A	Start condition
B	Transmission of the chip address $A0_H$ (writing mode)
C	Slave with address $A0_H$ sends ACK bit
D	Transmission of the register address (00_H)
E	Slave with address$A0_H$ sends ACK bit
F	Stop and start condition (restarting communication)
G	Transmission of the chip address $A1_H$ (reading mode)
H	Slave with address $A0_H$ sends ACK bit
I	Slave sends data stored at register address 00_H (21_H, high byte of the Chip ID)
J	Master sends ACK bit (transmission continues)
K	Slave sends data stored at register address 00_H ($F4_H$, high byte of the Chip ID)
L	Master sends no ACK bit (transmission completed)
M	Stop condition

Table 6.2: *Listing of the time sections in Figure 6.8. Each transmitted byte contains the eight data bits specified above and the corresponding four Hamming code bits.*

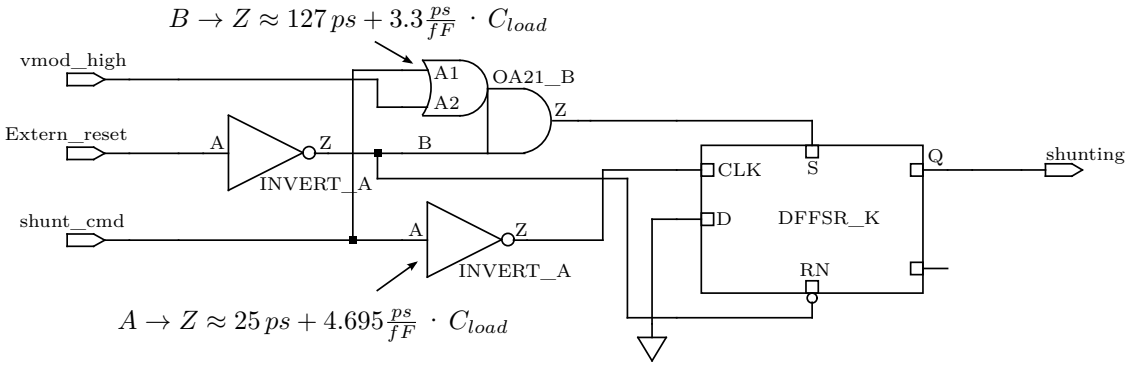


Figure 6.9: *Schematic of the synthesized shunting logic. The numbers show the signal propagation delays, which render it impossible to reset the shunting output with a falling edge of the shunt_cmd input.*

bus address $A0_H$ is shown in Figure 6.8. The time sections are explicated in Table 6.2. Besides the chip ID, the following operations work as expected when written and read:

- Reading of the Chip-ID (low- and high-byte)
- setting and reading of digital outputs,
- reading of digital inputs,
- writing of the ADC multiplexer input and starting the ADC conversion,
- reading of the ADC multiplexer input,
- setting and clearing bit 0 of address 06_H,
- reading bit 0 and bit 1 of address 06_H.

The remaining operations, related to the I2C-HC bus do not work as expected:

- Reading of ADC results (with values in the expected range),
- clearing bit 0 of address 06_H does not disable the shunting.

The unexpected observed behavior of both operations is described in separate subsections. Possible workarounds (if found) will also be given.

6.4.1 Malfunction of the Shunting logic

The function of the shunting logic is described in Section 5.2.2. While enabling the shunting and reading the shunting status bit (bit 1 of address 06_H) works as expected, clearing the shunt command bit (bit 0 of address 06_H) has no effect on the shunting status. Though the shunt command bit can be cleared and read back as '0', the shunting status bit remains set once it was set (by the either comparator or the logic). The only way to clear the shunting status is to reset the chip.

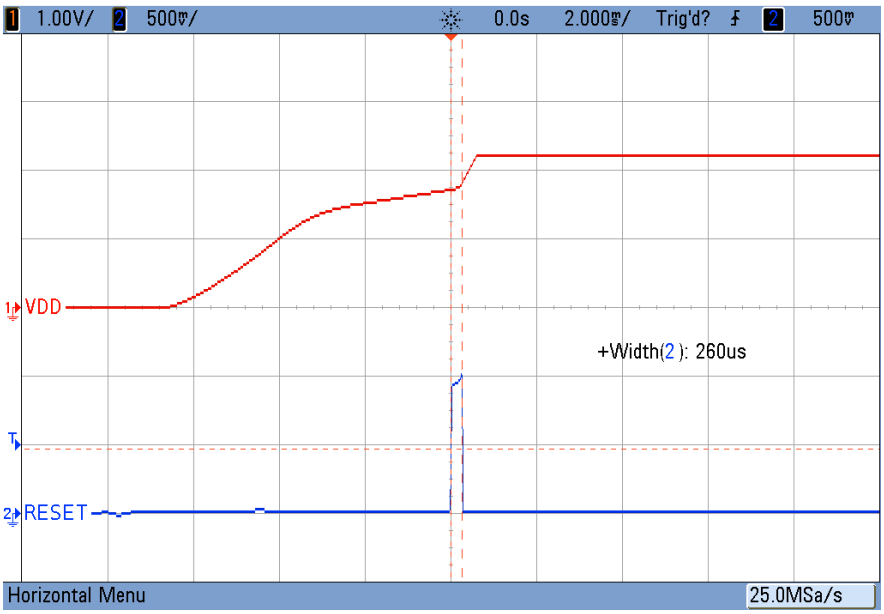


Figure 6.10: *Picture showing the reset pulse generated by the power-on reset block.*

The origin of this malfunction is a timing violation, which can be found in the synthesis of the shunting logic. A schematic of the synthesized shunting logic (extracted from the RTL[2] compiler, see Section work-flow) is shown in Figure 6.9. The estimated signal propagation delays for falling edges of the involved logic cells are also shown. The load capacitance of the flip-flop inputs can be assumed to be equal. Due to the large difference in the propagation delays, the rising edge of the flip-flop's CLK input is received ~100 ps too early and the flip-flop processes the wrong input states on the set- and reset-inputs. Hence, it is not possible to reset the shunting output, with a falling edge of the shunt_cmd input.

To make the PSPP chip usable for serial powering tests, a workaround was found to allow a deactivation of the shunting. In this workaround, a digital output pin of the PSPP is connected to the debug pin of the power-on reset line. If this output pin is set by the user, the logic core will perform an asynchronous reset which clears all internal registers (including the shunting state bit) and deactivates the shunting. For the tests performed in terms of this thesis, the debug pin of the reset signal was connected to bit '0' of the digital output on the Slave-board.

6.5 Testing of the power-on reset

The power-on reset block provides a short logic pulse, when the chip is powered up. Over a 10 kΩ resistor the output of the power-on reset block is routed to a bond pad and the external-reset input of the PSPP chip's logic core. This debug pin can be used to either check the power-on reset functionality or to reset the logic core manually. When the supply voltage of the PSPP chip is switched on, the power-on reset generates a

[2] **R**egister **T**ransfer **L**ogic

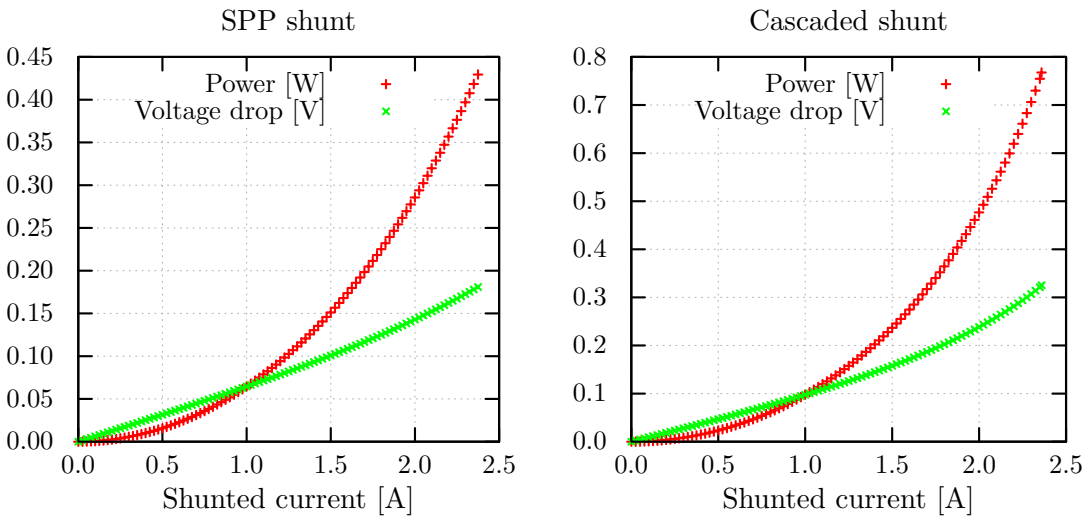


Figure 6.11: *Plot showing the measured voltage drop and power dissipation of the two shunting transistors of the PSPP chip while shunting different currents.*

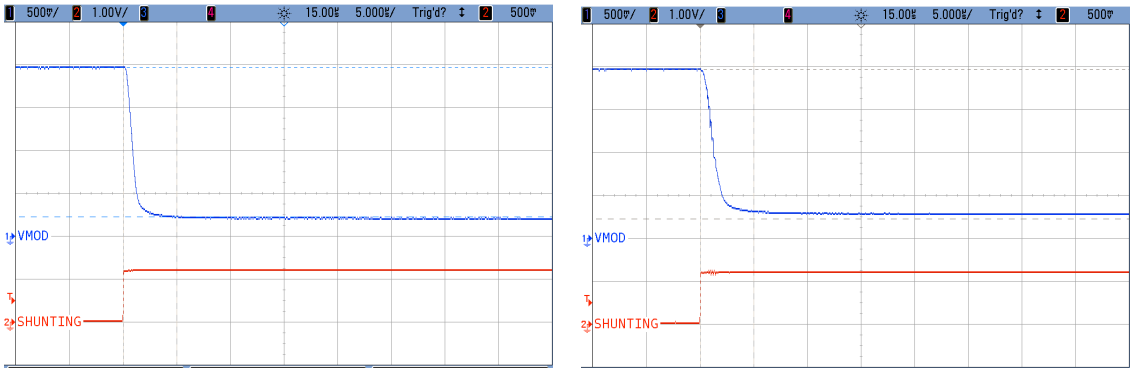
pulse shown in Figure 6.10. For this test, a single Slave-board was connected to a Master-board. The supply voltage of the PSPP chip on the Slave-board was 18 V at 10 mA.

6.6 Testing of the shunt transistors

To test the voltage drop of the shunting transistors, a constant current was applied to one of the shunting transistors, while the shunting was enabled. Figure 6.11 shows the voltage drop and the power dissipation of both shunting transistors depending on the shunted current. Thereby the voltage drop was measured as close to the chip as possible, but not on the chip itself. Hence the measured voltage includes the voltage drop of the bond wires. The maximum heat generation at a shunted current of 2.4 A is 429 mW and 768 mW for the SPP shunt and the cascaded shunt, respectively. The heat sinking capabilities of the carrier board glued to the PSPP chip die seem to be sufficient, for this amount of power dissipation, as none of the chips died during the tests. Currently, the idea is to place the DCS chip onto the stave flex, a thin cable made of Kapton and metal foil[3], to be as close to the modules as possible. It cannot be expected, that a chip with this large power dissipation glued onto a flex could survive, when the cooling fails, especially in an environment where the packing density is as high as in the inner tracker of ATLAS. The voltage drop of the cascaded shunt needs to be lowered significantly to be suitable for use in the pixel detector.

The time, necessary to execute the shunting command, coming from the I2C-HC bus is shown in Figures 6.12 and 6.13 on the following page for enabling and disabling the

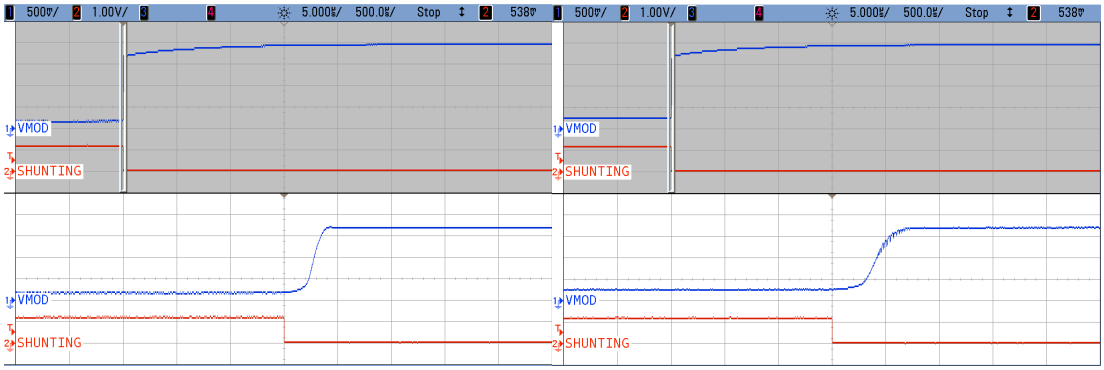
[3] copper or aluminum



(a) SPP shunt, shunting enabled. Execution delay $< 5\,\mu s$.

(b) Cascaded shunt, shunting enabled. Execution delay $< 5\,\mu s$.

Figure 6.12: *Measurements of the time delay, necessary to execute the shunting command. The shunted current measures 2.4 A. Diagram parameters: Time/div = 5 µs, Volt/div = 1 V for the module Voltage (VMOD), and Volt/div = 0.5 V for the shunting status output pin (SHUNTING).*



(a) SPP shunt, shunting disabled. The delay before the module voltage has completely risen is rather long due to power supply issues.

(b) Cascaded shunt, shunting disabled. The delay before the module voltage has completely risen is rather long due to power supply issues.

Figure 6.13: *Measurements of the time delay, necessary to deactivate the shunting. The shunted current measures 2.4 A. Diagram parameters are identical to Figure 6.12.*

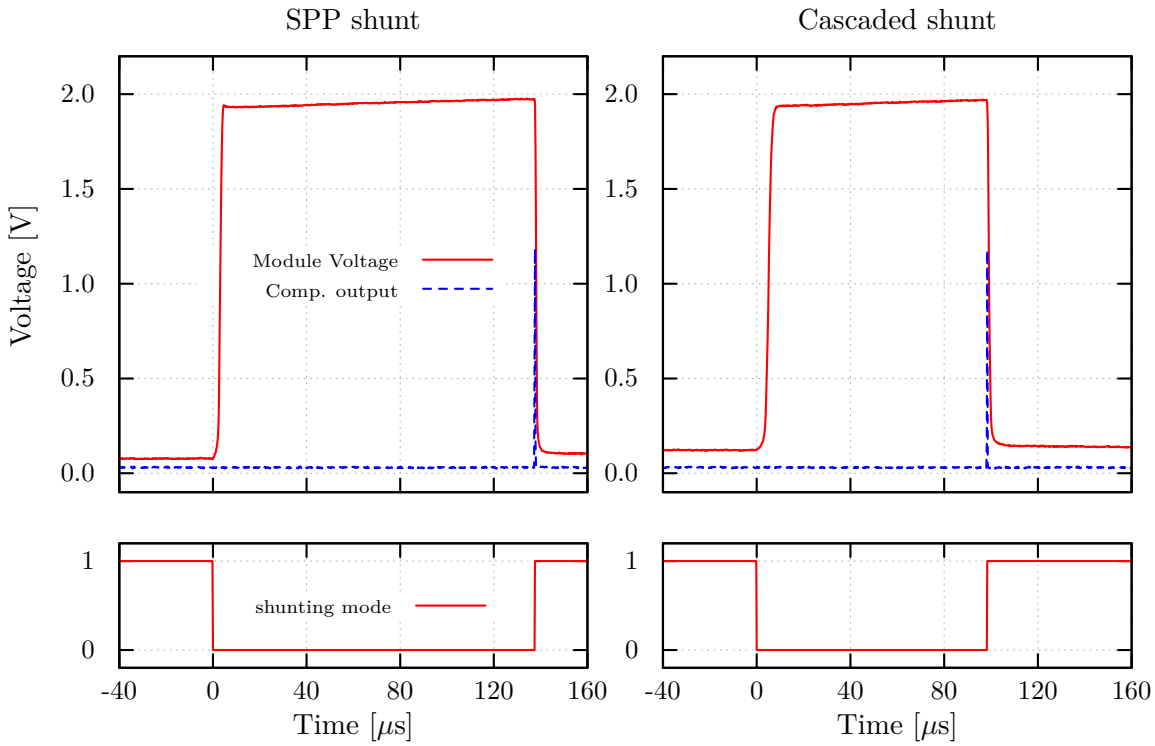


Figure 6.14: *Two snapshots of over voltage induced shunting. The upper diagrams show the module voltage as well as the comparator output. The lower diagrams show the digitized value of the shunting status. At the trigger point (time 0), the shunting is deactivated. When the module voltage reaches the threshold voltage (≈ 2 V), the comparator output triggers the shunting and the module voltage drops again.*

shunting, respectively. Due to the power supply running in current compliance mode, the execution delay is quite long when the shunting is disabled. It can be expected, that the recovery time of the module voltage is shorter, when used with a proper current supply for the serial powering chain.

To test the over voltage induced shunting, a two chip module was simulated on the slave board. The serial powering current was set to 1.36 A instead of 1.2 A (as required for a nominal voltage drop of ≈ 2 V). The number of simulated modules, the serial powering current and the series resistance in the serial powering line (6.7 Ω) have been evaluated and chosen to produce clearly visualized timing diagrams (adapted to the power supply behavior). Figure 6.14 shows two snapshots of over-voltage induced shunting, one for each shunting transistor in the tested PSPP chip. The threshold voltage was tuned to $2.0\,\text{V} \pm 50\,\mu\text{V}$ for this test. The rising of the module voltage is determined by the power supply.

Though the execution delays of the shunting seem to be rather short with less than 5 µs, only tests with real detector modules can proof the applicability of the shunting system in the PSPP chip.

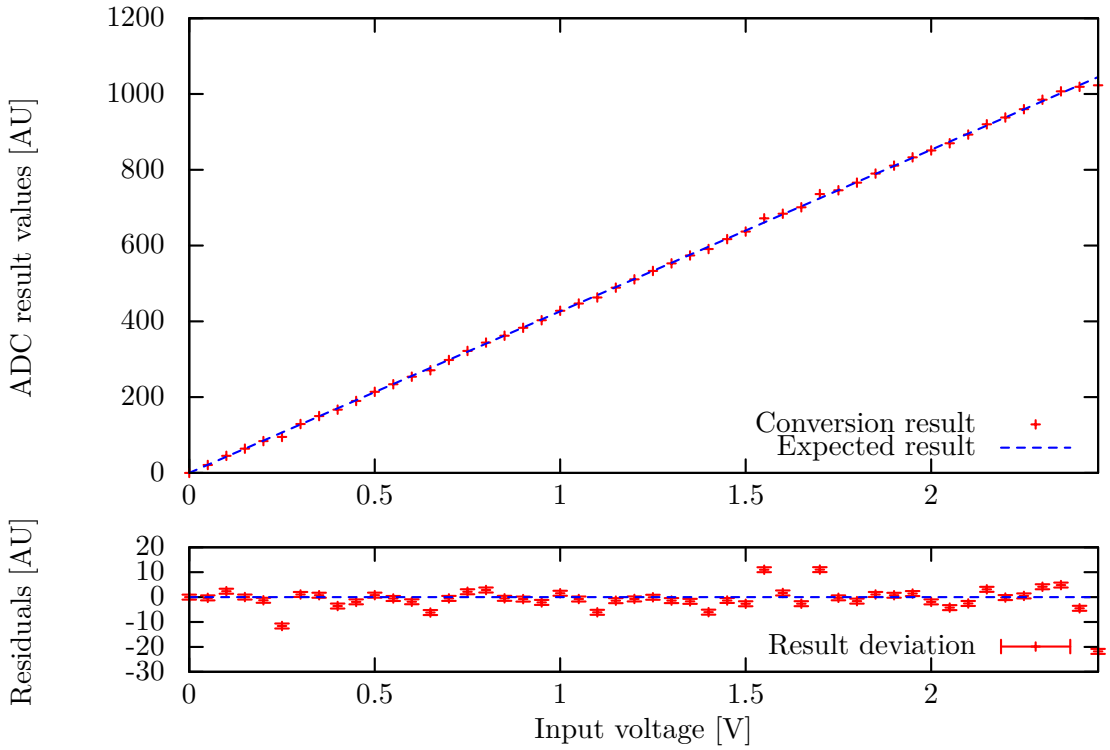


Figure 6.15: *Conversion results of the ADC depending on the input voltage, which was applied to the ADC input and the drain of the SPP shunt.*

6.7 Testing the ADC functionality

Unfortunately, it was not possible to operate the ADC in the PSPP chip as expected. It is possible to set the analog multiplexer value in the registers of the logic core and read back the correct value afterwards. The result registers in the logic core also change their values, after the multiplexer value has been written to the PSPP chip, so it can be assumed that a conversion has been executed. The programmed multiplexer channel number, however does not seem to have any effect, as all channels yield similar conversion results, independent of the voltages on the different ADC inputs. Furthermore, the different ADC input channels have unequal influence on the result values. A change of the ADC input seems to have the strongest influence on the conversion results. The best conversion results have been achieved, with the ADC input and the SPP shunt input of the PSPP chip (Pads 8 and 13 in Figure 5.16 on page 93) being connected and used as analog input. In this configuration, the dynamic range of the ADC lies between 0 V and 2.48 V. This matches the precision of the band-gap reference measured in Section 6.2.1. Figure 6.15 shows the ADC conversion results and the corresponding input voltages produced with the described setup. The deviation of the result from the expected value is also shown. Despite the coarse intervals between the conversions and the noise of the results, this plot shows that the conversion itself seems to work in

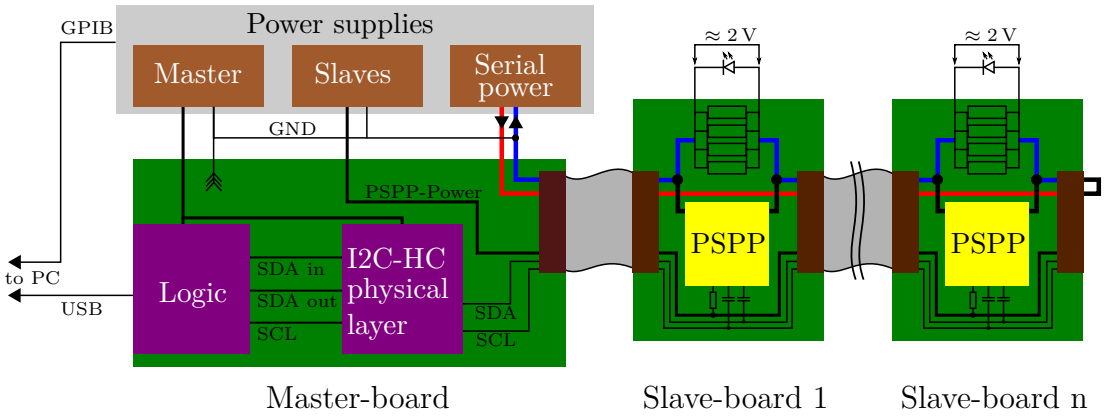


Figure 6.16: *Schematic showing the setup for the multiple-chip-chain tests. The large resistors on the slave board are 3.3 Ω (5 W, 10 %) and simulate the front end chips. The capacitance and LED in parallel to the resistors are used to stabilize the module voltages during shunting and to indicate the shunting status, respectively.*

this special case of operation. Thus the problems with the ADC are most likely caused by the analog multiplexer or the implementation of the ADC IP[4] block into the PSPP chip.

6.8 Testing of a five-chip-chain

The PSPP chip was also tested in a serially powered chain with up to five units. The setup for these tests is shown in Figure 6.16. To indicate the shunting status of a Slave-board, LEDs with a forward voltage of ≈ 2 V are connected to each board.

6.8.1 Issues with a voltage source

In the first test of the chain, an Agilent E3644A supply has been used as the power supply for the serial power as in the previous tests. As being a voltage source in current limitation mode, the E3644A has a large buffering capacitance on its output. This capacitance inhibits a fast change of the voltage drop over the entire chain. Thus, in case of one PSPP chip changing its shunting status, the voltage drop on each other Slave-board in the chain changes by the voltage drop of the changing Slave-board for a brief moment. This swinging module voltage can trigger the over-voltage induced shunting, if it exceeds the threshold voltage. This way, a chain reaction can be started, which switches all PSPP chips on the chain into shunting mode. Figure 6.17 on the following page shows in the upper two plots how the enabled shunting on Slave-board 1 leads to an increased module voltage on the other Slave-boards. Due to the limited number of oscilloscope inputs, only four voltages are shown. To avoid this, resistors can be switched in series to the chain, improving the regulator characteristics of the power supply by increasing its internal resistance. As seen in Figure 6.17 in the lower plots, the module voltage on the Slave-boards 2-4 does not exceed the threshold voltage,

[4] **I**ntellectual **P**roperty

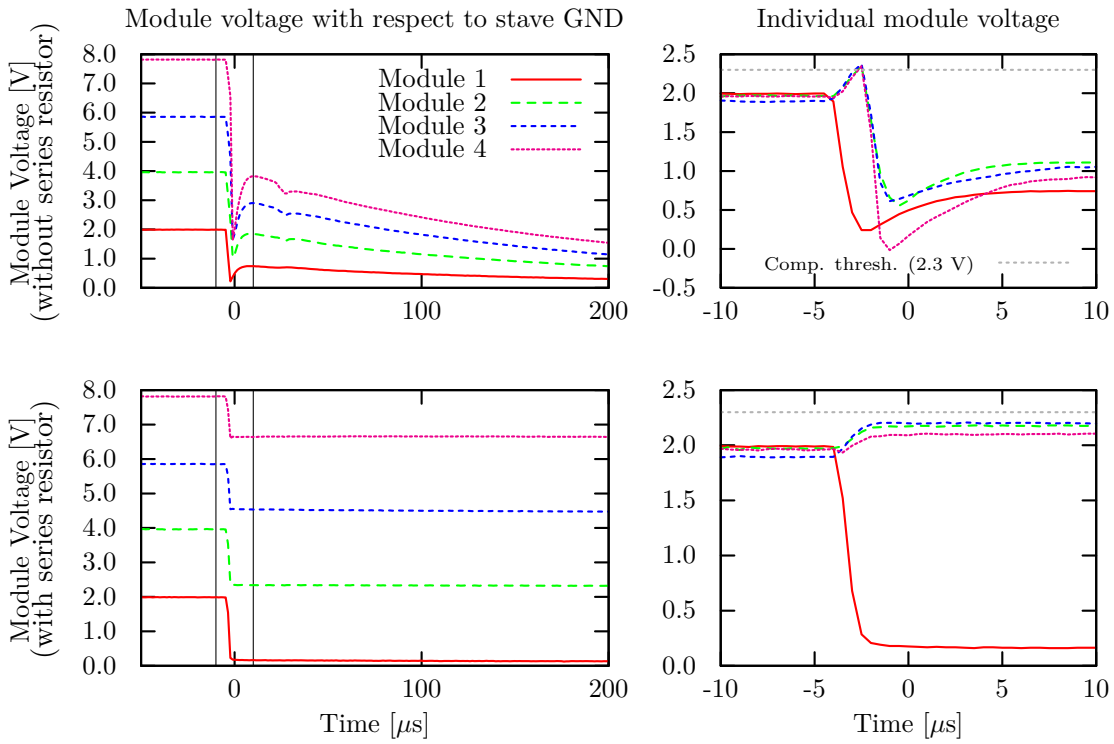


Figure 6.17: *Snapshots showing the the impact of one module to the rest of the stave, when the shunting mode is entered. At the time around 0 µs, the first module on the stave is shunted. The left column shows the supply voltages of the first four modules on the stave with respect to the stave GND, while the right column shows the voltage drops on the individual modules. Without a series resistor (upper plots) the module voltages 2 - 4 exceed the comparator threshold of 2.3 V and thus are switched off.*

when Slave-board 1 enters the shunting mode. The regulator characteristics of the power supply can react more smoothly with a resistor (here 6.7 Ω) in series. During both tests, one resistor was switched into the chain on each Slave-board and the serial powering current was set to 600 mA. The comparator thresholds were set to 2.3 V using 2.7 kΩ tuning resistors.

To test the regulator behavior, a step response in the load was simulated by switching one of the Slave-boards in the serial powering chain into shunting mode and back. Thereby the module voltages on the other Slave-boards were monitored. Figure 6.18 shows the measured voltage developments, measured with the oscilloscope. The current limitation regulator shows its infeasibility in two ways: On one hand, it takes ≈ 15 ms for the module voltages on the switched Slave-boards and those with higher index to reach their final values after the switching. On the other hand, despite the series resistor introduced above, switching induces a module voltage fluctuation of up to ≈ 0.5 V on all Slave-boards in the chain. This rather large possible fluctuation limits the safety margin, between the nominal operating voltage of a module and the

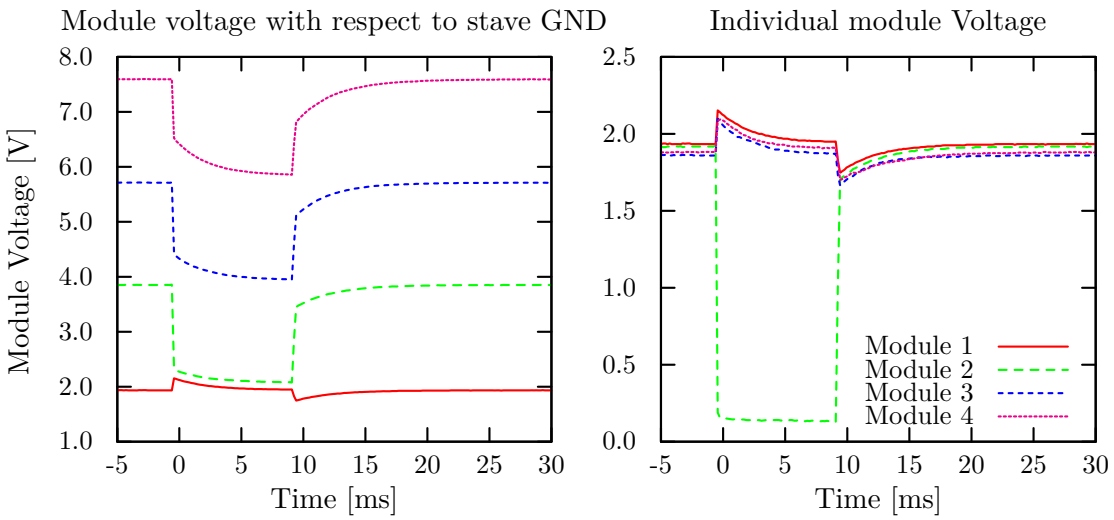


Figure 6.18: *Plot of the step response of the current limited voltage output of the E3644A. The settling time for the module voltages takes ≈ 15 ms and the regulator in the power supply generates a module voltage fluctuation of up to ≈ 0.5 V on all Slave-boards in the chain.*

over-voltage threshold, to a minimum of 0.5 V. As this measurement uses resistors as load on the serial powering chain, every change of the supply current produces a linear change in the supply voltage. This measurement can be interpreted as worst case. It can be assumed though, that the voltage regulators in the front end chips can tolerate fluctuations in the supply current up to a certain level, as their I-V input characteristics flatten to an input resistance of $R_{in} = 1\,\Omega$, after the shunt regulator started to work [47]. This would allow a smaller safety margin and thus a more secure operation of the detector modules.

6.8.2 Supplying with a current source

To ensure, that the problem of voltage spikes is caused by the power supply and not by the serial powering chain itself, the serial powering was also tested with a current source instead of a current limited voltage source. The used current source, shown in Figure 6.19 on the next page, is a self-made power supply provided by the Rutherford Appleton Laboratory. The reliability and remote controllability of this power supply is not as well verified, compared to the industrial designed ones. Hence it has only been used for this particular test, in which the supply current is constant and not close to the maximum allowed shunting current.

Again, the regulator behavior was tested by monitoring a step response in the load. Figure 6.20 on the following page shows a typical oscilloscope measurement of a step response. The current source regulator can handle fast changes on its load much better, compared to the previously tested voltage source. The module voltages reach their final values faster (≈ 290 µs) and the transition induced perturbation of the module voltages is smaller (≈ 0.07 V) as shown in Figure 6.20. Though the Figure also shows

Figure 6.19: *A picture showing a self-made current source, used for comparison measurements with the commonly used voltage sources, operating with current limitation.*

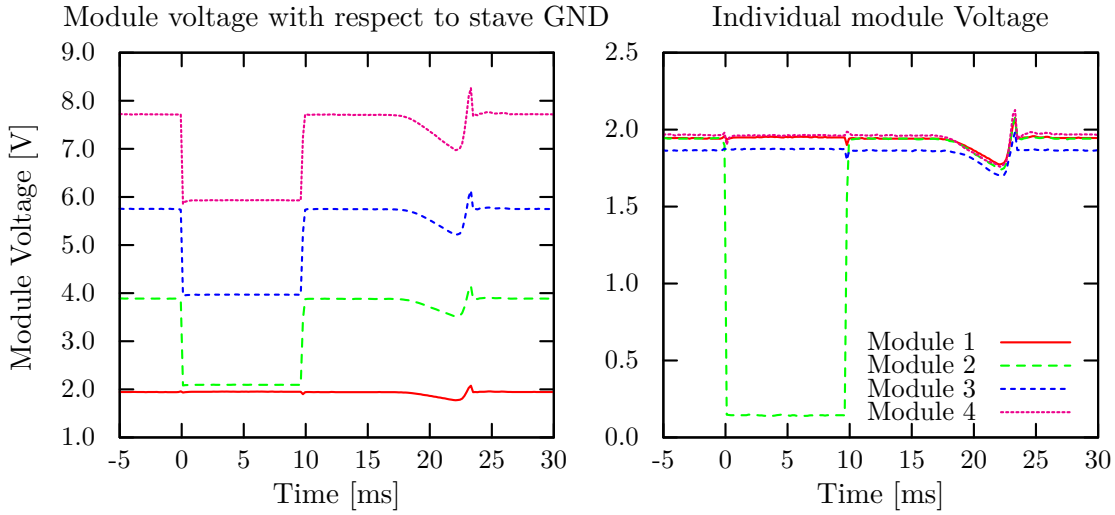


Figure 6.20: *Plot of the step response of the current source. The settling time for the module voltages takes* $\approx 290\,\mu s$ *and the regulator in the power supply generates a module voltage fluctuation of up to* $\approx 0.07\,V$ *on all Slave-boards in the chain.*

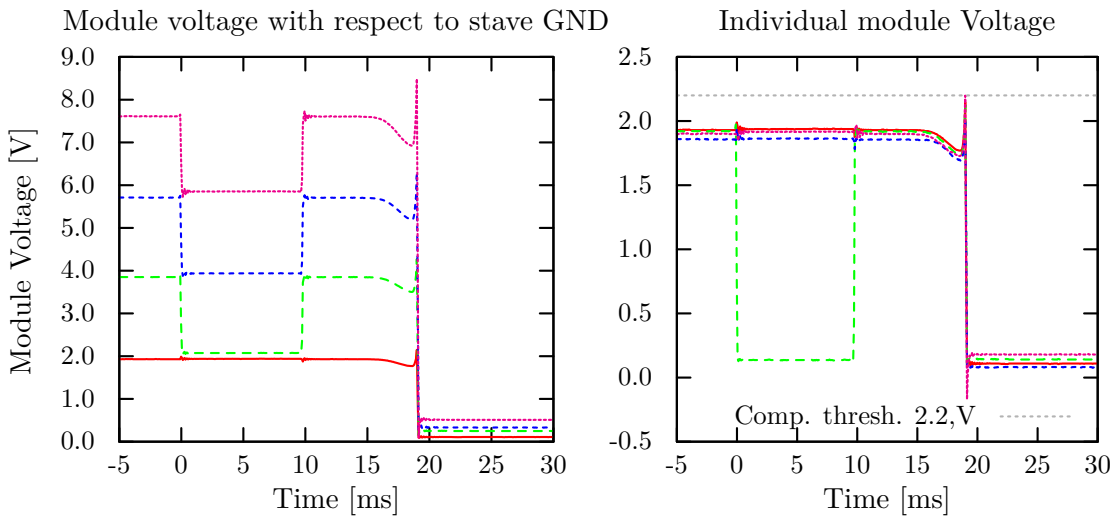


Figure 6.21: *Plot of the step response of the current source inducing an output voltage ripple of the power supply, which reaches the threshold voltage and thus disables the entire chain. The trace assignment is equal to Figure 6.20.*

a fluctuation in the module voltages some time after the switching occurred. Multiple measurements with larger time windows have shown, that this noise is not induced by the switching, as it occurs regularly with a frequency of $\approx 30\,\mathrm{Hz}$ and an amplitude of $\approx 180\,\mathrm{mV}$ on the current supply output. The amplitude of the individual ripples fluctuates and it seems that ripples, occuring shortly after the switching, can be larger. It was possible to operate the chain stably with a supply current of up to 600 mA, if the shunting status of each module does not change. A stable switching, though could only be achieved with a supply current $< 560\,\mathrm{mA}$. A ripple induced over-voltage shunting with a subsequent chain reaction is shown in Figure 6.21. After a time of $\approx 10\,\mathrm{ms}$, a ripple in the module voltage occurs, which reaches the threshold voltage and thus disables the entire chain.

Despite the lack of tests with real detector modules, the measurements show that the choice of an adequate power supply is not a trivial matter. Possible noise or switching induced voltage fluctuations of the output voltage of the power supply have to be taken into account for the definition of the threshold voltage. The threshold voltage itself should thereby be lower then the absolute maximum input voltage of the front end chip's shunt regulator to avoid any damage.

6.9 Results and outlook

After first rudimentary tests with the PSPP chip, most of the implemented functionality has proven its usability. Only the implemented ADC could not be operated satisfactorily. The fault in the design of the PSPP chip, which prevents the ADC from operating

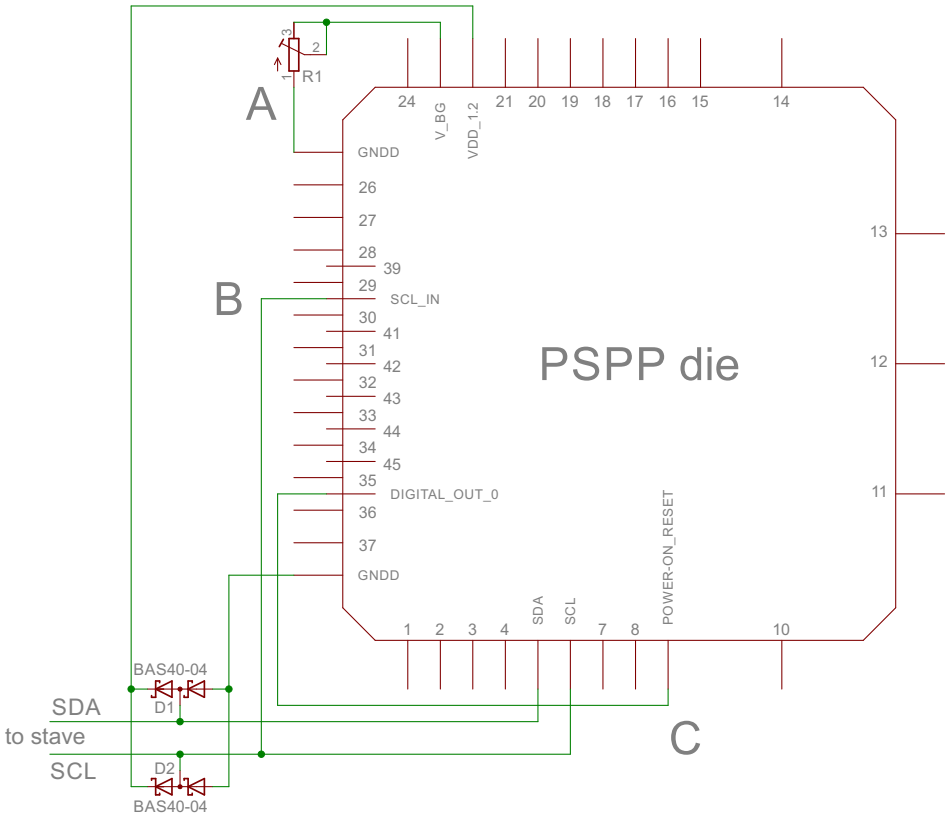


Figure 6.22: *Schematic, showing the workarounds, applied to the PSPP chip for the measurements and tests described above. A: Tuning resistor for the band-gap voltage. B: Bypass of the SCL physical layer. C: Generating a reset signal to deactivate the shunting.*

properly, has yet to be found. For all other design faults, encountered during the testing described above, the following workarounds were found:

- The too high output voltage of the reference voltage can be lowered by adding a load to the output pad of the reference voltage. In general, a value of 1 kΩ provides a sufficient lowering of the reference voltage, so that the 1.5 V supply voltage in the chip does not exceed into dangerous levels anymore. For precise comparator thresholds, a potentiometer of 2 kΩ as load allows a precise tuning of the reference voltage.

- The unstable I2C-HC communication, caused by the physical layer of the SCL input, can be stabilized bypassing the physical layer and feeding the SCL signal directly into the debug pin of the SCL signal in the chip. Thereby the SCL input should still be connected to benefit from the keeper structure in the physical layer.

- The timing violation in the shunting logic can be avoided, using the reset input of the PSPP's logic core. This can be done by feeding one of the digital outputs into the debug pad of the power-on reset. As the digital outputs, as well as the shunting logic is initialized with '0' values, writing a '1' to the digital output will reset the chip and hence the shunting logic.

Figure 6.22 shows a summary of all the workarounds implemented into the Slave-board to provide the highest possible yield of functionality for the performed tests.

With the workarounds applied, the tests of the PSPP chip have shown no evidence to inflict any damage to the supervised object. So the next test should be performed with real detector modules, providing that a proper reliable power supply is used for the serial powering chain.

For a complete evaluation of the PSPP chip, a lot more measurements are necessary. This includes:

- Quantitative evaluation of the regulator outputs including evaluation of
  - temperature dependance
  - specimen variations
  - long term stability
- long term communication tests investigating
  - bit error rate and correction capabilities depending on the number of nodes on the bus
  - tolerance against external noise
  - tolerance against environmental conditions expected for the use in the pixel detector
- measuring the influence of the system onto the quality of physics data taking.

Thereby the evaluation of temperature dependance plays a key role, as the detector control system has to work with both, an enabled and disabled cooling system. These measurements are very time consuming, and therefore could not be done prior to the preparation of this thesis. Irradiation tests have a low priority, as the PSPP, being a proof-of-principle test, is not designed to provide the radiation tolerance required in the detector. Only the cascaded shunt is designed entirely with thin gate oxides and not susceptible to threshold voltage drifts. Though the radiation could increase the leakage current, leading to a reduced current for the detector modules and an increased heat dissipation on the PSPP chip while the shunting is switched off. The design principle of the cascaded shunt could come into consideration to be used in the final chip, though the voltage drop of the transistor would have to be lowered by enlarging it.

In order to design the next prototype for a DCS chip, the deviation between the simulated and the measured band-gap voltage output also needs to be understood.

Conclusion and Outlook

In the years around 2020 the LHC will be upgraded to the HL-LHC. In terms of this upgrade, the ATLAS detector will also be upgraded. This also includes the pixel detector, the innermost of the sub-detectors in ATLAS. Thereby the powering concept of the pixel detector will be changed to reduce the material budget of the detector. From individual powering of each detector module, the concept changes to serial powering, where all modules of a powering group are connected in series. This change makes the development of a new detector control system (DCS) mandatory. Therefore, a new concept for the ATLAS pixel DCS is being developed at the University of Wuppertal. This concept is split into three paths: a safety path, a control path, and a diagnostics path. The safety path is a hard wired interlock system. The concept of this system will not differ significantly, compared to the interlock system of the current detector. The diagnostics path is embedded into the optical data read-out of the detector and will be used for detector tuning with high precision and granularity. The control path supervises the detector and provides a user interface to the hardware components. A concept for this path, including a prototype and proof-of-priciple studies, has been developed in terms of this thesis.

The control path consists of the DCS network, a read-out and controlling topology created by two types of ASICs: the DCS controller and the DCS chip. These ASICs measure and control all values, necessary for a safe detector operation in situ. This reduces the number of required cables and hence the material budget of the system. For the communication between these ASICs, two very fault tolerant bus protocols have been chosen: CAN bus carries data from the DCS computers, outside of the detector, to the DCS controllers at the edge of the pixel detector. For the communication between the DCS controller and the DCS chip, which is located close to each detector module, an enhanced I^2C protocol, the I2C-HC protocol is used.

A first prototype for the DCS chip was designed and tested in terms of this thesis. This prototype, the PSPP (Pixel Serial Powering and Protection) chip, was fabricated in a commercial 130 nm process as a proof-of-principle test. It contains all necessary functionality to supervise an entire serially powered stave. This includes, among others, a shunt regulator to generate the chips supply voltage, shunt transistors to switch off the serially powered modules, a comparator monitoring the supply voltage of each detector module, an I2C-HC-slave logic core, and the physical layers to create an I2C-HC bus with floating nodes. Thereby, the number of lines to supply and control the PSPP chips could be reduced to three per powering group, which keeps the material budget in the detector volume at a minimum.

The PSPP chip was tested and showed three minor and one major faults. Thereby all the minor faults could be resolved in the test setup by workarounds. The major fault affects the implemented ADC and still needs to be understood completely. Hence, reliable ADC conversions are not possible with the PSPP. Fortunately the remaining functions of the PSPP were tested successfully and it was possible to operate and supervise a serial power chain in the lab, similar to a power group in the detector. Furthermore, the tests with a serial chain of PSPP chips have shown, that the right choice of the power supply for a serially powered chain of detector modules is critical. During the tests it was not possible to find a power supply, which could satisfy the demands of a stable current source. Hence further investigation in this matter is necessary.

Besides the design and testing of the first prototype for the DCS chip, the need for hardness-by-design techniques was calculated, which are necessary to ensure that the high amount of radiation in the pixel detector volume does not interfere with the detector operation.

In the near future, long term tests with the PSPP chip are necessary, to evaluate the long term reliability of the implemented I2C-HC bus. Besides that, some analog components of the chip contain transistors with thick gate oxides and need to be replaced in the next prototype generations to meet the radiation hardness requirements of the DCS chip. Further prototypes should also contain layout techniques to enhance the radiation hardness of the chip in the digital blocks, such as triple modular redundancy (TMR) and Enclosed Layout Transistors (ELT). To setup a complete DCS network, a further prototype of the DCS controller, containing the physical layers for the two buses, is also necessary.

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