Terahertz Integrated Circuits in Silicon Technologies

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Declaration

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The thesis work was conducted from 2009 to 2013 under the supervision of Prof. Dr. Pfeiffer at the University of Wuppertal. This work was partially funded by the German Research Foundation (DFG) as part of the research training group GRK 1564 'Imaging New Modalities'.

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Abstract

Terahertz waves correspond to the frequency band of 0.3-3 THz of the electromagnetic spectrum. This region of the spectrum has been considered as a gap since detecting and generating terahertz waves have always been a scientific and a technical challenge. The interesting properties of terahertz waves have been first applied in astronomy and spectroscopy. This has lead the scientific community to develop and invent new technical solutions for this frequency range.

Because of the interesting properties of terahertz waves, applications have emerged in various domains such as medical imaging, security, safety, quality control and communication. However, the available solutions are bulky and difficult to integrate for portable applications.

Recently, different research groups have shown that standard silicon technology is a potential candidate to replace existing systems for terahertz generation and detection, enabling easy integration with on-chip readout and control electronics.

This PhD dissertation focuses on the design and analyses of room temperature terahertz direct detectors in different silicon technologies, their integration in a large camera system with on-chip readout and control electronics. The thesis addresses also the integration of control circuits for silicon based terahertz source arrays as well as imaging demonstrations.

The first step was to investigate single-pixel detectors in standard 65 nm CMOS bulk and 0.25 µm BiCMOS SiGe technologies. The detectors were antenna coupled and integrated in 3×5 pixel arrays. They made use of the non-linearity of standard devices for detecting the captured power by the integrated antennas. Novel detectors were

investigated and led to state-of-the-art performance in terms of operation frequency and sensitivity in comparison with other research on silicon devices.

But, what arouses great interest in standard silicon implementations are the large scale integration possibilities. Therefore, as the second step of this thesis, a 1 k-pixel CMOS based terahertz camera was implemented in a collaborative teamwork during this thesis. It was considered as state-of-the-art device in terms of operation frequency and system integration. Other implementation concepts were investigated and analyzed in this thesis for scalable and adaptable readout circuits.

The implemented detector systems were designed for active illuminations. In fact, their sensitivity can not detect passive radiation from the environment. Therefore, artificial sources were needed. As the third step of this research work, a terahertz control circuit was implemented in a 0.13 µm BiCMOS SiGe technology for a 4×4 source array radiating at around 0.53 THz. Control circuits for terahertz sources are a key feature to reduce power consumption and generate arbitrary patterns essential for terahertz active imaging.

As a final part of the thesis, terahertz imaging were demonstrated to show the capability of the implemented detectors, camera and sources. Scanned objects were shown at terahertz frequencies. Real-time terahertz imaging were demonstrated with the 1 k-pixel CMOS camera module as well as the evaluation of a monitoring application for a laboratory terahertz source.

Contributions

This thesis aims to investigate circuit design and characterization of silicon based terahertz detectors and sources. Parts of the circuit designs, implementations and the measurements have been done in a team work and are detailed below.

Chapter 1 Introduction
I have briefly introduced terahertz history from the 19^{th} century to nowadays potential applications involving the need of terahertz silicon devices. I have reviewed the the state-of-the-art of terahertz sources and detectors, with a focus on standard silicon based solutions that have been published in the scientific community.

Chapter 2 Theory of Terahertz Sources and Detectors in Silicon Technologies
I have presented sources and detectors theory based on literature of the investigated devices during this research work. I have also shown the figure of merit necessary to quantify the performance of terahertz devices that will be used in the next chapters.

Chapter 3 Terahertz Detectors Circuit Design and Characterization
The first part of the thesis was to investigate single-output terahertz detectors in different technologies. Small 3×5 evaluation arrays have been implemented.

In a 0.25 µm BiCMOS SiGe technology, HBT, SBD based detector have been designed. The antennas have been designed by Dr. Janusz

Grzyb and the layout have been implemented by Prof. Ullrich R. Pfeiffer. I have simulated the circuits and fully characterized them including antenna pattern in an anechoic chamber.

In a 65-nm CMOS bulk technology, CMOS based detectors have been implemented in a team work effort with Hani Sherry. I have designed the detector pixel test site and layout with Hani Sherry. I have redesigned a folded dipole antenna with Hani Sherry. The measurements were done in a team work with Hani Sherry, Neda Baktach and myself.

Chapter 4 Terahertz Camera Design and Implementation
My contributions for the camera design implemented in 65 nm CMOS bulk have been the active load circuit design, layout and the output buffer circuit. I have measured the CMOS bulk camera with Prof. Dr. Ullrich R. Pfeiffer in video and lock-in mode as well as antenna patterns.

In a 0.13-µm BiCMOS SiGe technology, I have designed one HBT, and two CMOS cameras. I have designed the readout circuit, implemented the layout and simulated the camera system. Dr. Janusz Grzyb has designed the antennas. The cameras are not measured at the submission time.

Chapter 5 Terahertz Source Array Control Circuit
I did the circuit design of the digital control and the layout implementation of a single pixel control circuit, Dr. Yan Zhao the oscillator array implementation and core oscillator design and Dr. Janusz Grzyb the redesign of the antenna used in other circuits. I have characterized the source array implementation.

Chapter 6 Terahertz Imaging Demonstrations
Raster scanning terahertz imaging with CMOS based single output detectors has been done in a team work with Hani Sherry and Neda

Baktash. I have done the terahertz images for the 0.25 µm HBT single output detectors.

I have programmed and realize the real-time video setup for the terahertz camera in transmission mode imaging setup with Prof. Dr. Ullrich R. Pfeiffer.

I have evaluated the real-time monitoring application setup with Dr. Jean-François Lampin at the University of Lille.

List of Publications

Two journal articles:

- R. Al Hadi, J. Grzyb, B. Heinemann, and U. Pfeiffer, "A terahertz detector array in a SiGe HBT technology," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2002–2010, Sep. 2013.
- R. Al Hadi, H. Sherry, J. Grzyb, Y. Zhao, W. Förster, H. Keller, A. Cathelin, A. Kaiser, and U. Pfeiffer, "A 1 k-pixel video camera for 0.7–1.1 terahertz imaging applications in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2999–3012, Dec. 2012.

Twelve conference publications:

- R. Al Hadi, J. Lampin, and U. Pfeiffer, "A real-time terahertz beam monitoring application with a 1024-pixel CMOS terahertz camera module," in *OSA, Conf. on Lasers and Electro-Optics* , Jun. 2014.
- J. Grzyb, R. Al Hadi, Y. Zhao, and U. Pfeiffer, "Design of differential driven on-chip antennas with harmonic filtering for silicon integrated mm-Wave and THz n-push oscillators," in *European Conf. on Antennas and Propagation*, Apr. 2014.
- U. Pfeiffer, Y. Zhao, J. Grzyb, R. Al Hadi, N Sarmah, W. Förster, H. Rücker, and B. Heinemann, "A 0.53THz Reconfigurable Source Array with up to 1mW Radiated Power for Terahertz Imaging Applications in 0.13μm SiGe BiCMOS," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 2014, pp. 256257.

- K. Statnikov, R. Al Hadi, M. Clemens, V. Hansen, O. Spathmann, J. Streckert, M. Zang, and U. Pfeiffer, "Methods for determining the exposure to THz radiation utilizing CMOS-based detectors," in *Int. Conf. on Infrared, Millimeter, and Terahertz Waves*, Sep. 2013, pp. 1–2.
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- J. Grzyb, H. Sherry, Y. Zhao, R. Al Hadi, A. Kaiser, A. Cathelin, and U. Pfeiffer, "Real-time video rate imaging with a 1k-pixel THz CMOS focal-plane array," in *SPIE Defense, Security, and Sensing Sym.*, Apr. 2012, pp. 1–4.
- R. Al Hadi, H. Sherry, J. Grzyb, N. Baktash, Y. Zhao, E. Öjefors, A. Kaiser, A. Cathelin, and U. Pfeiffer, "A broadband 0.6 to 1 THz CMOS imaging detector with an integrated lens," in *Microwave Symposium Digest (MTT)*, Jun. 2011, pp. 1–4.
- H. Sherry, R. Al Hadi, J. Grzyb, E. Öjefors, A. Cathelin, A. Kaiser, and U. Pfeiffer, "Lens-integrated THz imaging arrays in 65nm CMOS technologies," in *Radio Freq. Integr. Circuits Symp.*, Jun. 2011, pp. 365–368.

- E. Öjefors, N. Baktash, Y. Zhao, R. Al Hadi, H. Sherry, and U. Pfeiffer, "Terahertz imaging detectors in a 65-nm CMOS SOI technology," in *European Solid-State Circuits Conf.*, Sep. 2010, pp. 486–489.

Keywords

Terahertz, THz, sub-millimeter wave detectors, sub-millimeter wave imaging, silicon, CMOS, BiCMOS, SiGe, HBT, MOS, FET, SBD, substrate-contact, nonlinear device, terahertz direct detection, resistive mixer, square-law power detectors, distributed resistive self-mixing, quasi-static analysis, non-quasi-static analysis, responsivity, voltage responsivity R_V, current responsivity R_I, noise equivalent power, NEP, total responsivity, total noise equivalent power, silicon lens, terahertz source, terahertz source array, terahertz camera, terahertz imaging, raster scanning, real-time terahertz imaging, terahertz application, tomography, computed tomography, terahertz tomography.

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This work was partially funded by the German Research Foundation (DFG) as part of the research training group GRK 1564 'Imaging New Modalities'.

To my family

Contents

Chapter 1

Introduction

Terahertz waves correspond to the frequency band of 0.3-3 THz of the electromagnetic spectrum. This region of the spectrum has been considered as a gap since detecting and generating terahertz have always been a scientific and a technical challenge.

Scientists started looking into the terahertz region towards the end of the 19^{th} century. Their motivations were mainly exploratory and consisted of bringing together the optical and the electrical waves to observe the continuity of the electromagnetic spectrum. For that, two experimental approaches were possible, either down-converting optical sources or multiplying electronic frequencies. The scientists observed what Rubens called the "heat rays of great wave length" from an optical approach in 1897 [1], or in other words what Nichols named the "short electric waves" from an electronic perspective in 1923 [2].

These scientific achievements have continuously improved during the 20^{th} century [3], but what aroused the keen interest in terahertz waves were the applications, starting with the modern astronomy [4] and later developing in medical imaging [5], security [6, 7, 8], safety [9], communication [10], biological [11] and pharmaceutical industries [12].

In this chapter, an overview of terahertz applications is given with a brief review of existing terahertz solutions in section 1.1. The state-of-the-art of terahertz sources and detectors based on silicon technologies is presented as well as available readout and control circuits for terahertz sources and detectors in sections 1.2, 1.3 and 1.4. The scientific contribution of this research work to

the terahertz field is described in section 1.5. The organization of the thesis is presented in section 1.6.

1.1 Terahertz technology and its applications

Terahertz gained interest with the 20^{th} century astronomy. It found direct applications in astrophysics to understand stars formation. In fact, observing space at terahertz frequencies provided crucial details on the physical and chemical properties of the interstellar medium [13]. Terahertz served to observe the space gas clouds, galaxies and planets including our own atmosphere [14]. For that, heterodyne spectroscopy was used to determine the spectral signatures of gas clouds as well as nearby galaxies and reveal star formation activities. This has been extended to study the Earth atmosphere and validate ozone depletion models for instance [15], caused by global warming.

The scientific community have developed various technical solutions to generate and detect terahertz waves. These systems can be categorized in three domains which are thermal, optical and electronic based systems [16].

- Thermal terahertz systems:

Blackbody radiator is a thermal based terahertz broadband source with radiated power in the range of the nanowatts. It can radiate up to the infrared region which can be problematic in a characterization setup for instance. Therefore, terahertz filters are required for this type of sources [17]. Bolometers, pyroelectric devices and Golay cell are thermal based detectors [18, 19]. They convert the incoming terahertz radiation into a thermal energy. A thermally dependent electric device is usually used to sense the temperature variation of the absorbing material. These devices can be very wide-band and very sensitive. However they have large time-constants due to thermal dissipation. As a consequence, they are often cooled at cryogenic temperatures under very low pressure.

- Optical terahertz systems:

There is a large choice of terahertz sources based on optical systems and they can be divided in two categories: continues-wave (CW) and pulsed sources. In the

CW category, CO_2 optically pumped gas lasers are one of the high power sources available for laboratory experiments [20]. Based on the rotational frequency of a low pressure gas excited with a high power laser source, they can deliver a power of several hundreds of milliwatts. As a consequence, the terahertz frequencies are discrete lines and can be selected by changing the low pressure gas. However, within the same gas such as ethanol, several frequency lines can be found over several hundreds of GHz. Thermal detectors are usually used with such sources to control the beam shape and the excitation modes.

The Photo-mixer is another CW source with an output power of about few nanowatts at terahertz frequencies [21]. It is based on the mixing product of two lasers running at different frequencies. As a result, the intermediate frequency of the mixing product is continuously tunable which is very useful in spectroscopy application. The photo-mixers can also be used as detectors by making use of the same mixing principle.

The quantum cascade laser (QCL) is an optical based terahertz source and can be CW or pulsed [22]. In a QCL, electrons are injected into a periodic structure of a biased super-lattice [23]. The injected electrons undergo inter-sub-band transitions in a cascade process resulting in an emission of a photon at terahertz frequencies. QCL sources are capable of delivering power in the order of few milliwatts, but they require cooling at cryogenic temperatures.

Another pulsed sources are the time-domain systems (TDS). They are based on very shortly pulsed lasers in the order of few picoseconds [24]. With this technique, a wide-band terahertz pulse can be generated in a very short time. Photo-conductive sampling and electro-optical sampling detectors are usually used for such system.

- Electronic terahertz system:

For electronic sources, Backward Wave Oscillators (BWO) and Gyrotrons are high power terahertz sources [23]. They are capable of delivering terahertz power in the order of the Watt. However, they require a strong magnetic field to operate. Nowadays, electronic multiplied sources based on Gunn or Tunnel diodes are dominating the terahertz market. They are relatively compact in comparison to the previous technologies and are capable of delivering few hundred of microwatts

in the terahertz region. They make use of the high cut-off frequency of engineered diode in III-V compounds [25], and are built out of discrete components like multipliers and power amplifiers. In the same technology, harmonic mixers based on Gunn and Tunnel diodes constitute the major part of electronic detectors. They usually operate at room temperature but require wave guide technology and can not be integrated, for example, in large arrays.

- Terahertz applications:

The presented systems have found their use in civil applications because of the interesting properties of terahertz waves. In a similar direction such as in astronomy, material analysis make use of the interaction of mater with terahertz waves. In fact, organic molecules exhibit strong absorption in the terahertz range resulting in a unique signature of various material. This has been used in biological [11] and pharmaceutical industries [12] to analyze complex molecules in the terahertz range. Mainly time-domaine spectroscopy (TDS) is used for that in production chain for example.

Besides material analysis, imaging is one of the promising applications for the terahertz domain. It can be applied in various fields such as quality control, security screening [6], and body scanners where the non-ionizing properties of terahertz are safer in comparison to X-rays [7, 26]. Furthermore, terahertz imaging may be applied for medical purposes such as skin cancer detection where terahertz radiation is absorbed differently in healthy or cancerous cells [27].

Another emerging application of terahertz is communication [28]. The communication speed rates can greatly benefit from high frequency carrier. In the terahertz range high speed rate can be achieved with simple modulation techniques [10]. However, atmospheric attenuation is a limiting factor for long distance wireless communication. Therefore, short distance communication links for consumer electronics can be imagined for large volume data transfer.

In order to build compact and hand-held material analyzers, imaging and communication systems, the previously presented technologies are not feasible for high integration and large volumes. The major limiting factors of the existing terahertz systems are their size and maintenance costs. In fact, they often require to be operated at cryogenic temperature or under vacuum which limits

their integration capability and commercial application. With the ongoing research achievements on terahertz, standard silicon technologies are becoming the alternative to existing devices. Standard silicon technologies have the advantage to be commercially available with reasonable investment for large production volume.

1.2 Terahertz sources in silicon technologies

As it has been highlighted in the previous section, silicon based terahertz sources and detectors are real alternative to existing systems. Terahertz sources based on silicon technologies have been investigated by different research groups. With the constant advancement of the standard silicon technology, new technical solutions have emerged.

Electronic terahertz sources are commonly divided into two main categories: multiplier-chains and oscillators. In a multiplier chain circuit, power amplifiers (PA) are one of the key building-blocks to provide necessary on-chip RF power. They are usually designed in the mm-wave region were transistors have gain. Multiplier circuits such as doublers and triplers are then applied to reach the desired frequency. A 260 GHz power amplifier in standard CMOS technology could provide around 10 dB gain [29]. In the terahertz region, a $\times 18$ multiplier chain circuit can provide an output power of about -3 dBm at 0.32 THz [30]. A 0.82 THz transmitter with few microwatts of output power have been implemented in a SiGe BiCMOS process technology [31]. The main disadvantage of these solution are the DC power consumption in the order of few watts, and the large space taken by the layout area on silicon.

Unlike multiplier chains, oscillator circuits are very compact and can generate power in the order of milliwatts in the mm-wave region [32]. The maximum oscillation frequency is limited by the transistor maximum unity power gain frequency f_{max}. To overcome the technology limits and generate terahertz frequencies, harmonic oscillators are built. Triple-push oscillators have been implemented in a 65-nm CMOS technology, with oscillation frequencies around 0.3 THz [33, 34, 35, 36] and a maximum output power above 0 dBm [32]. A push-push oscillator has been designed in a 45-nm CMOS technology and delivered an oscillation frequency of

0.41 THz [37]. Going to an advanced technology such as 32 nm CMOS or engineered SiGe HBT would benefit from a higher f_T/f_{max} to increase the oscillation frequency [38, 39]. Fundamental oscillators are possible and an example has been published, but with limited output power [40] at 0.3 THz.

These oscillators are single cells and have a limited available power at terahertz frequencies. In order to increase the radiated power, power combining techniques are used to design oscillator arrays [41]. The power consumption of large oscillator arrays would increase by the number of on-chip elements. Therefore, control circuit are needed to overcome this problem and build compact and strong terahertz power sources in standard technologies.

1.3 Terahertz detectors in silicon technologies

Electronic detection methods in the terahertz range are commonly divided into two main categories: coherent (heterodyne) detection and incoherent (direct) detection methods. Recently, sub-harmonic heterodyne room temperature detectors have been demonstrated in standard SiGe BiCMOS technology [31, 42]. The detector circuits were driven by a local-oscillator (LO). The LO circuit consisted of multiplier chain built with power-amplifiers (PA) and multiplier circuits capable of up-converting an RF source in the range of 10 GHz to higher frequencies. The high-harmonics are then used to mix the incoming terahertz waves to an intermediate frequency (IF). Like electronic mixers, the heterodyne detectors are characterized by their noise figure (NF) and conversion gain (CG).

Although they operate well beyond the technology f_T/f_{max}, these detectors have shown good performance in comparison with other detectors (around 45 dB NF and 20 dB CG), enabling easy integration with on-chip readout electronics. However, LO driven detectors are DC power hungry solutions (around 0.4 W/pixel) [42]. As a consequence, the number of pixels is substantially limited. Therefore, direct power detectors without LO are preferable because of their lower power consumption and their ability to be integrated in large arrays.

Below the technology f_T/f_{max}, the performance of direct power detectors is boosted by low-noise amplifiers (LNA). Power detectors with LNAs have been demonstrated in CMOS technologies up to W-band (110 GHz) for passive ra-

diometers [43, 44]. Such detectors are characterized by their noise equivalent power (NEP) which is defined as the incident signal power required to obtain a signal equal to the noise in a 1-Hz bandwidth [45].

These detectors have achieved $NEPs$ as low as 36 fW/$\sqrt{Hz}$ with about 110 mW DC power consumption [43]. For the same application, heterojunction bipolar transistor (HBT) square-law power detectors with LNAs have been used up to D-band (170 GHz) [46, 47, 48, 49]. They have shown $NEPs$ as low as 14 fW/$\sqrt{Hz}$ and a DC power consumption of about approximately 90 mW [49].

Beyond the technology f_T/f_{max}, it is not possible to design LNAs. As a consequence, antenna coupled direct detectors are implemented. A very common solution is to use the non-linearity of a diode detector to directly down-convert the terahertz signal to DC. For this reason, silicon-based Schottky diodes have been applied with cut-off frequencies up to terahertz in CMOS [50] and SiGe [51] process technologies. Other type of detector based on bolometer has been implemented in a microelectromechanical systems (MEMS) silicon process technology [52]. The detector consisted of an antenna-coupled bolometer, where the terahertz radiation captured by the antenna was converted into heat in matched termination resistors on a thermally insulated platform. This can be achieved by a MEMS post processing step where all silicon is removed by etching.

Devices without additional process options are, however, preferred because of their lower fabrication cost. Low DC power consumption and room temperature terahertz power detectors in standard CMOS technologies have been recently demonstrated for active imaging [53, 54], with minimum noise equivalent power (NEP) down to 55 pW/$\sqrt{Hz}$ [55] at 0.65 THz. A detector based on an HBT device, which have been recently implemented in BiCMOS SiGe technology, have shown NEP of about 34 pW/$\sqrt{Hz}$ [56] at 0.32 THz. These detectors are very interesting because of their low power consumption, as low as few μW/pixel, which makes them especially suitable for large terahertz imaging arrays.

1.4 Readout and control circuitry

Terahertz source and detector arrays in silicon technology benefit from the available devices to build integrated analog readout and digital circuit which is not

possible in discrete waveguide based technologies. These circuits are necessary for integrating large array systems. Their purpose is to amplify analog outputs in the detector array case, to cut-down the power consumption by switching-off certain elements and reduce the pad count to simplify the packaging and eliminate additional off-chip readout electronics.

One of the first integrated pixel in CMOS technology included an in-pixel analog amplifier to drive capacitive load with 43-dB open-loop gain [53, 57]. An implementation with an integrator circuit of a 4×4 terahertz array have been shown in the literature [54]. The circuit included a digitally controlled readout scheme to serialize the signal of the array. Another implementation of such array with Schottky detectors has shown the integration of analog multiplexers and row buffers [50, 58]. A recent implementation of HBT based detectors in BiCMOS SiGe technology has shown good performance in power consumption over the array [56].

On the source side, a major effort is underway in the scientific community to implement high-power sources. A 4×4 source array with 820 mW of DC power consumption delivering 10 dBm isotropic radiated power (EIRP) at 0.3 GHz has been implemented [41]. The array was based on power combining with beam steering capabilities and injection-locked oscillators techniques. A digital circuit controlled the phase of the injection-lock frequency triplers to enable beam-forming and beam-steering. This has shown the great potential and the need to implement large arrays for active imaging application.

1.5 Scientific contribution to the terahertz field

Research on terahertz is a multidisciplinary field where various technical and scientific solution are still to be discovered and invented. It is a great opportunity to do this research work in a very dynamic community. The thesis focuses on silicon based solution for detecting and generating terahertz waves. The scientific contributions of the thesis are on detectors, cameras and sources implementation, as well as imaging demonstrations.

On the detection side, the first step of the thesis was to investigate various devices across two technologies:

- HBT in 250 nm BiCMOS SiGe technology [59],
- NMOS in 65 nm CMOS Bulk technology [60],
- SBD in 250 nm BiCMOS SiGe technology.

At the time of results publication, the HBT and CMOS circuits represented the state-of-the-art in terms of frequency of operation and performance. The SBD was an experimental implementation and therefore has not been published yet.

As a second step on the detector research, a camera system implementation has been investigated:

- world's first CMOS based 1 k-pixel terahertz camera in 65 nm CMOS Bulk technology [61, 62],

The 1 k-pixel CMOS terahertz camera is the fruit of a collaborative work with Hani Sherry, Dr. Janusz Gryb, Dr. Yan Zhao, Wolfgang Förster, Prof. Dr. Ullrich Pfeiffer and myself. I have contributed to the buffer and analog switches of the readout chain, the full characterization of the camera including the antenna patterns. It represented the state-of-the-art of terahertz detector implementation in terms of pixel-count, frequency of operation and system integration. A novel characterization method for large terahertz cameras operating in video mode has been introduced.

On the source side, a control circuit for a scalable terahertz source has been implemented:

- 4×4 terahertz source array in 250 nm BiCMOS SiGe technology [63].

The measurement results have been submitted and accepted for publication at the ISSCC. The implementation represent state-of-the-art results in terms of total radiated power, frequency of operation and pixel count. I have design the control circuit for the source array capable of powering on and off any pixel in the array at run time.

Finally, imaging demonstrations have been achieved with the implemented circuits to demonstrate cost-effective alternative to existing active terahertz systems.

1.6 Organization of the thesis

This manuscript is divided in six subsequent chapters following this introduction. They are organized as the following:

- **Chapter 2** reviews the theory of terahertz power detectors, oscillators and their figure of merit. Diode based power detector DC response is explained by the quasi-static equation. Frequency behavior of bipolar transistor direct detector is explored by Voltera series derivation. CMOS based terahertz detector are analyzed from the non-quasi-static approach in different technological nodes. The theory of terahertz oscillators is briefly reviewed in view of controlling source elements in large arrays.
- **Chapter 3** discusses the design methods and shows the implementation of silicon based terahertz direct detectors. Three devices are explored in two different technologies. Heterojunction bipolar detector (HBT) and Schottky barrier diode (SBD) are implemented a 250 nm BiCMOS SiGe technology. NMOS is integrated in a 65 nm CMOS bulk technology.
- **Chapter 4** presents the first 1 k-pixel CMOS terahertz camera. The circuit design challenges for large terahertz array system will be discussed, then implementation will be detailed. A novel characterization technique for the terahertz camera in video mode will be introduced. A pixel characterization is also shown for comparison with state-of-the-art detectors. An improved readout circuit for scalable terahertz arrays is presented and implemented.
- **Chapter 5** describes and discusses the design of the control circuit of a reconfigurable 4×4 terahertz source array and its characterization.
- **Chapter 6** will present imaging setups in transmission-mode. Rester scanned object and real time terahertz imaging results are presented. An evaluation of beam monitoring application is successfully presented for a high power terahertz.
- **Chapter 7** will summarize and conclude the work of this thesis. This chapter will also give a perspective on future work.

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Chapter 2

Theory of Terahertz Sources and Direct Detectors in Silicon Technologies

Terahertz silicon based source and detectors are very promising alternatives to the existing terahertz technologies. The sources can be based on multiplier chains or oscillators and the detectors may use the non-linearity of different devices to operate as square-law power detectors.

In this chapter, section 2.1 is dedicated to the analysis of a possible control circuit for oscillator based terahertz sources. In section 2.2, analyses of terahertz diode, bipolar and CMOS detectors are reviewed by quasi-static, Voltera expansion and non-quasi-static analyses.

2.1 Terahertz silicon based sources

As it has been presented in the introduction of this manuscript, it is possible to realize electronic terahertz sources in silicon technologies. Two type of sources can be distinguished, multiplier chains [1] and harmonic oscillators [2]. Despite the fact that multiplier chain sources may be used for coherent detection, they have two disadvantages which are the DC power consumption and the large layout area on silicon.

Harmonic oscillators are however very compact and present an advantage for large array integration. Two type of harmonic oscillator designs exist: the feedback design and the negative-resistance design. The design of silicon based oscillators is out of the scope of the thesis. Therefore, only a theoretical system analysis is given here in the perspective of controlling large array sources in silicon technology.

2.1.1 Control circuit of array sources in silicon technologies

A transistor in a specified technology can be characterized by the transistor short circuit current gain at unity gain frequency f_T, and the maximum unity power gain f_{max}. These two limits are defined by the technology process and are improved by device engineering.

Beyond f_T/f_{max} the transistor does not have gain. However, as it will be seen in the section 2.2 dedicated to power detectors, a transistor can still respond to an excitation with an attenuation behavior.

Bellow f_T/f_{max}, it is possible to build active circuits. To overcome the technology limitations, harmonic generators are therefore built. These generators consist of a combination of fundamental oscillators operating below the technology f_T/f_{max}. The harmonic component of the designed combination can be extracted at high frequencies.

To achieve high power sources a large number of such oscillators can be integrated on the same chip. But increasing the number of elements would increase the power consumption by the same factor. In such a system, the total power consumption is a key element that limits the array size for example. Therefore, to achieve large pixel count which favors diffused illumination, a control system is needed.

In such oscillators, stability conditions criterion applies to maintain oscillations [3]. Now modifying the stability conditions would bring the oscillator to operate in a different mode or to stop the oscillations. The control system would impact a specific oscillator in the array by modifying its stability. In a ring type of oscillator, this can be made by modifying or breaking the feedback loop. In a

negative resistance based oscillator, the control circuit would modify the stability criterion by inverting the resistance sign of the active element for instance. In both cases, the frequency of operation can be changed or the oscillator can be turned off to minimize power consumption.

For terahertz oscillator sources, the oscillation conditions are sensitive to the designed passive elements, and active components such as switches can be difficult to implement. For this reason, it is more favorable to implement the control circuitry to impact the biasing conditions of each oscillator.

2.1.2 Terahertz sources figures of merit

A terahertz source can be characterized by:

- P_{TX} the total radiated power,
- F_{RF} the frequency of operation and
- the DC power consumption.

At terahertz frequencies, the lack of on-wafer measurement equipment such as prob stations makes free space method the only possibility to characterize high frequency sources. Therefore, an electronic terahertz source is usually equipped with an antenna. It is characterized by its directivity D_{TX} at a specified frequency. In a free space system, P_{TX}, F_{RF} and D_{TX} are verified optically. As it will be seen in the next chapters, these measures are very critical for the characterization of a terahertz system.

The DC power consumption is often referred to the efficiency of the terahertz source and defined as the ratio P_{TX}/P_{DC} where P_{DC} is the DC power consumption.

2.2 Terahertz silicon detectors

2.2.1 Detectors theory

It is possible to analyze terahertz direct detectors by different methods. In this section, quasi-static analysis is first applied to diode based power detector. Then a bipolar detector is analyzed from Volterra expansion. As a third method, non-quasi static analysis is applied to CMOS based direct detectors.

2.2.1.1 Diode based detector

Terahertz direct power detectors are usually built with nonlinear devices. Such detectors provide a square-law rectification of the signal resulting in a DC output current or voltage proportional to the RF input power. This type of power detector can be a diode device for instance as shown in figure 2.1 (a).

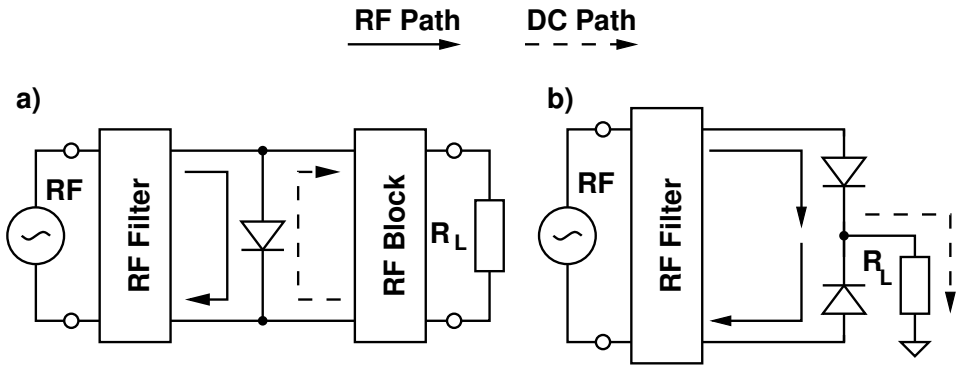

Figure 2.1: (a) Single-ended and (b) differential diode based square-law power detector. The bias circuit is omitted for the clarity of the figure.

To isolate the RF and the DC path, an RF filter with a DC block has to be implemented at the input of the detector. At the output, an RF block is needed in order to avoid leakage of the RF power into the output load. For example, the RF filters can be implemented with tuning stubs, and could contribute to the impedance matching. A differential topology as shown in figure. 2.1 (b) has the advantage to eliminate the RF block by creating an AC ground at the output.

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The rectification of the input RF power can be derived from the quasi-static equations of the diode. In forward bias conditions, the current can be expressed as a function of the bias voltage:

$$I(V) = I_0(e^{qV/(k_BT)} - 1) \tag{2.1}$$

with:

- I_0: is the reverse saturation current,
- q: is the elementary charge,
- k_B: Boltzman constante,
- T: the temperature in Kelvin.

When a small signal AC voltage ($v_{RF}(t) = A_{RF}cos(2\pi ft)$) is applied to the diode ($V = v_{RF}(t) + V_{bias}$) as shown in figure 2.1 (a), a square-law rectification results from the non-linearity of the diode. The DC component of this rectification can be derived from the current-voltage quasi-static expression in equation 2.1. The Taylor series expansion of the diode current can be developed as

$$I(V) = I_0(\frac{qV}{k_BT} + \frac{1}{2!}(\frac{qV}{k_BT})^2 + \frac{1}{3!}(\frac{qV}{k_BT})^3 + ...), \tag{2.2}$$

where the V can be replaced with the expression:

$$(v_{RF} + V_{bias})^2 = A_{RF}^2/2 + A_{RF}^2cos(2\omega t)/2 + V_{bias}^2 + V_{bias}A_{RF}cos(\omega t). \tag{2.3}$$

The harmonics of the resulting equation 2.2 will be filtered by the output RF block. As a result, the remaining DC component of the current is

$$I = \frac{q^2I_0}{(k_BT)^2}(\frac{A_{RF}^2}{4} + \frac{V_{bias}^2}{2}), \tag{2.4}$$

and it is directly proportional to the RF input power

$$I \propto \frac{A_{RF}^2}{4}. \tag{2.5}$$

This analysis is valid for GHz range power detector, and breaks down at terahertz frequencies because of parasitic elements that are not taken in consideration.

Therefore, other models should be used to determine the frequency response of the detector.

2.2.1.2 HBT based terahertz detector

In a bipolar technology, a single diode can be build out of a transistor by connecting the collector and the base terminals as presented in figure 2.2 (a). However, with the transistor third terminal, three basic single-stage topologies can be explored. The common emitter, common base, and common source topologies are presented in figure 2.2 (b) (c) and (d). For the same isolation reasons explained for the diode topology, RF filters and DC blocks are needed to avoid leakage of the RF power into the output load and vice versa.

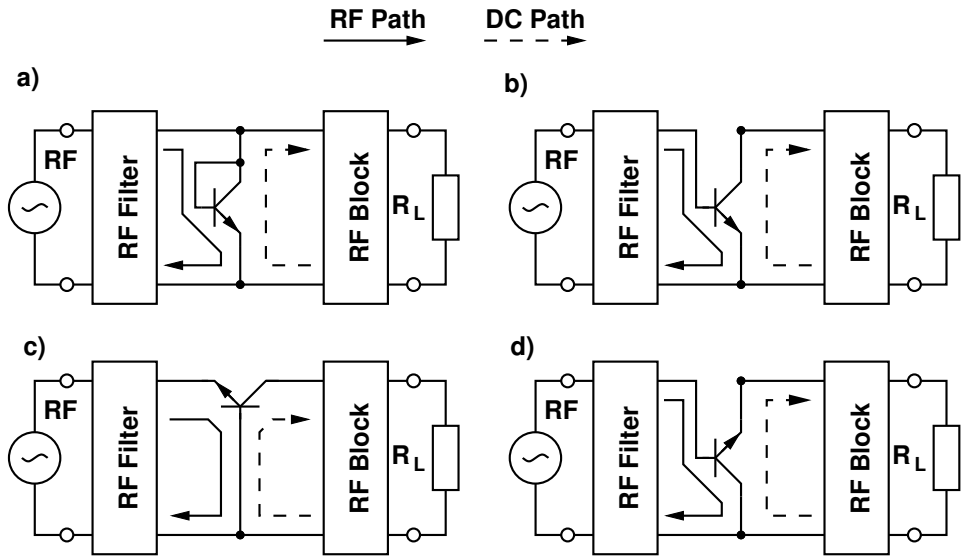

Figure 2.2: Possible HBT based direct power detectors. Diode connected transistor (a), common-emitter(b), common-base(c) and common-collector (d) stage configurations.

To analyze these detector stages, the same quasi-static analysis developed for the diode detector can be done and would lead to the same result $I \propto \frac{A_{RF}^2}{4}$. However, it would only give a DC analysis of the detected signal and would not give any information about the frequency response of the detector. Therefore, a Volterra series can be derived to incorporate the frequency dependent effects

of the detector. In this section, the common-emitter stage is reviewed. The large-signal model is presented in figure 2.3.

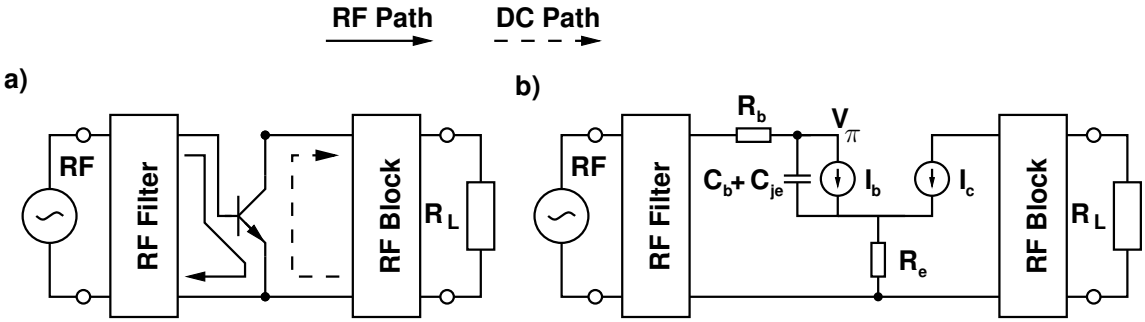

Figure 2.3: Common-emitter direct detector (a) and its large-signal equivalent circuit (b) for frequency analysis.

This analysis has been explored in the literature to study the nonlinearity effects of mixers and amplifiers [4]. It has been applied to square-law detectors [5] and is revisited here to underline the frequency dependence of the detector. From the small signal model of figure 2.3, the base voltage can be expressed as

$$V_b = (sC_{je}V_\pi + s\tau_F I_c + \frac{I_c}{\beta_0})(Z_b(s) + Z_e(s)) + I_c Z_e + V_\pi, \tag{2.6}$$

where:

- C_{je}: is the base-emitter junction capacitance,
- C_b: is the base charging capacitance,
- τ_F: is the forward transit time,
- β_0: low-frequency current gain with $I_c = \beta_0 I_b$,
- Z_b: is the base impedance,
- Z_e: is the emitter impedance.

The current can be expressed as Volterra series in frequency domain as

$$I_C = H_1(s) \circ V_B + H_2(s_1, s_2) \circ V_B^2 + ... + H_n(s_1, s_2, ..., s_n) \circ V_B^n, \tag{2.7}$$

where:

I_C: is the collector DC current,
$H_n()$: is the Volterra series n coefficient,
V_B: is applied base voltage,
s_n: is Laplace variable $j\omega_n$.

The operator $\circ$ indicates the multiplication of the each frequency component by $|H_n()|$ and the shifting by its phase. For the common-emitter configuration the Volterra kernel coefficients have been solved in [4] and are:

$$H_1(s) = \frac{g_m}{sC_{je}Z(s) + staus_F Z(s) + g_m\frac{Z(s)}{\beta_0} + 1 + g_m Z_e(s)}, \tag{2.8}$$

$$H_2(s_1, s_2) = H_1(s_1 + s_2)H_1(s_1)H(s_2)\frac{V_T}{2I_Q^2}(1 + (s_1 + s_2)C_{je}Z(s1 + s2)), \tag{2.9}$$

with:
Z: is the sum $Z_b + Z_e$,
I_Q: is the total current of the transistor,
g_m: is transconductance term I_Q/V_T.

The square-law rectification happens at the even order harmonics resulting in a DC response as described in Taylor expansion for the diode detector. Neglecting the high harmonic effects and low frequency gain, the resulting response can be calculated using the Volterra series coefficient $H_2(s_1, s_2)$ assuming $s_1 = -s_2 = s$ [5],

$$I_C = \frac{gmV_b^2}{2V_T(1 + g_m R_e)((1 + g_m R_e)^2 + R^2\omega^2(\frac{gm}{\omega_t} + C_{je})^2))}. \tag{2.10}$$

The resulting equation has been used to estimate the current response with bias condition at 94 GHz [5]. For that, the device estimated SPICE parameters may be used from a Design Kit to evaluate the detector response. In this section, the frequency characteristics are of interest and HBT SPICE parameters from IHP SG13G2 design kit have been replaced in equation 2.10. The resulting characteristics are shown in figure 2.4.

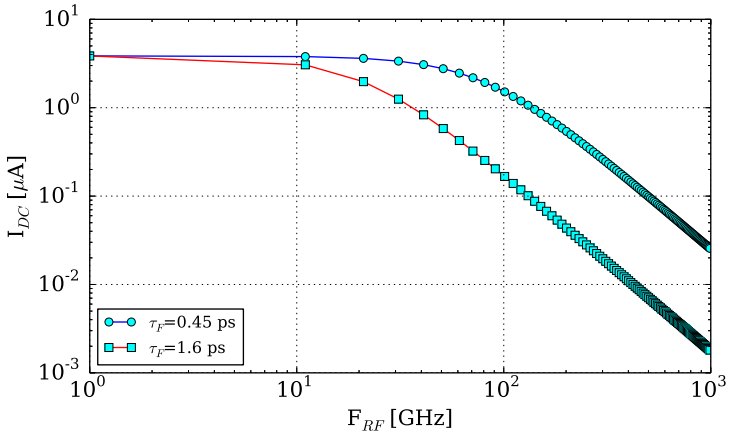

Figure 2.4: Caluculated DC response for an HBT direct detector to an RF input for common-emitter configuration of figure 2.3. 1.6 ps and 0.45 ps transit time were used for the calculation.

In the figure 2.4, two different transit time parameters have been used to underline the importance of the device speed impact on the DC response. The forward bias transit time given in the SPICE model of the design kit is approximately 0.45 ps.

At low-frequencies, the common-emitter configuration amplifies the input voltage resulting in a large second harmonic effect on the DC response. Beyond the transistor limits, the response is attenuated, however it is not negligible and in the fraction of the microamp of amplitude. The roll-off happens around at the transistor limits and is 20 dB/dec.

The comparison between a short and long τ_F for the same device bring the conclusion that fast transistors are in favor of a more efficient terahertz detector.

2.2.1.3 CMOS based terahertz detector

For a CMOS technology, the same analysis can be developed with similar detector configurations as presented for a bipolar technology in the previous subsection. A diode can be built out of a CMOS transistor by connecting the gate and drain as shown in figure 2.5 (a). Three other topologies are presented in figure 2.5 (b), (c), (d) and correspond to common-source, common-gate, and common-drain detector circuit.

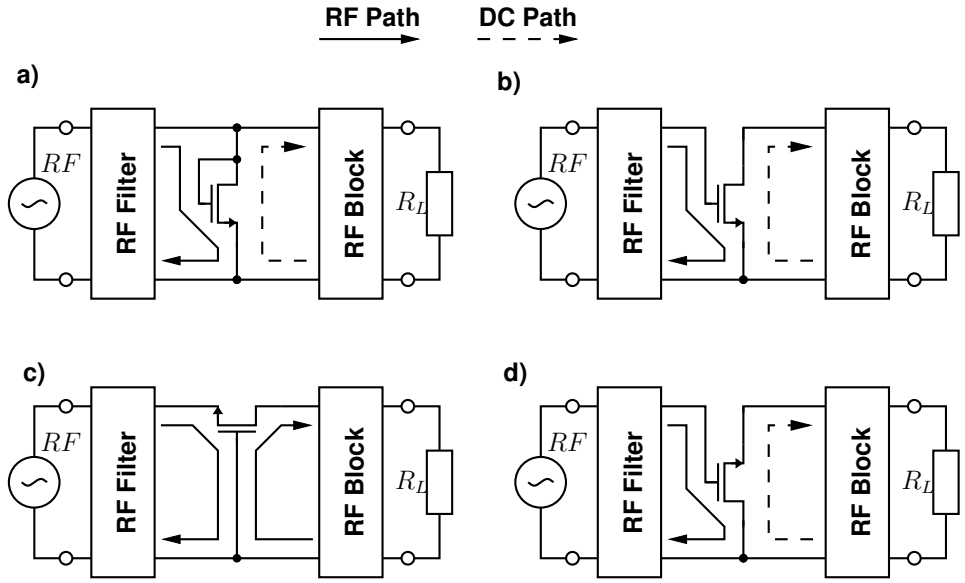

Figure 2.5: Possible CMOS based direct power detectors. Diode connected transistor (a), common-source(b), common-gate(c) and common-drain (d) stage configurations.

Quasi-static and Volterra series analysis can be applied to understand the power detection mechanism of the CMOS transistor. The methods used to analyze the DC response of a diode and HBT based detector are also valid for CMOS devices and would lead to the same conclusion drawn in the previous sections of this chapter. The output DC response is proportional to the input RF power and is strongly dependent on the frequency response of the transistor.

In this section, another method is reviewed to give a millimeter-wave design perspective to the CMOS based power detector. This method is based on the

non-quasi-static analysis of the transistor channel.

To conduct this analysis, the transistor can be seen as a non-linear transmission line according to figure 2.6 (a). This transmission line can be divided into small RC portions as shown in figure 2.6 (b).

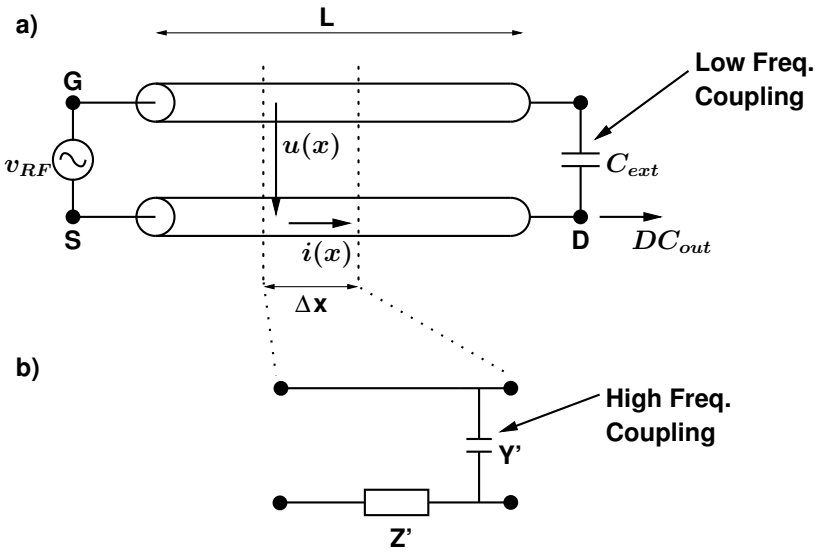

Figure 2.6: Transmission line model of the device (a) that can be divided into small RC portions (b) [6].

The received RF signal by the transistor will create a time-harmonic excitation of the gate-to-channel voltage $u(x,t) = u(x)e^{j\omega t}$, where $u(x)$ is the phasor function of the time-invariant amplitude and phase information along the channel. Transmission-line theory can be applied according to figure 2.6 (b), to derive the first-order differential equation (DE) for the voltage and current

$$\frac{du(x)}{dx} = -Z'i(x) \tag{2.11}$$

$$\frac{di(x)}{dx} = -Y'u(x), \tag{2.12}$$

where $Z' = R' + j\omega L'$ and $Y' = G' + j\omega C'$. Gate leakage currents ($G' = 0$) and inductive effects ($L' = 0$) are neglected. For strong inversion, in the linear

region of the transistor, the channel resistance per-unit-length R' is given by the channel conductance $1/R'(x) = \mu C'(u(x) - v_{th})$, where $C' = C_{ox}W$ is the gate oxide capacitance per-unit-length, W is the transistor width, and v_{th} is the transistor's threshold voltage. The two mixed first-order differential equations 2.11 and 2.12 can be combined into one second-order differential equation for $u(x)$ by solving equation 2.11 for $i(x)$ to eliminate $i(x)$ in equation 2.12. This leads to the following differential equation for $u(x)$

$$j\omega u(x) = \frac{d}{dx}[\mu(u(x) - v_{th})\frac{du(x)}{dx}]. \tag{2.13}$$

For a time-harmonic excitation, $j\omega u(x)$ is equal to $\frac{d}{dt}u(x,t)$. This leads to the following partial differential equation (PDE) for time and space derivatives as

$$\frac{\partial}{\partial t}u(x,t) = \frac{\partial}{\partial x}[\mu(u(x,t) - v_{th})\frac{\partial u(x,t)}{\partial x}]. \tag{2.14}$$

The primary use of the above PDE is to investigate the inner behavior of the transistor channel in order to understand the mixing procedure. There is no analytic solution to solve this PDE and numerical approach is necessary. Numerical solution of the PDE is shown in figure 2.7. The gate-to-channel voltage is calculated for device size of 250 nm, 130 nm and 65 nm for a small signal excitation at 1 THz.

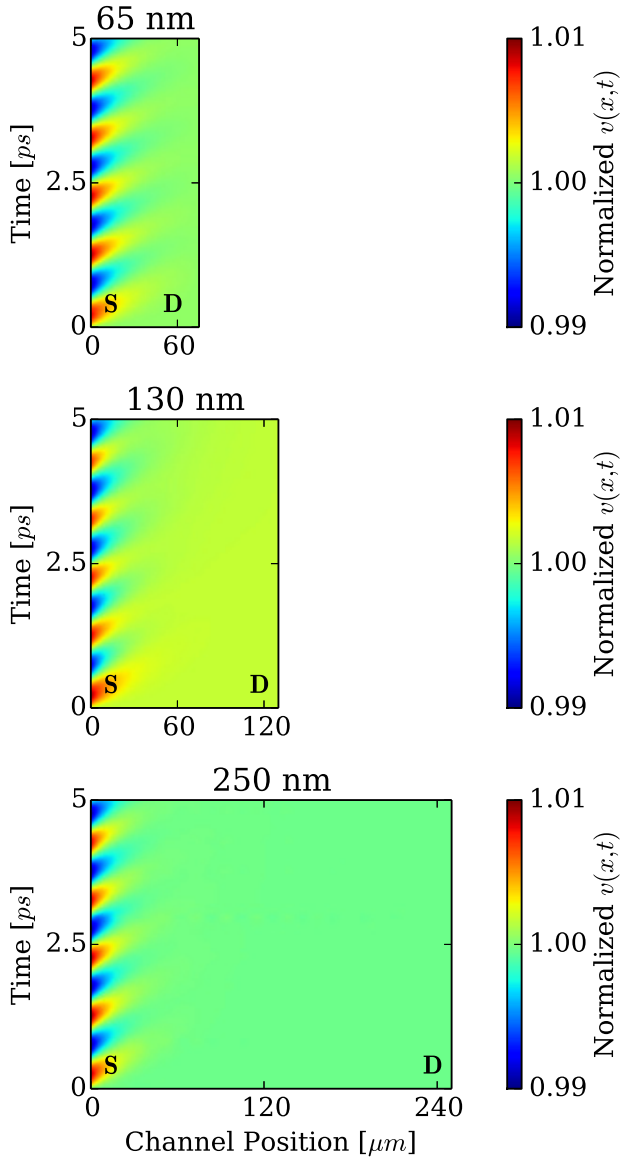

Figure 2.7: Numerical solution of the PDE 2.14. The gate-to-channel voltage is calculated for device size of 250 nm, 130 nm and 65 nm for a small signal excitation at 1 THz.

At the source terminal of the transistor the voltage excitation is exponentially attenuated and converts to a DC current. For a small channel device, the same behavior is calculated in 65 nm channel length. This brings the conclusion that

the square-law properties can be implemented in any CMOS device. However, going to a smaller channel length would benefit from the noise reduction of the non-used portion of the transistor.

Despite the fact that the PDE model gives information about the inner behavior of the channel, it is gradually invalid at higher frequencies. Therefore, the Boltzmann's transport equation [7] or the Wigner-Boltzmann [8] equation should be considered in the future to take realistic deep-sub-micron structures into account.

2.2.2 Terahertz detectors figures of merit

The responsivity (R) and the noise equivalent power (NEP) are a measure of the performance of terahertz direct detectors. The responsivity is a measure of the electrical output strength per input power (P_{in}). The output response of a direct detector can either be measured in current-mode

$$R_I = \frac{I_{out}}{P_{in}}, \tag{2.15}$$

or voltage-mode

$$R_V = \frac{V_{out}}{P_{in}}. \tag{2.16}$$

The resulting unit of the responsivity can be expressed in $[A/W]$ or $[V/W]$ depending on the measurement mode.

The NEP corresponds to the measured detector spot noise at a specific frequency for a 1-Hz bandwidth divided by the responsivity. The noise can be measured in current mode I_n such as

$$NEP = \frac{I_n}{R_I}, \tag{2.17}$$

or in voltage-mode V_n

$$NEP = \frac{V_n}{R_n}, \tag{2.18}$$

which leads to an NEP unit of $[W/\sqrt{Hz}]$.

From a characterization point of view, three physical parameters have to be measured in order to determine the performance of a direct detector:

- the output voltage or current,
- the output noise,
- the input power.

Depending on the readout mode, the output DC voltage or current can be estimated by the analysis of the device behavior at terahertz frequencies and has been reviewed in the previous subsections of this chapter.

However, the only measure of responsivity will not give any information about the SNR in presence of a terahertz signal. In fact, if an amplifier is used, the signal is multiplied by the gain and also the noise. Therefore, the noise measurement will be used to calculate the NEP of the detector and give an information about the SNR behavior of a detector for a specified amount of power.

In an on-wafer setup, it is convenient to measure the electrical input power injected to the detector circuit by the probes. However at terahertz frequencies, this is not possible due to the lack of suitable terahertz on-wafer equipments and optical measurement is needed. As a result, optical based devices are the only possibility to build terahertz detectors. The sources are equipped with antennas as well as the detectors.

For an antenna coupled setup, the available optical input power to the detector P_{in} can be calculated by Friis transmission equation is then given by:

$$P_{in} = \frac{P_{TX} G_{TX}}{4\pi r^2} A_{eff}, \tag{2.19}$$

with:

P_{TX}: is the source output power,
G_{TX}: source antenna gain
r: the distance between the detector and the source,
A_{eff}: the detector effective antenna area.

The A_{eff} can be calculated from the receiver antenna directivity D_{RX} such as:

$$A_{eff} = D_{RX}\lambda^2/(4\pi). \tag{2.20}$$

An accurate measurement of the optical responsivity and NEP requires an accurate measurement of the electrical response, the noise and the available power. This will be discussed in the next chapter where measurement results will be shown.

2.2.3 Readout circuit utility

As it has been described in the previous section, terahertz detector are possible in silicon technologies by using standard devices. However, the different theories around the detection mechanisms have led to the conclusion that the expected responsivity are very low. Therefore, efficient readout circuit is needed in order to extract with a small noise contribution the detector response to an incident terahertz power. This is more valid for large terahertz arrays where multi-pixel implementation can be achieved.

2.3 Chapter summary and conclusion

Terahertz sources and detectors can be implemented in silicon technologies beyond the frequency limitations f_T/f_{max}.

Harmonic oscillators are used for terahertz source and control circuitry is needed for large source array implementations. To simplify the design of control circuits, they can be applied to the DC nodes of a harmonic oscillator.

Analyses through different methods of terahertz power detectors have shown that devices beyond the technological frequency limits can respond to a terahertz excitation. The responsivity of such device is very small and readout circuits are necessary to implement large detector arrays.

These two conclusions will be verified in the following chapters by implementation and characterization of detectors and sources operating at terahertz frequencies.

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Chapter 3

Terahertz Detectors Circuit Design and Characterization

As it has been presented in the previous chapter, terahertz detectors can be built out of standard devices beyond the technology frequency limits f_T/f_{max}. A quantitative analysis of different detectors has led to the conclusion that best results can be expected from advanced technologies. As it will be described in this chapter, this is only possible if an optimization design approach is applied.

In this chapter, terahertz direct detector design methodology is first presented in the perspective of implementing antenna coupled detectors in different technologies. The design guidelines are drawn from the the previous chapter analysis and the matching condition necessary to build sensitive terahertz detectors as well as low noise optimization. Implementation results and analysis are then presented for HBT, CMOS and SBD based detectors.

3.1 Direct power detector design methodology

3.1.1 Responsivity and matching conditions

In the previous chapter, the detection mechanism have been reviewed leading to the conclusion that power detectors can be built with standard devices beyond the technology limits f_T/f_{max}. From an electrical point of view, the detector can be modelled as a coupled antenna receiver equivalent circuit. As it is presented in

figure 3.1, the antenna can be seen as a voltage source V_A with internal complex impedance $Z_A = R_A + jX_A$. The detector circuit would be a complex load $Z_L = R_L + jX_L$ connected to the antenna.

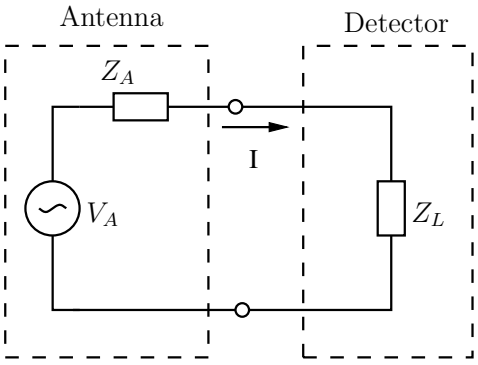

Figure 3.1: Equivalent circuit of an antenna coupled direct detector.

In this circuit, the maximum power transfer theorem is satisfied with the conjugate matched condition $Z_L = Z_A^*$. The maximum power available to the load can be written as

$$P_{L,max} = \frac{V_A^2}{4R_L} \tag{3.1}$$

As it has been seen in the previous chapter, the responsivity is defined as the electrical output strength per input power. For a square-law power detector, the electrical response of a periodic excitation results in a square-law dependency ($V_A^2 cos^2(\omega t) = V_A^2/2 + V_A^2 cos^2(2\omega t)/2$), where the DC component of this response is proportional to the input power (Taylor expansion in chapter 2).

Now, for a defined power at the antenna, a large voltage swing can be obtained by a large resistive load at the matching conditions of equation 3.1.

However, this impacts directly the noise performance of the detector. In fact, the thermal noise generated by the large resistance would degrade the noise performance of the detector. Therefore an optimized design conditions can be found. The matching have to be found in the same time for best electrical response and best noise performance which results in an optimum value.

As it will be seen in the sections dedicated to the implementation of different

detectors, this condition can be found by optimizing the size and bias conditions of the detectors for a given antenna.

3.1.2 Low frequency noise

As it has just been described, the noise performance are very important for direct power detectors. Since the power detector down converts the received RF power to DC, the responsivity will be measured relatively to the noise floor at low frequencies. The noise sources of a semiconductor device can be divided into three main categories for 1 Hz bandwidth:

- thermal noise $v_n = \sqrt{4k_BTR}$,
- shot noise $i_n = \sqrt{2Iq}$,
- flicker or $1/f$ noise.

With:

k_B: is Boltzman constante,
T: is the temperature in Kelvin.
R: is the resitance of the device,
I: is the DC current of the device,
q: is the elementary charge,

The thermal noise will always impact the measurement of any electronic system. However, it is directly proportional to the equivalent resistance of the device. Therefore, optimization of the detector is necessary to match the device for low noise performance and keeping the responsivity as high as possible.

The shot noise corresponds to the fluctuation of the charge carries through the semiconductor device. This noise can greatly effect the performance of the terahertz detectors. Therefore, low current density devices are preferred to reduce its effect. In the HBT detectors case, low-frequency noise matching can be applied to mitigate the contribution of the base-emitter shot noise. Concerning CMOS detectors, non-biased channel operation is preferred. This mode is also named "cold" operation and benefit greatly to the transistor by eliminating the shot noise.

Unlike thermal and shot noise, flicker noise can be difficult to mitigate from a design perspective. However, modulation techniques have been used to measure the different devices and overcome the $1/f$ noise.

In the next sections, detailed analyses of the different implementations are presented.

3.2 HBT based terahertz detector

The recent advancement in SiGe HBT technologies has enabled new design possibilities starting from 60 GHz circuits [1]. The technology evolution has been constant during the last years. European projects such as "dotfive" and "dotseven" have contributed to join efforts and develop fast technologies by improving the process and demonstrating circuits at very high frequencies [2].

In this section, an analysis and implementation of an HBT based terahertz power detector in a 250 nm BiCMOS SiGe is presented. Design considerations, implementation and measurement analysis are presented in the following subsections.

3.2.1 Design considerations of an HBT based terahertz detector

As it has been presented in the previous chapter, terahertz detectors are commonly built with non linear devices such as diodes. The non-linearity of the device provides a square-law rectification of the signal resulting in a DC output current or voltage proportional to the RF power.

A diode can be build out of a bipolar transistor by connecting the collector and the base. The differential structure has the advantage to create an AC ground at the output and interface readout circuit as it is shown in figure 3.2 (a). The RF signal is injected at the base-collector shared terminal. For a vertical device, where the collector is very large in comparison with the emitter, diode connected detector might have reduced performance. In fact, the capacitive coupling to the substrate through the collector region reduces the RF power being injected into the device, while being dissipated in the substrate. A first solution to reduce the

substrate coupling is to use a common-emitter circuit topology. In this case an RF block would be required as shown in figure 3.2 (b).

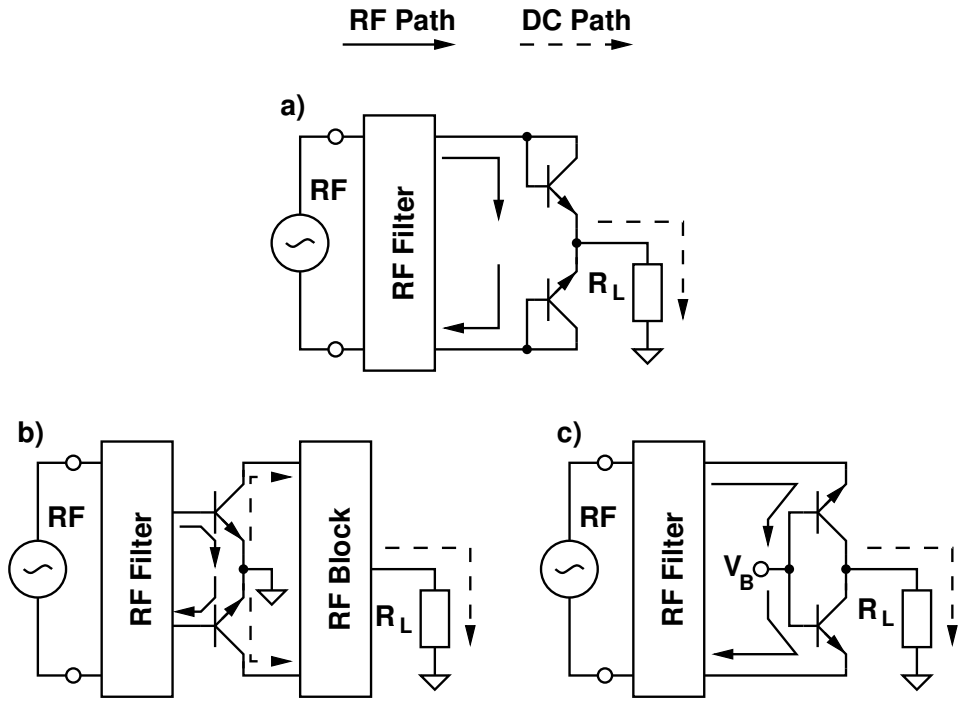

Figure 3.2: Possbile differential HBT based terahertz detectors. Diode connected (a), commun-emitter (b) and commun-base (c) are presented.

To better isolate the RF to substrate coupling, a differential common-base circuit can be used where the base and the collector are AC ground as shown in figure 3.2 (c). This differential configuration gives three advantages. The first advantage is an output AC ground where no extra RF block is required. This makes the design easier to interface to conventional readout circuitry and avoid any potential losses from RF blocks. The second advantage is an extra degree of freedom of the bias operating point, in comparison with the diode connected device. This extra freedom can be used for detector optimization. The third advantage is the isolation to the relatively large substrate.

To support the choice of the differential common-base detector of figure 3.2 (c), a simulation has been done in the IHP 250 nm BiCMOS SiGe technology to investigate its performance as shown in figure 3.3. Ideal RF filters and blocks

have been used for the presented simulation. Furthermore, the input port always provides a conjugated impedance match to the detector at all frequencies.

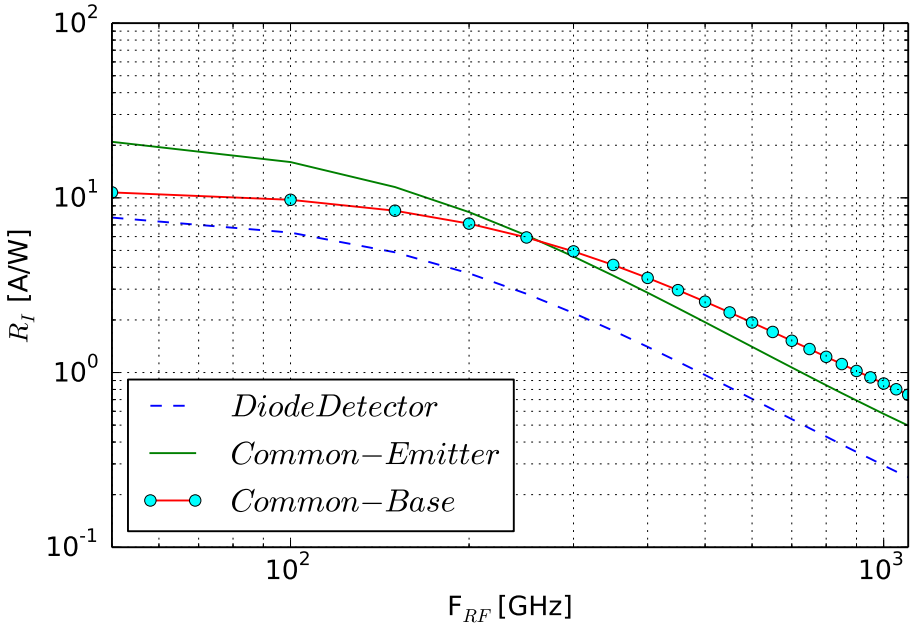

Figure 3.3: Simulated maximum responsivity of the differential detector topologies shown in in figure 3.2(a,b,c). A conjugate matched port and ideal RF filters/blocks have been used for this simulation. Same bias conditions are applied for comparison.

The differential diode connected transistor of figure 3.2 (a), with the signal fed at the base-collector shared terminal, has shown the lowest responsivity. Below f_T/f_{max}, where the transistor can provide gain, the differential common-emitter topology of figure 3.2 (b) has the higher responsivity. Above f_T/f_{max} where the transistor attenuates the injected signal, this benefit is lost and the differential common-base circuit configuration of figure 3.2(c) has shown better performances and has been implemented with respect to the highest expected responsivity.

This can be further clarified by looking into the charge carriers. They are driven back-and-forth through the small base-emitter junction as indicated in the cross-sectional view in figure 3.4. The DC down-converted charges are collected and extracted through the large collector region. As a consequence, the RF does

not leak into the relative large collector and substrate region.

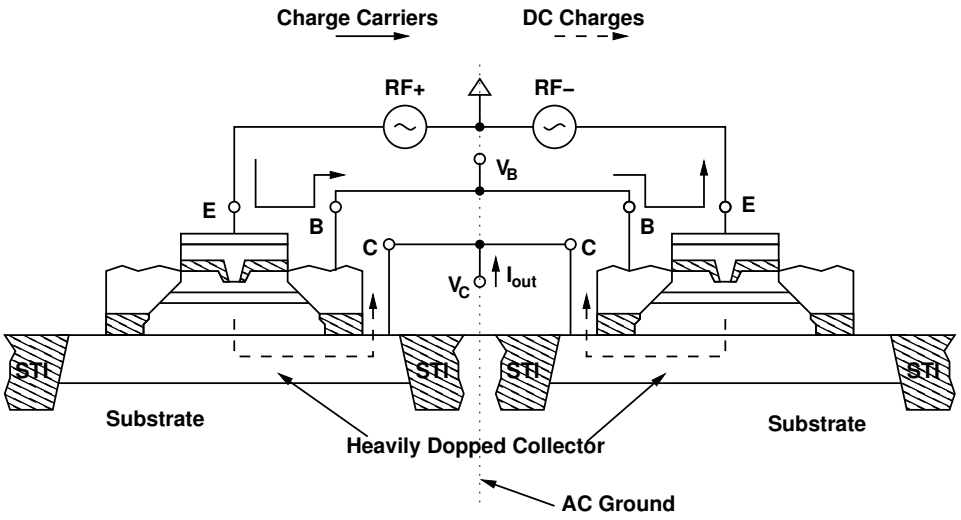

Figure 3.4: Simplified cross-sectional view of the differential common base HBT terahertz detector [3].

The detector benefit clearly from the transistor high cut-off frequencies (f_T/f_{max}) as it as been demonstrated by Volterra series in the chapter 2. This has been possible by continued device scaling and parasitic capacitance and resistance reduction, which is beneficial for the signal injection into the transistor [2].

3.2.2 HBT detector circuit implementation

The implementation choice of the detector has been the common-base topology with respect to the highest expected responsivity. The common-base detector circuit design makes use of the base-emitter diode of the SiGe HBT as a non-linear element to directly down-convert a terahertz power to DC. A differential ring antenna capturing the terahertz power is connected to the emitters of the differential pair as shown in 3.5.

The antenna has been designed to radiate through the silicon substrate and a silicon lens. In view of known device model uncertainty which have not been verified at terahertz frequencies, the antenna design approach was to provide a broadband 100-Ohm port impedance to the detector. The simulated detector real

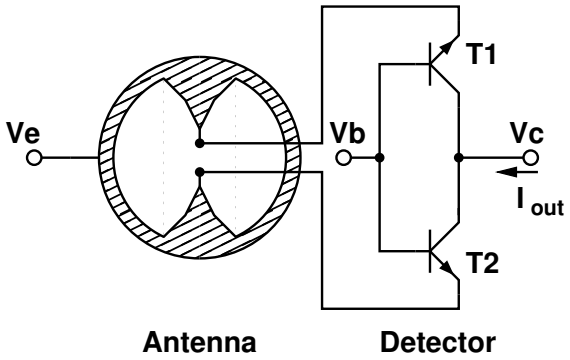

Figure 3.5: Differential common-base HBT terahertz detector pixel schematic [3].

and imaginary impedance are shown in figure 3.6 and compared to the antenna impedance. This approach makes the design more robust against device model variations. Due to this approach, the matching conditions discussed earlier are not satisfied which results in a return-loss and reduced output response.

The HBT terahertz detector has been implemented in a 3×5-pixel array. Figure 3.7 shows the circuit schematic of the array. All pixels share the same base DC bias. A DC ground is provided to the emitter through the antenna. Each pixel is connected to an output to be read separately.

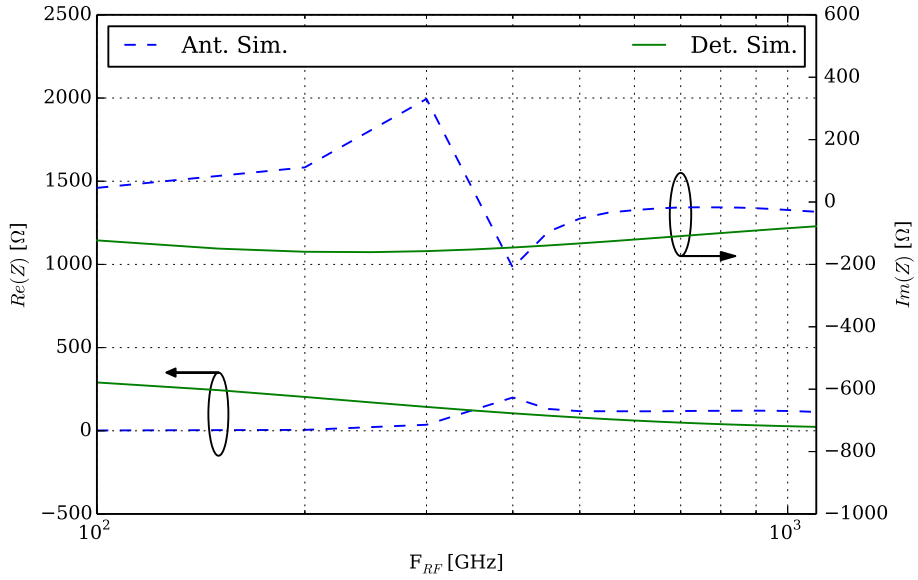

Figure 3.6: Simulated real and imaginary parts of the input impedance of the implemented differential common-base detector in comparison with the antenna impedance.

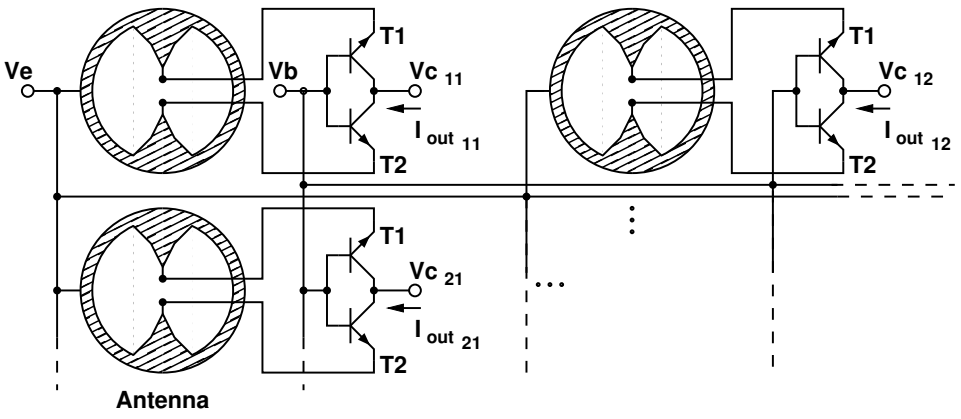

Figure 3.7: Schematic of the differential HBT based detector array. A current readout of the detector response has been performed for each pixel separately [3].

The chip has been manufactured in an experimental 250 nm BiCMOS SiGe technology from IHP Microelectronics. A micrograph of the manufactured chip is shown in figure 3.8. The die thickness is 150 µm. It has been glued to the back of a 3-mm diameter silicon lens and mounted on a low cost printed circuit board.

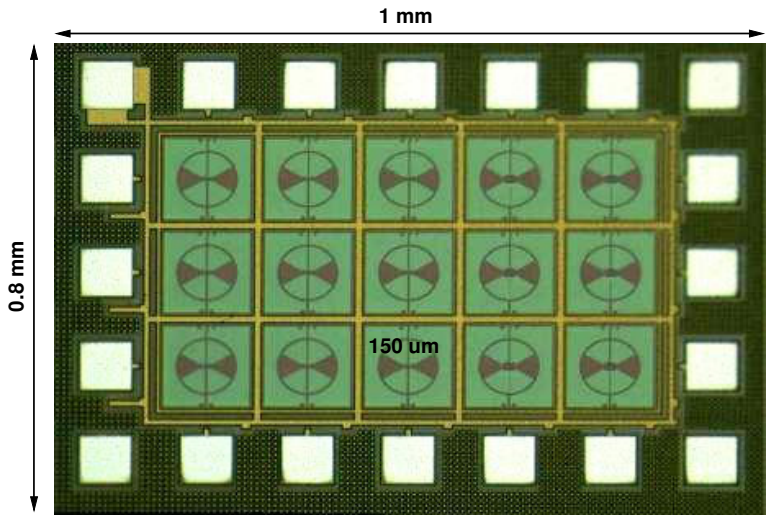

Figure 3.8: Micrograph of the manufactured HBT detector array chip. The detectors have been arranged in a matrix of 3×5 pixels.

In the next subsection, the characterization of the detector is presented. As mentioned above, the design choice of the antenna impacts the detector responsivity since the matching conditions were not satisfied. Therefore, the optical performance of the HBT detector can be further improved with an optimized antenna design.

3.2.3 Measurement results and analysis of the HBT terahertz detector

The implemented HBT based terahertz array has been characterized in free space. An accurate measurement of the optical responsivity requires an accurate measurement of the available optical input power P_{in} available to the detector pixel. A terahertz source with a measured total output power P_{TX} and a specified antenna gain G_{TX} was used to illuminate the detector placed at a distance r as shown in the measurement setup of figure 3.9. Current readout with a low-noise 1000-V/A transimpedance amplifier has been used. Its gain has been deembedded from all data. The output signal and the spot-noise have been read at the chopping frequency with a spectrum analyzer.

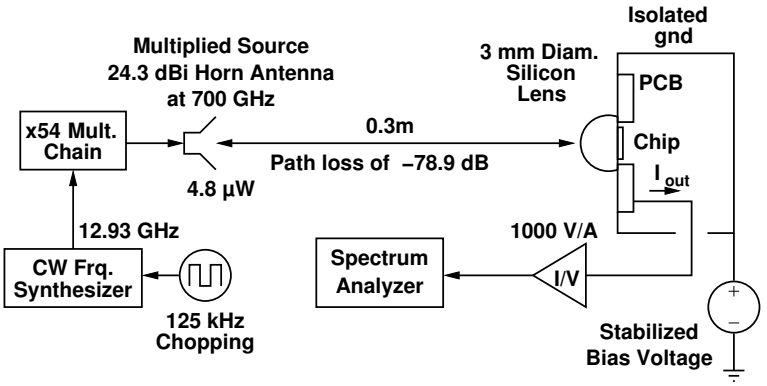

Figure 3.9: Free-space characterization setup for R_I and NEP measurements of the detector. The current readout has been performed with a transimpedance amplifier [3].

In this measurement section, the available power to the detector is first verified by the measurement of the terahertz source total power and the verification of the detector directivity. Then, current responsivity and spot-noise measurement are shown in details.

3.2.3.1 Power calculation and antenna pattern

As presented in figure 3.9, the terahertz multiplied source is equipped with a specified 24.3-dBi horn antenna at 0.7 THz. It has been characterized with an absolute power-meter between 0.6-1 THz. Figure 3.10 shows the variation of the directivity G_{TX} in this frequency range as well as the measured peak power P_{TX} in dBm and in µW.

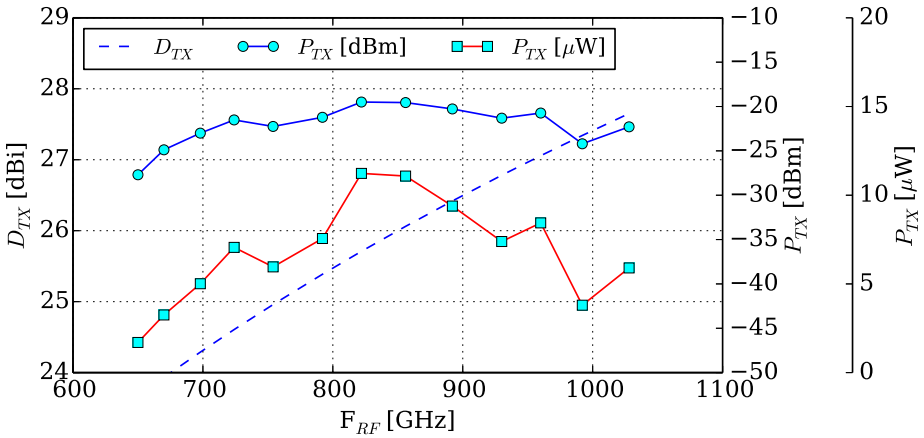

Figure 3.10: Characteristics of the terahertz multiplied source used in firgure 3.9. The directivity is calculated from the manufacturer specification. The total power is measured with an absolute power-meter.

The available input power to the detector according to Friis transmission equation is then given by:

$$P_{in} = \frac{P_{TX} G_{TX}}{4\pi r^2} A_{eff}, \tag{3.2}$$

where $A_{eff} = D_{RX}\lambda^2/(4\pi)$ is the effective antenna area and D_{RX} the receiver antenna directivity. The D_{RX} of the on-chip antenna can be measured by placing the packaged sample in an anechoic chamber and measure its pattern. A similar setup shown in figure 3.9 has been used for this measurement. The relative variation of the output detector current has been measured while the center-pixel detector is rotated over its antenna E-plane and H-plane. These variations have been measured for a source frequency of 0.65 THz. They have been normalized

and plotted in figure 3.11 and figure 3.12 with simulation results.

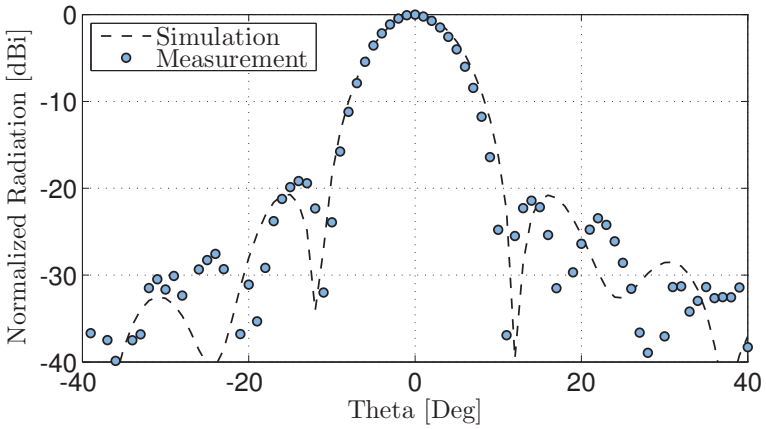

Figure 3.11: Measured and simulated normalized radiation pattern in E-plane cut at 0.6 THz [3].

The measured main lobe has shown a good correlation to the electromagnetic simulations provided by Dr. Janusz Grzyb. This measurement has been repeated over the 0.65-1 THz frequency band. To extract the directivity of the integrated antenna from the radiation pattern, an approximation formula has been used. For a narrow beam patterns, the directivity can be calculated from the Pereira and the Kraus approximations [4]. It is estimated from the half-power-beam-widths θ_1 and θ_2 of the E-plane and H-plane such as

$$D_{Kraus} = \frac{4\pi}{\theta_1\theta_1} \tag{3.3}$$

$$D_{Pereira} = \frac{32ln2}{\theta_1^2 + \theta_1^2}. \tag{3.4}$$

These two formulas are only approximations to estimate the directivity from the measured patterns. The ideal directivity can be calculated from the collecting aperture of the lens such as

$$D_{Ideal} = \frac{4\pi Aperture}{\lambda^2}. \tag{3.5}$$

The result of the measured directivity is compared to the ideal directivity

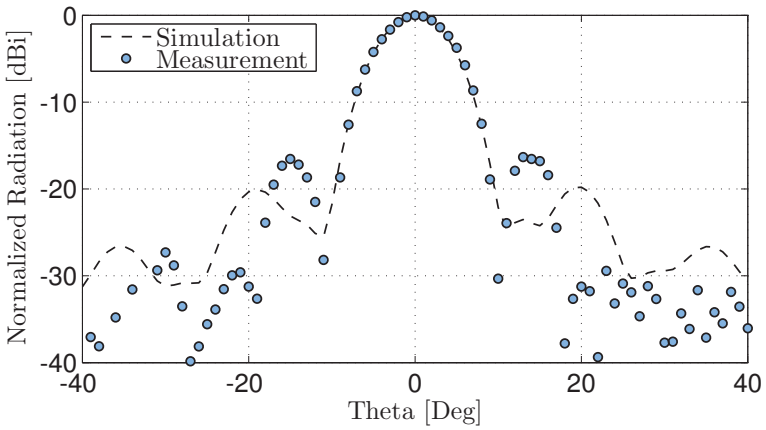

Figure 3.12: Measured and simulated normalized radiation pattern in H-plane cut at 0.6 THz [3].

calculated from the collecting aperture of the 3-mm silicon lens and are shown in figure 3.13.

The calculated directivity from the collecting aperture of the 3-mm silicon lens corresponds to the physical upper limit. As it is presented in the results figure 3.13, estimated directivity from the measured data correlate the increasing behavior of the ideal value with the frequency. However, at the lower frequency range, the estimations are slightly higher than the physical limit. This can be explained by the inaccuracy of the formulas. Therefore, in the following sections, calculated directivity from the physical aperture will be used as a conservative estimate for characterizing the different detectors.

3.2.3.2 Optical Responsivity and NEP Measurements

As previously described in this chapter, the detector needs to be biased at an optimum point where simultaneously high responsivity and minimum output noise is achieved, in other words, where the NEP reaches its minimum. This optimum bias point depends on the RF operation frequency. Below the technology f_T/f_{max}, the optimum detector bias may be seen as a class-B amplifier, where the detector circuit still provides some gain while being almost switched off for low noise contribution [5]. Above f_T/f_{max}, the class-B configuration does not provide

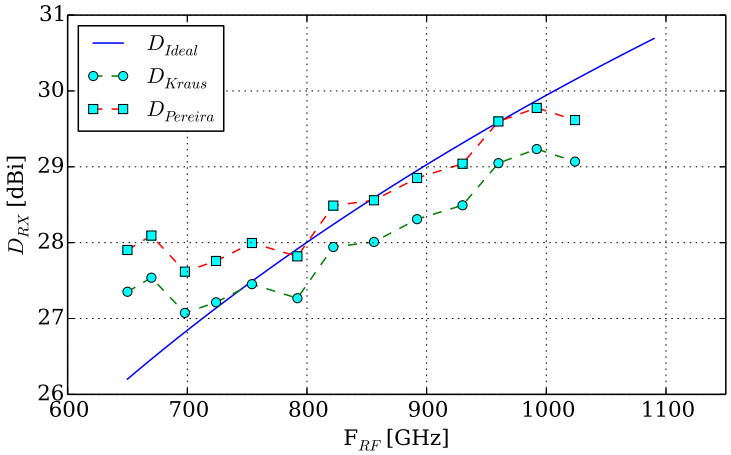

Figure 3.13: Ideal directivity calculated from the collecting aperture of the 3-mm silicon lens in comparison with the measured directivity approximated by Krau and Pereira formulas.

any gain, therefore, the non-linear operation point will at a higher bias point.

For this analysis, the optimum non-linear bias point of the base-emitter diode is first shown in figure 3.14 from the DC bias conditions. Then, the effect on the output noise by the bias is presented in figure 3.15 and indicates the shift of the 1/f noise corner and the noise floor at higher bias current densities.

The output DC current of a single pixel is shown in figure 3.14. As can be seen in the figure, the nonlinear behavior of the detector appears to be at its maximum between a 0.8-0.85 V base-emitter bias.

The output noise spectrum of two different bias points is shown in figure 3.15. The detector has been biased with a low impedance voltage generator at the shared base terminal. Therefore, most of the shot-noise base current is shorted through the external voltage generator. Through the base resistance some of this current noise converts to a voltage noise which still creates a much reduced noise floor at the collector shared terminal as opposed to a high impedance current bias, used to characterize the device corner frequency in [6, 7, 8, 9].

In the following measurements, the modulation frequency F_{CH} has been fixed to 125 kHz to characterize the detector performance for a sweep of bias points.

The R_I and the NEP versus the source chopping frequency are shown in

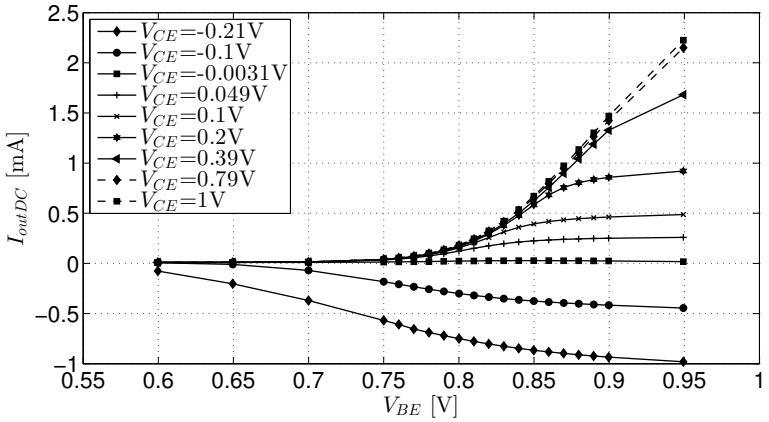

Figure 3.14: Measured DC output current of the pixel under test for different base-emitter bias voltages [3].

figure 3.16. This measurement has been done at a bias point of $V_{BE} = 0.83$ V and $V_{CE} = 1$ V. With a transimpedance amplifier of 1 MHz bandwidth, the R_I is constant for the different chopping frequencies. The NEP decreases to 50 pW/$\sqrt{Hz}$ from 100 kHz chopping frequency.

Figure 3.17 and figure 3.18 shows the measured variation of R_I and NEP for a sweep of base-emitter voltage (V_{BE}) and collector-emitter voltage (V_{CE}).

To better represent the variation of R_I and NEP, the optimized bias points are shown in figure 3.19 and figure 3.20. A maximum R_I of 1 A/W is found for V_{BE}=0.83 V and the minimum NEP of 47 pW/$\sqrt{Hz}$ is found at $V_{BE} = 0.81$ V. For $V_{CE} > 0.1$ V, the R_I is higher that 0.9 A/W for an NEP between 48-55 pW/$\sqrt{Hz}$. A harmonic-balanced simulation of the VBIC transistor model has been added for comparison to the measurement results. Unfortunately, low-frequency $1/f$ noise effect were not modeled for the used device.

The RF frequency characteristic of the detector has been verified between 0.65-1 THz. The source delivers a measured power of 1.7-11.2 µW. The NEP variation from 0.65-1 THz is shown in figure 3.21.

Ideally the square law detector circuit should respond with a 20 dB roll-off versus frequency, however, the antenna is a tuned element of the detector circuit and has a lower frequency cut-off as shown in the simulated NEP in figure 3.21. Reflections between the antenna and the detector have been estimate with a

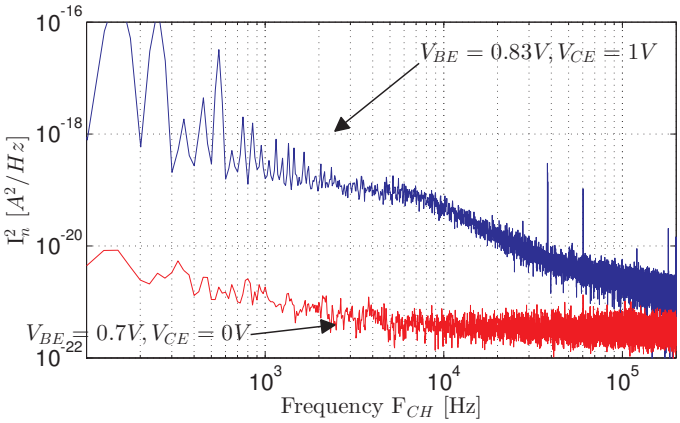

Figure 3.15: Measured output current noise spectrum of the HBT based pixel at different bias point [3].

conjugate matched detector. Simulation values rely on the device model accuracy at terahertz frequencies.

3.2.4 Section conclusion on HBT SiGe based detectors

In this section a terahertz detector based on HBT devices has been implemented in a 250 nm BiCMOS SiGe process technology. The choice of the common-base detector has bee motivated by the simulation results. The detector have been optimized to operate beyond the technology f_T/f_{max} where the nonlinearity of the HBTs base-emitter junction is used as the main detection element.

My contributions were on the characterization of the detector and the bias optimization for a high frequency operation. The minimum measured NEP was of about 50 $pW/\sqrt{Hz}$ at 0.7 THz with a bandwidth of about 200 GHz. The measurement results are summarized and compared to other detectors in table 3.1 at the end of this chapter.

The analyses of the HBT measured detector has led to consider the low frequency noise matching at the base-emitter junction to reduce shot noise and optimize the NEP.

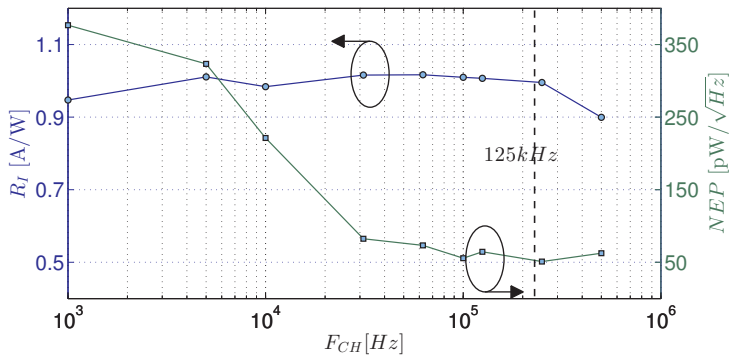

Figure 3.16: Variation of measured NEP and R_I of the HBT detector versus chopping frequency F_{CH} at a bias point of V_{BE}=0.83 V and V_{CE}=1 V [3].

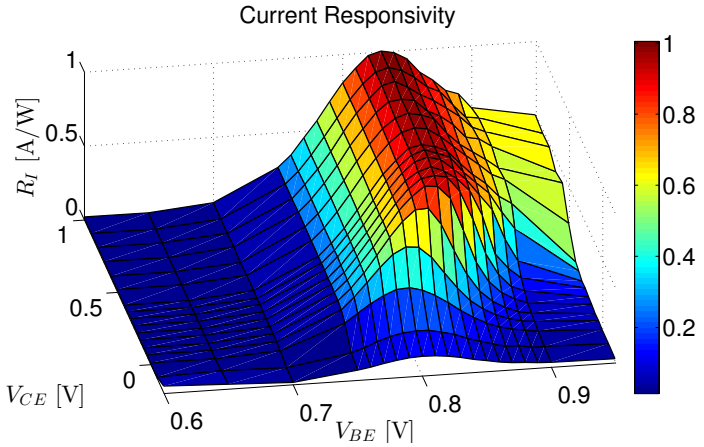

Figure 3.17: Measured R_I of the HBT detector at 0.7 THz and 125 kHz chopping frequency for a sweep of bias points [3].

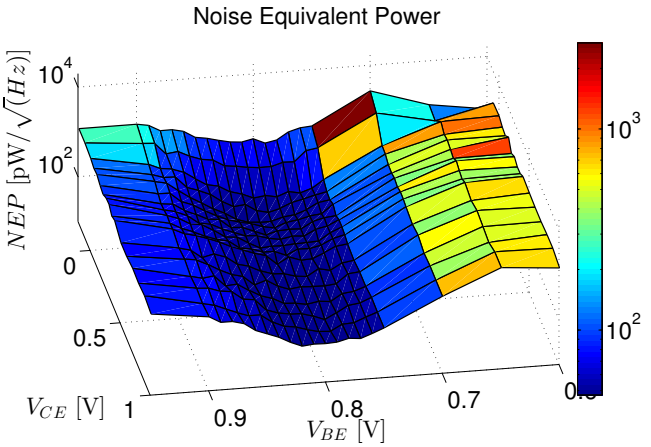

Figure 3.18: Measured NEP of the HBT detector at 0.7 THz and 125 kHz chopping frequency for a sweep of bias points [3].

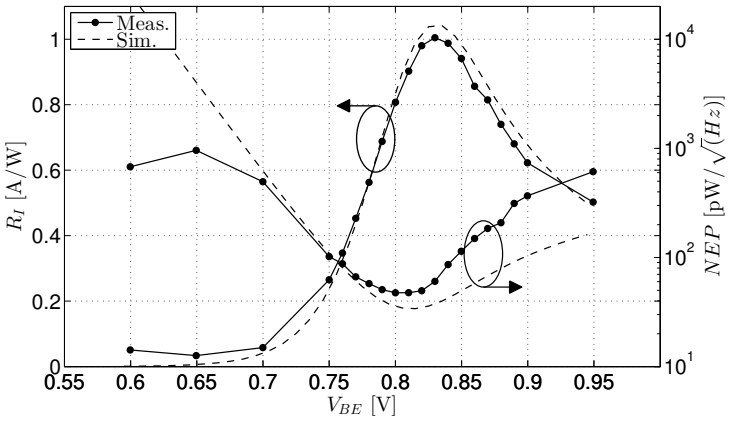

Figure 3.19: Measured R_I and NEP of the HBT detector at 0.7 THz and 125 kHz chopping frequency for base-emitter sweep and an optimized collector-emitter bias [3].

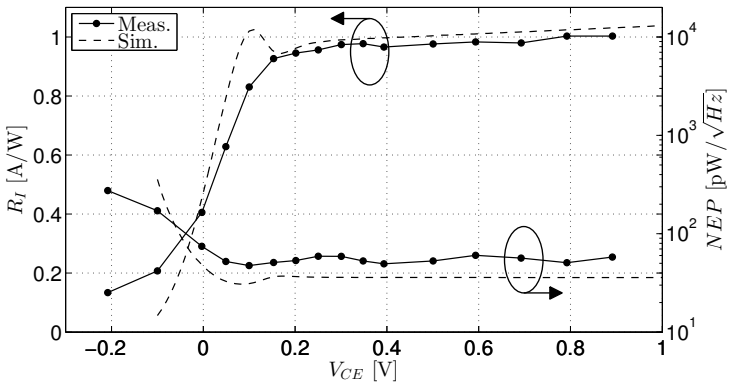

Figure 3.20: Measured R_I and NEP of the HBT detector at 0.7 THz and 125 kHz chopping frequency for collector-emitter voltage sweep and an optimized base-emitter bias [3].

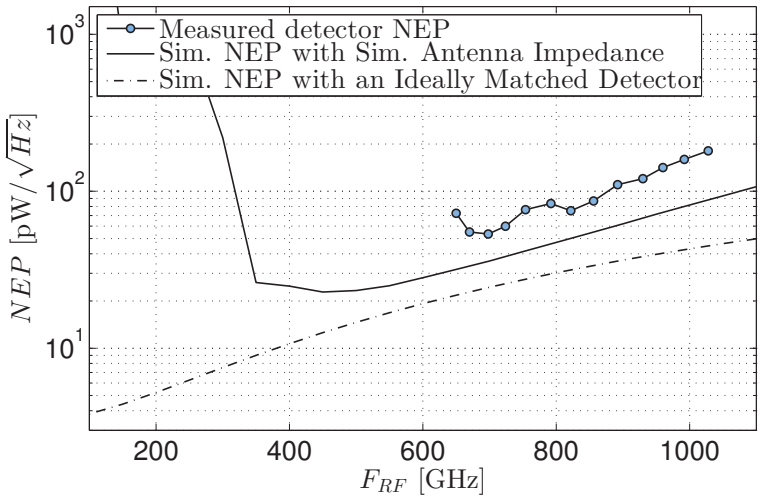

Figure 3.21: Measured optical NEP of the HBT detector at 125 kHz chopping frequency for a sweep of the terahertz source frequency from 0.65-1 THz. The simulated NEP with the antenna impedance and efficiency and an ideally matched detector are also shown [3].

3.3 CMOS based terahertz detector

The last decades CMOS technologies have been driven by various applications such as mobile phones, computers and almost all consumer electronic products. This demand is exponential and contributes to the evolution of the CMOS process to create faster, smaller and power efficient devices.

The terahertz field could greatly benefit from the CMOS process. The high integration level and the large volume possibilities are missing ingredients to the existing terahertz technologies.

As it has been presented in the introduction chapter, it is possible to build terahertz direct detectors in standard CMOS process. The non-quasi-static study of chapter 2 has shown that going to a smaller technology node would potentially improve the responsivity of such detector. In this section, an implementation of a CMOS based terahertz detector in a 65 nm CMOS bulk technology is presented.

3.3.1 Design considerations of CMOS based terahertz detector

The choice has been made to use CMOS detectors as "cold" non-biased devices to reduce $1/f$ and shot noise contributions. The design approach of an NMOS detector starts from the gate driven differential topology of figure 3.22 (a). To improve the mixing efficiency of such a detector and define the high frequency condition, a RF short can be introduces by an external capacitance as shown in figure 3.22 (b). In this section, it is proposed to connect the RF source directly to the drain of the detector pair as shown in figure 3.22 (c).

In contrast to the gate-driven approach, the proposed circuit detector of figure 3.2 (c) has the advantage eliminate the need of an RF block at the output.

To further demonstrate the validity of this design a simulation results of the different topologies is shown in figure 3.23. At low frequencies, where the transistor could potential have gain, the gate driven topology has the best responsivity performances. In contrary, at high frequencies, the device is attenuating the signal. Therefore, the gate driven circuit is not efficient. To simulate the circuit with the capacitance between the drain and the gate, a realistic value of 20 fF

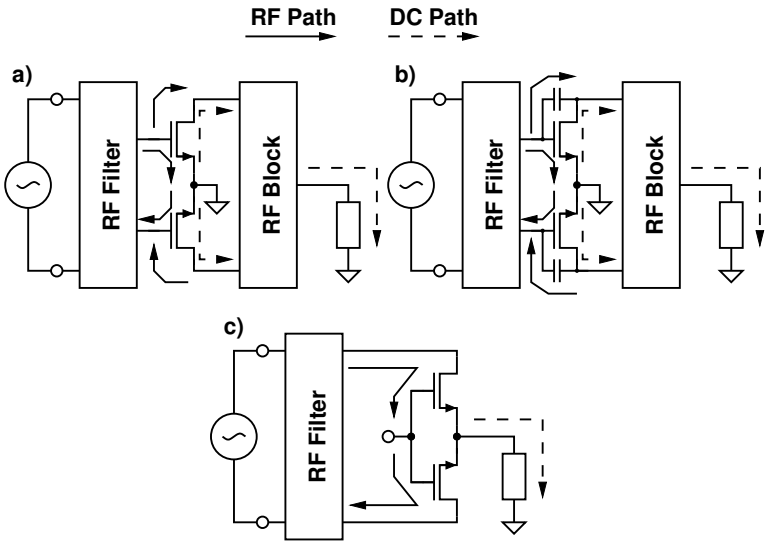

Figure 3.22: Possible differential terahertz detectors based on NMOS device.

composed of metal capacitance has been used. The drain driven approach has shown the best performance in terms of responsivity at high frequencies.

3.3.2 CMOS terahertz detector implementation

Minimum length devices have been implemented with gate dimensions of 1 μm and width of 65 nm. At the design time, the width of the devices was selected as a trade-off between high responsivity (small width) and low thermal noise voltage (large width) .

An on-chip folded dipole antenna has been implemented using the top metal layer. The antenna provides a relatively large bandwidth the high input a impedance for best responsivity results. The physical length of the dipole is 56 μm, which corresponds to a resonant frequency of 1 THz.

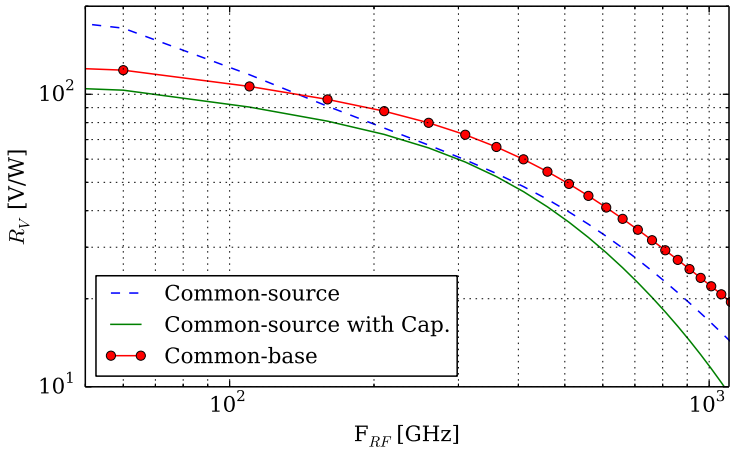

Figure 3.23: Simulated maximum responsivity of the differential detector topologies shown in in figure 3.22 (a,b,c). A conjugate matched port and ideal RF filters/blocks have been used for this simulation.

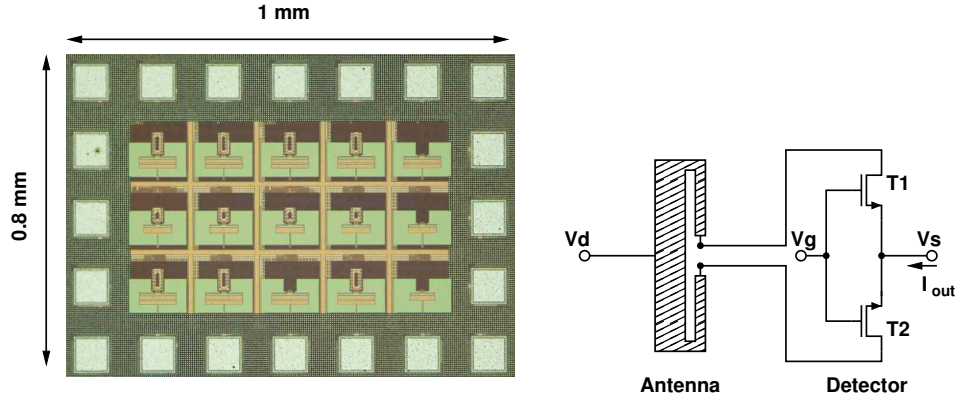

Figure 3.24: Implemented NMOS detector with dipole antenna and chip micrograph.

3.3.3 Measurement results and analysis of CMOS based terahertz detector

Different packaging condition have been explored and are illustrated in figure 3.25. The idea behind this measurement is to verify the need of the silicon lens for the designed pixel.

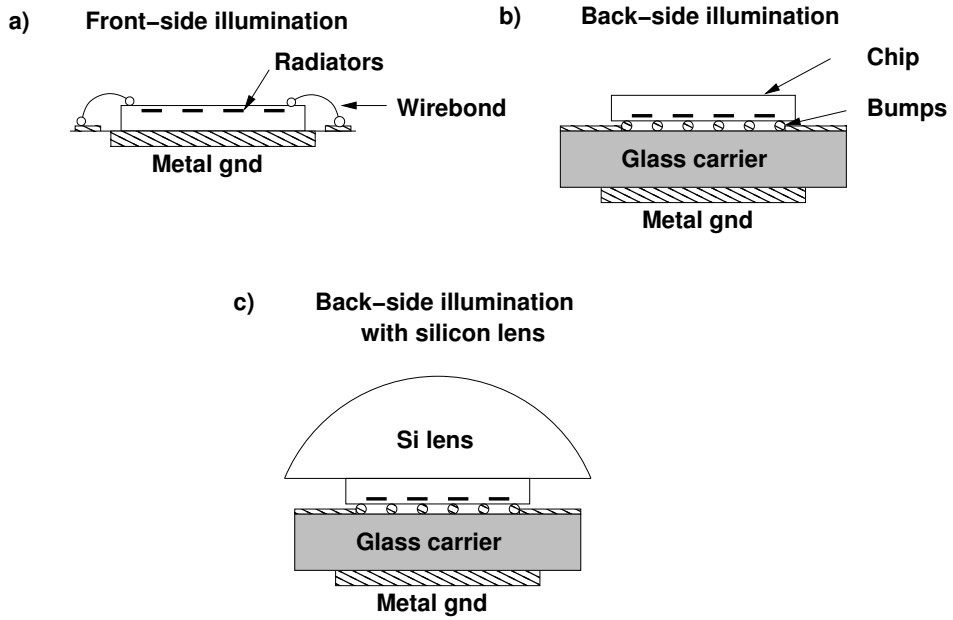

Figure 3.25: The detector chip mounted for a) front-side radiation, b) back-side through-substrate radiation, and c) coupled to an integrated lens.

The sample has been measured in back-side-illumination at 1 THz and the result is shown in figure 3.26.

The result indicate a minimum NEP of about 66 pW/$\sqrt{Hz}$. This value is dependent of substrate mode and therefore, a verification of the antenna pattern would be need.

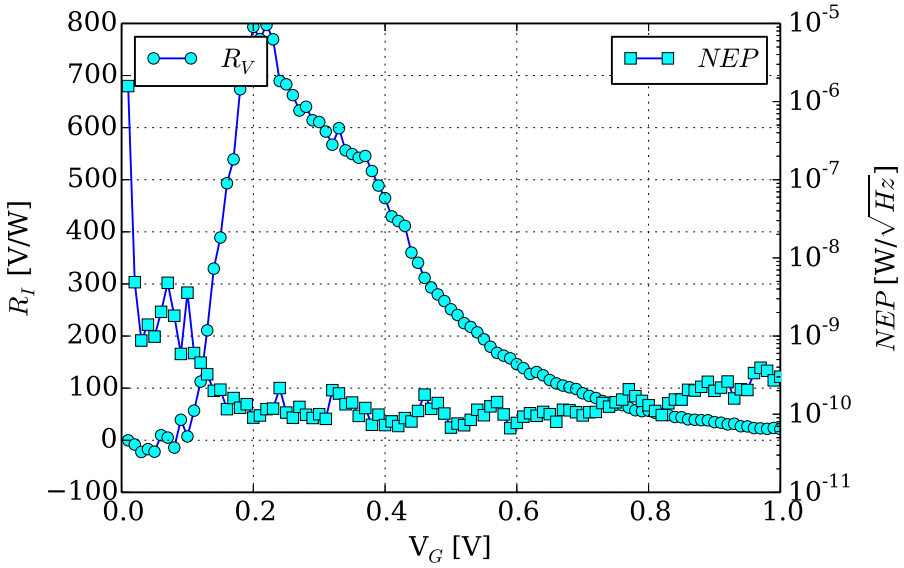

Figure 3.26: Responsivity and NEP in back-side illumination of figure 3.25 (b).

3.3.4 Section conclusion on CMOS based detectors

In this section, an experimental packaging conditions of the CMOS based detector with folded antenna have been shown. The front and back-side illumination have confirmed the need of a silicon lens for the designed antenna. This was one of the first implemented circuit during this thesis and therefore not optimized. My contributions were on the design, implementation, packaging and characterization in a team work with Hani Sherry. A comparison to other detectors is presented in table 3.1.

3.4 Schottky diode based detector

Commonly Schottky diodes are used for direct detection because of their high cutoff frequencies in comparison to standard devices [10]. The advancement in silicon technologies has enabled many semiconductor manufacturers to offer a Schottky diode in their process options with additional costs.

During this research work, an experimental Schottky diode has been offered in IHP 250 nm BiCMOS technology and has been investigated to demonstrate the functionality of the diode. It is an experimental process and design choices have been taken to evaluate the offered device.

3.4.1 Design approach of a Schottky diode detector

The differential based diode detector has been introduced in the previous chapter 2. It has the advantage to create an AC ground at the output of the detector which makes it easy to interface with conventional readout circuitry. Two possible diode connected detectors are presented in figure 3.27 (a) (b) and are the cathode and anode fed detectors. RF filters are needed in order to isolate the RF and the DC path as it has been explained in the previous analysis of this chapter.

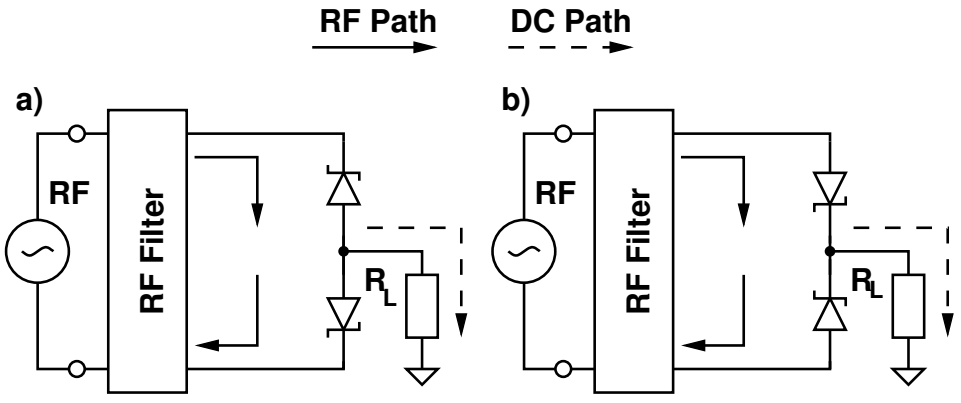

Figure 3.27: Possible differential terahertz detectors based on Schottky diode. Cathode(a) and anode (b) fed detectors are shown.

Best performance are achieved when the maximum power is injected into the diode junction. In the investigated vertical Schottky diode, the cathode is formed

by the isolation layer in contact with the substrate. On top of the cathode, the Schottky junction is processed and the anode is built. Therefore, the cathode fed circuit might have reduced performance in comparison with the anode fed. In fact, the capacitive coupling to the substrate through the cathode region reduces the RF power being injected into the Schottky junction, while being dissipated in the substrate.

To back this design choice, simulation results are shown if figure 3.28, where ideally matched devices have been used in order to compare the frequency current response of both topologies at the same bias conditions.

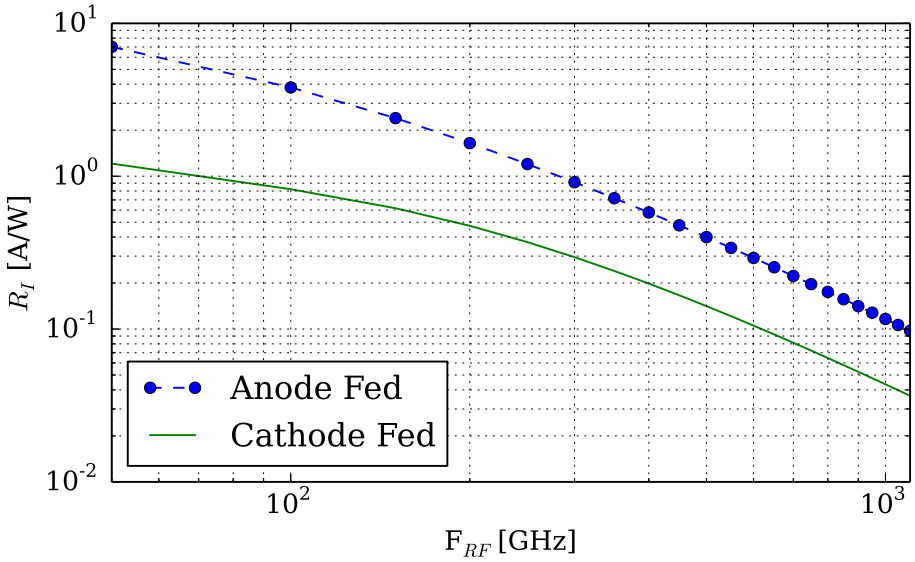

Figure 3.28: Simulation results of the two differential terahertz detectors based on Schottky diode of figure 3.27 with ideally matched devices.

The anode fed detector topology has show the best current responsivity. It has confirmed that, in the cathode fed topology, a part of the RF input power is being lost in the substrate. To further clarify this effect, a simplified cross-sectional view of the anode fed detector of figure 3.27 (b) is illustrated in figure 3.4 where charge carriers are indicated. The DC down-converted charges are extracted from the cathode.

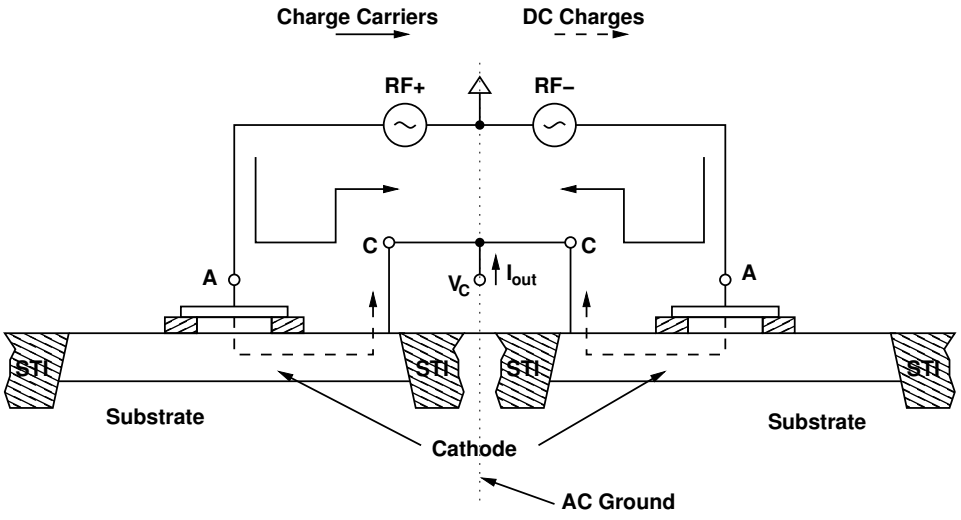

Figure 3.29: Crossectional view of the detector.

3.4.2 Implementation of a Schottky diode direct detector

From the previous design considerations on the differential diode detector, the anode fed Schottky based detector has shown better performance than the cathode fed topology because of the reduced substrate coupling. It has been selected with respect to the highest expected responsivity and implemented. The design consists of a ring antenna coupled to the anodes of the diodes and is shown in figure 3.30.

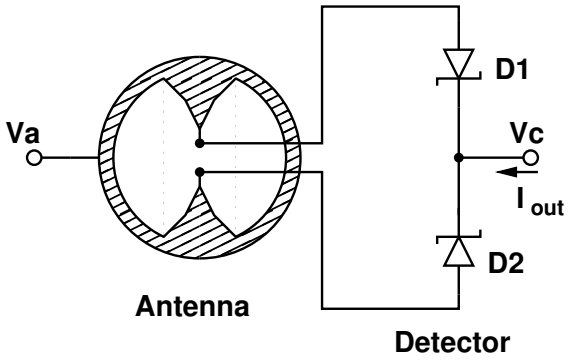

Figure 3.30: Pixel schematic of the differential anode fed Schottky terahertz detector.

With the available model in the design-kit, the simulated input impedance of the differential Schottky detector has shown a real part between 400-50 Ω and a capacitive imaginary part of 1000-300 Ω from 0.3-1.2 THz as shown in figure 3.31. Since it was an evaluation device, the choice has been made to use a ring antenna with a broad-band 100-Ω port impedance. This design choice would impact the responsivity of the detector since the matching condition were not satisfied. The detector and the antenna impedances are presented in figure 3.31.

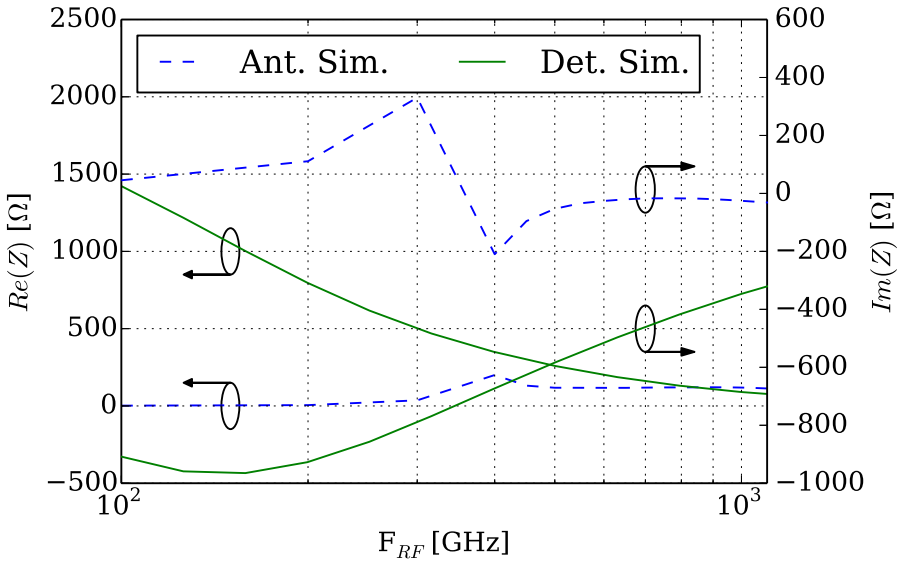

Figure 3.31: Simulated real and imaginary parts of the input impedance of implemented Schottky detector.

The pixel has been integrated in a 3×5 test-site array and fabricated in 250 nm BiCMOS technology. The chip micrograph is shown in figure 3.32 and has occupied $1times0.8$ mm^2 silicon area. The pixel size is $150times150$ μm^2. Each pixel has been connected to a separate output.

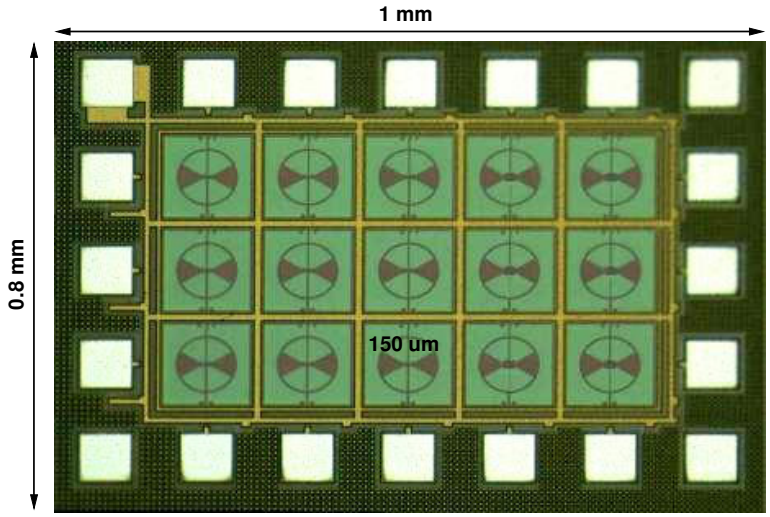

Figure 3.32: Micrograph of the manufactured chip. The detectors have been arranged in a matrix of 3×5 pixels

The chip has been glued to the back of a 3 mm diameter silicon lens.

3.4.3 Experimental results and analysis on Schottky diode terahertz detector

The diode based detector have been characterized in a free space configuration using the setup of section 3.2. For this measurement, the objective was to validate the functionality of the Schottky diode for future implementations. Therefore, it has been only characterized at 0.65 GHz. The results are shown in figure 3.33.

The peak R_I is about 0.07 A/W and the minimum NEP is around 2 $nW/\sqrt{Hz}$. In comparaison to the simulated results, the responsivity has shown good correlation. However, there is a large difference between the simulated and the measured $NEPs$. This can be explained by the noise behavior of the Schottky diode and

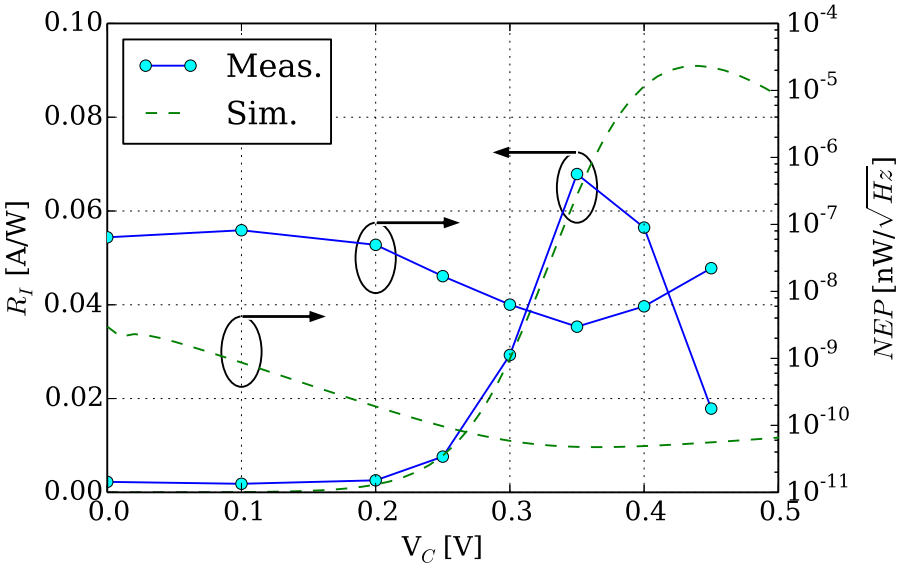

Figure 3.33: Measureed R_I

the modeling. The model did not include $1/f$ noise at that time and therefore showed only the contribution of the shot noise.

In the literature, experimental results have shown that Schottky diode $1/f$ noise corner is around few MHz, and systematically high modulation frequencies have been used to characterize the implemented detectors [10].

In this case, better performance can be expected from the implemented detector at higher modulation frequencies. For instance around 1 MHz modulation frequency, the NEP can achieve one order of magnitude better than the presented values of figure 3.33 leading to NEP values below 200 pW/$\sqrt{Hz}$.

3.5 Section on SBD detector

My contribution to this section was the verification of the functionality of the implemented SBD terahertz detector. The measured current responsivity at 0.65 THz has been of about 0.07 A/W. The NEP has been measured at 1 kHz modulation frequency , and therefore, the NEP can be further improved to at

higher chopping frequency and could potentially be below 200 pW/$\sqrt{Hz}$

3.6 Chapter summary and conclusion

In this chapter, HBT, NMOS and SBD based detectors have been explored to demonstrate terahertz detectors beyond the technology frequency limits f_T/f_{max}. The performance of different detectors are summarized in table 3.1 and compared to other implementations. This chapter has also highlighted the possibilities to make use of the silicon technology for future implementation in large number and scale.

My contributions on the HBT and SBD detectors have been the device simulations and the characterization results. Experimental results have shown that HBT bias conditions are very important to overcome certain noise contributions such as shot noise. On the CMOS process, I have contributed to design of the source fed device with Hani Sherry and the characterization.

The presented implementations can further be improved by an optimized antenna design.

Table 3.1: Performance comparison of terahertz single output detectors.

Tech.	Device	f_T/f_{max} [GHz]	max R	min NEP [pW/$\sqrt{Hz}$]	BW [THz]	Chopping [kHz]	Year	Reference
SiGe								
0.25 µm	HBT	280/435	1 A/W, 0.7 THz	50, 0.7 THz	0.65-0.85	125	2013	Sec. 3.2
								[3]
	SBD	-	0.07 A/W, 0.65 THz	2000, 0.65 THz	-	1		Sec. 3.4
	NMOS	f_T =35	80 kV/W, 0.6 THz	300, 0.6 THz	-	16	2008	[11]
0.18	HBT	240/280	18 kV/W, 0.32 THz	34, 0.32 THz	0.31-0.34	10	2013	[12]
0.13 µm	HBT	270/330	11 kV/W, 0.17 THz	10, 0.17 THz	0.16-0.17	1	2012	[13]
0.12 µm	HBT	180/220	5 MV/W, 90 GHz	2.4, 94 GHz	0.083-0.1	10	2010	[14]
CMOS								
65 nm	NMOS	160/200	800 V/W, 1 THz	66, 1 THz	0.6-1	1	2011	Sec. 3.3
								[15]
65 nm SOI	NMOS	160/200	1 kV/W, 0.65 THz	54, 0.65 THz	-	1	2010	[16]
0.13 µm	NMOS	-	1.8 kV/W, 1.05 THz	-	*0.3-1	30	2011	[17]
0.13 µm	SBD	f_T =2000	323 V/W, 0.28 THz	29, 0.28 THz	0.27-0.29	1000	2012	[10]
0.15 µm	NMOS	-	11 V/W, 4.1 THz	1330, 4.1 THz	*0.35-4.3	-	2011	[18]
Other								
YBCO	-	-	190, 1.6 THz	20, 1.63 THz	0.3-1.6	-	2011	[19]
BiSb/Sb	-	-		130, 0.8 THz	-	1	2012	[20]

*3-dB Bandwidth was not stated

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Chapter 4

Terahertz Camera Design and Implementation

Terahertz direct detectors based on silicon technologies are feasible and their performance are approaching the non-silicon based devices as it has been demonstrated in the previous chapter. However, what arouses great interest in standard silicon implementations are the large scale integration possibilities. Until now, non-silicon based terahertz detectors are more sensitive than the previously presented silicon solutions. However their production is limited in number and external discrete readout components are necessary. Unlike that, standard silicon is a commercially available and reliable technology with high integration possibilities in large scale. In other words, it is possible to integrate on the same chip the previously presented detector in a large number and make use of the technology possibilities to design a compatible on chip analog and digital circuits, with repeatability guaranty by the process for a large production volume. This is precisely what other terahertz technologies suffer from and limit their commercial development targeting hand-held devices for applications such as terahertz imaging.

This chapter is about bringing forward single detector to a highly integrated camera chip, with multi-pixel readout feature, control circuitry and implementing it in a hand-held camera device. The design challenges of such a system are numerous and described in sections 4.1. The Wold's first terahertz 1 k-pixel

camera implemented in a 65 nm CMOS bulk technology is presented in section 4.2. The circuit architecture and details on the readout electronics are given as well as the full characterization of the camera. A novel measurement method of terahertz cameras performance is also introduced. In section 4.4 an improved readout circuit with switched-capacitor in-pixel-amplifier is presented. Three different cameras have been implemented in a 0.13-µm BiCMOS SiGe technology. The presented readout circuit has the advantage to be usable for any type of terahertz direct detector offered in this technology.

4.1 Design challenges of a large terahertz camera in silicon technologies

The design challenges of a terahertz camera system are multiple and start with the pixel response to the terahertz waves. At terahertz frequencies, the responsivity to an input power is very limited. In fact, the efficiency of such detractor requires additional components to amplify the converted signal and distributed over the readout network.

To achieve this, in pixel amplifiers are required with low noise contributions. Further more, in a camera system, the readout path of the signal is also sensitive to noise contribution from the switching elements such as the analog multiplexers.

In order to overcome these issues, the design of a terahertz camera requires low-noise, high-gain to buffer and multiplex the collected signals over the chip.

4.2 First 1 k-pixel CMOS terahertz camera

The first 1 k-pixel CMOS terahertz camera chip has been design and implemented in a teamwork effort. The following subsections describe the camera circuit design in a 65-nm CMOS process technology from STMicroelectronics in detail.

4.2.1 Circuit architecture

The readout circuit scheme of the NMOS terahertz detector makes use of the detector circuit to reset itself at a reference voltage. It has the advantage to reduce the number of elements connected to the detection node.

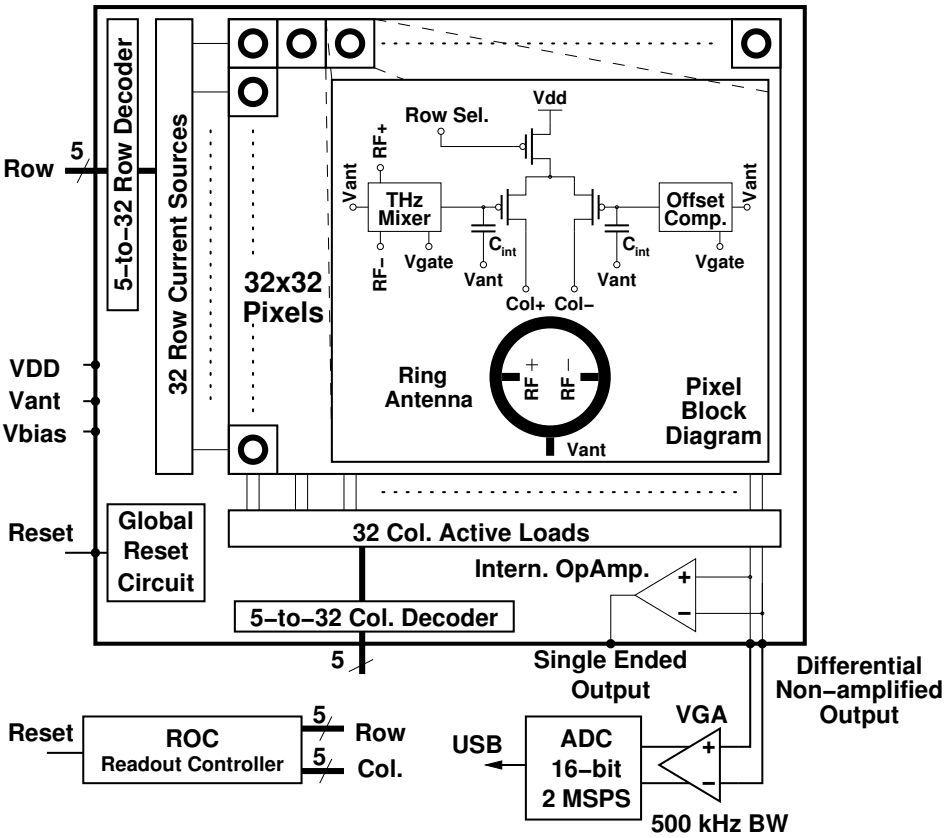

Figure 4.1: Block diagram of the camera chip. Externally required components are indicated as appropriate [1].

The imager architecture follows a global shutter readout scheme as indicated in the array block diagram in figure 4.1. Each active pixel consists of a detector, a reset circuit, an integration capacitor and a blind pixel for offset compensation, both followed by a differential amplifier.

Each row of the array is biased up at a time and columns are selected by a row/column decoder, which is controlled by an external programmable logic device (CPLD) located inside of the camera module. The multiplexed signals

of the array can either be read differentially before an on-chip buffer amplifier or single-endedly. The camera chip is packaged in a compact module with an external analog-to-digital converter (ADC) powered via a universal serial bus (USB). The digital video stream may be displayed on a computer by a dedicated video capture software.

4.2.2 Detector front-end and reset circuit

The detector consists of an on-chip ring-antenna as shown in figure 4.2, feeding a differential NMOS detector pair with a minimum gate length of 60 nm. The detector transistor may be seen as a current source in parallel with the channel conductance of M1 and a C_{int} integration capacitor. The integration/reset time constant, therefore, can be controlled by the voltage level of the reset signal applied to the gate of M1. The camera was designed for 25 fps. Although, this leaves sufficient time for integration (40 ms per frame), the required integration capacitor would be too large to be integrated on chip. The available pixel area only fit an integration capacitor $C_{int} = 8$ pF with an integration time constant of about 0.1 μs.

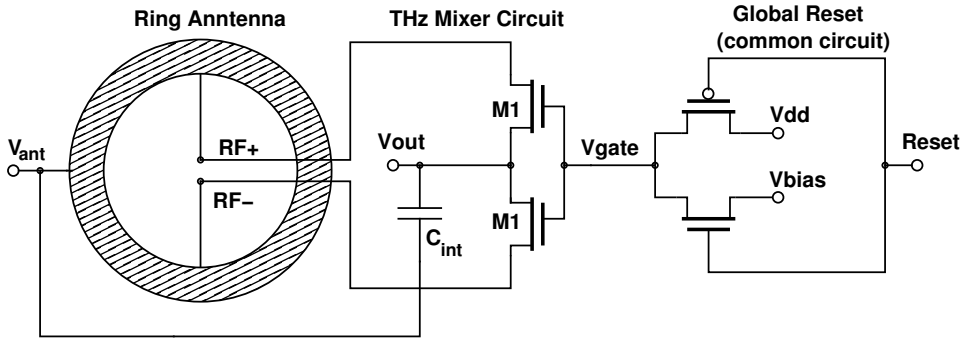

Figure 4.2: Single pixel terahertz mixer schematic with its ring antenna and reset circuitry [1].

4.2.3 Readout circuit

In terms of the readout circuit design, the key challenge is to achieve low power consumption levels without scarifying the responsivity and noise equivalent power.

An active pixel circuit provides noise immunity and in-pixel amplification. In order to lower the average power consumption per pixel, only the in-pixel amplifiers of a single row are activated at a time.

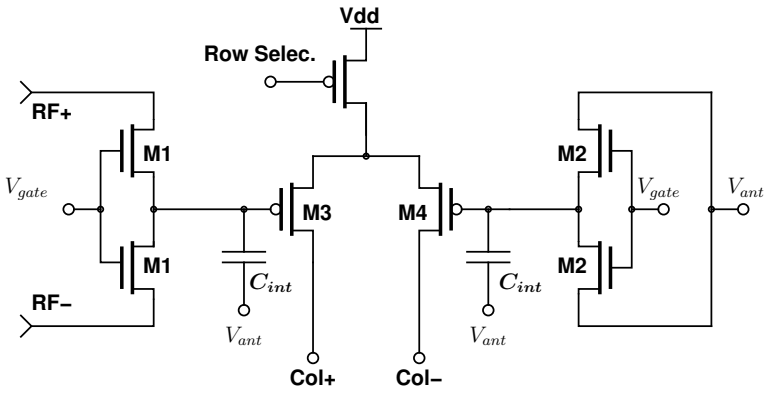

Figure 4.3: Pixel circuit with detector, blind detector circuit and differential cascode stage [1].

Figure 4.3 shows the circuit schematic of the active part of a pixel circuit. The row select signal is being shared among a row of pixels, whereas the Col± signal is shared among a pixel column. The detector transistor M1 is followed by a readout transistor pair M3/M4 acting as a differential pair with an attached offset compensation circuitry (blind reference pixel). The blind reference pixel circuit is not connected to an antenna, and therefore, is used to produce a reference potential for offset compensation of the differential pair stage operated in open-loop. The gate bias of the transistor pair M3/M4 is provided by V_{ant}. This voltage is applied either through the active pixel or through the blind reference pixel. In the case of M3, this bias voltage is further applied through the common node of the antenna.

An operational amplifier with DC-offset compensation is designed to drive capacitive load at the output such as ADC or an additional buffer.

4.2.4 Array implementation and circuit layout

Figure 4.4 shows the block diagram of the digital selection unit. The row and column selection is realized by using 5-bit addresses for row and column selection. Two auxiliary enable signals switch decoders off during the charging period of the integration capacitors. A single row is biased up at-a-time and the differential pairs in each column share a common active load (M6-M7) providing a simulated open-loop gain of 50 dB per pixel. A digitally controlled multiplexer selects a single pixel to be further buffered by a unity-gain amplifier. This readout scheme enables parallel operation of 1024 pixels, while the readout circuitry activates only a single row (32 elements).

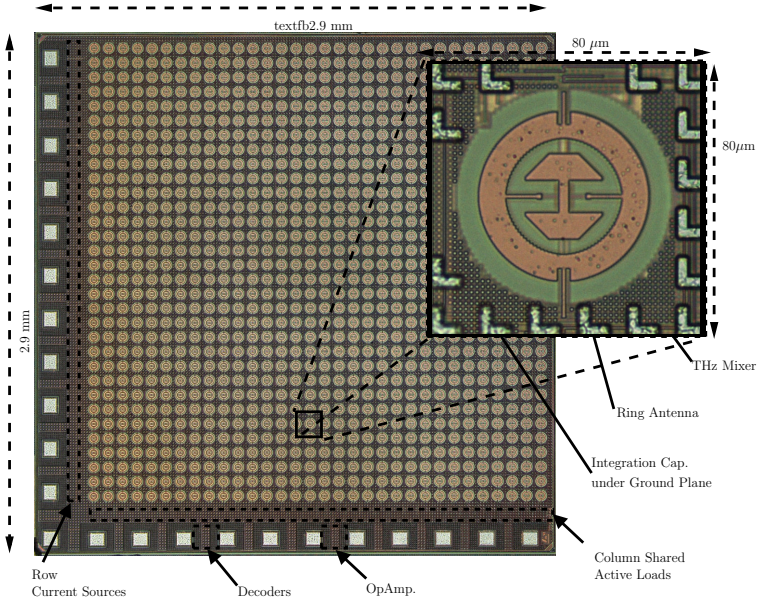

Figure 4.4: 32x32 FPA chip complete die micrograph (2.9×2.9 mm^2) and a single detector topography (80×80 μm^2).

The array micrograph is presented in figure 4.4. The die size is 2.9x2.9 mm^2.

4.2.5 Camera module design

The terahertz camera, shown in figure 4.5, is packaged in a 5×5×3 cm^3 metal box to demonstrate low-power and low-cost packaging solutions for hand-held

applications. It is connected to the data acquisition board via a single 8 wires RJ45 cable. It consists of a silicon lens attached to the chip back-side, a readout controller (ROC) implemented in a complex programmable logic control device (CPLD) driven by a clock generator (CLK), a low noise variable gain amplifier (VGA) and a regulated power supply as presented in figure. 4.6. All components are mounted on four assembled printed circuit boards (PCB) as shown in figure 4.5. The total power consumption of the camera module is 280 mW and the VGA gain was set to 5 dB with a 500 kHz video bandwidth for all measurements reported in the next section.

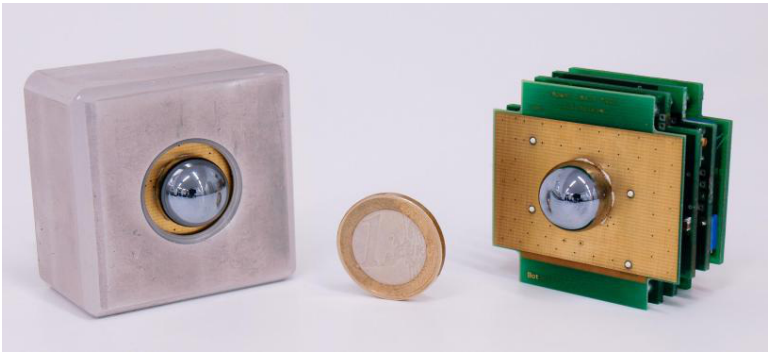

Figure 4.5: Picture of the terahertz camera module with and without its housing. A 1 Euro coin is placed in between for size comparison [1].

The analog output of the compact terahertz camera was sampled with up to 2 MSPS by an external 16-bit ADC and was sent to a computer via a USB to be displayed on a screen. The developed software displays a three dimensional graphic in real time of the streamed data as shown in the demonstration setup figure 4.7. It enables basic image processing of the video stream starting with a dark calibration frame for fixed pattern noise reduction.

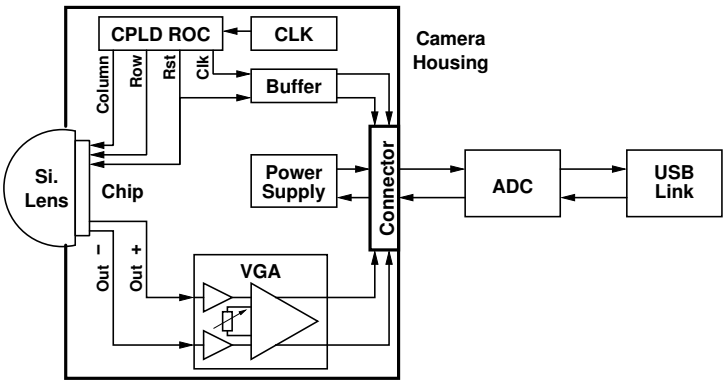

Figure 4.6: Camera module block diagram indicating the cameras readout controller (ROC) and the analog buffer circuitry. The VGA was set to a 5-dB gain followed by a low-pass filter with a 500-kHz video bandwidth. Note that all results described in the next section are based on this camera hardware [1].

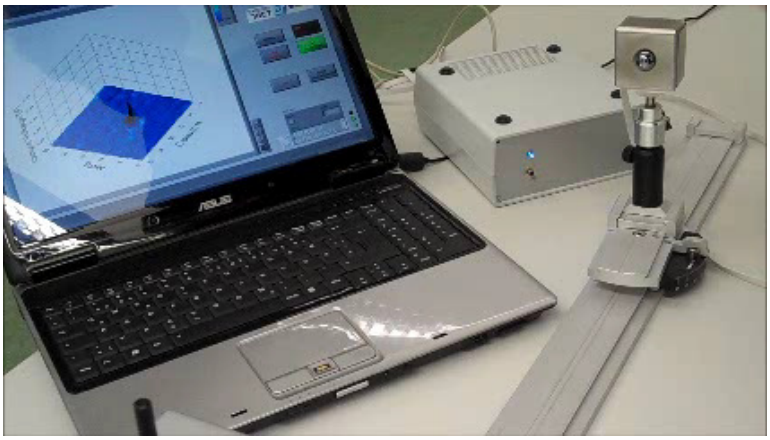

Figure 4.7: Camera module operating in active illumination setup. The analog output of the camera is sampled by the external ADC and sent to the computer where the 1024 pixel video stream is displayed [1].

4.2.6 Characterization results of the first 1 k-pixel terahertz CMOS camera

The 1 k-pixel terahertz CMOS camera can be operated in video mode or single pixel output. In video mode, switching noise and other operation artifact should be characterized. Therefore, a direct method of camera characterization is proposed in the first part of this subsection. However, for comparison with other terahertz devices, a single pixel performance is shown in the second part.

4.2.6.1 Characterization in video-mode

A direct method of camera characterization at video-rates is shown in figure 4.8. A continuous-wave (CW) source without modulation illuminates the camera. A Polytetrafluorethylen (PTFE) lens, with a focal length (f) of 10 cm, is placed in the center distance between the source and the camera (S=15 cm). The terahertz beam is focused onto the silicon lens in order to ensure that all the available source power is projected onto the silicon lens aperture. At 0.86 THz, a 6 μW of power was measured with an absolute-power after the PTFE lens and in front of the camera module.

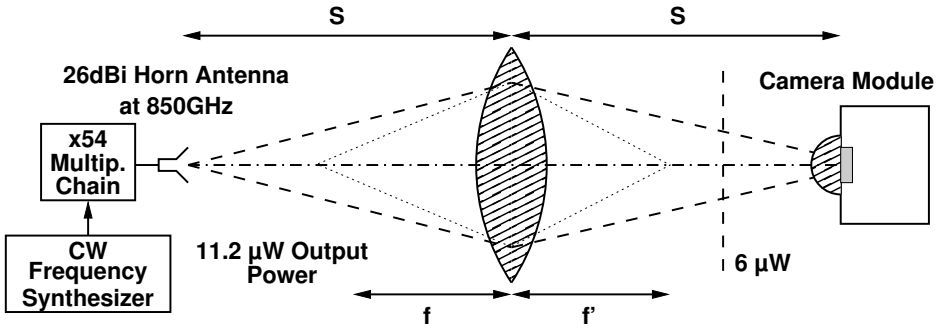

Figure 4.8: Characterization set-up for video-mode. The readout controller (ROC) is active and the terahertz source is operated in continuous wave mode [1].

In this setup, the beam splits over some, but not all, pixels of the FPA. The camera responsivity R_v can be calculated as the sum of the array response divided

by the total available input power as

$$R_v = \frac{\sum_{pix=1}^{1024} V_{pix}}{P_{in}}. \tag{4.1}$$

In this video-mode, the noise is integrated over the full 500-kHz video bandwidth. The NEP_{total} is calculated from the measured RMS image noise $V_{N,total}$ divided by the camera responsivity from equation. 4.1 as

$$NEP_{total} = \frac{V_{N,total}}{R_v}. \tag{4.2}$$

The NEP_{total} presents an average over more than one pixel, and therefore, includes pixel-to-pixel variations. The NEP per $\sqrt{Hz}$ can be calculated from the analog video bandwidth (BW) of the camera module as $NEP{=}NEP_{total}/\sqrt{BW}$. However, this supposes a flat noise power spectral density.

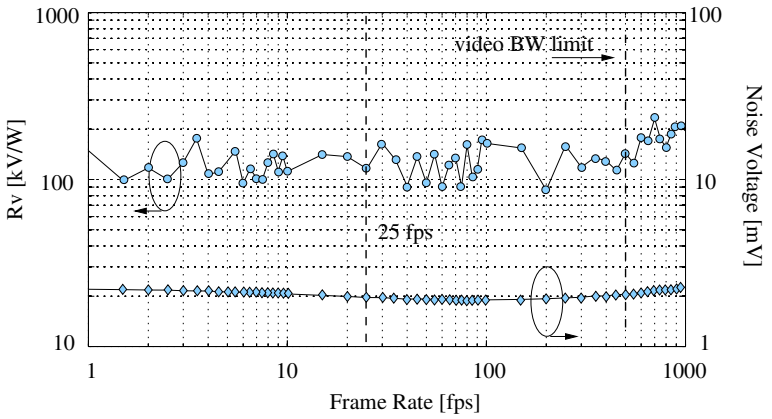

Figure 4.9: Measured R_V at 856 GHz and the measured RMS image noise $V_{N,total}$ of the camera module versus frame rate. The data includes a VGA gain of 5-dB [1].

Figure 4.9 shows the measured camera R_v at 0.86 THz including the measured RMS image noise $V_{N,total}$ for 1-1000 fps. Note, that in this measurement R_v stays about constant up to the video bandwidth limit. Beyond 500 fps R_v increases and the $V_{N,total}$ drops down which is a measurement artifact because the fame rate is

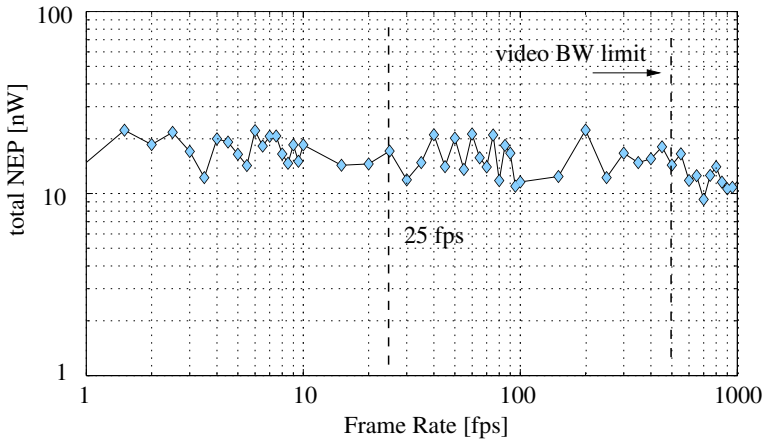

Figure 4.10: Measured NEP_{total} at 856 GHz of the camera module versus frame rate [1].

beyond the video bandwidth. From 1-500 fps the camera's R_v is about constant within 100-200 kV/W. Note that this data includes a 5-dB VGA gain and was taken for a detector bias at minimum NEP. The camera NEP_{total} measured at 0.86 THz for 1-1000 fps is shown in figure 4.10. From 1-500 fps the camera's NEP_{total} is about constant within 10-20 nW and drops down beyond the video-bandwidth which is again a measurement artifact. At 25 fps the R_v is 115 kV/W and the NEP_{total} is 12 nW.

This measured NEP_{total} refers to the integrated noise over the camera bandwidth and can not be compared to the single pixel operation where the terahertz source would be modulated. However, a correlation between the two operation modes exists. In other words, a design leading to the best single pixel performance would lead to an enhanced NEP_{total} in video mode.

4.2.6.2 Single pixel characterization in lock-in-mode

In this second part of the characterization subsection, pixels are measured by lock-in technique. The readout controller (ROC) is switched off and the pixel under test is permanently selected.

Unlike the total NEP_{total} method presented in the previous subsection, this method requires accurate specifications of the source antenna gain, the receiver

directivity and further requires precision alignment in the far-field of the high-gain receiver antenna.

The source antenna characteristics has been covered the the previous chapter. The antenna directivity study has led to the conclusion that the lens area should be used as a conservative estimate of the antenna directivity. This corresponds to a D_{RX} of 40.2-44.2 dBi for a 15 mm diamiter silicon lens between 0.6-1 THz.

The measurement setup is similar to the one used in the previous chapter and is shown in figure 4.11. A frequency synthesizer (12-19.4 GHz) was AM modulated with a 100Hz-to-5kHz square-wave. The signal was then multiplied by 54 to generate a pulsed 650-to-1028 GHz signal with an output power in the range of 1.7-11.2 μW. A spectrum analyzer was used to observe the pixel output voltage and the spot-noise at the modulation frequencies.

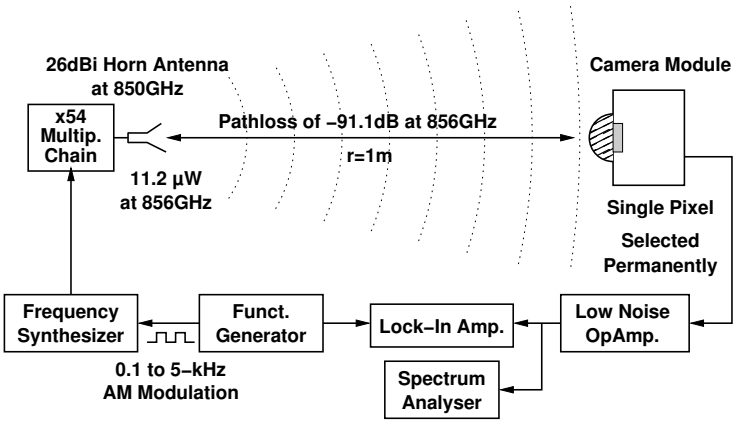

Figure 4.11: Characterization setup for pixel by means of lock-in techniques according to Friis transmission equation The ROC is off and the terahertz source is modulated (none-video mode) [1].

The R_v and NEP were measured at various detector bias points and chopping frequencies across the 0.65-1 THz frequency band. Figure 4.12 and figure 4.13 show the R_v and the NEP data at 0.856 THz for V_{bias} from 0.8-1.8 V and chopping frequencies from 100-5000 Hz (including a 5-dB VGA gain).

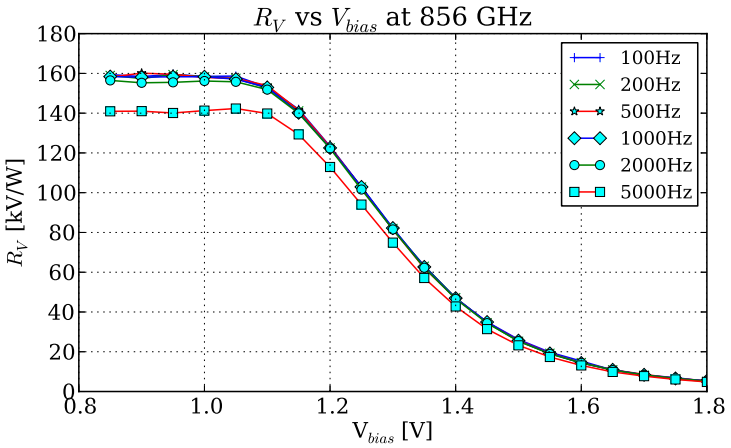

Figure 4.12: Measured camera R_v at 0.856 THz versus gate bias and at 1 meter distance from the source for different chopping frequencies. The data includes a VGA gain of 5-dB.

At a 5-kHz chopping frequency, the minimum NEP is 100 pW/$\sqrt{Hz}$ at a 1.25-V V_{bias} and the maximum R_v is 140 kV/W. The R_v includes 5-dB gain of the camera module and the NEP includes thermal detector noise, additional noise from the in-pixel cascode stage, the active load and current sources, however, they are not representative of the camera in operation.

From 0.65 THz up to 1 THz the maximum R_v and the minimum NEP are presented in figure 4.14 and figure 4.15 for different chopping frequencies. The -3 dB bandwidth is about 200 GHz. The pixels can operate beyond the characterization frequencies. The shown results are limited by the available measurement equipment to go at higher frequencies.

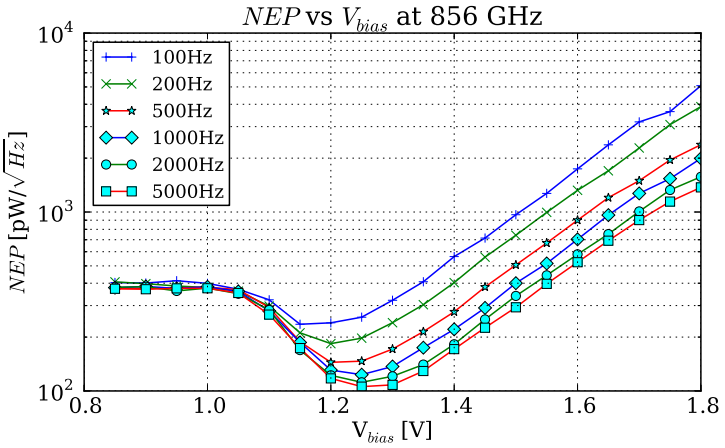

Figure 4.13: Measured NEP at 0.856 THz versus gate bias at 1 meter distance from the source for different chopping frequencies.

4.3 Section conclusion on the CMOS terahertz camera

In this section, the world's first 1 k-pixel CMOS based terahertz camera module has been presented. It demonstrates a real implementation of a hand-held terahertz device. My contributions are mainly on the charcterization of the camera module and the system implementation. I have also participated to the design of the camera circuit more specifically on the readout amplifier, the active load and analog switches.

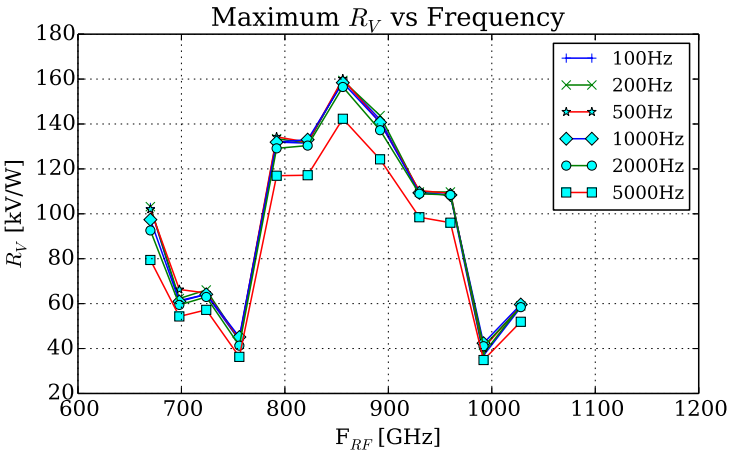

Figure 4.14: Measured maximum R_V versus frequency at 1 meter distance from the source for different chopping frequencies. The data includes a VGA gain of 5-dB.

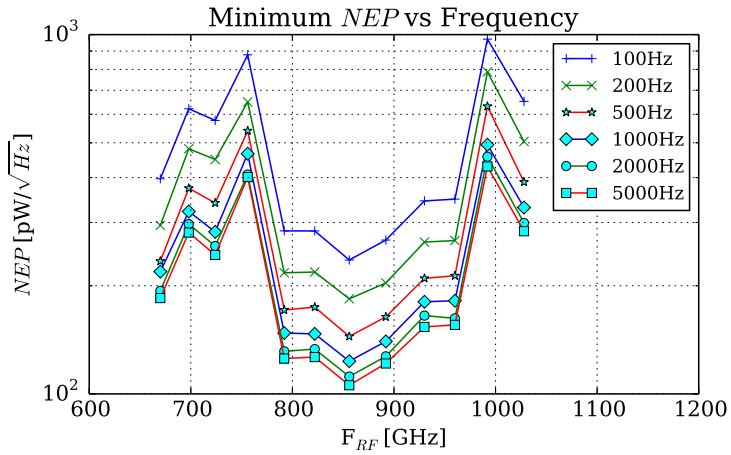

Figure 4.15: Measured minimum NEP versus frequency at 1 meter distance from the source for different chopping frequencies.

4.4 Readout circuit improvement for scalable terahertz cameras

The previously presented terahertz camera circuit was the World's first terahertz CMOS implementation. It has been considered as state-of-the-art device in the scientific community. However, it has been designed for CMOS based detectors and can not support other detector device such as Schottky diodes.

In this section, a camera chip circuit in 0.13 µm BiCMOS SiGe technology is presented. The readout circuit has the advantage to be compatible with the available detector implementations in this technology. Three variations of the terahertz camera chip have been designed. The cameras are based on CMOS and HBT square-law direct detectors. One camera chip consists of a bipolar detector array with a tuned antenna center frequency around 0.6 THz. The two other designs are based on CMOS detectors with a variation on the antenna center frequency.

4.4.1 Circuit architecture and readout

The readout circuits of the three arrays have been designed in the CMOS part of the technology. The main target of the design was to build a compact readout electronics that can be compatible with both types of detectors (CMOS and HBTs) and can be adapted to other type of detectors such as Schottky diodes for instance. The other important design challenge was to build the arrays as a building block with the pixel count as a parameter. This would give the flexibility to build any array pixel count, without the redesign of the digital or analogue parts, within the limits of the readout circuit speed.

Therefore, a synchronous shift-register control logic has been implemented for rows and colums to select a specific pixel. Figure 4.16 shows the circuit block diagram of the implemented array. One row is selected with the vertical shift register while one column is connecting one pixel at the time to the analogue output buffer. The row digital circuit controls the biasing network of the in-pixel amplifier.

The in-pixel readout circuit is show in figure 4.17. As mentioned before,

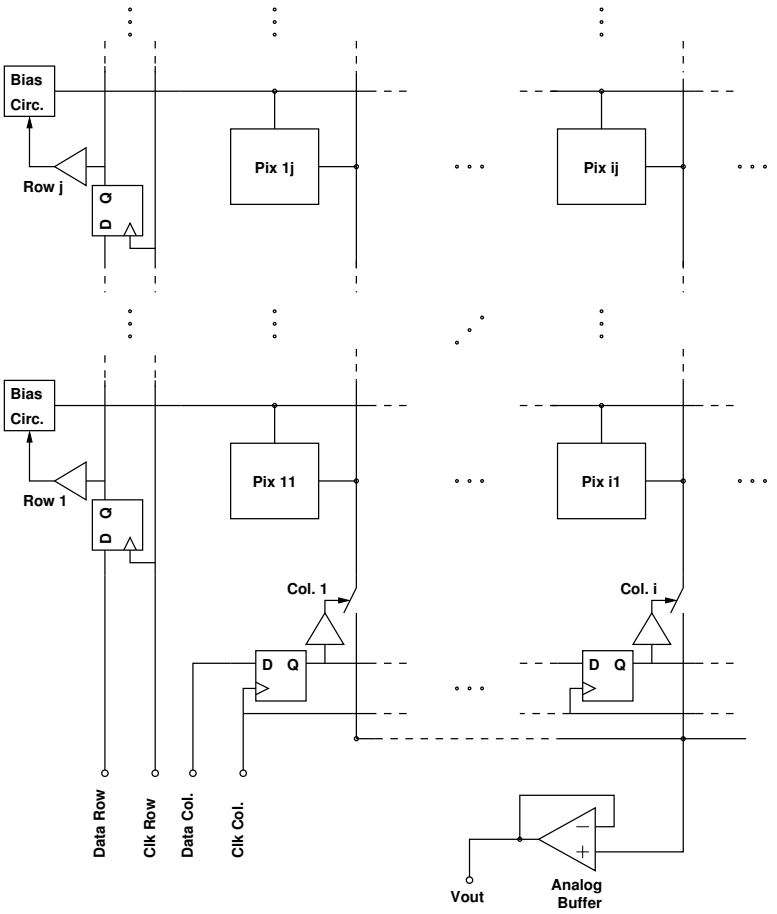

Figure 4.16: Scalable terahertz camera block diagram.

the circuit has been designed in the perspective to interface any terahertz direct detector delivering a DC voltage or current proportional to the detected RF power. The circuit is based on switched-capacitance integrator. It is necessary to have a reference or blind pixel for minimizing DC offsets. Since the core circuit of the detector without the antenna is very small (a pair of minimum size device), it is very convenient to integrate a reference detector per pixel. However, it would be possible to have one reference pixel per row. This solution would reduce power consumption if the detector has to be biased with a current for instance. The reset of the pixel happens at the amplifier circuit and do not effect the detector bias.

The readout and amplification of the detector happens at the pixel amplifier.

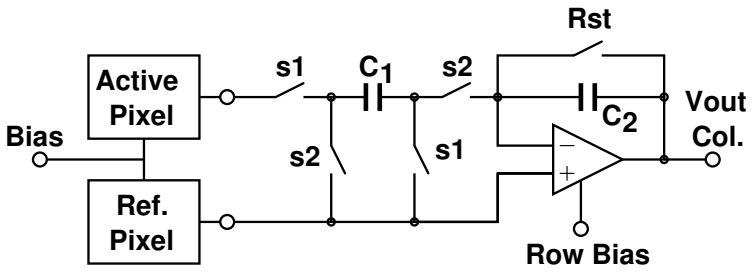

Figure 4.17: In pixel switched capacitance amplifier for scalable terahertz camera chip.

It consists of two capacitances, an amplifier and five analog switches. Before going through the analysis of the amplification process, the capacitance are assumed to be discharge and all switches open.

The capacitance C_1 is first charged by closing the switches $s1$. In switched capacitance circuits, this step is often called sampling. After sampling the DC voltage at the pixel, the switches $s1$ are open again. At that time, the charges on the capacitance are invariant. Then switches $s2$ are closed. At that moment, charges are transfered from the capacitance C_1 to C_2. The amplifier will deliver the necessary charges to bring the circuit to a new stable position. Now if the capacitance C_2 happens to be smalled than C_1, and the amplifier would have enough gain to compensate the charges on C_2, the voltage gain of this circuit can be write as

$$A_v = \frac{C_1}{C_2}, \tag{4.3}$$

Now, if the previous step is repeated without switching on the reset Rst, the charges would accumulate on the capacitance C_2 resulting in an amplification of the pixel response. A low-pass filter is then needed in order to mitigate the switching effects.

To clarify that, a simulated response of a 5×4 pixel array is shown in figure 4.18. This time domain simulation validate the functionality of the pixel amplifier and the digital control circuit. Pixel (2,1) and pixel (3,2) being active emulated to be active.

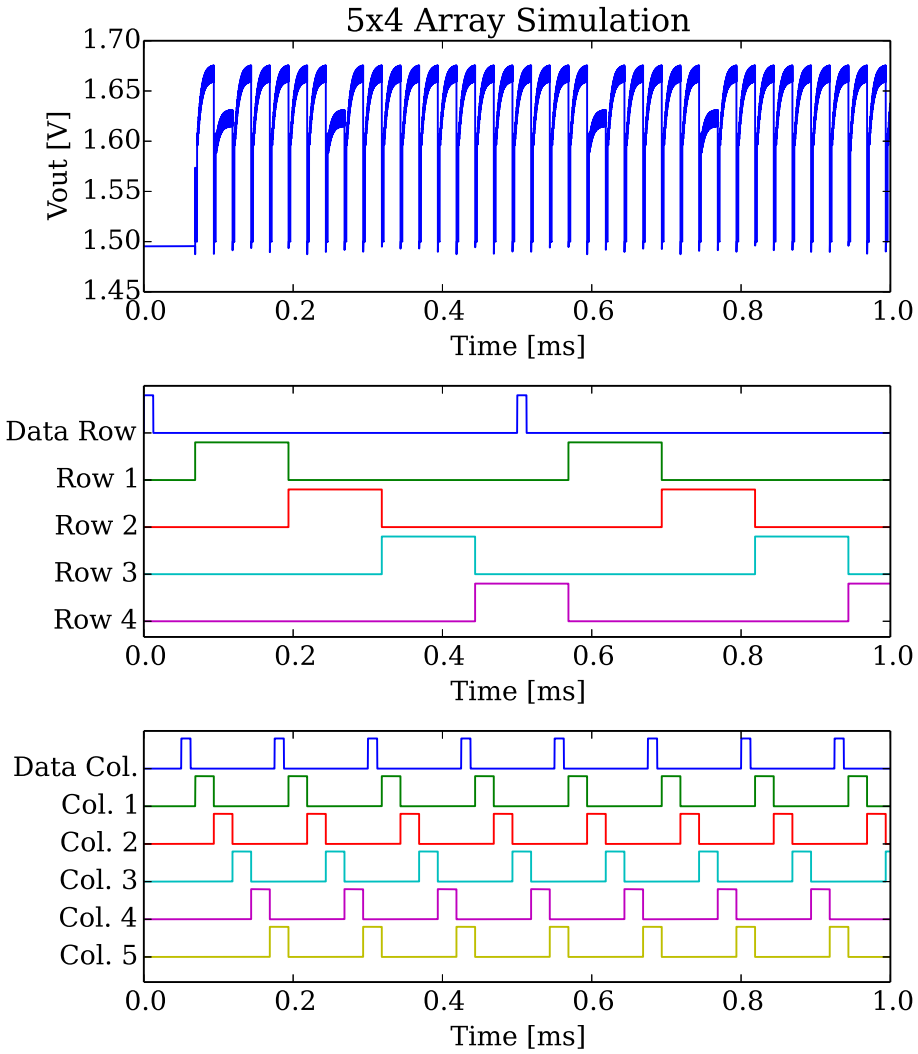

Figure 4.18: Simulated time diagram of a 5×4 array. The analogue output is first shown, then row and column digital control simulated results are presented.

4.4.2 Circuit implementation

The circuit implementation has the advantage to be re-used without the redesign of the pixel readout and is compatible pixels as small as 80x80 m2.

The antenna area is the most space consuming component of the design. The active detector is located in the center of the pixel and feed by the differential antenna. The reference pixel is shared by one row and located at the beginning of the row (at the left of the corner pixel). The choice to share the reference pixel has been motivated by the reduction of the array power consumption. The biased detector has a power consumption of about few hundred of micro-amperes. The flexibility of the readout circuit has enabled easy re-design of the array.

4.4.3 Chip packaging and camera module design

The chip layout of the different cameras has been chosen to implement several chip in the same package. Since the integrated antennas of different detectors have to radiate through the substrate and a silicon lens, up to four camera chips can be packaged on the same lens as presented in figure 4.19. With the CMOS implantation layout, this packaging option can achieve up to 2.5 kpixel resolution. The control circuit of the module would control simultaneously four chips.

4.4.4 Section conclusion on improved readout circuit

In this section, an implementation of a novel terahertz camera with in-pixel amplifier has been presented. The design can be adapted to various detectors. Three implementations have been realized in a 0.13-µm BiCMOS technology. The presented packaging solution can combine several chips with a 2.5-kpixel resolution.

This implementation has not been measured at the submission of this thesis.

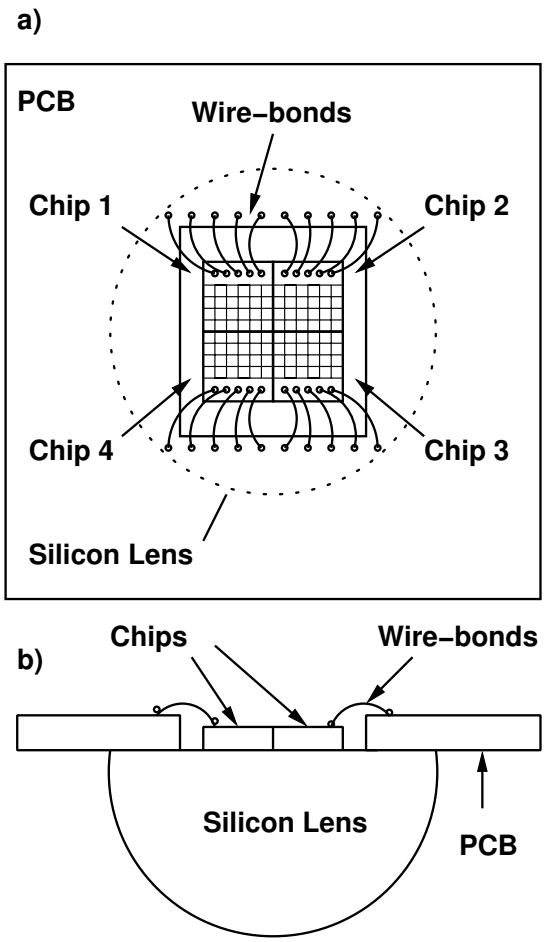

Figure 4.19: Combination of four camera chips in one packaging configuration.

4.5 Chapter summary and conclusion

In this chapter, the world's first CMOS terahertz camera module have been presented. The camera has been packages in a hand-held low-power device. Another implementation in BiCMOS technology present the advantage to be flexible and can support a high number of pixels.

My contributions to the first CMOS camera is on design of analog switches and the output amplifier. I have contributed to the integration and characterization of the full camera module including visualization software.

As it will be seen in the imaging demonstration chapter, the need of a real-time camera for active terahertz system is a great advantage.

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Chapter 5

Terahertz Source Array Control Circuit

Terahertz sources are necessary for active terahertz systems in silicon technologies as it has been presented in the previous chapters. Electronic terahertz source are currently dominated by waveguide based technologies with a limited radiated power per element. To overcome the power limitation, a combination of sources can be imagined. However, the current technologies are expensive to produce and their size can be a limiting factor for a large number of elements. Recently, terahertz sources with an output power approaching the milliwatt have been demonstrated in standard silicon technologies [1, 2, 3, 4]. They are based on compact harmonic oscillators and make use of standard devices. They could benefit from the large scale properties of the silicon technology to integrate a large number of elements. In such a system, a control circuit is necessary to select different elements in large arrays. This would lead to save power consumption and control lightning condition for imaging system for instance.

In this chapter, the control circuit of a 4×4 terahertz source designed in a 0.13-µm BiCMOS SiGe technology is presented. The architecture of the source array and details about the control circuit design and implementation are given in section 5.1. Then, characterization results and analyses are presented in section 5.2.

5.1 Control circuit of the terahertz source array

5.1.1 Source array architecture

Terahertz sources based on compact harmonic oscillators are very promising for delivering high power radiation at terahertz frequencies for imaging application[1, 5, 6]. Their compact size in comparison with multiplier chains is their main advantage [7]. The challenges of such systems are the total radiated terahertz power, the frequency of operation and the DC power consumption.

Power combining techniques [3] have been used to increase the total radiated power of such oscillator, and harmonic frequency generation to achieve terahertz oscillation frequencies. However, the power efficiency of such oscillators are in the order of 1.4 ‰ [5]. To achieve reasonable power consumption for large arrays, a control circuit is mandatory to reduce power consumption over a large circuit and offer programmable diversity for active terahertz imaging systems.

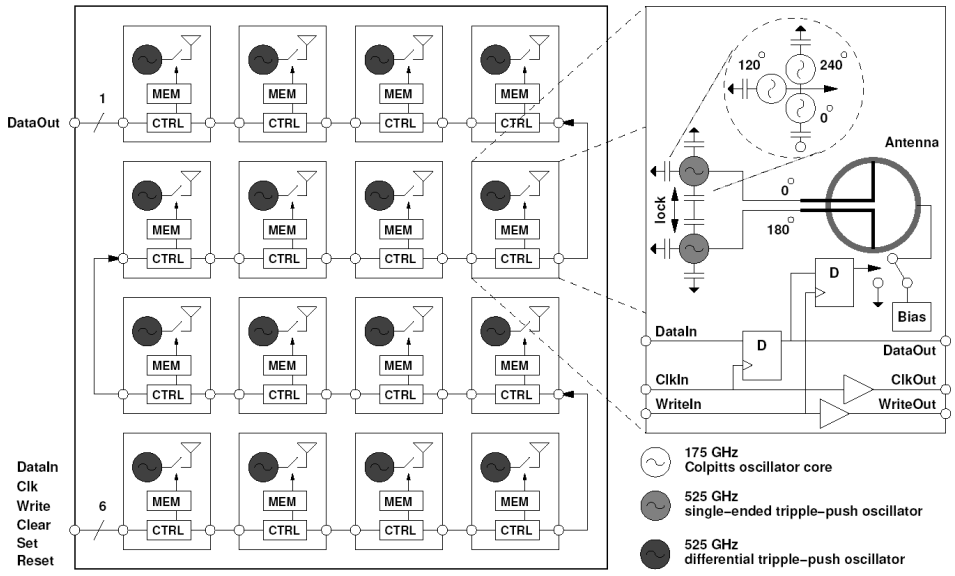

Figure 5.1: Terahertz source array block diagram [8].

To address these challenges, a scalable source array have been implemented in a 0.13 µm SiGe BiCMOS technology. The architecture includes control circuitry and in-pixel memory to configure the terahertz lighting conditions in real-time as

indicated in figure 5.1.

The core of a pixel consists of a differential ring-antenna driven by two triple-push oscillators locked at 180° out-of-phase. Each oscillator is built-out of three Colpitt oscillators which are locked at 120° out-of-phase and operating at a fundamental frequency of 177 GHz. These combinations of locked phases allow the structure to radiate the third harmonic at 0.53 THz through the differential antenna.

To control the array, each pixel can be powered down independently such that arbitrary pattern configurations can be loaded. For that, one control circuit is integrate per pixel modifying the bias condition of the Colpitt oscillators and turning them on or off according to a received command.

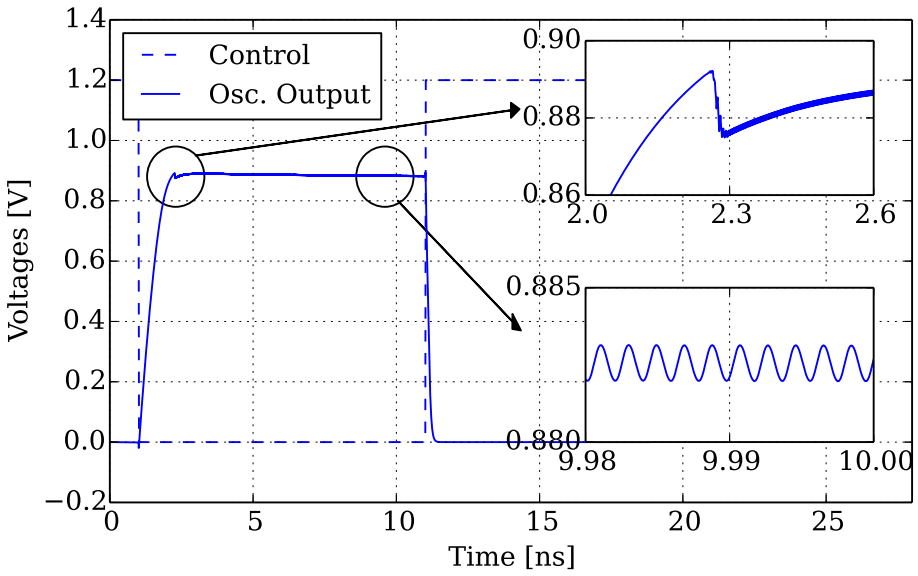

Figure 5.2: Simulation of the startup time.

The important parameter of such a structure is the start-up time of the oscillators. As it has been seen in chapter 2, this process is a statistical event and can vary with the temperature and the biasing conditions. To estimate this time, a transient simulation of the triple push oscillator is show in figure 5.2. In this simulation, part of the passive elements have been replaced by ideal blocks.

The starting time is in the order of the nanosecond and essentially based on the settling of the bias condition necessary to bring the structure to oscillate. This estimation indicates that the start-up time can be negligible with the targeted terahertz illumination condition for producing 25 fps imaging for example and will not be effected by the control circuitry.

5.1.2 Shift register circuit design

The array control circuit is implemented in the CMOS portion of the technology. It consist of a common non-overlapping clock driven by an external 1.2 V clock signal, and a 16-bit synchronous latched shift register spread across the array.

The non-overlapping clock circuit schematic is presented in figure 5.3. It is based on crossed NAND-flip-flop circuit with time delay generated from cascaded buffers. The input of this circuit is driven by an external clock signal, and generates two 180° out-of-phase clocks ϕ_1 and ϕ_2 with the same frequency.

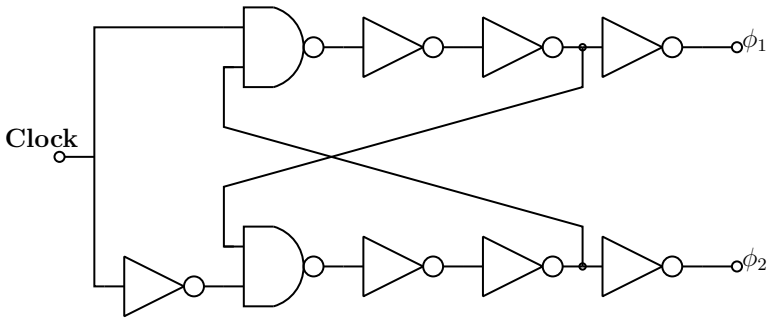

Figure 5.3: Non-overlapping clock circuit schematic.

In each pixel, a shift register cell circuit is implemented and consists of two synchronous edge-triggered D-flip-flop with set and clear inputs. The first D-flip-flop is the data carrier and serves to shift the input data to the next-pixel. The second D-flip-flop drives the oscillator switch. Upon receipt of a rising edge of the write signal, the state of the first shift register is copied into the 16 output registers of each pixel and drive each oscillator power-down switch. A detailed schematic of the pixel control circuit is presented in figure 5.4 and the transient simulation results is shown in figure 5.5.

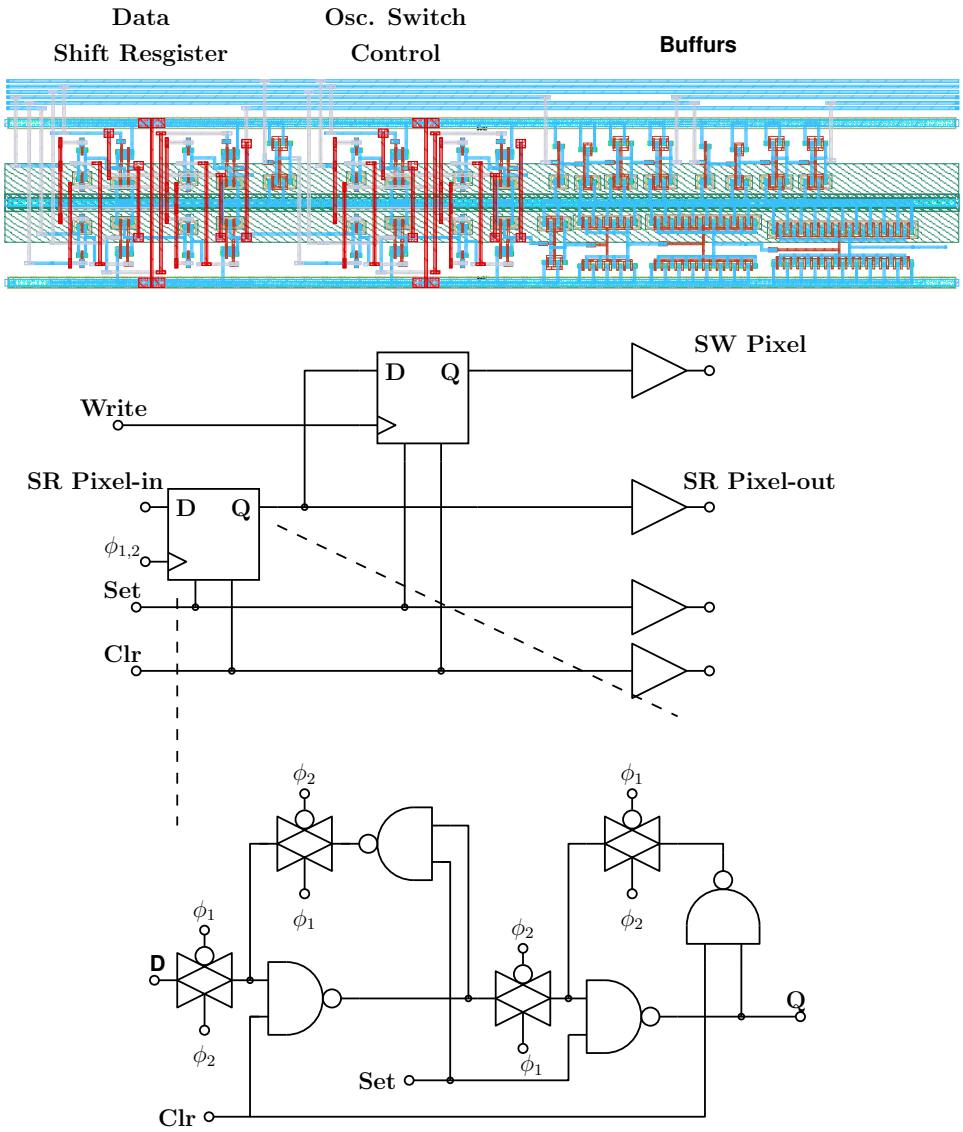

Figure 5.4: Pixel control circuit schematic and layout.

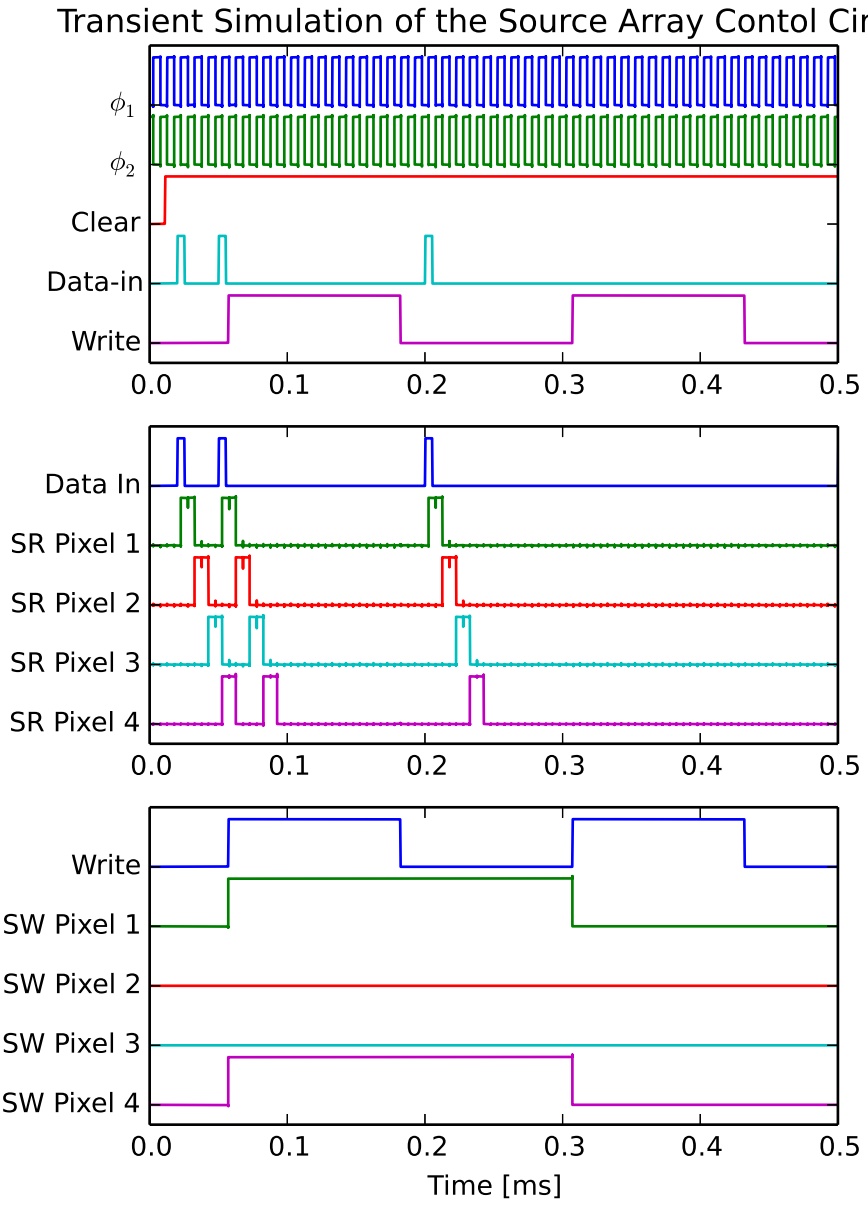

Figure 5.5: Transient simulation of the control circuit of the terahertz source array.

5.1.3 Source array circuit implementation and packaging

The chip was fabricated in a 0.13m SiGe BiCMOS technology and is shown in figure 5.6. The total array size is 2×2.1 mm^2 with a pixel size of 520×520 μm. 20 pads have been implemented with ESD protection to prevent the control circuit from damage.

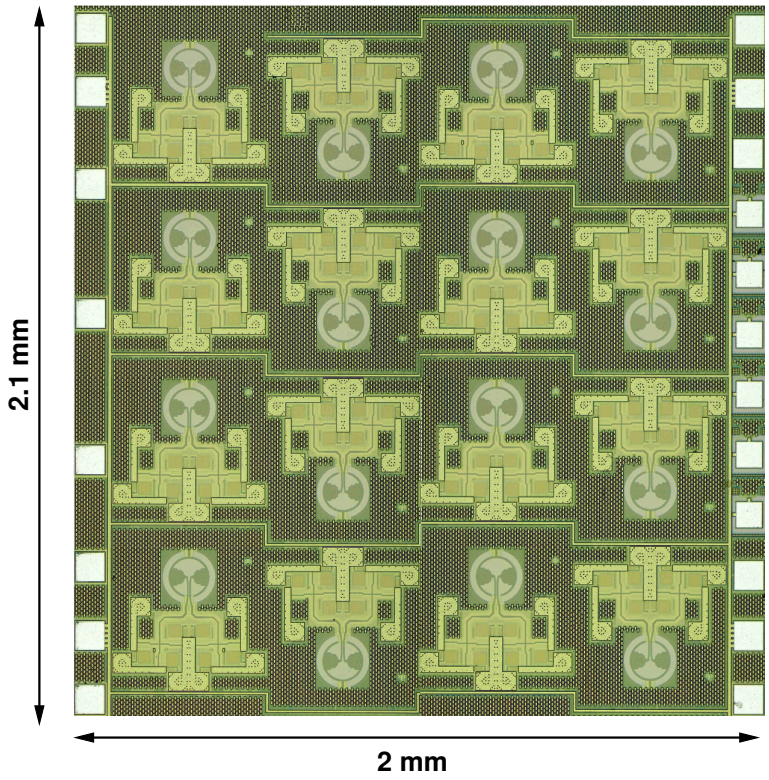

Figure 5.6: Chip micro-graph of the terahertz source array [8].

The chip have been glued to the back of a 15 mm hyper-hemispherical silicon lens. To demonstrate low-cost packaging solutions for hand-held applications, the overall assembly was mounted and wire-bonded onto a FR4 PCB as presented in figure 5.7.

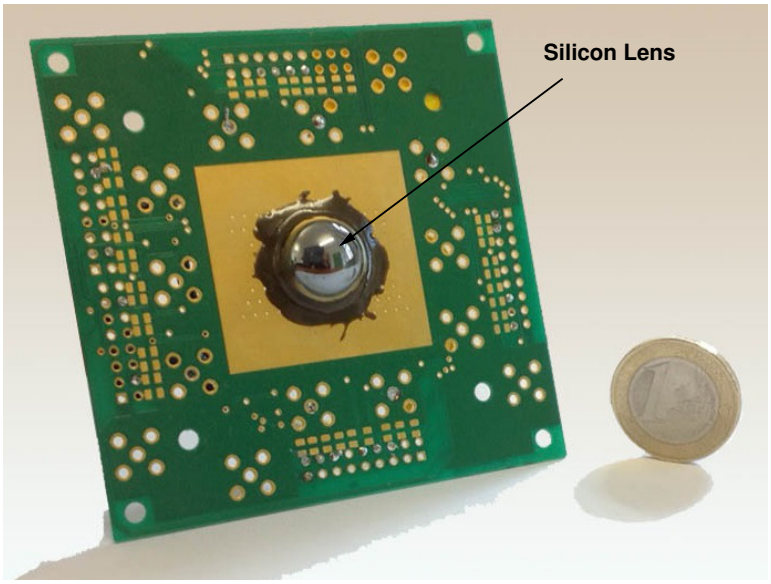

Figure 5.7: Terahertz source array packaging with silicon lens on low-cost PCB. A 1 Euro coin is placed for size comparison [8].

5.2 Terahertz source array characterization

5.2.1 Frequency and power measurement

To verify the operation frequency of different pixels in the implanted array, a harmonic mixer have been used in a free space measurement setup as illustrated in figure 5.8. A 18^{th} harmonic mixer equipped with a diagonal horn antenna capturing terahertz frequencies has been placed in front of the packaged source array. The mixer local oscillator (LO) input was driven by a synthesizer at around 30 GHz. This LO stage was followed by a multiplier and a diplexer stages delivering the intermediate frequency (IF) output with a bandwidth of 3 GHz. The IF corresponds to the mixing product of the LO 18^{th} harmonic and the RF signal captured by the antenna. It has been measured with a spectrum analyzer. For alignment reasons of the harmonic mixer horn antenna and the packaged array, a single pixel has been permanently selected by the control circuitry to perform this measurement.

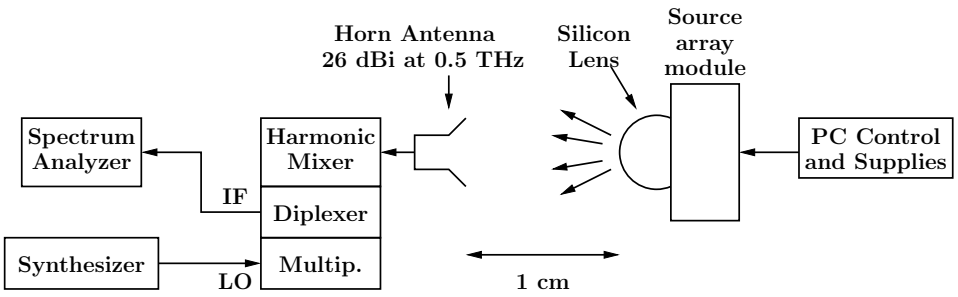

Figure 5.8: Frequency measurement setup of the silicon based source array with a harmonic mixer [8].

To explore the tunning range of the oscillator, the source array power supply has been swept between 0.8-2.6 V. Like a voltage controlled oscillator (VCO), each bias point would correspond to a different radiated frequency and power. Therefore, the radiate power has been measured with an absolute power-meter device as shown in figure 5.9. To use the power measurement device, the source array has to be modulated between 10-100 Hz. This could be done optically by a mechanical chopping wheel or electronically by the modulating the bias of the

source array. The electronic chopping has been chosen by driving externally the source array with a function generator.

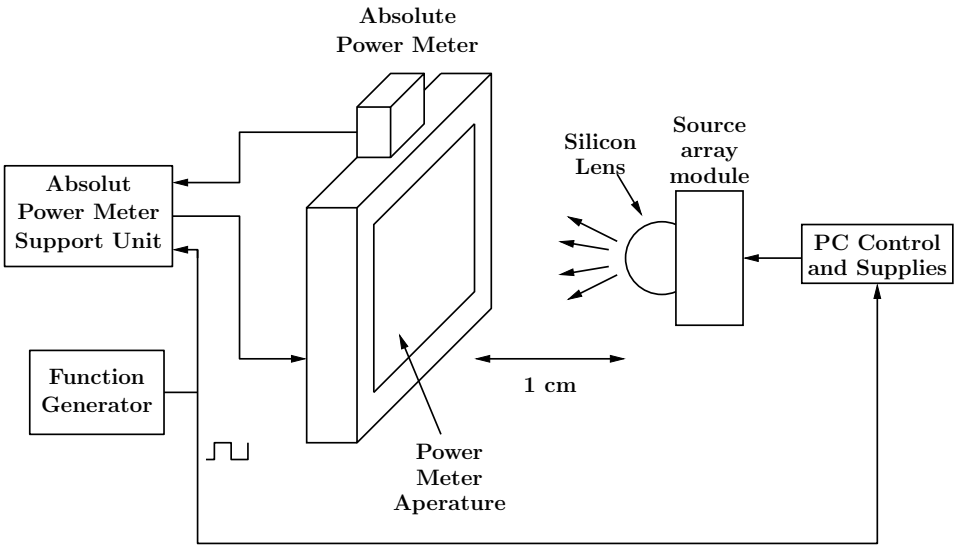

Figure 5.9: Power measurement setup of the silicon based source array with an absolute power-meter [8].

The results of the frequency and power measurement of a selected pixel are presented in figure 5.10. At a supply voltage of 2.4 V, the selected pixel has delivered up to 85 µW of total power. The tunning frequency range has been observed between 0.536-0.519 THz for a supply voltage sweep of 1-2.4 V. The maximum output power has been achieved at the high bias voltage.

With the same setup used in figure 5.9, all the 16 pixels of the array have been turn on and the total radiated power has been measured at different supply bias. In the same time, the array power consumption has been recored. Both results are shown figure 5.11. The maximum radiated power of the array is about 1 mW at 0.4 ‰ efficiency. The average radiated power was 62.5 µW per pixel. The difference between the maximum radiated power measured for one pixel and the average value for the array can be explained be the asymmetrical distribution of the power over the array.

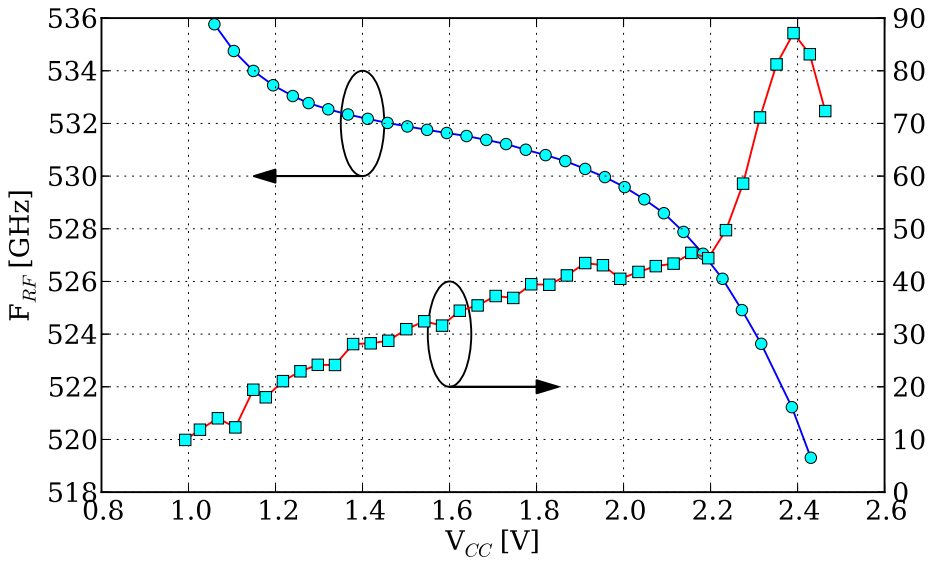

Figure 5.10: Power measurement setup of the silicon based source array with an absolute power-meter [8].

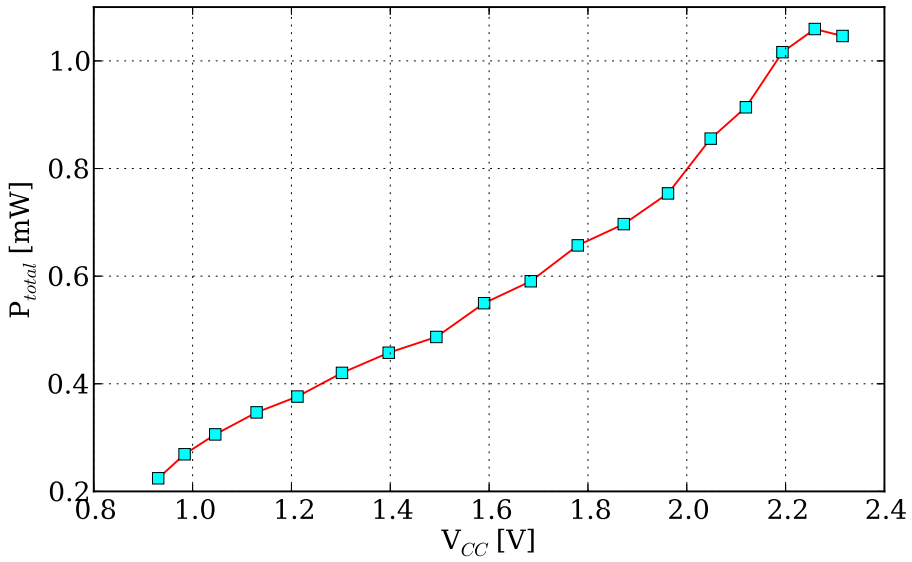

Figure 5.11: Power measurement setup of the silicon based source array with an absolute power-meter [8].

5.2.2 Pattern and control circuit capabilities

In order to verify the control capability of the array, a pattern measurement setup has been used. The terahertz source array has been placed in an anechoic chamber and modulated with an external function generator. The silicon based hetojuction bipolar transistor (HBT) terahertz detector presented in chapter 3, has been placed at a 1-m distance from the source array. A buffer and a lock-in amplifier have been used to record the received signal at the HBT detector as illustrated in figure 5.12. The source array module was rotated in θ and ϕ angles, while the lock-in amplifier signal was synchronously recored.

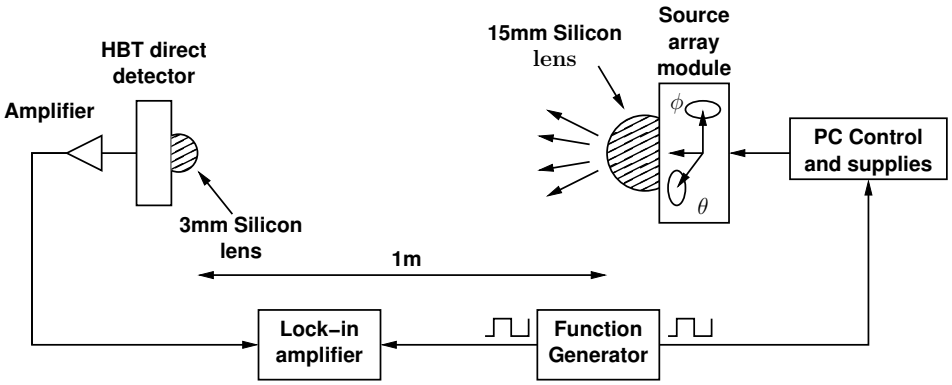

Figure 5.12: Pattern measurement setup of the silicon based source array.

The resulting patterns are shown in figure 5.13. Different pixels have been selected through the control circuit for each pattern measurement. The 16 pixels have covered a 30 deg. field-of-view. To further improve the operation of this terahertz source array, a periodic pattern can be loaded at run time to avoid chopping externally the power supply. Such operation will require real-time monitoring capabilities and will be presented in the next chapter.

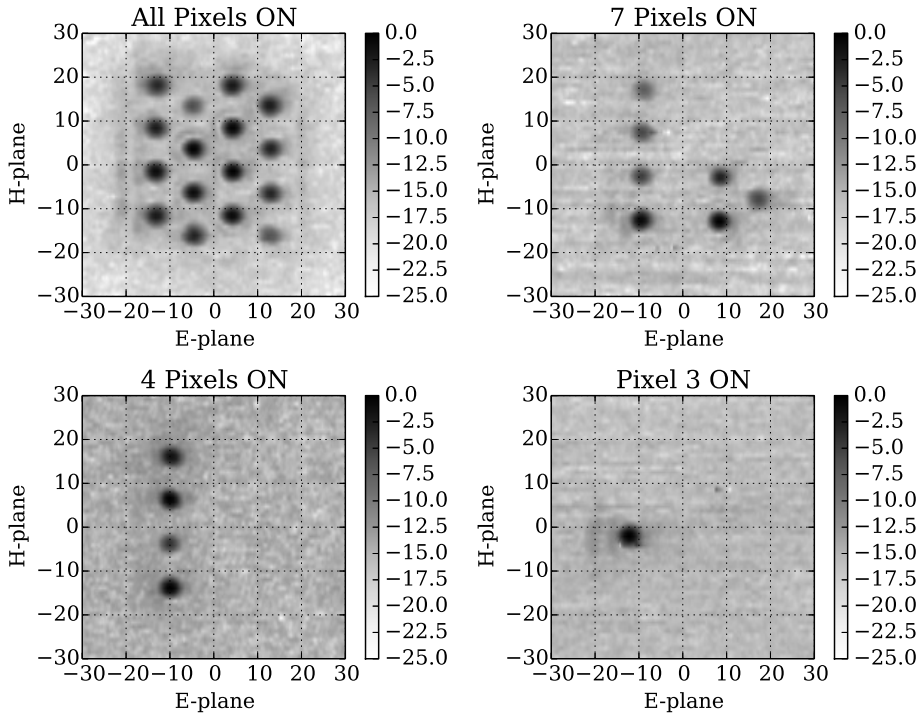

Figure 5.13: Pattern measurement results of the silicon based source array with arbitrary selected pixels [8].

5.3 Chapter conclusion

In this chapter a system level implementation of a silicon based terahertz source array with control circuitry has been presented and characterized. The maximum radiated power of the array was about 1 mW at 0.53 THz with 0.4 ‰ efficiency. This is the highest frequency and power measured for silicon based terahertz sources at the time of the submission of this thesis.

My contribution to the source array module has been the control circuit design and the characterization of the array. The control circuit is based on a shift register elements integrated in each pixel and capable of loading arbitrary patterns at run time. The choice to integrate the control circuit for each pixel has given the potential to implement larger source arrays without the redesign if the circuit architecture. This is a key feature for a high power source array to deliver controllable light conditions at terahertz frequencies.

Future improvement can be implemented to the control circuit such as an in-pixel voltage controlled source. This would enable the end-user to select different radiated frequencies and create 3D terahertz images for example.

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Chapter 6

Terahertz Imaging Demonstrations

Terahertz waves could potentially cover a large field of application as it has been described in chapter 1. One of the aspects of terahertz is the possibility to create an image of a scene where objects have different transmission or refection properties at terahertz frequencies [1]. For that, terahertz imaging may be done in a passive or an active mode.

The concept of terahertz passive imaging relies on the high sensitivity of the detector to capture the natural radiation emitted or reflected by objects in the field of view. External sources are therefore not required to create an artificial illumination. Passive (radiometric) imaging is the preferred method for outdoor stand-off detection for example [2]. However, such imagers typically operate in the lower frequency range (50-110 GHz), where on chip low-noise amplifiers (LNA) are available to provide the required sensitivity and noise performance [3].

Since low-noise amplifiers at terahertz frequencies are still unavailable in silicon, active imaging is currently the only way to implement terahertz systems in standard silicon technologies. In this case, one source or an array of sources may be used to create an artificial illumination in order to capture terahertz images with silicon based detectors.

Active imaging may be done in reflection or transmission mode. In refection mode, like in visible light imaging, sources and detectors are placed in front of the

scene. The detection system is equipped with optics to collimate the collected power being reflected by the objects. In transmission mode, the objects are placed between the source and the detector. Collimating optics are also used but to collect the transmitted power through the objects.

In this chapter, active transmission mode imaging demonstrations are presented. They have been done with the implemented detectors during this thesis. Raster scanned objects in transmission mode are shown in section 6.1 with HBT and CMOS detectors. Real-time transmission mode imaging are presented in section 6.2 with the implemented 1-kpixel CMOS terahertz camera at a frame rate of 25 fps. The implemented terahertz source array is also imaged with the CMOS camera and results are shown in section 6.3. In section 6.4, an evaluation of a beam monitoring application for laboratory high power sources is presented.

6.1 Scanned objects at terahertz frequencies

Terahertz imaging have been of a particular interest in astronomy. Mapping Space in the terahertz domain gave a complementary information to the radio and infrared existing data about star formation [4].

However, creating such images was difficult. In fact, at that time, existing detectors had long time-constants increasing the acquisition time from several hours to several days. In 1995, an image of a scanned object with a readout acquisition rate of about few minutes has been realized [5]. The imaging setup was based on an optoelectronic terahertz time-domain spectroscopy system (TDS). A femto-second pulse source was used to excite an optically gated transmitter. Through a delay path, the same source was exciting an optically gated receiver. The terahertz beam delivered by the transmitter was first collimated and then focused down to a focal point by a pair of lenses. At that point an object was placed. An other pair of lenses were used to collect and focus the transmitted terahertz radiation through the object on the detector. The object was mechanically moved at the focal point of the imaging system. A two dimensional image was created by recording the response of the detected signal. The first scanned objects were an integrated circuit in a plastic packaging and a leaf with different water concentration levels. What made this experiment possible is the short time

constant of the used detector in comparison with bolometers.

In this thesis a similar optical setup have been used to produce terahertz images with single output detectors. Polytetrafluoroethylene (PTFE) lenses were used to focus the beam of a modulated source to a focal point then onto the detector silicon lens. At the focal point, an object was mechanically scanned using computer controlled translation stages as illustrated in figure 6.1. While the object was moved in the vertical plane, the output signal of a single output detector was synchronously read and stored by a data acquisition system based on lock-in technique. These signals were processed and a terahertz image of the scanned object was produced.

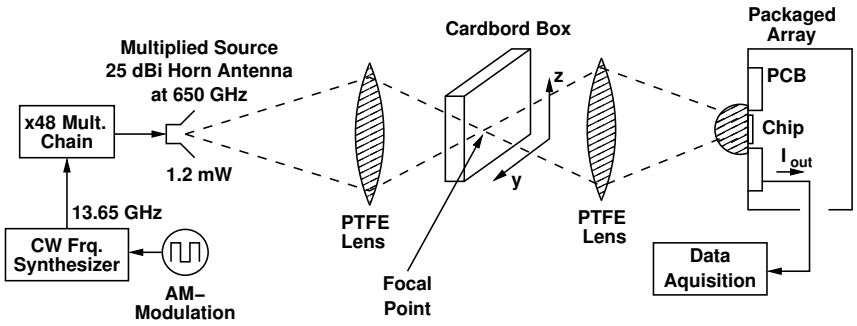

Figure 6.1: Raster scanning terahertz imaging setup [6].

The dynamic range of the terahertz image would depend on the detector sensitivity and noise performance that have been presented in the detector design chapter 3. In the configuration where a single detector is used, the chopping frequency of the pixel would define the modulation rate of the source for best SNR operation.

Figure 6.2 shows a terahertz image of hidden objects in a cardboard box. It represent a picture of 260×120 pixels with few millimeter resolution for a total scanning time of about 7 minutes. This image have been created with the HBT based detector implemented in a BiCMOS SiGe process technology and presented in chapter 3.

To achieve better optical resolutions, higher terahertz frequencies can be used. Figure 6.3 shows a transmission-mode images at 1 THz of a plastic badge and an paper envelope in a similar setup used in figure 6.1. For these images, the

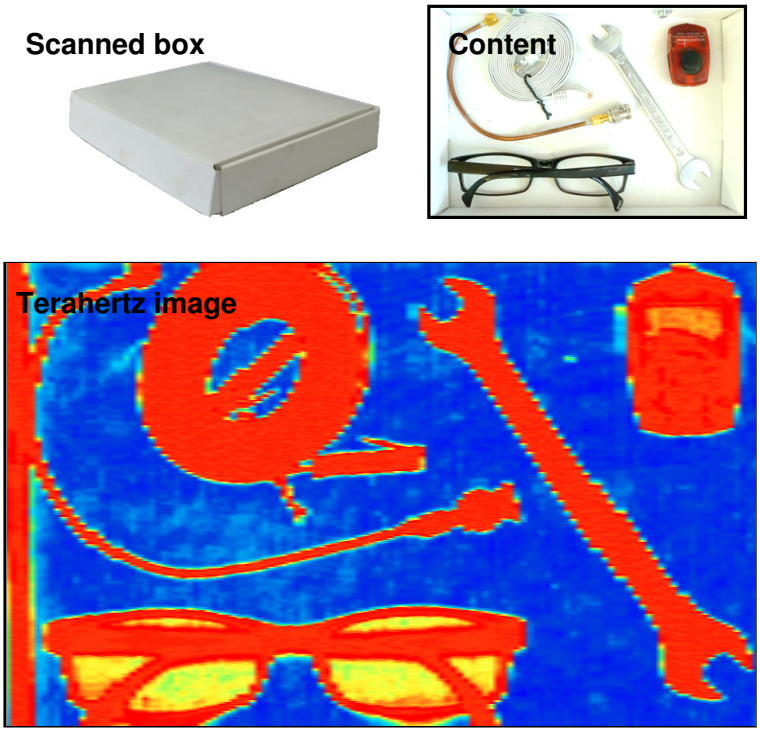

Figure 6.2: Terahertz image of a scanned cardboard box with hidden objects at 0.65 THz in transmission mode (260×120 pixels resolution) created with the HBT based detector of chapter 3 [6].

CMOS detector implemented in a 65 nm technology and presented in chapter 3 have been used. For the experiment, a source capable of delivering around few micro-watts of power at 1.03 THz have been used.

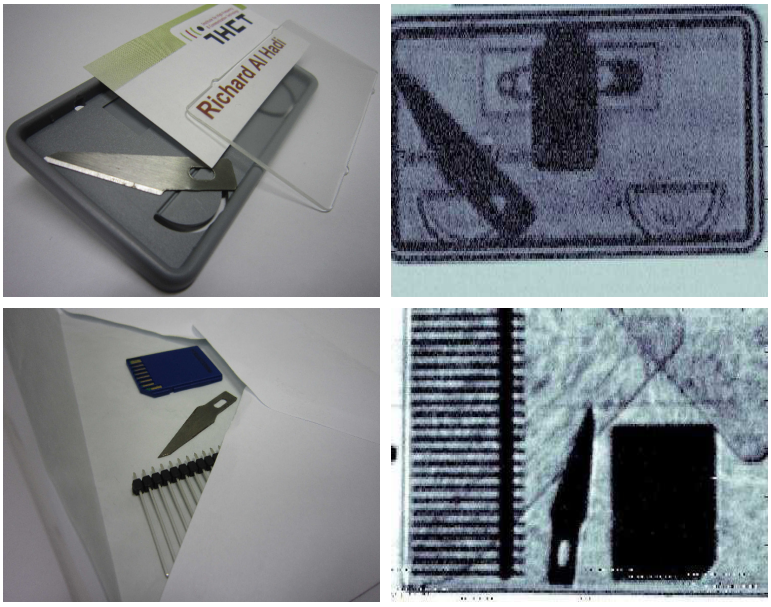

Figure 6.3: Transmission-mode images at 1 THz of a plastic badge and an paper envelope with hidden object such as metal blade, electronic jumpers and a memory card. This image has been created with the CMOS based detector of chapter 3

6.2 Real-time terahertz imaging

As it has been presented in the previous section, it is possible to acquire terahertz images of various object with a single pixel detector by raster scanning. The main disadvantage of this technique is the image acquisition time in the order of few minutes.

With the implemented and analyzed 1 k-pixel terahertz camera module of chapter 4, it is possible to record in real time up to 500 fps a multi-pixel image. However, the previously presented setup can not be used for this purpose.

To build a real-time imaging setup, the first step was to create a parallel Gaussian beam from a conventional 0.65 THz source equipped with a 25-dBi horn antenna. In order to achieve that, the source was placed at the focal length of a first PTFE lens. This would constitute the object plane of the imaging setup. The terahertz camera is equipped with a silicon lens and would require an external lens to project the object plane onto the camera focal plane. Therefore,

as a second step, another PTFE lens is placed in front of the camera such that the object plane is projected onto the hyper-hemispherical silicon lens of the camera module. The second lens almost matches the field-of-view of 46 *deg* of the camera. This setup is illustrated in figure 6.4.

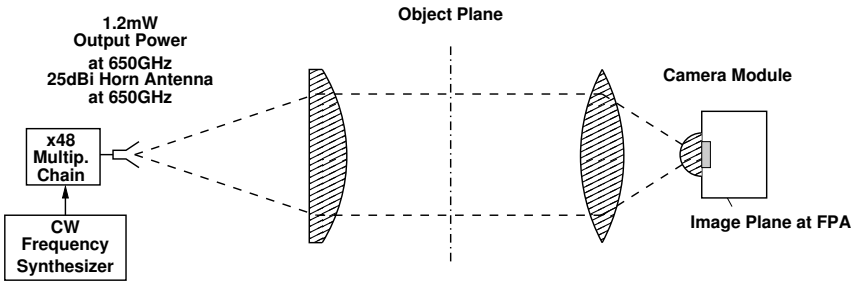

Figure 6.4: Transmission mode terahertz imaging setup. A single terahertz source illuminates the object plane and projects it onto the camera module [7].

This basic imaging setup was designed to demonstrate imaging in video mode at 25 fps. Digital still frames recorded with it are shown in figure 6.5. It shows a picture of a metal wrench with a 6 mm opening and still frames from the recored video sequence where the wrench was moving.

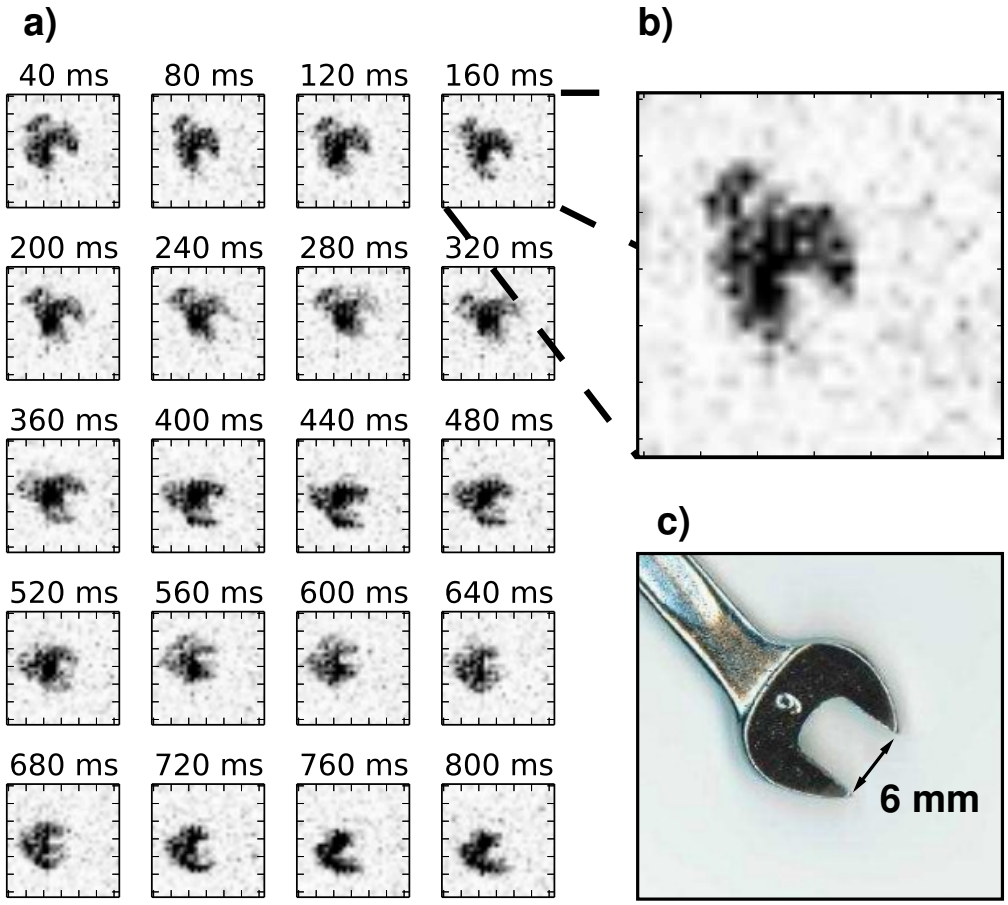

Figure 6.5: Digital still frames taken from a 25 fps video stream of a 6 mm wrench in (a) and (b), the visual image is shown in (c) for comparison. The video was taken at 0.65 THz in transmission mode as indicated in figure 6.4

6.3 Silicon based terahertz source array monitoring in real time

To demonstrate a complete silicon terahertz imaging system with the 1 k-pixel camera module, the implemented 4×4 silicon based source array of chapter 5 has placed in a basic imaging setup as illustrated in figure 6.6.

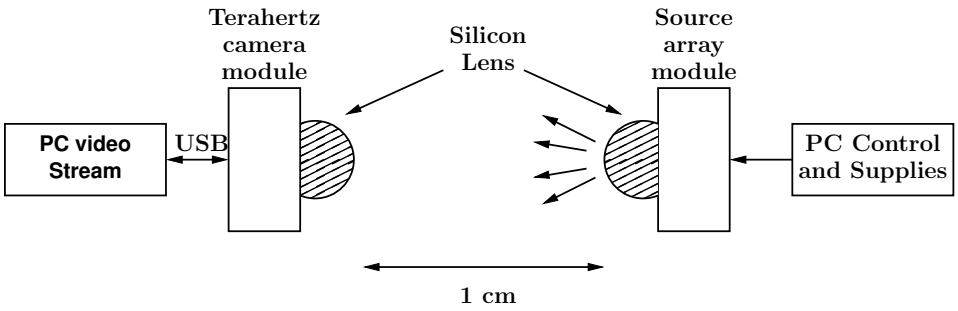

Figure 6.6: Silicon based imaging demonstration setup with the 4×4 silicon based source array and the 1 k-pixel camera module.

The camera recorded in real-time the incident power delivered by the source. In this particular setup, no additional optical elements were used. The 4×4 terahertz source elements were radiating in continuous wave mode (CW) without chopping at about 0.53 THz with a total power above 0-dBm. At 0.5 THz, the sensitivity of the camera is in the lower range, however the source array pixels can be clearly seen with the camera module.

The camera has recorded the arbitrary pattern loaded to the source array by the implemented control circuit. The presented system is very simple but has shown the potential of future applications for large terahertz array systems.

To further improve such system, the optical path can be simulated and optical elements can be used in order to project all the radiated power into the camera. Furthermore, additional sources can be introduced in this setup to create a diffused illumination source.

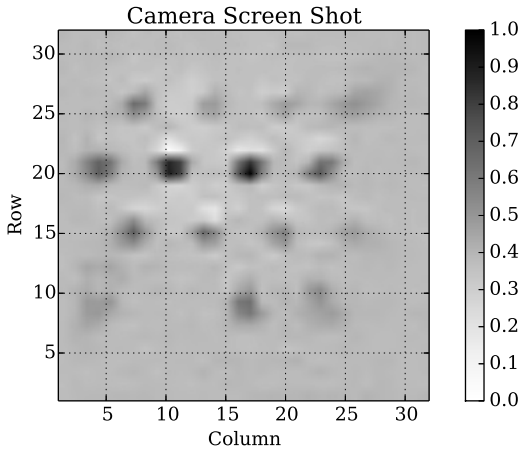

Figure 6.7: Silicon based imaging results of the setup illustrated in figure 6.6. The source array pixels were clearly revealed by the camera.

6.4 Beam monitoring application of a CO_2 pumped gas based terahertz source

From the demonstrations that have been presented in the previous sections of this chapter, an application of a real-time terahertz imaging system has been evaluated successfully. This application would concern high power terahertz sources, such as optically pumped gas lasers. The purpose of the application is to monitor in real-time the beam pattern of a source during an experiment.

The terahertz source principle is based on the optical excitation of a low pressure gas such as methanol. The CO_2 laser beam excites different vibrational levels of the gas molecules corresponding to different emitted terahertz frequencies. In such system, the frequency and power are very sensitive to variation on the pressure levels or the laser mechanical elements. As a consequence, the source could have different emission modes due to temperature fluctuation which result in a non-uniform beam pattern not desirable during an experiment.

To monitor such variations, infrared cameras are currently used to image a terahertz absorber during the experiment. The absorber converts the terahertz waves to heat and then temperature variations are imaged with the infrared cam-

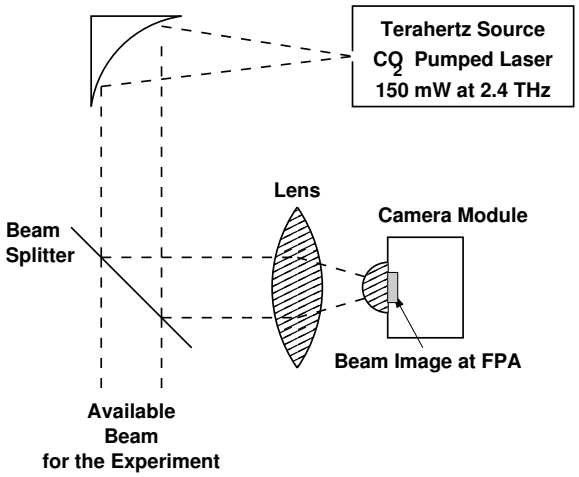

Figure 6.8: Image of a CO_2 pumped terahertz source beam with the 1 k-pixel CMOS terahertz camera. A beam-splitter is used to monitor the output beam of the source during an experiment in real-time [8].

era. This method has the disadvantage to be dependent on the temperature time constant of the absorber. This leads to slow observation on the beam degradation and is very time consuming during the experiment.

What is proposed in this section, is to use the implemented terahertz camera to monitor in real-time the terahertz source during an ongoing experiment as it is shown in figure 6.8.

To monitor in real time the source, a beam-splitter may been used to project a fraction of the source beam into the camera, then a lens with a short focal length has been placed to illuminate the focal plane array.

The results of this experiment are shown in figure 6.9. The terahertz source has been tuned to deliver around 100 mW at 2.4 THz. This frequency corresponds to the high power ray of the excited methanol gas. The fundamental mode of the source corresponds to a relatively circular beam shape as shown in figure 6.9 (a). Changing the dimension of the laser cavity would effect the excitation mode of the methanol molecules and would make the source to radiate in a non-desired mode. This mode would translate into a non-uniform beam pattern as shown in figure 6.9 (b).

This experiment has shown the potential of a real-time application of the

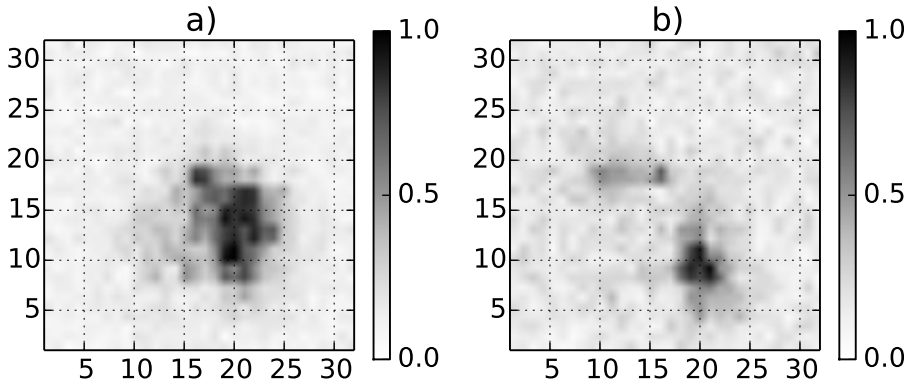

Figure 6.9: Image of the beam shape of the CO_2 pumped gas terahertz source with the 1 k-pixel CMOS terahertz camera in different modes. The fundamental mode corresponds to a relatively circular beam shape (a) while the non-desired mode presents two maximums (b) [8].

terahertz camera. The beam quality of a high power terahertz source. This experiment is possible in other technologies such as bolometer based cameras [9]. However, filters and attenuators are mandatory to avoid any damage to the camera which is not the case for the CMOS based terahertz camera.

6.5 Chapter conclusion

The goal of this chapter was to demonstrate terahertz imaging systems. This has been done with the single output detectors and the multi-pixel CMOS camera implemented and characterized during this thesis.

My contribution to the different demonstrations was to build and program different hardware to acquire images of various objects at terahertz frequencies. Raster scanning technique and real time imaging setup have been presented as well as a monitoring application for high power sources.

The real-time advantage offered by the 1 k-pixel terahertz CMOS camera can be combined to scene reconstruction algorithms in future work. This would increase the field of view [10] and could cover novel applications in the security domain. Furthermore, analyses and Visualization of Multi-spectral Data [11] can

be applied to achieve better imaging resolution.

The presented real-time beam monitoring application can be further improved with a pattern recognition algorithms and real-time feedback in order to correct the beam quality.

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Chapter 7

Conclusion

This thesis has presented the investigations, implementations and analyses of room temperature terahertz devices in silicon technologies.

The first step of the thesis was the investigation of single output detectors in different silicon technologies beyond the frequency limits f_T/f_{max}. HBT, NMOS and SBD based detectors have been implemented and characterized. Measurement techniques have been used to reduce the shot noise of HBT terahertz detectors by low frequency noise matching. Novel broadband detector has been implemented in CMOS technology and do not require tuning elements to operate. The functionality of an experimental SBD has been verified. The implementations have shown state-of-the-art results in comparison with other silicon implementations.

The second part of the thesis was to bring forward the implemented detectors to a camera system level. The world's first CMOS terahertz camera has been implemented in a collaborative team work. It presented state of the art implementation. My contribution was part of the camera design an the full characterization of the camera. An other implementation in a BiCMOS technology is presented with a potential packaging option combining up to 2.5 k-pixel array.

The third part of the thesis concerned the implementation and the analyses of a control circuit for high power silicon based source array. I have contributed to the design and implementation of the circuit control as well as characterization of the full array. The control circuit of such a terahertz source array is a key element to create light conditions and save power consumption. Arbitrary patterns have

been created by programming the source array.

As a final part of the thesis, imaging demonstration setups have been implemented. Raster scanning of various object have been shown with the CMOS and HBT terahertz detectors at different frequencies. A real-time transmission mode imaging setup have been demonstrated with the 1 k-pixel terahertz camera. Also, an evaluation of a potential application of high power sources have been successfully demonstrated with the 1 k-pixel CMOS camera.