Terahertz Circuits and Systems in CMOS

A PhD dissertation presented by

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To

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Declaration

I, Hani Sherry, hereby declare that I have written this PhD thesis independently, unless where clearly stated otherwise. I have used only the sources, the data and the support that I have clearly mentioned.

I declare that no portion of the work referred to in this dissertation has been submitted in support of an application for another degree or qualification of this or any other university or other institute of learning.

Hani Sherry

Abstract

This PhD dissertation presents and analyses various room-temperature circuits for Terahertz detection and generation implemented in CMOS 65nm bulk and 28nm FDSOI throughout the course of the thesis. The work discusses the methodology of design and feasibility of fully-integrated focal-plane arrays of detectors in CMOS technologies as potential commercial solutions for various THz applications.

The interesting characteristics of the Terahertz portion (300GHz-3THz) of the Electromagnetic spectrum incite plenty of applications ranging from safe and non-invasive medical imaging (cancer detection, dental imaging, pharmaceutical and other), security screening and chemical detection, safety inspection and quality control, astronomy, ultra-high data-rate communications and many others.

However, this region of the Electromagnetic spectrum has been dubbed the *THz-Gap* due to the lack of commercial sources and detectors. Classical THz-systems, therefore, have been explicitly dominated by expensive technologies that suffer from low-integration levels and high operational costs. Consequently, current THz-products have been limited to single or few pixels only with raster-scanning techniques to produce single THz image-frames. Therefore, and contrary to the current state-of-the-art, developing such applications with commercial viability will require portability and high integration-levels, video-rate speeds, low power-consumptions as well as room-temperature operation. Reasonably, Silicon-based technologies that are the core of the vast majority of commercial and high-end electronic products seem to be a tempting solution to bring this *THz-Gap.*

The investigations of this PhD thesis evolve from the theoretical analysis to the optimisation of naked detectors implemented in various technology nodes and illumination topologies, up to the implementation of a 1 k-pixel video imager that includes on-chip signal multiplexing, amplification and processing. Terahertz source design based on 5-push harmonic oscillators is discussed and aimed at attaining the highest frequencies possible in CMOS. Terahertz imaging systems are also discussed in the context of their corresponding applications, link budgets and feasibility.

Thesis Contributions

This thesis is based on a series of personal original contributions as well as co-designed circuits. Some of the work appears in the published literature and other are pending characterisation. The thesis has involved both design and measurements. The circuit characterisation was carried out at the University of Wuppertal labs. I was involved in chip packaging and wire-bonding, lens-gluing, electrical and optical setup preparations, and measurement of the designed circuits.

Regarding circuit design, I have designed and taped-out a variety of circuits. The contributions could be summed up as follows:

Chapters 2 and 3:

- A thorough analysis of terahertz detectors and their figures of merit are presented. The analysis involves various parameters necessary for the optimisation of the responsivities and noise equivalent powers of the naked detectors.
- A detailed noise analysis of Terahertz direct detectors is discussed
- Gate-chopped and output-chopped detectors for noise reduction are suggested.
- Technology-based comparison for efficient Terahertz detection is presented with respect to bulk, partially depleted, and fully depleted CMOS process technologies.
- Various Illumination topologies were implemented, measured and analysed.
- The design and measurements of broadband source-driven differential NMOS detectors were done together with Richard Al Hadi.
- Optimised Terahertz direct detectors were implemented in 65nm Bulk CMOS. I have carried out a detailed impedance analysis across various detector sizes and detection topologies, and antennas were designed by Dr. Janusz Grzyb to match the corresponding impedances. I carried out detectors' characterisation across various frequencies of operation, modulation frequencies, and gate biasing.
- Common-well differential field effect detector
- First trial of FDSOI direct detectors was designed and measured. The design was not optimised as RF models were not available at the time of design. Measurements of three detectors were carried out across frequencies of operation, modulation frequencies, as well as body and gate biasing. The noise levels were compared between 65nm bulk and 28nm FDSOI for the same device sizes.
- Detectors with output combining were presented
- Novel circuits for dual polarisation detection were presented with prospects in polarisation diverse imaging and in heterodyne imaging.

Chapters 4:

- I have designed the pixels of the 1kpixel video camera including the in-pixel electronics in schematics and layout level

- I have packaged, set up, programmed an FPGA, and measured the camera chip for the initial publication at the ISSCC2012 with the assistance of several colleagues

Chapters 5:

- I have designed in 65nm bulk CMOS two 5 push ring oscillators for 600GHz and 900GHz output frequencies
- I have designed a heterodyne detector utilizing the 600GHz ring oscillator as an LO
- I have designed a modified Wilkinson power combiner, combining two of the 600GHz oscillators with novel concept of mutual locking

Chapters 6:

- I present imaging results of several imaging techniques for single pixel and multi-pixel imaging of some of the detectors I have designed

List of Publications

1) J. Grzyb, H. Sherry, A. Cathelin, A. Kaiser, and U. R. Pfeiffer, "*Toward Low-NEP Room-Temperature THz MOSFET Direct Detectors in CMOS Technology*," in International Conference on Infrared Millimeter and Terahertz Waves, IRMMWTHz, 2013.

2) R. Al Hadi, H. Sherry, J. Grzyb, Y. Zhao, H. Keller, W. Foerster, A. Kaiser, A. Cathelin and U.R. Pfeiffer, *"A 1kPixel CMOS Camera Chip for 25fps Real-Time Terahertz Imaging Applications"*, JSSC December 2012.

3) H. Sherry, *"Design of Multipixel Terahertz Imagers Using Silicon Technologies"*, invited forum talk, IEEE Custom Integrated Circuits Conference, San Jose, October 2012

4) J. Grzyb, H. Sherry, Y. Zhao, A. Kaiser, A. Cathelin and U.R. Pfeiffer, *"On the Co-Design Between On-Chip Antennas and THz MOSFET Direct Detectors in CMOS Technology"*, IRmmWaveTHz conference, September 2012.

5) J. Grzyb, H. Sherry, Y. Zhao, R. Al Hadi, A. Kaiser, A. Cathelin and U.R. Pfeiffer, *"Real-time video rate imaging with a 1k-pixel THz CMOS focal-plane array"* SPIE conference, Baltimore, April 2012

6) H. Sherry, J. Grzyb, Y. Zhao, R. Al Hadi, A. Kaiser, A. Cathelin and U.R. Pfeiffer, *"A 1kPixel CMOS Camera Chip for 25fps Real-Time Terahertz Imaging Applications"* ISSCC, San Francisco, Feb. 2012.

7) H. Sherry, R. Al Hadi, J. Grzyb, E. Öjefors, A. Cathelin, A. Kaiser and U. R. Pfeiffer *"Lens-Integrated THz Imaging Arrays in 65nm CMOS Technologies"* RFIC, Baltimore, June 2011

8) R. Al Hadi, H. Sherry, J. Grzyb, N. Baktash, Y. Zhao, E. Öjefors, A. Kaiser, A. Cathelin and U.R. Pfeiffer, *"A Broadband 0.6 to 1 THz CMOS Imaging Detector with an Integrated Lens"* IMS, Baltimore, MD, June 2010

9) E. Öjefors, N. Baktash, Y. Zhao, R. Al Hadi, H. Sherry and U. Pfeiffer, *"Terahertz imaging detectors in a 65-nm CMOS SOI technology"* ESSCIRC, Seville, September 2010.

Keywords

Terahertz imaging, Terahertz communication, THz detection, THz generation, Silicon Technologies, CMOS, 65nm Bulk and SOI, PDSOI and FDSOI, self-mixing, active and passive sensing, direct and coherent detection, heterodyne and homodyne receiver; blackbody and thermal radiation, Planck distribution, Rayleigh-Jeans limit, brightness temperature; atmospheric propagation, water vapour absorption, HITRAN database; waveguide, diagonal-horn antenna, ring antenna, lenses, hyper-hemisphere, antenna theorem, antenna directivity and gain, effective aperture, diffraction limit; Gaussian beams, flicker noise, shot and thermal noise, quantum noise; bolometer, Golay cell, Schottky diode, low-noise amplifier; coupling and quantum efficiency, conversion gain, noise figure, RF, IF, LO, Gaussian, Boltzmann, Poisson, Rayleigh; signal-to-noise ratio (SNR), Responsivity (ℜv), noise-equivalent power (NEP), Friis' transmission equation

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I anticipated the profound difficulty in drawing my acknowledgements to the many people I would like to thank, that I have postponed this section numerously. And here I am amidst a warm *nuit Grenobloise* just before finalizing this manuscript, pondering the love I have been bestowed by every single person. It is not the dread of forgetting some, but rather the endless gratitude I owe to everybody that has made this work come to light, were no words can wholeheartedly describe.

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"Aye, I suppose I could stay up that late."- James Clerk Maxwell

To my wonderful family

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Chapter I- Introduction

Ever since the discovery of Electromagnetism around the mid-18th century, succeeded by the derivation of the four famous Maxwell's equations, and our view to the universe has been revolutionized. Even our perception of our very existence has leaped forward dramatically. What our eyes see are but tiny portions of the vastness of the EM spectrum. The ability to access spectra beyond the visible light has ignited the endless technological booms, and scientists and engineers teamed up to devise apparatuses that could either sense or produce at will specific bands of this radiation.

The beauty of the EM spectrum is that it conveys various transverse characteristics across its breadth, based on interactions and behaviours within the media in which the waves propagate. This variety of characteristics instigate distinct and diverse interests leading to multiple applications from communication to imaging and sensing as well as fundamental scientific research.

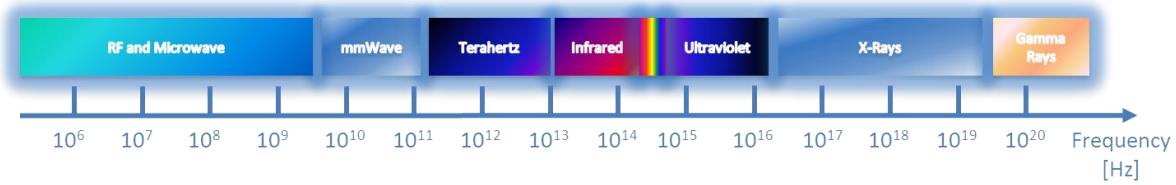


Figure 1-1: The Terahertz place within the Electromagnetic spectrum

Amongst the most compelling and scientifically-stimulating regimes of the EM spectrum is the Terahertz region. As the name suggests, this region conveys waves oscillating at rates on the order of 10^{12} oscillations per second, equivalent to sub-millimetres in wavelength. The engineering society likes to loosely identify the Terahertz-region as where any frequencies run from 300GHz up to 30THz, where 300GHz is equivalent to almost 1mm of wavelength. Figure 1-1 shows the location of the terahertz regime within the Electromagnetic spectrum. Effectively, in comparison to millimetre-waves and micro-waves the wavelengths are far shorter, yet longer than infra-red and visible light.

What rouse research within this regime are the voluminous applications that need to or could be supported within the frequency range. The key to understanding this vastness of applications, as will be demonstrated shortly, lie within the intrinsic characteristics of this portion of the EM spectrum. Multiple interactions with matter exist within this bandwidth, and many chemical, biological, molecular, and physical structures exhibit unique fingerprints and rotational modes at specific frequencies within the THz domain.

Beyond the interactions there lie more explicit behavioural specificities [1], [2]. THz radiation is characterised by high absorption peaks for oxygen molecules and polar liquids such as water [3], [4], [5]. However, THz radiation penetrates many non-dielectric materials, such as fabric, foam, plastic amongst many[6], [7], [8], whilst they are almost totally reflected by metals. An additional

characteristic is derived from the photon-energy levels of the Terahertz rays. At 1THz, the radiation has a photon energy level of 4.1meV, as opposed to the MeV levels at XRays.

The combination of these characteristics has therefore brewed the variety of applications that have established heightened activities in the recent decade [9]. The application space of the Terahertz regime is widening as more interested groups are joining the research efforts. These applications span over a wide range of fields that may seem disconnected in modalities and characteristics. However all of these applications are linked by the characteristics of the Terahertz band itself. Categorically, these applications either fall within the imaging, material characterisation, or the communication fields. We define below sets and subsets of interesting applications that have either been already identified or that have potential prospects.

1.1. THz Applications

Imaging Applications

Probably the first application-space that comes to the minds of all persons involved or aware of the T-Rays is Terahertz imaging for security screening. It has effectively turned into the most sought-after application. Full-body scanners have been an interest for highly sensitive facilities and public spaces, such as airports, governmental compounds, or open space festivals. Originally, security screening was either based on metal-detectors, X-Ray back-scatter imagers, or millimetre-wave passive and/or active imagers. Comparatively, Terahertz radiation is safe relative to X-Rays due to the much lower photon energy that is believed to cause no damage to living tissues through ionization. Therefore, THz radiation seems promising for airport non-invasive full-body security scanners [10], [11], [12].

Chemical characterisation and drug screening and identification is also possible, either for human-carried substances or for scanners of parcels and mail [13] and that is due to the intrinsic characteristics of certain chemicals that exhibit specific reflectivity, absorption, and refractive signatures [14], [15], [20].

Another set of applications lie within the domain of safety of public, industrial spaces, and private households. These applications take the form of detection of gases such as Hydrogen cyanide and Ammonia, or sensing the air quality within a closed space. As Terahertz rays can penetrate non-dielectric materials, applications extend to non-destructive quality control and inspection of hidden defects, non-uniformity and cracks [16], [17]. Figure 1-2 is an example of detection of hidden objects and the revelation of cracks that are unseen to the naked eye.

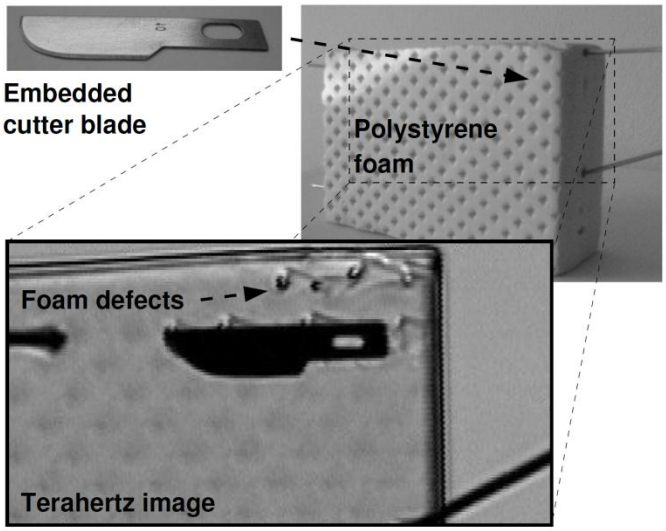
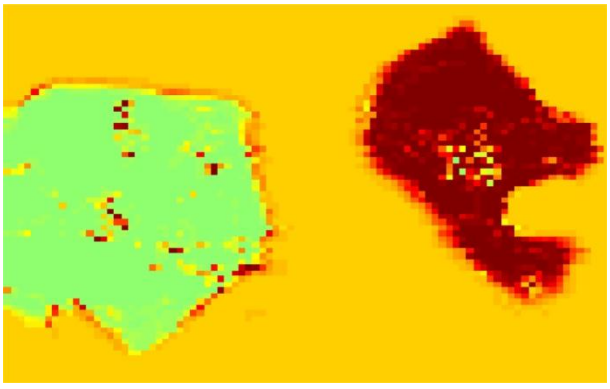


Figure 1-2: Terahertz image using a 65nm CMOS SOI detector revealing hidden objects and foam inner cracks unseen by visible light [18].

Medical and biomedical imaging is also one of the most promising fields that have been undergoing extensive research in the recent years. The primary benefit arises from the safe energy-levels of the radiation as well as the much higher spectral resolution contrary to mm-wave and microwave imaging. Spectroscopic imaging is capable of revealing and analysing various biological and chemical conditions. THz imaging has been applied to analyse breast-tumours [19], [20], skin hydration and skin cancer [21], [22], [23], [24], liver cancer [3], [25], and colon cancer as shown in Figure 1-3. Terahertz radiation was used to monitor wounds healing [26]. A catalogue of optical properties of tissues exposed to THz pulsed radiation was developed by Fitzgerald and Berry *et al.* [27], [28]. It was also shown that THz radiation could benefit in dental imaging [29], [30], [31] to identify and monitor tooth-decay and development of carries. Furthermore, the application space extends to the pharmaceutical industries and the analysis of tablets and chemicals through productions [30], [32].



(a) **(b)**

Figure 1-3: (a) THz image of excised colon tissue showing healthy tissue in green and cancerous tissue in dark red (fake colours). (b) Imaging performed by THz system from Teraview [33]

THz Communications

Communications has been deemed one of the exciting opportunities in the near and mid future. In fact, the demand for high data rates is ever-increasing and is running shoulder by shoulder with the technological advancement and the globalisation of industry as well as knowledge and expertise. As the traditional communication spectra are congested, the Terahertz regime is a widely unlicensed spectrum by the wireless regulation bodies around the globe [34], [35], [36]. Communication over a THz carrier frequency could solve the lack of available spectrum, as well as the wide bandwidth could lead to utterly high data-rates [37], [38], [39], [40], [41]. However, as signal attenuation is high and power levels are low then communication links necessitate highly-directive systems leading to point-to-point communications within short ranges. Yet, this may come for the benefit of securing the short range links where confidential information could be relayed fast and securely.

1.2. State of the Art in THz Detection and Generation

Terahertz Detectors

Despite the appealing abundance of applications the Terahertz domain, bringing those potentialities into realization is a different story. The Terahertz band lies right in the middle of the two converging technologies, the optical and the electronic realms. Both technological-realms do not intertwine, and are literally separated by the terahertz band. As a limiting consequence, the existence of detectors and sources has never made it to large-scale manufacturing nor was transformed to commercially-driven applications. Of course, most of the applications demonstrated above are of a commercial or wide-scale taste. Therefore, the science and engineering world dubbed it the *Terahertz-Gap*, as it serves a challenging frontier to be bridged with novel concepts and innovative technologies.

However, THz detectors and sources do exist. Traditionally, radio astronomy was the main application-space beyond 300 GHz where mixers have been developed based on Schottky diodes. Much advancement has been attained in the recent decades up to the very recent days. Schottky diodes were initially designed with III-V compounds, with impressive performances [42], [43], [44], [45]. Even focal plane arrays existed especially for radio astronomy with cryogenically cooled devices [46], [47]. However these technologies are expensive in terms of manufacturability, mass-production, as well as packaging where wave-guides are essential for signal coupling.

Besides the Schottky-based detectors there exist thermal-sensing based detectors, namely bolometers and micro-bolometers [48], [49]. These technologies exhibit very good performance levels and they excel in passive imaging. Other types of detectors are based on Josephson junctions [50][51] with stacking abilities in 2D arrays[52]. Other existent solutions are based on Golay cells [47], pyro-electric detectors [42], bolometers, micro and nano-bolometers [54], [55].

A few companies in the millimetre-wave and sub millimetre-wave domain started to exist recently, such as Teraview [33], QMC [56], NEC [57], TRAYCER [58], TeraOptronics [59], and Virginia Diodes [60]. However, as mentioned above, all of these technologies either are expensive to manufacture, bulky and power consuming, or require cooling. Additionally, an impediment common to all of these solutions is their incompatibility with the conventional and mainstream microelectronics. There has long been a consensus amongst the technical and commercial communities that utilising Silicon based technologies are the most commercially viable for consumer-

like technologies for what processes bring in terms of maturity, integration level and performance, and most importantly yield and mass-production capabilities. Indeed, with the impediments of the above mentioned technologies, silicon-based very large scale integration (VLSI) seems to be the most attractive ones of all. Furthermore, the high-frequency capabilities of silicon technologies steadily improve through scaling, which enables high integration levels and low power consumptions at higher frequencies. However, their low f_T/f_{max} are still a limiting factor for terahertz applications where transistors do not exhibit any gain beyond these frequencies.

There have been recent outcomes on Silicon based Schottky mixers with promising results. Schottky detectors in HBTs with performances mainly enhanced by the advanced scaling of the technology with f_{max} values reaching 500GHz [61], [62]. CMOS based Schottky detectors have also appeared in the recent years [63], [64], [65]. However, all of these technologies are active-sensor based, as the sensitivities are not high enough for passive imaging.

Coherent THz imaging in CMOS was also demonstrated with spatial LO-supply [66], [67] or by supplying the local oscillators externally and utilising a harmonic of the fundamental. A great deal of recent work, however, focused on developing room-temperature direct detectors. Direct detectors exhibit wide bandwidths and are extremely feasible for array realisation, essentially due to the ultra-low power consumption as well as the minimal pixel-space required. Basically, there is no need for LO synthesis and routing for pixel detectors, which is also attractive because THz LO generation is quite difficult. However, since direct detectors are less sensitive they must operate over a wide RF bandwidth, making the design of an effective coupling antenna assigned to each detector a very important and potentially challenging activity.

Krekels *et al.* have first demonstrated detectors in GaAs HEMT technologies [68]. Dyakonov and Shur have explained the response as a non-resonant response to plasma-wave excitation of a 2D electron-gas [69]. Knap *et al.* then later exposed Silicon FETs to terahertz radiation in [70], [71]. Direct detection in FETs was later explained by means of non-quasi static analysis as a distributed resistive self-mixing process in a non-biased field effect transistor [72], [73].

Further work on CMOS direct detector emerged in the last two years with more research groups joining the efforts [47], [74], [75], [76]. Designs of direct detectors in 250nm CMOS followed [73] with on chip antennas and amplifiers. Then, designs in 130nm CMOS for broadband detection [77], as well as designs in 65nm CMOS bulk and SOI was demonstrated with various packaging techniques [18], [78], [79]. Most recently, we demonstrated large-scale integration by a 1kpixel CMOS camera for THz imaging [80], [81] . A THz staring imager with readout electronics was also presented in [82]. This background study demonstrates the increased activity on design using Silicon technologies with researchers aiming for further large-scale integration.

It is essential to mention the two main imaging techniques: active imaging and passive imaging. Passive imaging relies on the sensing of the black-body radiation of the object under test. All matter in this universe emits radiation based on the intrinsic temperature of the body, and the brightness at a specific frequency follows the Rayleigh-Jeans approximation [83]. There exists a variety of radiometers that are capable of sensing passively [48], [49], [84], [85]. However, CMOS-based detectors fall short on the sensitivity for passive imaging, especially with the fact that no low-noise amplifiers exist beyond the technology speed limits. Therefore, active imaging is, thus far, the only possible technique for CMOS based detectors. This includes a THz source illuminating the object

under test. Then, the THz detectors are used to collect the information either in transmission-mode, where the signals penetrate through the object, or in reflection-mode, where the signals bounce off it.

Terahertz Sources

On the matter of Terahertz sources, there exists a variety of solutions based on high frequency Gunn, IMPATT and Tunnel diodes, quantum cascade lasers, femto-second lasers, backward wave oscillators, traveling wave tubes, Photo-mixer sources [50] [86] [87]. All of these solutions are not feasible for high integration and are power-hungry.

For Silicon-based or MMIC based sources, we can distinguish two main types of THz sources: multiplier-based sources where a lower frequency is fed into the inputs of a multiplier chain, or oscillator-based sources.

For multiplier based sources, earlier work by Moussessian demonstrated a grid of frequency doublers, reaching very high output powers on the order of 24mW at 1THz, using Schottky diodes, and consuming around 47W [88] . Other Schottky barrier multiplier chains were demonstrated recently [78], [89], [90]. SiGe HBT technologies with frequencies at 325GHz [91] and 825GHz full-transceiver solutions based on BiCMOS technologies [62] were presented. Of course these design benefit from the high f_T/f_{max} of the technologies. There are also non Silicon based technologies with frequencies reaching 1.5THz [42], [92], [93]. CMOS designs also exist at the lower end of the THz region, [94], [95] with traveling wave frequency multipliers attaining 6.6dBm output power at 240GHz within a 220-275GHz range.

As for the oscillators, two types exists: fundamental oscillators that oscillate and transmit frequencies below the technology limit where the transistors exhibit power gain; the second type is harmonic oscillators, where a fundamental frequency oscillating below f_T/f_{max} is normally tuned out and a higher order harmonic is extracted from the oscillator core.

A 300GHz fundamental oscillator was designed in 65nm CMOS bulk technology [96]. A 324GHz frequency generator in 90nm digital CMOS with 4GHz tuning range under 1V supply voltage by using a linear superposition method was designed [97].

Fundamental colpitts at 165GHz in a SiGe bipolar technology with an output power of -15dBm were recently shown in [98]. Triple push oscillators with 3rd harmonic power-combining were demonstrated with a 482GHz oscillator generating 0.16 mW in a 65nm CMOS process [99]. Then, a lens integrated triple push oscillator with mutual coupling and power combining was demonstrated at 288GHz in [100]. Coupled oscillator design have shown potential for increasing output power for THz oscillators [101] with 0.46mW power at 320GHz and 0.76mW at 290GHz. A broadband 480GHz passive frequency doubler in 65-nm Bulk CMOS with 0.23mW output power was also recently presented [102].

In the author's view, the lower end of the THz domain holds higher potential for the near future, with sources of higher integration levels employing power combining may be deemed beneficial for all silicon solutions.

1.3. Purpose of this Thesis

The primary aim is to investigate possibilities of more adequate terahertz systems for the various application fields that have been demonstrated above. It is essential here to define "adequate" as potential replacement-systems that would provide added benefits for the specific application(s) in terms of cost, size, power consumption, ease of use, and sensitivity. And as the entire engineering world is based on employing intelligent trade-offs, it will be apparent hereafter that the subtleties of various parameters serve as added dimensions of choice for the Terahertz engineers and scientists. For instance, airport Terahertz systems for security screening would require the sensitivity levels be as high as possible, with frame rates that would not impede the huge flows of passengers. On the other hand, applications in the fields of quality control may require less stringent analysis-time.

The main focus of this thesis is centred on designing circuits and systems based on CMOS process-technologies. CMOS has always been the favoured candidate for high-yield low-cost mass-production. The maturity of CMOS technologies in terms of theory, design, manufacturing, characterisation, and packaging has been pivotal to bridging the major technological advancements of our recent decades with daily life customers. However, at ultra-high frequencies, CMOS technologies confront their fundamental barriers where performance begins to roll-off drastically.

Traditionally, engineers look upon the f_T/f_{max} limits as their design edges. These limitations will be sufficiently explained in the next chapters; however it is important to note at this point that all the work that will be presented hereafter is based on circuit-design beyond the traditional f_T/f_{max} limits of various technologies. It is what we can term as "*The Unexplored Regimes of CMOS*" for the detection-end and "*The Squeezing of CMOS*" for the source-end. Through non-quasi-static analysis we will soon explain how CMOS transistors could yet be operated at THz frequencies even though the transistors are effectively attenuating the signals. It has only been a few years since researchers have started looking into CMOS performance within the Terahertz domain, thus this thesis could serve as part of the collective efforts being invested in developing the yet infant state of the art.

The discussions will develop an understanding of single pixel design comprising merely of an antenna and a THz mixer. Analysis of various process technology choices, packaging options, detector topologies and dimensioning, antenna structures, noise performances, as well as readout choices will be presented. Eventually, building on the understanding of naked detector performances this thesis investigates possibilities of multiple element cameras with higher levels of integration.

On the other hand, this thesis explores capabilities of frequency synthesis within the region of Terahertz using Silicon solutions. This is aimed at the penultimate target of an all-Silicon solution for THz-systems; a much needed breakthrough for widening the margins of THz applications. By all means, since the main focus of this work is design in CMOS, or in a more generalized aim, in Silicon technologies, it is thus wise to identify the possibilities of commercialisation and industrialization of any potential solutions in Silicon. Given the fact that the current THz market is a niche one, any concepts hereafter are either to perturb and replace already existent industries, or to create and establish markets that have not existed at all.

1.4. Organization of this Thesis

This thesis is organised in the following manner: chapter 2 demonstrates the theory of THz mixing, starting from the quasi-static modelling that is valid for low frequencies, on towards the non-quasi-static analysis valid for the high frequency domain. The basic detector building-blocks and circuits will then be presented, along with the relevant figures of merit related to THz direct-detectors.

In chapter 3, the theory from chapter 2 is expanded to discuss methodologies of efficient THz-detectors design. This will include an in-depth analysis of the different aspects of the design from technology comparisons, packaging techniques as well as the intrinsic device characteristics. Afterwards, implemented and characterised THz detectors in 65nm bulk CMOS and 28nm FDSOI will be presented. These include the design and measurements of various test structures including single-pixel detectors, multiple output detectors, as well as polarisation-diverse detectors.

Chapter 4 presents the world's first 1kpixel THz video camera designed and implemented in 65nm CMOS bulk technology from STMicroelectonics. Camera and detector characterisation results will be presented. This chapter serves as a demonstration of the viability of CMOS technologies for Terahertz direct detectors.

Chapter 5 speaks about Terahertz frequency generation in 65nm CMOS. A 5push ring oscillator design and implementation will be presented. The ring oscillator is used a local oscillator for an integrated heterodyne mixer, which will also be presented in this chapter.

Terahertz imaging systems and setups from single pixel to multi-pixel setups will be presented in chapter 6. This chapter discusses the feasibility of terahertz system design requirements in terms of link-budgets, in view of the sensitivities of the available CMOS Terahertz technologies.

A global conclusion of the work is discussed in chapter 7 with a summary of this work and future prospects.

Chapter II- Theory of Terahertz Detection Using CMOS Technologies

Terahertz detection in field effect transistors could be explained by non-quasi static transistor behaviour. In this chapter the theory of mixing using field effect transistors (FETs) is explained. This theory has first been developed by [72], [73], and an expansion with respect to different detector topologies will be presented here and in the next chapter. First, the low frequency relations based on quasi-static analysis will be derived. Then, the analysis will be extended to the Terahertz regime by employing non-quasi-static analysis. Afterwards, various circuit schematics for both direct and heterodyne/homodyne detection that could be designed according to the derived theory will be shown. Finally, the various figures of merit relevant to THz direct detectors with their corresponding measurement setups and techniques will be explained.

The theory described in this chapter will serve as the essential basis for the next chapter on design methodologies, where design optimization and implementation will be inspired by analysis of the various parameters presented here.

2.1. Theory of Terahertz Mixing in CMOS

This section discusses in detail the theory of Terahertz mixing using *Field Effect Transistors* (FET). First, the square-law equations from quasi-static analysis that hold for low frequencies such as radio frequencies (RF) and microwave frequencies are extracted. Then, this analysis is transported to higher frequencies based on non-quasi static (NQS) analysis of the transistors. A partial differential equation (PDE) that governs the step-wise distribution of the voltages along the channel will be derived. The analogy between the NQS model that we will present here and the over-damped plasma wave dynamics described in literature by [69], [103]. Accordingly, we will demonstrate the various detector topologies and the figures of merit.

2.1.1. Quasi-Static Analysis

At low frequencies of operation the electrical behaviour of field effect transistors is mathematically described according to the well-known quasi-static modelling. The lower frequencies are defined to be the range well-below the transient frequency f_T of the transistors. In this case, the finite charging time within the inversion layer is not considered. In other words, the voltage variations at the device terminals are slow enough for the charges to follow instantaneously within the device, and at any position. This is in contrast with the behaviour of the FET at higher frequencies such as the Terahertz spectrum. Therefore, a FET in its quasi-static operation can be described by different mathematical models based on the biasing conditions that place the FET in specific operation regimes. Following, the drain to source time-dependant current $i_{DS}(t) = I_{DS} + i_{ds}(t)$ in relation with the gate to source biasing voltage $v_{GS}(t) = V_{GS} + v_{gs}(t)$ and the drain to source voltage $v_{DS}(t) = V_{DS} + v_{ds}(t)$ in a common source configuration that effectively defines the three regimes of operation will be presented.

In the sub-threshold region, a drain to source current $i_{DS}(t)$ can be related to the gate to source biasing by an exponential relation according to (1)

$$i_{DS}(t) \approx I_{D0} e^{\frac{v_{GS}-V_{TH}}{nV_T}} \quad (1)$$

Where

- $V_T = \frac{kT}{q}$, is the thermal voltage
- $n = 1 + \frac{C_d}{C_{ox}}$, with C_d being the depletion capacitance, and C_{ox} the oxide capacitance
- I_{D0} is the current when $V_{GS} = V_{TH}$

In the ohmic (linear) region, the current $i_{DS}(t)$ can be described by a quadratic relation as in (2)

$$i_{DS}(t) = \frac{W}{L} \mu C_{ox} \left(v_{GS}(t) v_{DS}(t) - V_{TH} v_{DS}(t) - \frac{v_{DS}^2}{2}\right) \quad (2)$$

And in the saturation region, the current $i_{DS}(t)$ can be described by (3)

$$i_{DS}(t) = \frac{1}{2} \frac{W}{L} \mu C_{ox} \left[(v_{GS}(t) - V_{TH})^2 (1 + \lambda v_{DS})\right] \quad (3)$$

These equations reveal the exponential and quadratic relations related to the time harmonics, $v_{gs}(t)$ and $v_{ds}(t)$. Observing the case of the linear region with its corresponding quadratic relationship one can deduce the analogy with the following trigonometric relation (4)

$$A\cos(a) * B\cos(b) = \frac{A*B}{2}[\cos(a+b) + \cos(a-b)] \quad (4)$$

This relation is the core of what is known as *signal mixing* or *signal multiplication*. Signal mixing leads to frequency translation by creating cross-modulation products as the sums and differences of two harmonics that are mixed together. In other words if two different time-harmonics $\cos a$ and $\cos b$ are applied at the proper terminals of mixer, say an FET-based mixer, two intermediate frequencies (IF) should appear at the output at the sums and differences of the *a* and *b* tones. This is the concept of a heterodyne receiver, and its block diagram is shown in Figure 2-1. In this case a radio frequency (RF) of frequency f1 is mixed with a local oscillator (LO) of frequency f_2, thus creating an IF at $f_1 + f_2$ and $f_1 - f_2$. A homodyne receiver is a special case of the heterodyne receiver, and is realised by applying a local oscillator frequency f_2 equal to the received RF f_1. Then, the IF is at DC and at the double of the frequency. The benefit of a heterodyne receiver is the preservation of the phase information. This information could be utilised for the design of RADAR imagers or 3D imagers through the extraction of the intensity and the depth of an image. However, the design of heterodyne and homodyne mixers imposes difficulties and will be noted and discussed later on.

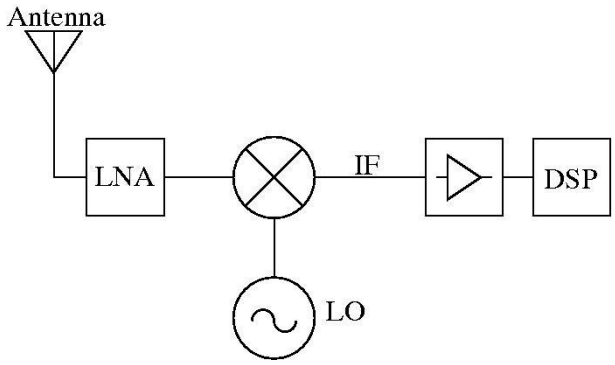


Figure 2-1: Block diagram of a heterodyne detection (coherent) system

On the other hand, one single tone could also be fed into the mixer. To create cross-modulation products in this case, this input frequency should be provided to both input ports of the mixer. This could be realized by RF-short-circuiting both terminals of the mixer via an external coupling capacitor $C_{coupling}$. Then, a zero-IF appears also at the output, similar to homodyne-reception yet with only one input frequency. This is called direct-detection or incoherent detection and its block diagram is shown in Figure 2-2. It first appeared in 1981 for RF frequencies [104], and was employed later on in several direct detection systems [105], [106], [107],[108].

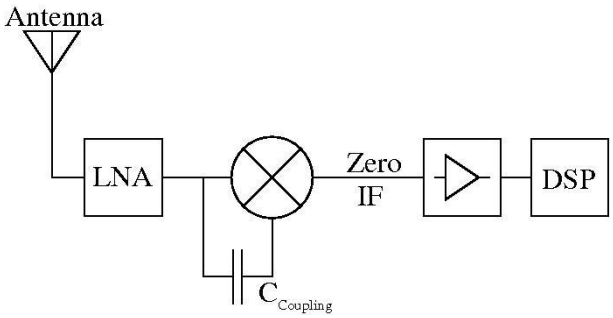


Figure 2-2: Block diagram of a direct power detection (incoherent) system

On the circuit level, both topologies benefit from the non-linearities that an FET channel exhibits, as described in (1)-(3). For instance, to realise an RF direct detector, and considering the triode or Ohmic region, one should apply a DC gate bias voltage V_{GS} larger than V_{TH}, and an input time-harmonic radio frequency $v_{RF}(t)$, giving a gate-source voltage of

$$v_{GS}(t) = V_G + v_{RF}(t) \quad (5)$$

By connecting a gate-to-drain external coupling capacitor as in Figure 2-3, in analogy with Figure 2-2, the drain's AC potential is tied to the gate's ac potential at high frequencies, $v_{ds}(t) = v_{RF}(t)$, whilst the DC bias is constrained to the gate and blocked from the drain end. This is equivalent to a high-pass filter. This leads to a time-harmonic appearing at the drain end which is equal to $v_{RF}(t)$, and referenced to an AC-ground at the source-end.

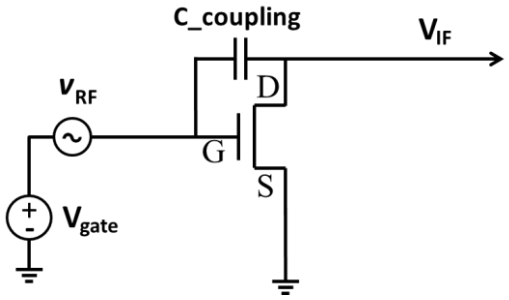


Figure 2-3: Direct detection circuit using FET

Dividing $i_{DS}\,(t)$ by $v_{DS}(t)$ gives the time-dependant channel conductance $g_{DS}\,(t)$

$$g_{DS}\,(t) = \frac{i_{DS}\,(t)}{v_{DS}\,(t)} = \frac{W}{L}\,\mu\,C_{ox}\,(v_{GS}\,(t) - v_{TH} - \frac{v_{DS}}{2}) \tag{6}$$

Substituting for $v_{DS}(t)$ and $v_{GS}(t)$ gives

$$g_{DS}\,(t) = \frac{i_{DS}\,(t)}{v_{DS}\,(t)} = \frac{W}{L}\,\mu\,C_{ox}\,(V_{GS} + v_{RF} - v_{TH} - \frac{v_{RF}}{2}) \tag{7}$$

Knowing that

$$i_{DS}\,(t) = g_{DS}\,(t) v_{DS}\,(t) = \frac{W}{L}\,\mu\,q_{CH}(t)\,v_{DS}\,(t) \tag{8}$$

where $q_{CH}(t) = C_{ox}(v_{GS}(t) - V_{TH})$ is the quasi-statically time-varying charge-density along the inversion-layer. Substituting for the RF time-harmonic gives

$$i_{DS}\,(t) = g_{DS}\,(t)\,v_{DS}\,(t) = g_{DS}\,(t)\,v_{RF}\,(t) \tag{9}$$

$$i_{DS}\,(t) = \frac{W}{L}\,\mu\,C_{ox}\,\left[\frac{v_{RF}^2}{2} + v_{RF}(t)(V_{GS} - V_{TH})\right] \tag{10}$$

Considering a sinusoidal time-harmonic and substituting for the drain-source current relation for the Ohmic-region will be:

$$v_{RF}(t) = V_{RF}\sin\omega t \tag{11}$$

$$i_{DS}\,(t) = \frac{W}{L}\,\mu\,C_{ox}\,\left[\frac{(V_{RF}\sin\omega t)^2}{2} + (V_{RF}\sin\omega t)(V_{GS} - V_{TH})\right] \tag{12}$$

$$i_{DS}\,(t) = \frac{W}{L}\,\mu\,C_{ox}\,V_{RF}^2\,\left[\frac{1+\sin(2\omega t)}{4}\right] + \frac{W}{L}\,\mu\,C_{ox}\,V_{RF}\sin\omega t\,(V_{GS} - V_{TH}) \tag{13}$$

eventually leading to the square-law relation of the generated drain-source DC current with respect to the square of the incident RF voltage

$$I_{DS} = \frac{W}{L}\,\mu\, C_{ox}\ \frac{V_{RF}^2}{4} \propto\ P_{RF} \tag{14}$$

and the output DC voltage which is proportional to the power of the detected radio frequency

$$V_{DS} = \frac{I_{DS}}{G_{DS}} = \frac{V_{RF}^2}{4(V_G - V_{TH})} \propto\ P_{RF} \tag{15}$$

This brings the analysis to a very interesting point which defines the basis of all the design methodologies and decisions for THz detectors to be presented afterwards.

In the forthcoming section this analysis will be exported to the Terahertz frequencies regime by employing a non-quasi static analysis. From that point on, the figures of merit for THz detection and their corresponding methods of characterisation will become apparent. The theoretical description will be broadened to an in-depth analysis and design methodology for single and multiple pixel THz detectors in chapter 3. The analysis will convey an electrical and electromagnetic understanding, and the constraints will be met with corresponding design techniques.

2.1.2. Non-Quasi-Static (NQS) Analysis

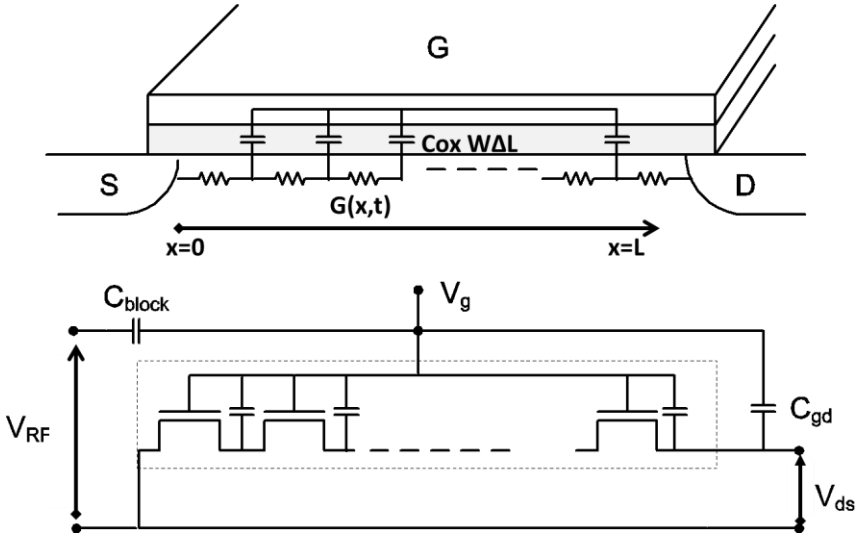


Figure 2-4: Non-quasi static channel of a FET [79]

Extending the previous analysis towards the THz-regime requires accounting for the inertia of the charge carriers, therefore, the previous approximation breaks down and non-quasi-static effects based on carrier transport equations should be used. The signal oscillations are faster than the charge distribution within the channel, and therefore the charges do not have enough time to cross the entire channel. Accordingly, the channel could be modelled *non-quasi-statically* and is divided into infinitesimal segments comprised of the unitary channel conductance, g_n(v), with a position dependant conductivity, $G(v(n\Delta x,t))$, where $g_n(v) = \frac{G(v(n\Delta x,t))}{\Delta x}$ per Δx segmentation. Similarly, the gate-to-channel capacitance C_{ox} is divided into unitary Δx segments, C_n, where $C_n = WC_{ox}\Delta x$.

Consequently, g_n is controlled by the position dependent voltage $v(n\Delta x,t)$ which is provided by corresponding gate-capacitance segment, C_n. Therefore, these infinitesimal segments resemble the mixer topology represented in Figure 2-3, where the segmented conductance g_n is modulated by a time-harmonic signal coupled through the C_n portion of the gate-channel capacitance. The entire transistor is, thus, viewed as N tiny transistors in series, equipped intrinsically with their gate-drain coupling capacitors.

Furthermore, employing the Kirchoff's Current Law (KCL) at the infinitesimal junctions in Figure 2-4 gives the following current relations:

$$i_{g,n-1} + i_{g,n} = i_{C_n,n} \tag{16}$$

$$g_{n-1}(v_{n-1} - v_n) - g_n(v_n - v_{n+1}) = C_n \frac{d(v_n)}{dt} \tag{17}$$

Thus, for unitary segments, a PDE could be deduced

$$\frac{\partial}{\partial x}\left[G(v(x,t))\ \frac{\partial v(x,t)}{\partial x}\right] = C_{ox}W\ \frac{\partial v(x,t)}{\partial t} \tag{18}$$

Wherein, for strong inversion, one would substitute for

$$G(v(x,t)) = \mu\, C_{ox} W\, (\, v(x,t) - V_{TH}) \tag{19}$$

giving the PDE that governs the position and time dependant voltage along the FET channel

$$\frac{\partial}{\partial x}\left[\mu\, (v(x,t) - V_{TH}) \frac{\partial v(x,t)}{\partial x}\right] = \frac{\partial v(x,t)}{\partial t} \tag{20}$$

This partial differential equation could only be solved numerically, and it has been solved in[109]. The boundary conditions were set as:

$$v(0,t) = V_{RF} \sin \omega t + V_{GS} \tag{21}$$

$$v(L,t) = V_{GS} \tag{22}$$

where the gate-drain AC potential is well-tied together either via the external coupling capacitor C_{gd} for lower frequencies, or intrinsically via the C_n segmented-capacitors for higher frequencies. The solutions have shown that only a small portion of the channel, close to the drain-terminal where the gate-drain excitation takes place, exhibits signal propagation. The damping of the signal is exponential, and the remaining portion of the channel towards the source-end is composed of distributed parallel gate-channel capacitances and distributed series channel-resistances.

From the above formulation one would deduce the following:

- Mixing at Terahertz frequencies is possible due to the distributed nature of the channel, allowing distributed resistive self-mixing.
- The signals do not need to propagate entirely through the channel, and only a portion of the channel in the proximity of the coupling nodes is responsible for the mixing. Meaning, even lower technology nodes are capable of Terahertz detection.
- The un-modulated section of the channel where the signals could not propagate acts as an unused noise portion of the detector. Therefore, higher technology nodes with shorter channel length lead to lower thermal noise levels, in addition to the reduced detector parasitic capacitances that could enhance the detector efficiency.

In analogy with the case for over-damped plasma-wave dynamics (non-resonant case) presented by Dyakonov and Shur [69][110], the following PDE can be observed

$$-\frac{C'}{e}\frac{\partial v(x,t)}{\partial t} = \frac{\partial}{\partial x}\left[G_{ds}(x)\, \frac{\partial v(x)}{\partial x}\right] \tag{23}$$

which resembles the non-quasi-static modelling of distributed resistive self-mixing within the transistor.

$$\frac{\partial}{\partial x}\left[G\big(v(x,t)\big)\frac{\partial\, v(x,t)}{\partial x}\right] = C_{ox} W \frac{\partial\, v(x,t)}{\partial t} \tag{24}$$

Therefore, and in contrast with the plasma-based explanation, this NQS modelling explains the mixing process from circuit theory arising from the intrinsic segmentation of the FET transistor. However, this model assumes a gradual channel approximation of the Poisson equation. It also assumes uniform carrier density, drift velocity and potential profiles along the channel, and the absence of hot-carrier effects. Therefore, the validity of the PDE model is gradually lost at higher frequencies if smaller transistors and larger field gradients are used. Accordingly, more accurate

modelling for deep-submicron structures should employ the Boltzmann's transport equation or the Wigner-Boltzmann [111].

2.2. Circuits Schematics for Terahertz Detection

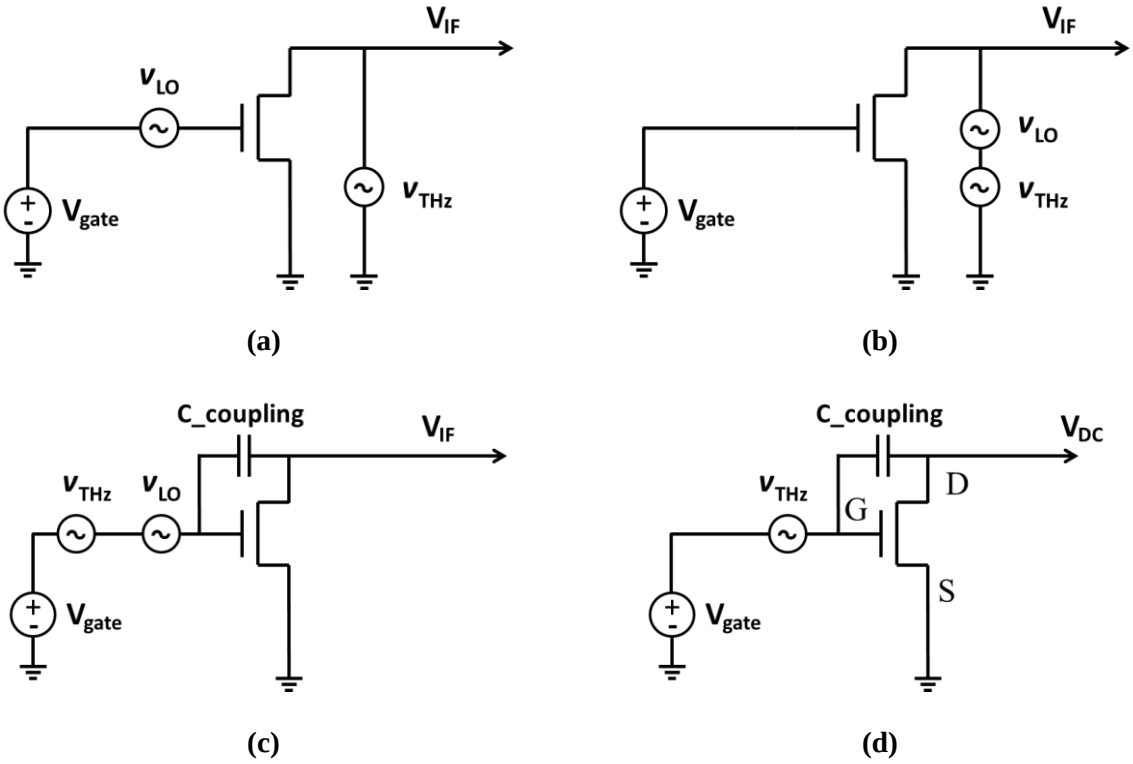


Figure 2-5: (a-c) Terahertz heterodyne detection topologies using passive FETs in common-mode and (d) Terahertz direct detection topologies using passive FETs in common-mode [72] .

Building upon the above derived theory of Terahertz mixing, one could design a variety of Terahertz detection circuits that operate at room temperature. These circuits range from direct detection (zero IF output) through self-mixing of the incident THz radiation, homodyne detection (zero IF output) where two sources of the same frequency are used, or heterodyne detection (low IF output) where two sources with different frequencies are used to produce an output IF at the difference frequency. For heterodyning, usually one of them is an on-chip or off-chip local oscillator or both frequencies are provided spatially in the case of heterodyne detection.

2.2.1. Single-ended THz detectors for Heterodyne and Direct Detection:

Resorting back to the original transistor models for an FET in the Ohmic region, the drain to source current with respect to the gate to source and drain to source time harmonics is expressed by (2)

$$i_{DS}(t) = \frac{W}{L}\,\mu\,C_{ox}\,(v_{GS}(t)\,v_{DS}(t) - V_{TH}\,v_{DS}(t) - \frac{v_{DS}^2}{2}) \qquad (2)$$

From this relation there exist four different resistive circuit topologies shown in Figure 2-5 that create cross-modulation products. For the resistive mode, where the transistor is unbiased at its drain, the following could be observed:

Hetero/Homodyne detection:

- The first term of (2), $v_{GS}(t)\, v_{DS}(t)$, shows that the RF could be applied to the gate-source terminals and the LO to the drain-source, or vice-versa, and the circuit is shown in Figure 2-5.a
- The last term of (2), $\frac{v_{DS}^2}{2}$, shows that sum of the RF and the LO could be applied to the drain-source terminals, as shown in Figure 2-5.b

Direct detection and hetero/homodyne detection:

- Utilizing the first term of (2), $v_{GS}(t)\, v_{DS}(t)$, shows that direct detection could only be attained by using an external coupling capacitor to create an AC short-circuit between the gate and the drain terminals. Then, the RF (and another LO in the case of hetero/homodyne detection) could be applied to the gate-source or the drain-source terminals, and the circuit is shown in Figure 2-5.c,d. However, as explained in section 2.2.2, the non-quasi static transistor modelling reveals that the intrinsic transistor oxide capacitance is responsible for tying the gate to the drain, to act as an AC short-circuit. Yet, the external capacitor creates a better AC-shunt at lower frequencies for broadband detection.

Direct detection circuits are favoured for their ultra-low power consumption due to the unbiased transistors as well as the fact that no local oscillators are needed. The operation is normally at room temperature, and no cooling is required to attain good sensitivities. They also exhibit ultra-wide bandwidth properties. However their sensitivities are inferior to homodyne and heterodyne detectors. Besides, as the output is at DC the system is hit by the very high 1/f noise of the readout circuitry.

Detector Chopping:

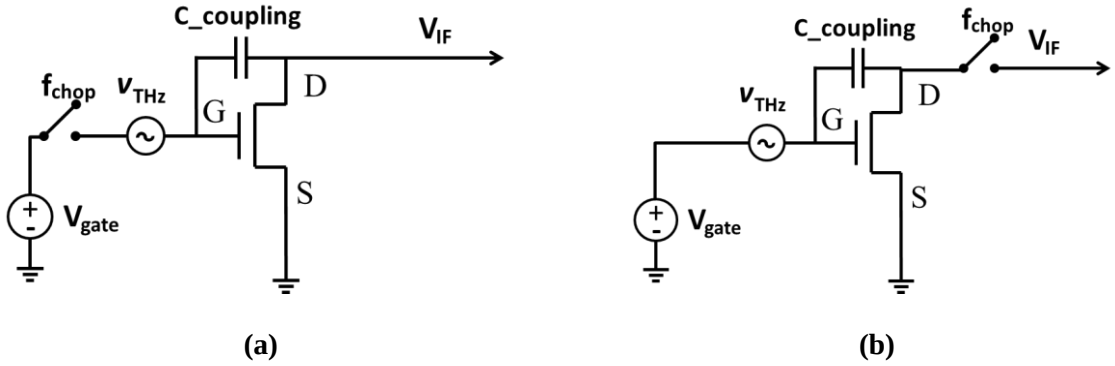


Figure 2-6: FET detector chopping to reduce 1/f noise (a) at the gate and (b) at the output.

One method to overcome the 1/f noise is to pulse or amplitude-modulate the source frequency at a frequency f_{chop} which consequently shifts the output DC voltage by Δf_{chop} away from the pink-noise levels. Of course this depends on the availability of the equipment allowing electronic chopping at the source-end. Otherwise, on/off modulation could be employed at the gate of the transistors as shown in Figure 2-6.a with a LOW/HIGH switched biasing levels ranging between, for example, $V_{gate} = 0.3V\ up\ to\ 0.4V$ where the transistor is in the detection mode, at a switch rate of f_{chop} at 1-kHz. In this case, the effective gate bias would be $V_{average} = 0.35V$ where the transistor is in the detection

mode, and a 1-kHz signal will always exist at the output node of the detector without a THz input power. In the presence of the THz input power, an offset voltage would appear atop the 1-kHz signal, proportional to the input power. The chopping could also be employed at the output of the detector as in Figure 2-6.b, yet this induces switching-noise into the readout chain. Both chopping techniques will translate the 1/f noise of the detector by the chopping rate, yet will help avoid the 1/f noise of the readout chain. This method could be designed as part of a chopped instrumentation amplifier at the detector output.

The same concepts described here could also be used in the presence of a modulated input THz signal. In this case, further low-frequency mixing takes place within the transistor, and the signal appears at the sums and differences of the mixed modulation frequencies.

2.2.2. Differential gate-drain coupled THz detectors (Direct Detection):

Figure 2-7 shows a schematic diagram of a differential square-law detector circuit based on NFET transistors with non-biased (cold) channels with coupling supplied to the gates of the transistors. The gates of the differential NFET pair T1/T2 are provided with the received terahertz signal from the THz balanced antenna. The received signals at both nodes are 180 degrees out of phase and their amplitude is half of the total signal voltage, each.

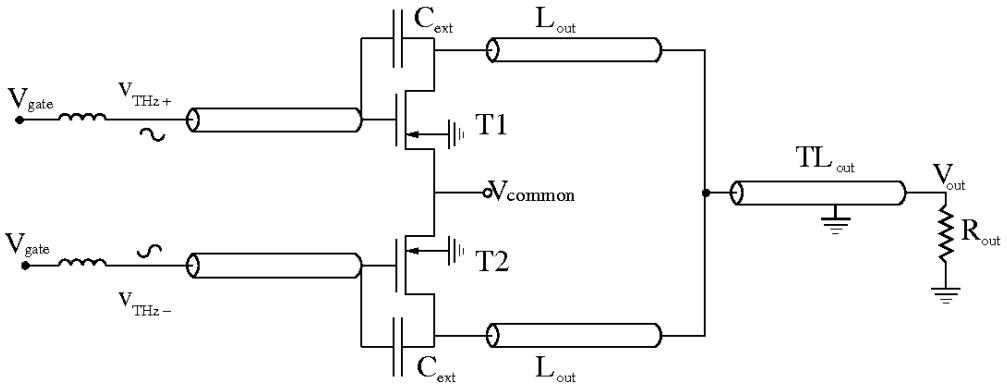


Figure 2-7: Differential THz direct detector based with the signals fed through the gate

A gate-bias voltage V_{gate} is also applied through the antenna. Since the common mode voltage V_{common} forms a virtual ground, half of the input signal appears as a time varying $v_{gs}(t)$ gate-source voltage across each transistor. Two large MOS coupling capacitors C1/C2 are used to tie the drain potentials of the transistors to their respective gates at terahertz frequencies.

Effectively, as described in the non-quasi static analysis, the intrinsic gate oxide capacitances play the role of the coupling capacitors. Hence, the $v_{ds}(t)$ voltage across the channel shifts simultaneously with the $v_{gs}(t) - modulated$ channel conductance over a period of the terahertz wave, thus generating a dc current by square-law detection. Two quarter-wave long transmission-line stubs L_{out} are used to extract the generated DC signal to the on-chip or off-chip amplifier without disturbing the terahertz signal at the drain nodes.

This differential circuit topology necessitates the implementation of the external capacitors for better RF coupling. This means it is space consuming and more difficult in terms of layout implementation to insure proper signal propagation and coupling especially at THz frequencies where any

modification of the signal leads is a significant modification of both the impedance levels and the signal properties.

This topology also exhibits a narrow-band performance due to the transmission line stubs at the outputs, which could be seen as a benefit for frequency-selective applications or an impediment for applications with spectroscopic characteristics.

2.2.3. Differential source coupled THz detectors (Direct Detection):

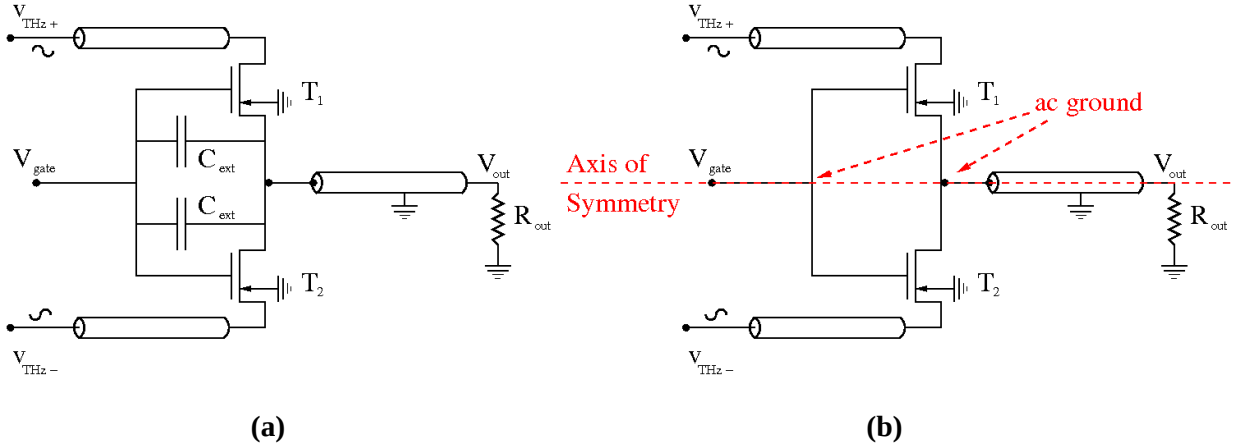


Figure 2-8: Differential THz direct detector based with the signals fed through the source. (a) Differential structure of the FET broadband THz resistive self-mixer (b) with the virtual ground shown.

Contrary to the gate-driven approach, there exists a more favourable circuit topology for THz detection with much wider bandwidth characteristics. Figure 2-8 shows a differential circuit schematic square-law terahertz detector based on signal coupling through the transistors sources. In contrast to the gate-drain coupling approach presented above, the RF power from the antenna is provided to the source terminals of the two NMOS transistors Tl and T2 in the present design. The gate and drain terminals of the transistors are connected together, thus creating virtual grounds for the RF voltage.

In this balanced configuration, half of the RF signal generated by the antenna appears as a $v_{gs}(t)$ voltage across the gate-source junctions of each transistor and contributes to the distributed self-mixing process in the channel. The rectified output current or voltage is extracted from the shared drain node. This configuration eliminates the need for quarter-wave stubs and coupling capacitors, which are necessary in the gate-driven detector design in order to tie the RF potential of the gate and drain together and to provide isolation of the output port from the antenna. Hence, a wider operating bandwidth can be obtained with the source-driven detector than with the gate-driven one.

2.3. Characterization of Terahertz Detectors

2.3.1. Figures of Merit

Direct THz power detectors performance is characterised by the responsivity $\Re$v and the noise equivalent power NEP. These figures of merit could be presented as the *optical* or the *electrical* responsivities. The ideal electrical Responsivity and NEP of a THz detector assume a 100% coupling efficiency and a total impedance-match. The current Responsivity $\Re$i is expressed in [A/W] and voltage Responsivity $\Re$v is expressed in [V/W].

The voltage electrical-responsivity and current electrical-responsivity ($\Re_{\mathrm{v}}$ and $\Re_{\mathrm{i}}$, respectively) of the detector are measures of how much output voltage or current a detector is capable of generating from a certain input power. These electrical responsivities are calculated from the detected output voltage divided by the available power to a pixel as follows:

$$\Re_{\mathrm{v}} = \frac{V_{out}}{P_{in}} \tag{25}$$

$$\Re_{\mathrm{i}} = \frac{I_{out}}{P_{in}} \tag{26}$$

The noise-equivalent power is a measure of input power of the detectors where the SNR reaches unity; i.e. defining the detectors power-sensitivity. The voltage-referred electrical noise-equivalent power (NEP) is then derived from the measured detector noise voltage variance divided by the voltage responsivity, $\Re_{\mathrm{v}}$:

$$NEP_v = \frac{\sqrt{N_v}}{\Re_{\mathrm{v}}} = \frac{\sqrt{\bar{v}_n^2}}{\Re_{\mathrm{v}}} \tag{27}$$

In the case of cold-FETs, the noise voltage is theoretically dominated by thermal noise arising from the channel resistance. The thermal noise is calculated from the well-known Johnson-Nyquist noise relationship with the Rayleigh-Jeans approximation $\bar{v}_n^2 = 4k_BTBR$, where k is the Boltzmann constant $k_B = 1.3806488 \times 10^{-23}\, m^2\,\mathrm{kg}\, s^{-2}\, K^{-1}$, T is the temperature in Kelvin, B is the bandwidth in Hertz, R is the resistance in Ohms. Accordingly, the voltage noise equivalent power could be estimated to be

$$NEP_v = \frac{\sqrt{4kTBR}}{\Re_{\mathrm{v}}} = \sqrt{\frac{4^3 kT(v_{GS}-V_{TH})}{R_{in}^2\left(\frac{W}{L}\right)\mu C_{ox}}} \tag{28}$$

Similarly, the current noise equivalent power could be calculated from the measured noise current and the calculated current responsivity as follows:

$$NEP_i = \frac{\sqrt{N_i}}{\Re_{\mathrm{i}}} = \frac{\sqrt{\bar{i}_n^2}}{\Re_{\mathrm{i}}} \tag{29}$$

$$NEP_i = \frac{\sqrt{\frac{4kTB}{G}}}{\Re_{\mathrm{v}}} \tag{30}$$

However, the estimation of the noise equivalent power based only on the thermal noise is not complete, as it does not account for the 1/f flicker-noise arising from the mixing-process itself within the FET. The next chapters will thoroughly discuss the issue of noise. The noise analysis will show that at certain input power-levels and output loading conditions the THz detector is capable of generating enough voltage to sustain a self-bias even within cold-FETs, and in return increasing the flicker-noise levels. Also it will show high 1/f noise levels exist in the FETs with relatively high 1/f knees means that the performance is highly dependent on the modulation frequency of the transmitted THz frequencies.

On the other hand, the responsivities and noise-equivalent powers defined here assume a 100% efficiency of power reception; i.e. the electrical figures of merit. This is a measure that allows differentiating between the optical and the electrical responsivity and noise-equivalent power, where the optical figures of merit are more realistically application oriented. The optical measures characterise the actual performance of the system. In return, an optimum is attained for a performance that equates the optical responsivity to the electrical responsivity. This basically means attaining highest electrical performances is fundamentally based on the detection circuit design; however, attaining the highest overall performance requires the best possible power harvesting (antenna coupling efficiency) and signal delivery to the detectors as well as minimum signal losses. Hereafter, a consistent co-design between the electrical and optical chains is of utter necessity, and we will be expanded in the following sections.

Defining the Detector input power:

Following the above discussions, the available power received per pixel should be quantified to calculate the detector's optical FOMs. Here we elaborate; the optical responsivity therefore is based on the received power at the antenna/air interface. For a diverging beam from a point source located at a distance R from detector antenna, the received power P_{in} can be calculated using the *Friis Transmission Equation*:

$$P_r = P_t\, G_t\, \frac{A_{eff}}{4\pi R^2} \tag{31}$$

Where P_t is the total transmitted power in Watts, G_t is the gain of the transmit antenna, A_{eff} is the effective area of the receive-antenna, R is the distance in metres separating the receiver from the source.

To estimate the electrical FOMs, the actual power received at the detector input needs to be quantified. Further parameters should be included. As this link comprises of antennas at both ends of the chain, polarization and alignment of antennas and impedance mismatches as well as signal damping are included as follows:

$$P_{r,det} = P_t\; D_t(\theta_t, \emptyset_t)\, D_r(\theta_r, \emptyset_r)\, \left(\frac{\lambda}{4\pi R}\right)^2 e^{(-\alpha R)}\, (1 - |\Gamma_t|^2)\, (1 - |\Gamma_r|^2)\, |p_t p_r^*|^2\, (1 - R_s) \tag{32}$$

Where:

- $D_t(\theta_t, \emptyset_t)$ is the transmitting antenna directivity as a function of the antenna misalignment defined by vertical θ_t and horizontal $\emptyset_t$ tilts with respect to the bore-site
- $D_r(\theta_r, \emptyset_r)$ is the receiving antenna directivity as a function of the antenna misalignment defined by vertical θ_r and horizontal $\emptyset_r$ tilts with respect to the bore-site

- λ is the wavelength in metres
- R is the distance from the source to the detector in metres
- $e^{(-\alpha R)}$ is the distance-dependant damping factor based on the α absorption coefficient and the distance R separating the receiver and the detector
- Γ_t and Γ_r are the transmitting and receiving antennas reflection coefficients, respectively, derived from the antenna-detector impedance mismatch
- R_s is the Fresnel reflection coefficient at the air-silicon interface
- p_t and p_r^* are the polarisation vectors of the transmitting and receiving antennas, respectively

This equation highlights the importance of antenna alignment, polarization and impedance match to attain a higher received power at the detector input relative to the power available at the antenna/air interface. However, for optical responsivity measures, the received power should be quantified according to (31) as it is a true measure of the operating system.

The effective area of the receive-antenna could be accounted for as the physical area of the detector in an FPA arrangement without silicon lenses, based on the assumption that neighbouring pixels share the received power spills at their apertures and therefore will only receive as much as their physical areas, as explained in [109]. Applying the same logic to a lens supported detector, i.e. the physical area of the hemisphere projected onto the direction normal to the propagation direction of the incident wave, we get an A_{eff} equivalent to πR^2, where R is the radius of the collecting aperture. This result overestimates the real effective area but it gives an upper boundary of the calculated responsivity and is based on the assumption that real effective area of the aperture antenna is never larger than its physical area. The receive-antenna gain is calculated as follows:

$$G_r = \frac{4\pi A_{eff}}{\lambda^2} \tag{33}$$

The directivity could also be simulated using commercial full-wave 3D Electromagnetic simulators such as HFSS or EM-Pro or estimated based on [112]. Plus, the directivity should be measured using a well-defined and precise antenna measurement setup, as explained in [81].

As for the lens-equipped detector, if the lens is not AR coated, a minimum of 30 % of the incident power is reflected back, using the Fresnel equation:

$$R_s = \left[\frac{n-1}{n+1}\right]^2 \tag{34}$$

Voltage Dynamic Range

Another important measure defining the detector performance is the output voltage dynamic range. This is defined by the maximum output voltage (related to the maximum responsivity) divided by the noise-floor voltage. This could be reported in dBV, and it defines the output levels to be quantized for imaging, and it largely assists the design of the analogue circuitry. Also, a wider voltage dynamic range directly impacts the image quality and contrast

2.3.2. *Measurement Configurations*

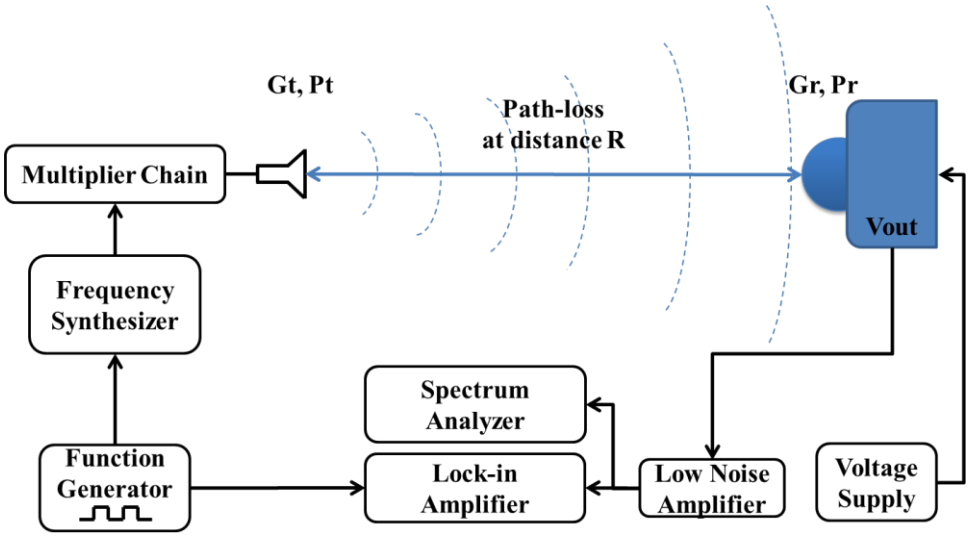


Figure 2-9: Free-space characterization setup for a pixel by means of lock-in techniques. The path-loss is calculated according to *Friis transmission equation*. In the case of a multi-pixel camera, the ROC is off and the terahertz source is modulated (non-video mode).

2.3.2.1. *Single-pixel detector (direct detectors) characterisation*

THz direct detectors are characterized in a free space measurement setup as shown in Figure 2-9. In this case, pixels are characterized by means of lock-in techniques in accordance with the *Friis transmission equation*. Should a multi-pixel camera be used, the readout controller (ROC) is switched off and the pixel under test is permanently selected. Otherwise, in a single pixel setup the pixel is powered up. The detector and source should be placed in their corresponding far-fields for the *Friis* equation to be valid, and should be aligned for maximum power reception.

The challenge arises from the fact that the $\Re_v$ calculation requires accurate knowledge of the pixel input power P_{in}. Therefore, this method requires accurate specifications of the source antenna gain, the receiver directivity and further requires precision alignment in the far-field of the high-gain receiver antenna. For instance, in the case of high-gain receiver antenna the far-field could be at a distance of 1m. Once P_{in} is known, the responsivity and the NEP can be derived from DC measurements of the output signal V_{out} and spot noise V_N measured at the chopping frequency.

Figure 2-9 illustrates a typical measurement setup used to characterize a standalone pixel in non-video mode. It comprises of the following electronic and mechanical equipment:

- A frequency synthesizer could be AM or pulse modulated with a frequency-tuneable square-wave. The purpose of the AM modulation is to facilitate detection in the presence of a DC-offset and a 1/f -noise floor.
- A frequency multiplier that multiplies the signals provided by the synthesizer. Commercial THz sources use diagonal horn antennas to couple and radiate the THz waves
- An absolute-power calorimeter at the wave-guide port of the source antenna to calibrate the source output power at the various source frequencies.

- A spectrum analyser or a lock-in amplifier read and visualize the pixel output voltage and the spot-noise at the modulation frequency. The lock-in amplifier requires a reference signal from the frequency synthesiser.
- Tuneable voltage supplies for the detectors.
- External low-noise voltage amplifiers for voltage-mode readout or current amplifiers for current-mode readout. The amplification factor should be deducted from the measured output voltage or current levels when calculating the figures of merit.
- Mechanical positioning motors and axis for detector/source alignment.

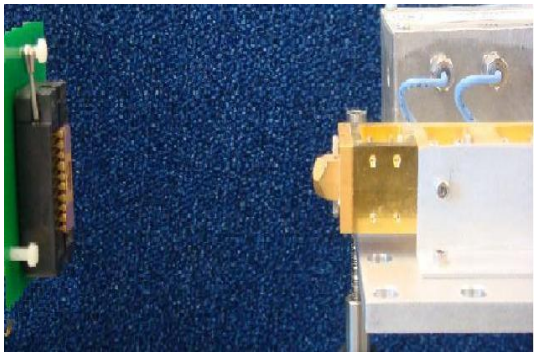


Figure 2-10: Photograph of a *VDI source* at 0.65THz equipped with a diagonal horn antenna illuminating a CMOS THz detector in free-space [60].

Figure 2-10 shows an optical photograph of a typical measurement setup comprising of a 0.65THz source from *VDI* [60] equipped with a diagonal-horn antenna, and a CMOS THz detector array mounted on a FR4 PCB board.

Such a measurement setup is useful for the characterisation of single pixel, either in a standalone detector topology or within a matrix of detectors. In this case, however, when a matrix is operated in video-mode it is essential to also characterise the entire matrix performance where switching-noise and on-chip amplification account to the majority of the overall performance. Note that in this measurement the NEP depends on the chopping frequency for a non-flat noise power spectral density. Therefore, the total NEP which is the integral of the NEP over the video bandwidth is a more relevant parameter in video-mode.

2.3.2.2. Multi-pixel camera characterisation in video-mode

In the case of a multiple pixel matrix the non-video mode of characterisation is not a relevant representation of the camera in operation as switching noise should be accounted for. A direct method of camera characterization at video-rates is shown in Figure 2-11. A continuous-wave (CW) source illuminates the camera. In this case, the source is not modulated. The idea of this setup is to squeeze the output power from the THz-source into the camera aperture. This method requires the use of plastic lenses that are transparent to THz radiation and exhibit low losses. The terahertz beam is focused onto the silicon lens in order to ensure that all the available source power is projected onto the Si-lens aperture. The impinging source power should also be measured with an absolute-power calorimeter after the PTFE lens and in front of the camera module to account for the losses after the optical chain. The beam normally splits over some of the pixels of the FPA. Overall, the camera responsivity $\Re_v$ can be calculated as the sum of the array response divided by the total available input power as

$$\Re_{v,TOTAL} = \frac{\sum_{pixel=1}^{n\ pixels} V_{pixel}}{P_{in}} \quad (35)$$

In this video-mode, the source is running continuously and the noise is integrated over the full video bandwidth BW. The $NEP_{v,TOTAL}$ is calculated from the measured total RMS image noise $V_{n,TOTAL}$ divided by the camera responsivity as

$$NEP_{v,TOTAL} = \frac{V_{n,TOTAL}}{\Re_{v,TOTAL}} \quad (36)$$

Note, that the $NEP_{v,TOTAL}$ presents an average over more than one pixel, and therefore, includes pixel-to-pixel variations. The NEP per $\sqrt{Hz}$ can be calculated from the analog video bandwidth (BW) of the camera module as $NEP = \frac{NEP_{v,TOTAL}}{\sqrt{BW}}$. However, this supposes a flat noise power spectral density which is not the actual case with the frequency dependant 1/f- noise.

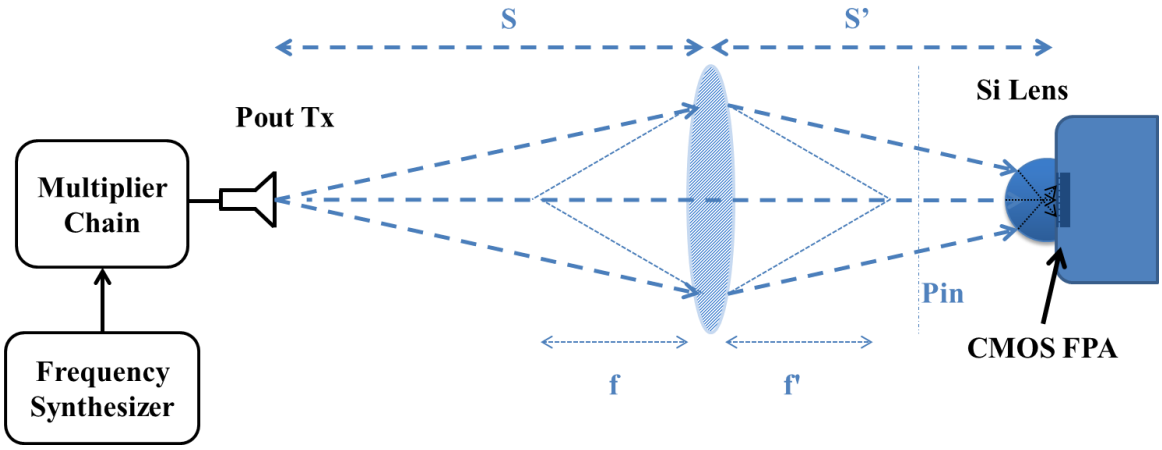


Figure 2-11: Video camera characterization setup. The setup is adjusted to squeeze the emitted radiation onto the FPA at an angle that counter-effects the lens *field of view*.

2.4. Chapter Conclusions

In this chapter the quasi-static and non-quasi static equations that explain Terahertz mixing in FETs were derived. Various mixer topologies for direct and heterodyne mixing in CMOS were then presented in single-ended and differential output topologies. Ideas for detector chopping were presented to reduce the effect of 1/f noise in the detectors at lower frequencies.

Figures of merit for direct detection with a demonstration of different measurement techniques were presented for single pixel and multi-pixel FPA imagers. The next chapter will be an expansion of this one, with an in depth analysis of the design, optimisation, and operation of THz direct detectors according to the EM and Electrical parameters.

Chapter III- Design Methodologies for Efficient Terahertz Detection in CMOS

In view of the theory of detection and the various circuit realisations as well as the figures of merit discussed in chapter 2, this chapter discusses design techniques for efficient THz direct detection. This design philosophy entails both efficient THz radiation coupling to the detectors and efficient THz mixing and readout.

Efficient radiation coupling necessitates the knowledge of the entire quasi-optical chain, including radiation polarization, beam-form, antenna/lens reflections, antenna gain, substrate and metal loss mechanisms, as well as antenna/detector impedance match.

Efficient detector mixing requires insight into the electrical properties of the MOS detectors, substrate losses, parasitics, detector noise model, as well as output impedance and readout schemes. However, various parameters mutually influence one another, as will be seen soon. Therefore, the need for electrical and electromagnetic co-design reveals itself for the Terahertz designers, and will be presented in the following section.

This chapter is dedicated to explaining the design methodology of single pixel Terahertz direct detectors in CMOS based on resistive mixing. A theoretical investigation backed by implemented and characterised designs in various technology nodes, packaging topologies and measurements boundary conditions have led to a thorough understanding of the detection principles and constraints. This amounts to a profound set of parameters guiding the design methodology.

Implementation details and results for THz detectors in 65nm Bulk CMOS and 28nm FDSOI CMOS will be shown in two subsections subsequently. Eventually, the resultants of these investigations will converge into a generic methodology for Terahertz receiver design, and will lay grounds for the design of multi-pixel Terahertz focal-plane array (FPA) imagers that will be shown in Chapter IV.

3.1. Terahertz Mixer Design

A typical Terahertz detection circuit is shown in Figure 3-1. It comprises of the three main levels: the THz Antenna, the THz mixer, and the output loading and analogue/digital readout. All levels are interrelated at the electrical and quasi-optical levels. Design of multi-pixel THz cameras require further levels, and will be discussed in chapter 4.

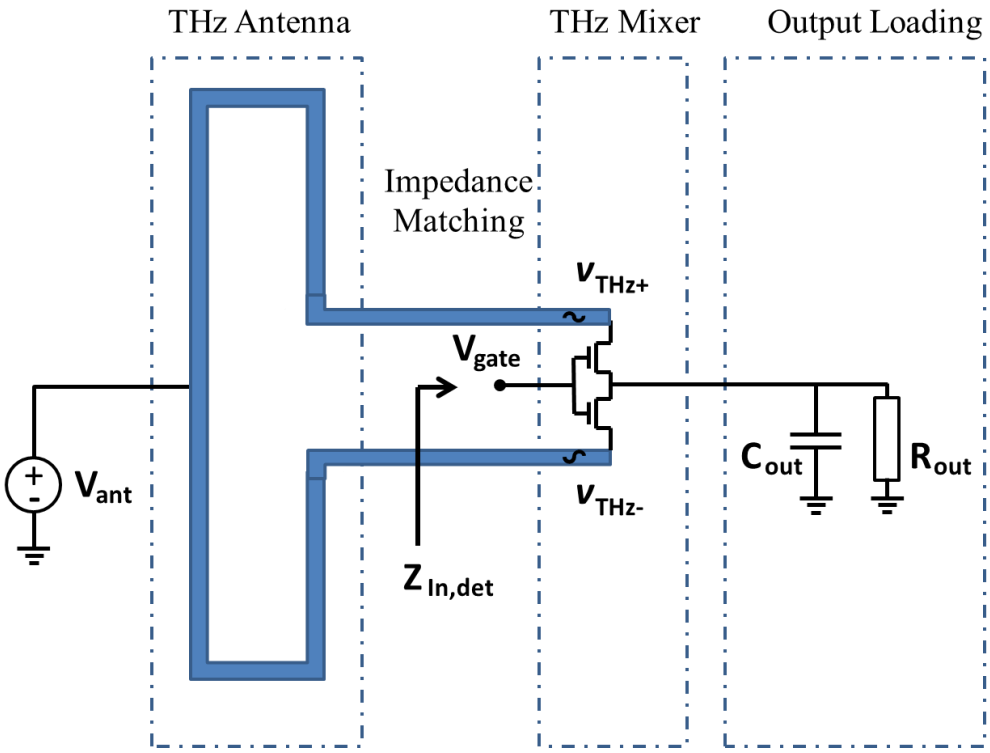


Figure 3-1: Terahertz detector basic building blocks

DC and RF characteristics

The main aim is to maximize $\Re_v$ and minimize NEP. However, It is hard to define a unique set of $\Re_v$ and NEP values defining the detector performance. Both quantities are frequency dependant and multiple parameters influence one another. The transistor sizing and impedance matching will be discussed hereafter in view of the various parameters. They will be presented as per simulations using the PDK's non-quasi static models based on PSP models.

The major design considerations could be arranged in the following categories:

- *Complex-conjugate impedance matching* at the antenna-detector interface: This varies according to the transistor sizing and the detector topology (Detector topologies: source coupled or gate-drain coupled topology; differential or single ended detection).
- *Antenna efficiency and gain*: The efficiency is an EM requirement as it defines the ability to couple the Electromagnetic radiation and transform it to an electrical current. The gain on the other hand defines the directivity and efficiency of the antenna.

- The load impedance at the detector output (R_{out} and C_{out}) with respect to the detector mode of operation, the voltage readout or current readout. The output loading impacts the theoretical responsivities that vary in the three distinct biasing regions of the FETs. For instance, the sub-threshold region with voltage-mode readout favours high load impedance due to the high channel resistivity. Capacitive loading has a degrading influence on the high-frequency output signals in case of chopping.
- The THz signal power level: This varies from the minimum detectable levels up to the saturation levels of the THz-detector.
- Transistor dimensioning: The current responsivity increases proportionally to the transistor W and inverse-proportionally to the transistor L. The voltage responsivity, however, increases with the increase of the detector input impedance defined by shrinkage of both W and L. Yet, the combination of W and L comes at the cost of varying the noise performance in both level and nature. The NEP is proportional to $\sqrt{L}$ and inversely proportional to $\sqrt{W}$, but at the same is inversely proportional to the input impedance, as shown in equation (33). High transistor responsivity could potentially self-bias the cold FETs, and therefore flicker noise becomes considerable. Furthermore, device dimensioning should be considered in view of the feasible antenna design, as impedance requirements could become stringent or unrealistic.
- Output voltage levels: this sets the voltage dynamic range. Naked detectors with off-chip detectors could yield ultra-low noise levels and signal measurement sensitivity. However this sensitivity is impacted by the readout minimum readable signal, and thus a strong enough detector output is necessary to result in a decent voltage dynamic range.

These challenges are analysed and detailed afterwards. However, it is essential to note that any realistic design is always challenged by the system-level requirements as well as the available equipment. As explained earlier, sources are limited in power and therefore increasing detector sensitivity is essential to harvest as most as possible of these available signals.

3.1.1. Device Dimensioning and Detector Operation Mode

Equation 13 represents the output current relation with the input power when operating the detector in *current-mode*, that is to say when the detector is shorted at the output. I_{ds} is directly proportional to the transistor physical width, W, the carrier mobility, μ, and inversely proportional to the transistor channel length, L.

I_{ds} is also proportional to the power of the RF signal, which is equivalent to the square of the voltage drop across the detector generated by this RF signal. The RF signal power is fixed, and is merely defined by the link-budget and the coupling efficiency, as will be detailed later. However, the voltage drop across the detector is proportional to the square-root of the signal power multiplied by the input impedance, and could only be increased with the increase of the input impedance from Ohm's-law

$$V_{RF} = \sqrt{P_{RF} \times Z_{in,detector}} \tag{37}$$

From this relation we can conclude two important factors that impact the output current. First, to increase I_{ds} the detector input impedance should be increased to create a larger V_{RF}, however this should be attained in view of the W/L proportionality, as described above. The designer should take into account the fact that decreasing both W and L lead to a higher input impedance, yet I_{ds} also

requires W to be increased. Therefore, the designer should maintain the shortest channel length possible, with a mutually designed input-impedance versus channel width design trade-off.

Second, it is not enough to design for high detector input impedance regardless of the antenna impedance. The input impedance of the transistors is defined by the detection topology and its device dimensions, and is related to the intrinsic capacitive elements at the junctions and oxide as well as the bias-dependant channel resistance. For a maximum power transfer from the source, defined here by the antenna, to the load, defined by the detector, the source complex impedance should be equal to the complex conjugate of the load complex impedance. This is also understood from transmission-line theory, where the reflection coefficient Γ is zero only when:

$$Z_{in,antenna} = Z^{*}_{in,detector} \tag{38}$$

Where:

$Z_{in,detector}$ is the input impendance of the detector

$Z_{in,antenna}$ is the input impedance of the antenna

And * denotes the complex conjugate of the input impedance of the detector; leading to $\Gamma = 0$, given by

$$\Gamma = \frac{Z_{in,detector} - Z_{in,antenna}}{Z_{in,detector} + Z_{in,antenna}} \tag{39}$$

Therefore, any antenna/detector mismatch would create reflections at their plane of discontinuity, and a portion of the signal will be reflected back to be dissipated in or re-radiated by the antenna.

To conclude this section on current mode detector operation, the device input impedance should be increased to attain a higher voltage drop created by the received THz signal. At the same time, the antenna should be designed to form a complex-conjugate match to the detector input impedance. Of course one would assume that the highest detector input impedance would create the largest voltage drop, however this sets unreasonable antenna impedance requirements. Therefore the device dimensioning comes hand-in-hand with the feasible antenna design, as will be discussed in the following section.

Accordingly, the maximum power delivered to the FET at total impedance match is calculated to be

$$P_{in,antenna} = \frac{1}{4\, Z_{in,detecor}} v_{rf}^{2} \tag{40}$$

On the other hand, equation 14 presents a different behaviour for the *voltage mode* of operation of the Terahertz detector. By voltage-mode a high output-impedance that creates the largest output voltage signal, optimally an open-circuit, is assumed. In this case, the device width and length, W and L, respectively, cancel out from the numerator and denominator. The output voltage V_{DS} is therefore only proportional to the input voltage drop v_{rf} which is related directly to the impinging input power. As discussed above, this voltage drop is increased by increasing the input impedance of the detector. Here, though, the decrease of the channel width W is favourable alongside the decrease in the channel length L, contrary to the operation in current-mode. Therefore, whichever the device minimum dimensions allowed by the technology should be used to ascertain highest output voltage drops, in

ideal conditions. For example, in 65nm bulk CMOS technologies the smallest FETs are 300nm wide and 60nm long, and in 28nm FDSOI CMOS technologies the smallest FETs are 200nm wide and 28nm long for shortest channels; and 80nm wide by 60nm long for narrowest channels.

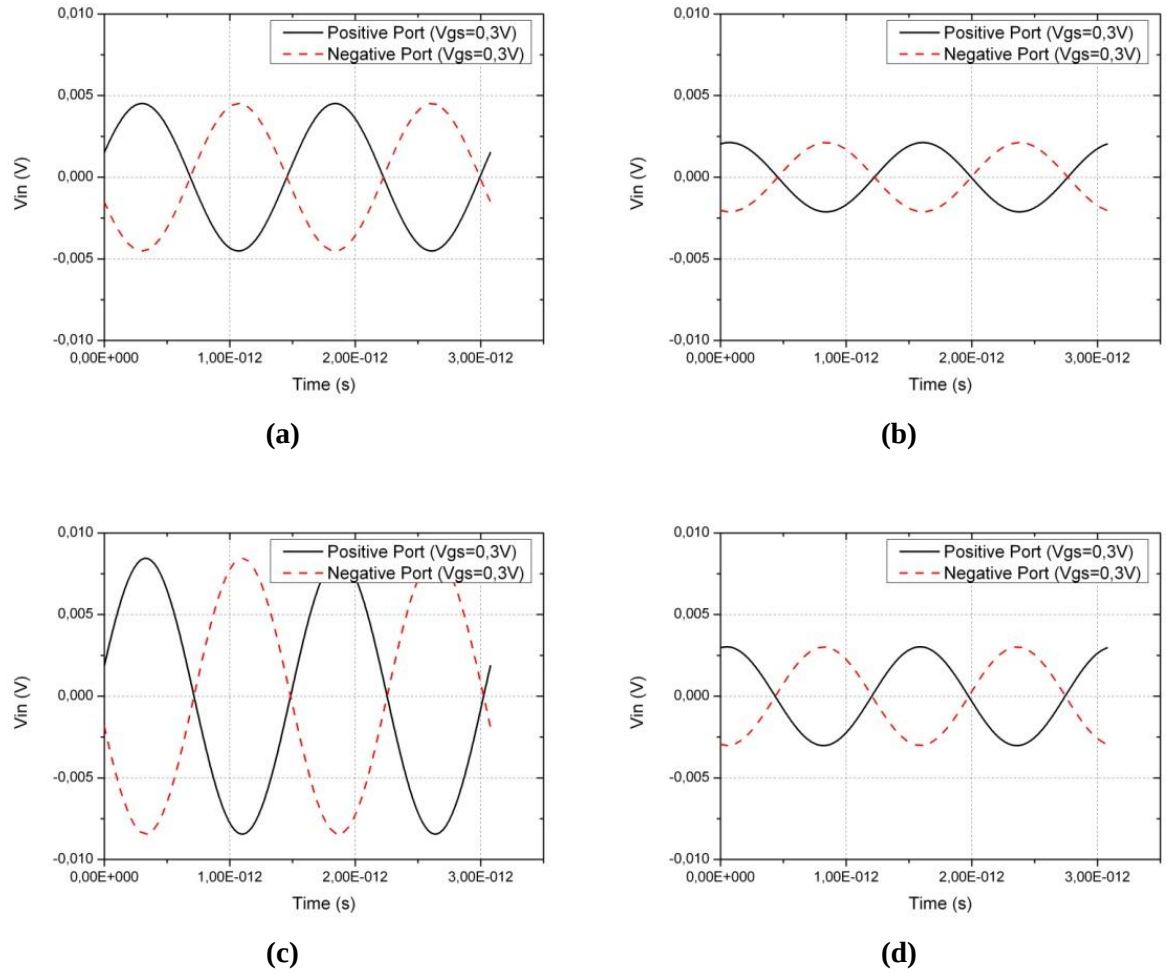


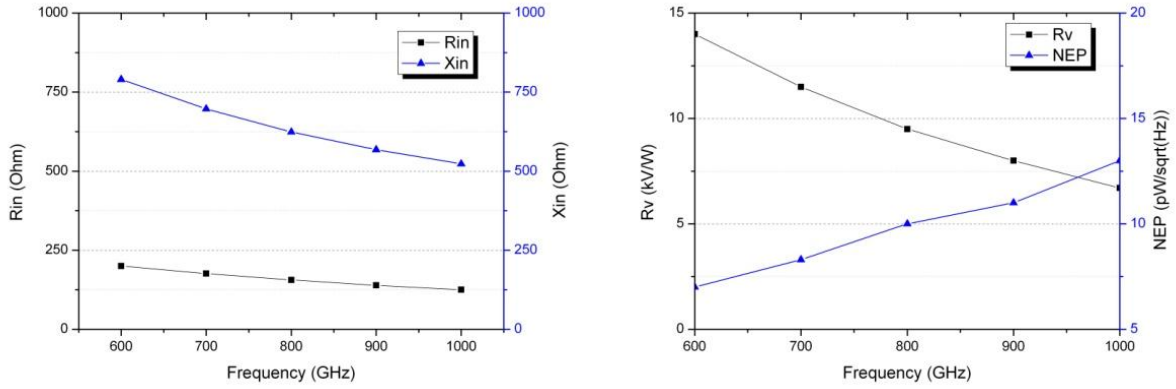
Figure 3-2: Simulated time-domain voltage swing at the differential ports of a source driven Terahertz detector in 65nm CMOS. The plots correspond to (a) matched and (b) mismatched 1µm/0.06µm detectors, and (c) matched and (d) mismatched 0.3µm/0.06µm detectors. The input power is set at 10nW for a 650GHz input frequency.

As in current-mode, the antenna impedance should exhibit a complex conjugate match to the detector input impedance to allow maximum power transfer. Matching is also gate-bias dependant, as the input impedances of the detectors largely vary as the channel is created.

Investigating the input impedances of the smallest FETs reveals extremely high resistive and capacitive impedance levels; setting utterly stringent requirements for antenna/detector impedance matching. This does not mean that these detector sizes are unfavourable, but rather a comparative study of the feasible antenna design with respect to the different sizes is required to dimension the detectors.

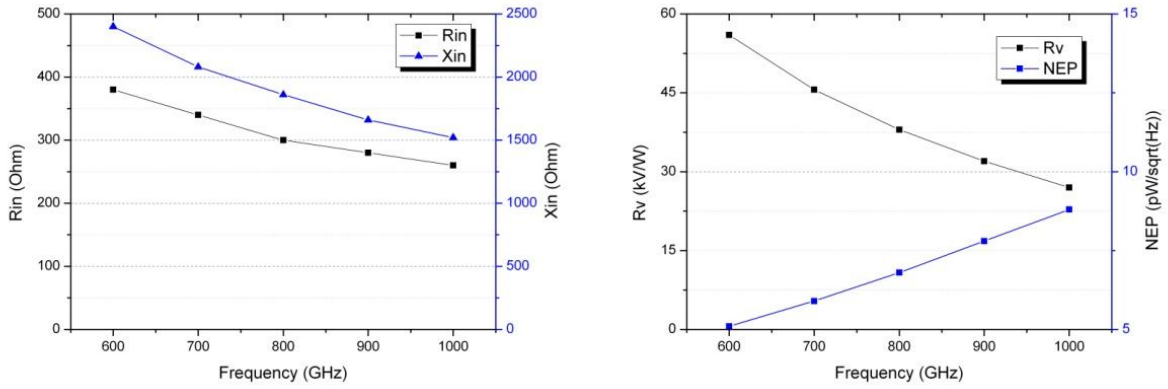
Figure 3-2 shows the voltage swing at both ports of source driven differential NFET THz circuits of various dimensions in 65nm bulk CMOS. The figure shows that smaller detectors create a larger

voltage drop at the inputs when the impedance is totally matched, and of course is attenuated due to reflections when mismatched. The wider detector exhibits a lower voltage at its input.



(a) **(b)**

Figure 3-3: (a) Optimum R_{in} and X_{in} at V_{GS}=0.4V and the corresponding (b) $\Re v$ at V_{GS}=0.15V and NEP at V_{GS}=0.3V based on harmonic balance simulations of source driven Terahertz detector of 1µm/0.06µm dimensions at 1-kHz chopping frequency. The input power is set at 10nW.



(a) **(b)**

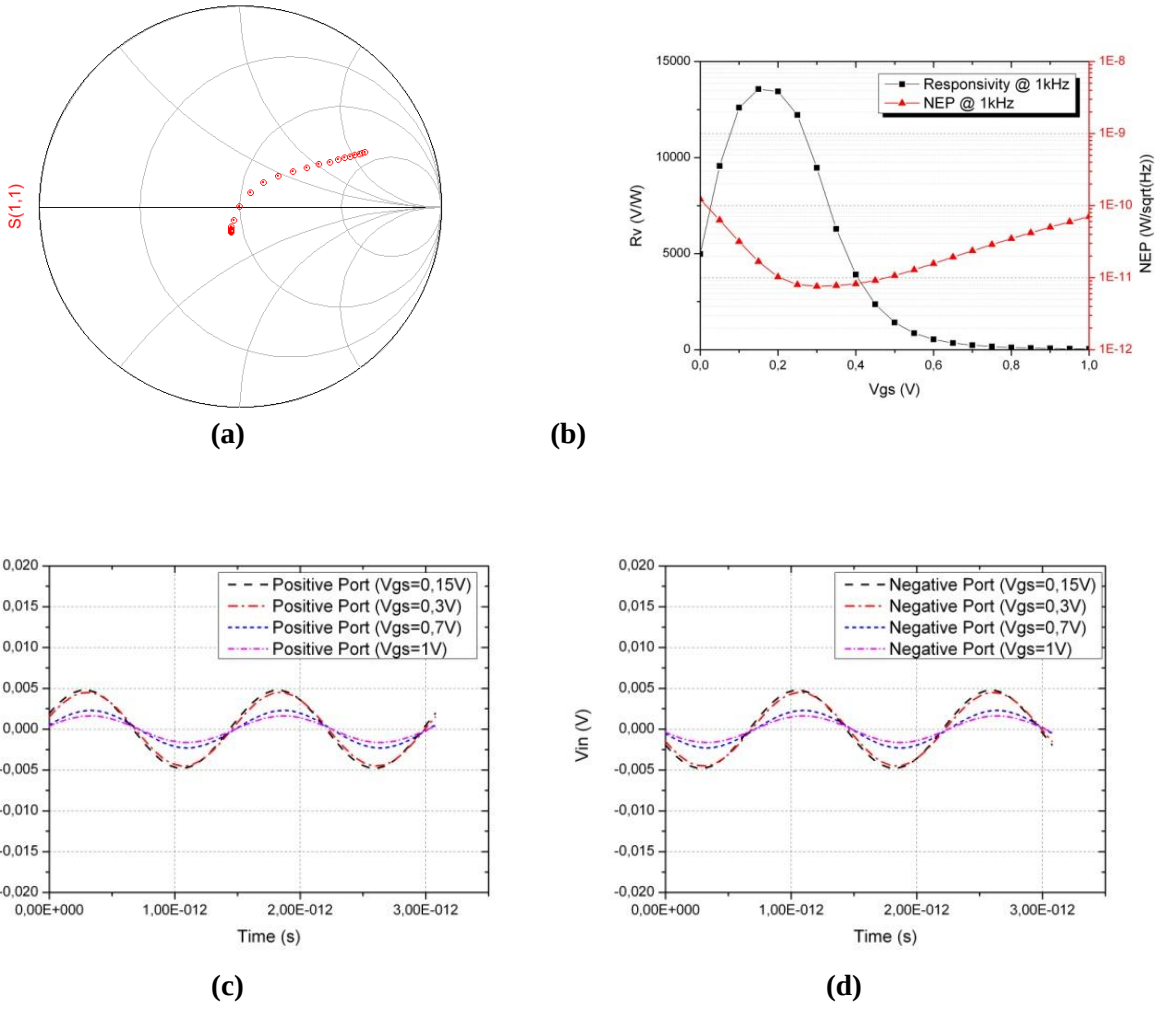
Figure 3-4: (a) Optimum R_{in} and X_{in} versus frequency at V_{GS}=0.4V and the corresponding (b) $\Re v$ at V_{GS}=0.2V and NEP at V_{GS}=0.3V based on harmonic balance simulations of source driven Terahertz detector of 0.3 µm/0.06 µm dimensions at 1-kHz chopping frequency. The input power is set at 10nW.

Optimizing detector $\Re v$ and NEP over a wide frequency range requires appropriate broadband match between antenna and detector devices to attain efficient RF signal transfer. The ideal antenna should be inductive in nature and must present high input impedance for both real and imaginary parts in order to match the parasitic capacitances and the channel resistance of the MOSFET in the sub-threshold and weak-inversion operation mode.

Figure 3-3 shows a simulation of various frequency-dependant optimum impedance levels required to attain the maximum electrical $\Re vs$ and lowest electrical NEPs for a differential NFET pair driven from the sources, with device dimensions of 1um wide and 60nm long and a gate bias of 0.4V. This plot shows that high impedance required to attain the lowest NEPs required, and as expected, these

impedances roll-off as the frequency of operation is increased. The capacitive parasitics within the intrinsic device start to decrease with the increase in frequency. This plot also shows that the PSP model-based results show a drop in mixing efficiency as the source frequency increases.

On the other hand, Figure 3-4 shows the same simulation of optimum impedances but with a device of 300nm width and 60nm length. As expected by the theoretical modelling, the impedance required is much higher compared to the wider devices, which of course is more challenging for the antenna design. Another observation here, which also aligns with the theory derived in chapter two, is related to the simulated values of the $\Re$vs and NEPs for totally matched detector. Detectors with smaller dimensions exhibit much higher input impedances, and in return, much larger voltage drops at their inputs. Therefore, the theoretical $\Re$v and NEP of the W/L=300nm/60nm devices is much higher than those of the W/L=1µm/60µm. Both Figure 3-3 and Figure 3-4 reveal that the detectors of smaller sizes attain higher $\Re$vs and smaller NEPs, going down to $5pW/\sqrt{Hz}$.



(a) **(b)**

(c) **(d)**

Figure 3-5: (a) Simulated S11 at frequency=650GHz with an antenna impedance of Z_{ant}=153+j787Ω versus gate bias from 0V to 1V, and the corresponding (b) $\Re$v and NEP versus V_{GS} based on harmonic balance simulations of a source driven Terahertz detector of 1µm/0.06µm dimensions at 1-kHz chopping frequency. The $\Re v_{max}$ =13.5kV/W and NEP_{min}=7.5pW/√Hz. (c) and (d) show the balanced ports' voltages. The input power is set at 10nW for a 650GHz input frequency.

Figure 3-5.a shows a Smith-Chart with simulated S11 plots at 650GHz for an NFET based differential resistive mixer of W/L=1µm/60nm with respect to the gate bias of the transistors. The detector's simulated input impedance is Z_{in}=150-j800Ω when the transistors are biased at 0.25V. The antenna is thus designed to match one bias point, and the detector is therefore mismatched at different gate voltages. Therefore deciding on the impedance levels to be matched per frequency is inspired by the detector operation region. The highest attained ℜv is 13.5kV/W for this device and the minimum NEP at 1kHz chopping is $7.5pW/\sqrt{Hz}$, shown in Figure 3-5.b. The variations of the input voltage at the positive and negative ports of the differential detector are shown in Figure 3-5.c,d. They show that the out of phase voltages decrease in amplitude as the gate voltage is changed from the optimum bias where the impedance matching was done.

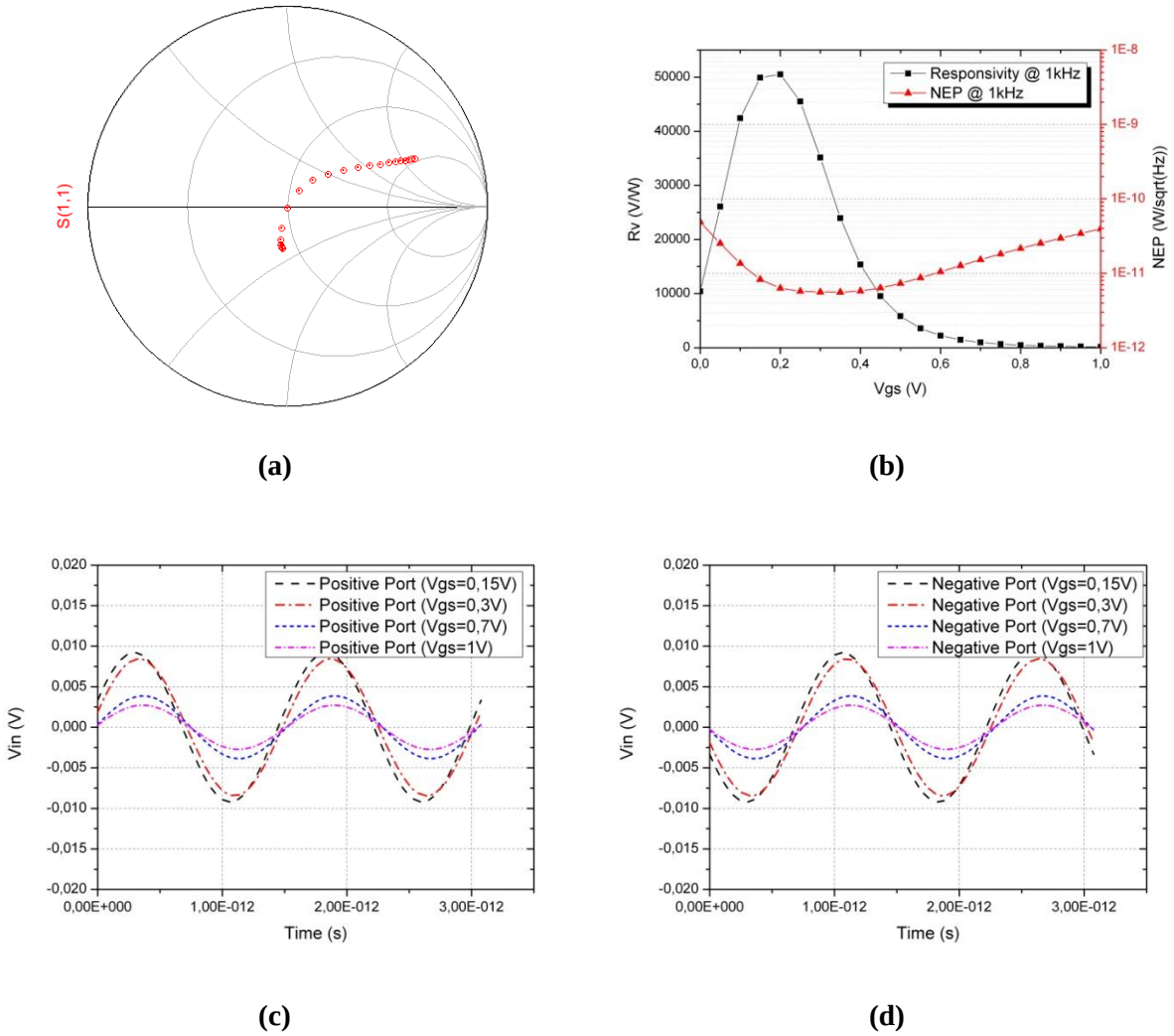


Figure 3-6: (a) Simulated S11 at frequency=650GHz with an antenna impedance of Z_{ant}=405+j2200Ω versus a gate bias from 0V to 1V, and the corresponding (b) ℜv and NEP versus V_{GS} based on harmonic balance simulations of a source driven Terahertz detector of 0.3µm/0.06µm dimensions at 1kHz chopping frequency. ℜvmax =50kV/W and NEP_{min}=5pW/√Hz. (c) and (d) show the balanced ports' voltages. The input power is set at 10nW for a 650GHz input frequency.

Figure 3-6.a shows a Smith-Chart with simulated S11 plots at 650GHz for an NFET based differential resistive mixer of W/L=0.3µm/60nm with respect to the gate bias of the transistors. The detector's input impedance is Z_{in}=405-j2200Ω when the transistors are biased at 0.25V. The antenna is thus

designed to match one bias point, and the detector is therefore mismatched at different gate voltages. One observes here the high capacitive element that needs to be tuned out to attain the best NEP numbers, as opposed to the impedance levels of the wider device. The highest attained $\Re v$ is 50kV/W for this device and the minimum NEP at 1kHz chopping is $5pW/\sqrt{Hz}$, shown in Figure 3-6.b, and these figures are far better than those for the wider device. The voltage variations at the differential input ports of the device are shown in Figure 3-6c,d and are higher than those in Figure 3-5.c,d due to the higher input impedance of the device. Both simulations are performed with the same input power level of 10nW and a 100% antenna efficiency is assumed.

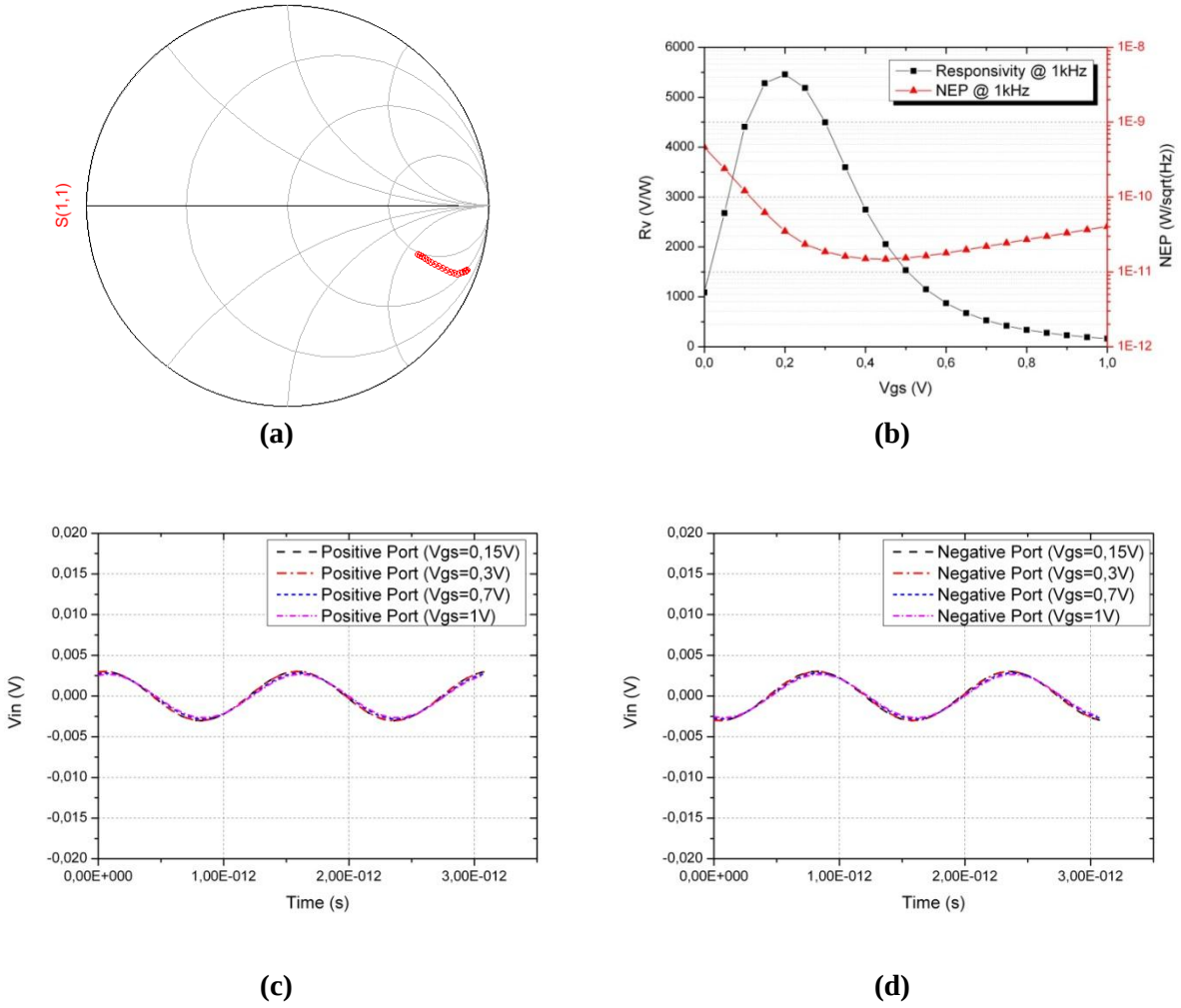


Figure 3-7: (a) Simulated S11 at frequency=650GHz with an antenna impedance of Z_{ant}=360+j360Ω and the corresponding (b) $\Re v$ and NEP versus V_{GS} based on harmonic balance simulations of a source driven Terahertz detector of 0.3µm/0.06µm dimensions at 1kHz chopping frequency. The $\Re v_{max}$ =5.5kV/W and NEP_{min}=14pW/$\sqrt{Hz}$. (c) and (d) show the balanced ports' voltages. The input power is set at 10nW for a 650GHz input frequency.

The same conditions for a detector with 2µm gate length and 200nm gate width were also simulated. As expected the impedance levels are even lower. The detector input impedance at 0.4V is Z_{in}=100j-380Ω which is an even further relaxed requirement on the antenna side.

It is essential to mention a remark on the design of high impedance detectors such as detectors of minimum size in a specific technology. The fact that a total match is difficult to attain does not mean

the detector is not a feasible choice. Simulations show that even when the detector is quite mismatched it could still be competitive to wider or longer detectors of relaxed input impendence.

Figure 3-7.a shows S11 simulations of the same detector topology with NFETs of 300nm gate width and 60nm gate length. The real maximum $\Re v$ could be attained with an input impedance of Z_{in}=400+j2200Ω, and is 50kV/W. Of course this is a very high impedance value and is deemed unfeasible for the antenna design. However if the detector is designed with an antenna impedance of Z_{in}=450+j450Ω, which is a much feasible value, the detector would still exhibit a good responsivity of 5.5kV/W and an NEP of $14pW/\sqrt{Hz}$. The alignment of NEP minima and $\Re v$ maxima can be achieved by proper transistor sizing for some predefined chopping frequency and load impedance.

3.1.2. Output Impedance Dependence

Having decided on the device sizing and the corresponding input impedance matching, another parameter that influences the output voltage level is the output impedance. The limited load impedance at the detector output (R_{out}) is primarily responsible for the responsivity attenuation in the sub-threshold region (high channel resistance) and the responsivity rises in the weak inversion regime, as shown in Figure 3-8. The maximum responsivity ($\Re v_{max}$) with the corresponding location of the operation point defined by gate-source voltage (V_{GS}) is a function of both load impedance and device channel length. This is utterly important when designing the readout integrated circuits to ascertain the output signals are not degraded by improper loading.

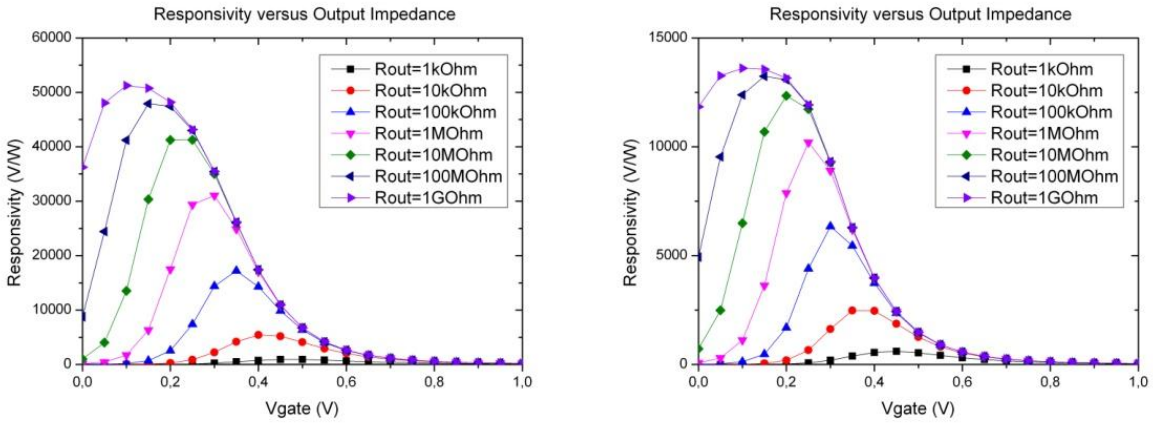
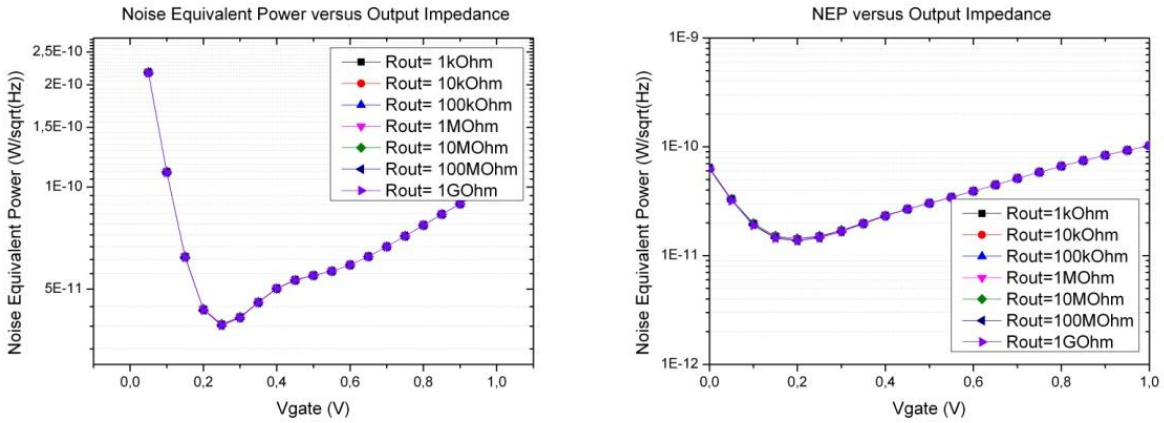


Figure 3-8: Simulated $\Re v$ with respect to R_{load} variations for (a) an impedance matched 0.3µm/0.06µm FET pair in differential source-coupling mode and (b) an impedance matched 1µm/0.06µm device. The input power is fixed at 100nW and the frequency=650GHz.

NEP minima and the corresponding $\Re v$ maxima, however, do not necessarily closely coincide with the location of $\Re v_{max}$ on the V_{GS} axis. They are a result of the interrelation of the device channel noise and the drain response to gate bias. In the sub-threshold region, NEP follows the close-to-exponential v_{GS} dependence of the channel resistance. It is important to emphasize that the high voltage responsivity achievable by providing the appropriately high output resistance does not necessarily improves NEP because the equivalent voltage noise spectral density at the output also increases. This is shown in Figure 3-9, where the NEP values remain unchanged with the varying output impedance. Even though the NEP remains unchanged, it is important to develop a high $\Re v$. Higher output levels

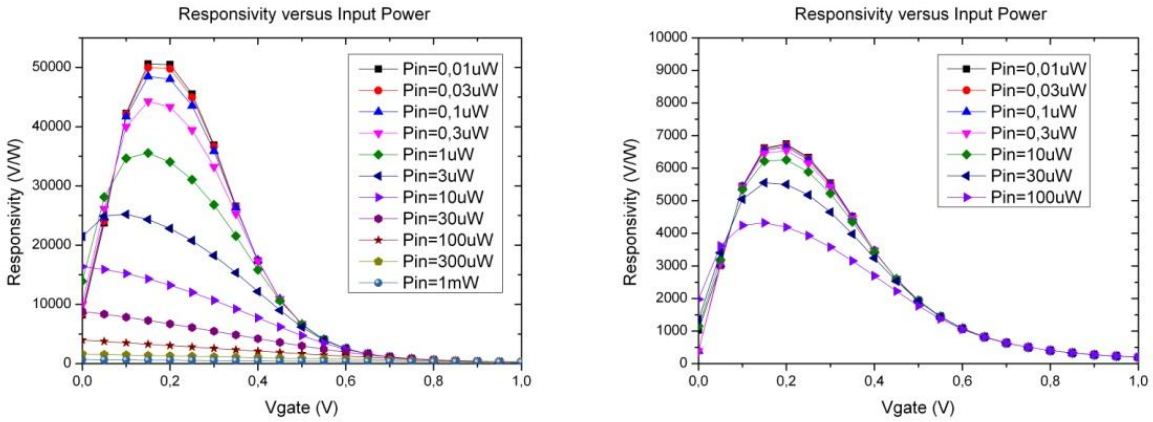
relax the requirements of the readout circuitry and increases the voltage dynamic range. The effect of the responsivity on the noise level is discussed in the following section on noise analysis.



(a) **(b)**

Figure 3-9: Simulated NEP with respect to R_{load} variations for (a) an impedance matched 0.3µm/0.06µm FET pair in differential source-coupling mode and (b) an impedance matched 1µm/0.06µm device. The input power is fixed at 100nW and the frequency=650GHz.

3.1.3. Input Power Dependence



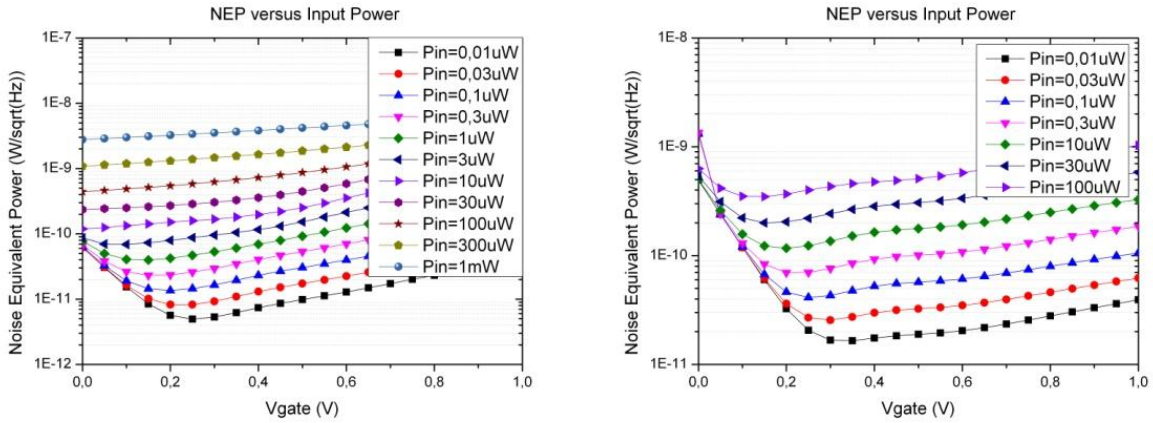
(a) **(b)**

Figure 3-10: Simulated voltage responsivity of detectors with respect to detector input power for (a) an impedance matched 0.3µm/0.06µm FET pair in differential source-coupling mode and (b) an impedance matched 1µm/0.06µm device. The chopping frequency is fixed at 1kHz and the frequency=650GHz.

The THz mixer dependence on input power level defines the minimum detectable power, the detector linearity, as well as the saturation level. Unfortunately measurements for THz detector linearity have not been validated yet. Simulations of the detector responsivity and the impact on the noise equivalent power have been simulated. Figure 3-10.a,b show the simulated responsivities of 0.3µm/0.06µm

devices and 1µm/0.06µm devices, respectively. The graphs show that whilst the smaller devices attain much higher responsivities compared to the bigger devices they saturate faster. For example, comparing a 10µW input power for both devices shows that the responsivity of the smaller device is degraded significantly compared to the wider device. This is owed to the saturation of the device.

At this point the benefit of differential transistors becomes apparent. As the signal power received is divided in half and balanced between both nodes of the differential transistors, the working input dynamic range is enlarged. However, as will be seen afterwards, as the noise contributors are effectively doubled the sensitivity may be reduced for lower input power levels.



(a) **(b)**

Figure 3-11: Simulated NEP of detectors with respect to detector input power for (a) an impedance matched 0.3µm/0.06µm FET pair in differential source-coupling mode and (b) an impedance matched 1µm/0.06µm device. The chopping frequency is fixed at 1kHz and the frequency=650GHz.

The dependence of the noise on the input power is also evident in Figure 3-11. The combination of the detector responsivity saturation along with the increased noise level could even deteriorate the NEP values at a faster rate, as the NEP is linked to both parameters. A few-fold of NEP increase appears for both device sizes due to the increase in input power. The next subsection describes the reasons behind the increase in noise with respect to input power and the detector responsivity.

3.1.4. Noise Analysis, Temperature and Modulation Frequency Dependence

The main noise contributors in a cold-FET based direct detection circuitry are [113]:

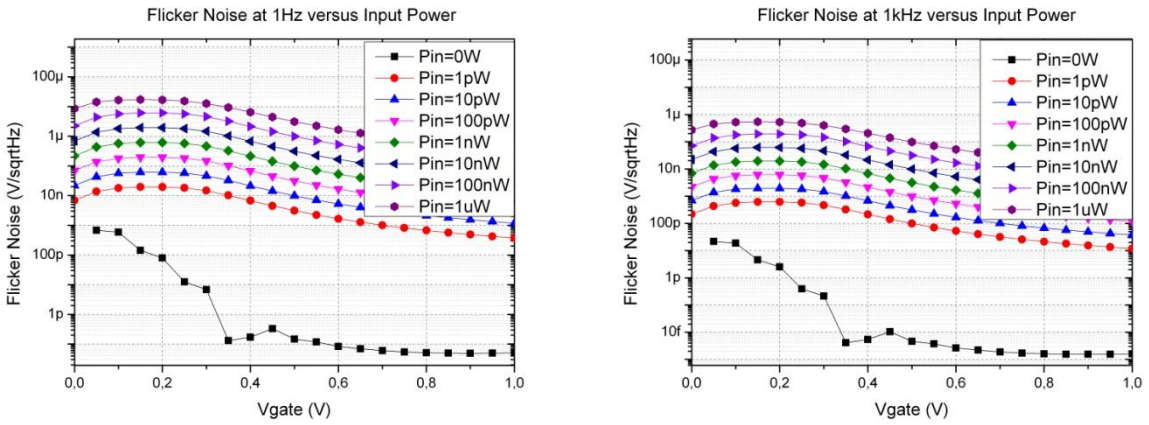
1) Johnson-Nyquist noise or Thermal noise from the gate-bias dependant channel resistance. Employing the Rayleigh-Jeans approximation, the relationship of the noise power variance is as follows: $\bar{v}_n^2 = 4kTBR$
2) Flicker noise arising from the trapping and de-trapping of electrons with a power spectral density proportional to 1/f [114], [115]

Flicker noise may become a considerable part of the overall device noise even in cold-biased FETs [116][117][118]. The flicker noise level depends on the device sizing, chopping frequency, and the input signal power level. The explanation emerges from the following. The mixing process generates a DC voltage within the transistor, which in return modulates the channel. This creates a fluctuation in

the non-quasi-static channel conductance and the DC mixing product generates a small current within the transistor. Therefore, flicker noise starts to exist. Recall that this conductance is only partially involved in the mixing process, as per the non-linear RC-ladder channel-modelling described in the previous chapter. Therefore, any slight variation in this conductance may be significant. Furthermore, as this flicker noise is dependent on the internal self-bias from this DC-noise, it is thus apparent that the larger this DC voltage the higher the flicker noise-level.

Several factors will impact this DC-level increase, and in return the flicker-noise increase. Assume a zero-IF output, i.e. the output signal is at DC and is not chopped at all. Primarily, it is the efficiently-delivered power to the transistor that directly increases this flicker noise. As the power increases, the converted THz to DC increases, quantified by the electrical responsivity.

Figure 3-12.a demonstrates this behaviour. This simulation relates to a 1µm/0.06µm source-fed differential detector that is perfectly matched at a gate bias of 0.4V. At a 1Hz noise frequency, the flicker noise level increases a 1000 times across power levels from P_{in}=1pW to P_{in} =100nW, with the largest input power leading to a noise level around 6µV/√Hz. It is valid to note that these power levels resemble the realistic levels available at the mixer ports. For an input power of 0W the flicker noise is reduced drastically and is almost insignificant, therefore revealing the direct linkage of the power level to the flicker noise.



(a) **(b)**

Figure 3-12: Output flicker noise voltage of 1µm/0.06µm detectors with respect to detector input power (a) at 1Hz and (b) at 1kHz

A well-known technique to reduce the effect of the flicker noise is to modulate and operate the transistors at higher frequencies beyond the 1/f-knee. For instance, Figure 3-12.b shows the effect of chopping at 1-kHz, where the entire flicker-noise levels are reduced around a 100 times across the same input powers as in Figure 3-12.a.

The 1/f noise was simulated at a gate voltage of 0.15V for a 1µm/0.06µm differential detector, with respect to input power and chopping frequencies. The simulations are shown in Figure 3-13 and they reveal the roll-off of flicker noise as the chopping frequency increases. Therefore, chopping at higher frequencies will have a direct impact on the NEP levels as the noise levels vary accordingly.

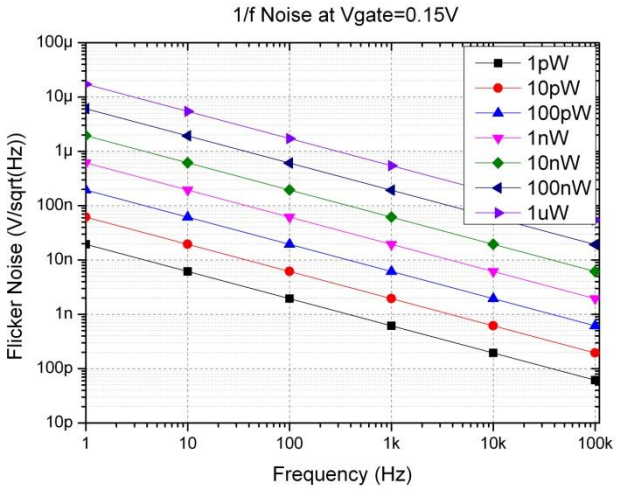


Figure 3-13: 1/f Noise of 1µm/0.06µm differential detectors over various noise-frequencies with respect to input power variations

The flicker noise of the same device was also simulated across the gate bias with respect to varying chopping frequencies and with an input power of 1nW and is shown in Figure 3-14. This plot shows that flicker noise increases around the highest responsivity regions and could be visualised by the humps in the curves. Again this due to the larger DC voltage generated by the device.

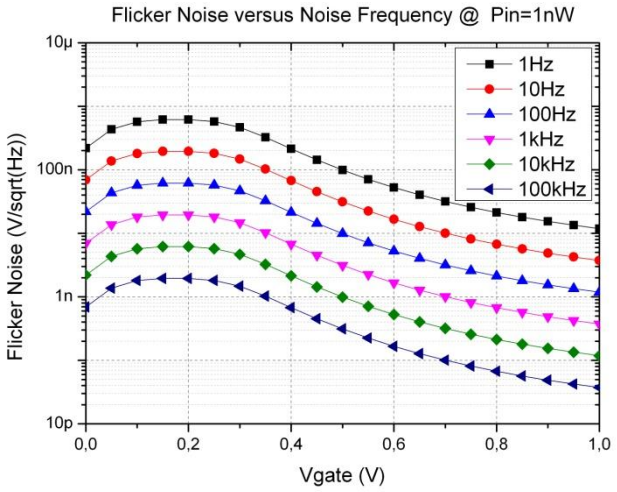
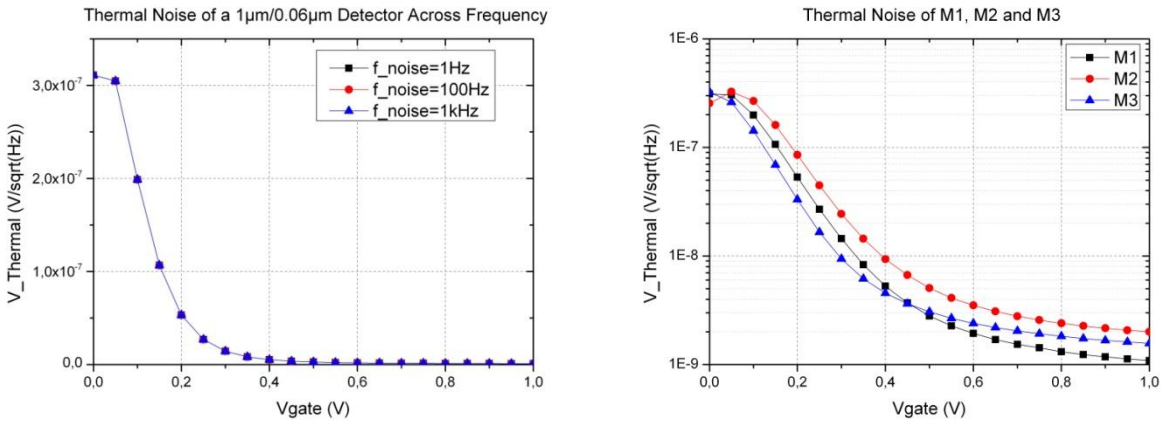


Figure 3-14: 1/f Noise of 1µm/0.06µm differential detectors with an input power of 1nW over various noise-frequencies



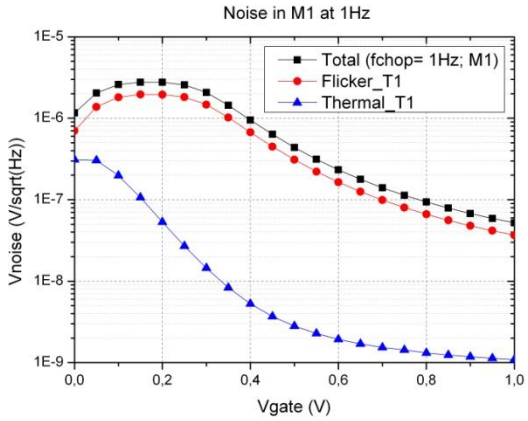
(a) **(b)**

Figure 3-15: (a) Thermal noise voltage for a 1µm/0.06µm versus gate bias and at 1Hz, 100Hz, and 1kHz noise frequencies. (b) Thermal noise voltage for M1, M2, and M3 versus gate bias and at 1kHz. *M1*: Differential Terahertz Mixer with 1µm/0.06µm each NFET. *M2*: Differential Terahertz Mixer with 0.3µm/0.06µm each NFET. *M3*: Differential Terahertz Mixer with 1µm/0.2µm each NFET.

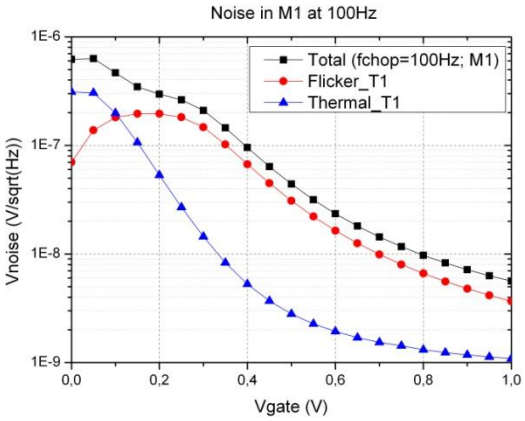
On the other hand thermal noise is the other noise contributor. Thermal noise, or Johnson-Nyquist noise, is white-noise; so it is frequency independent. In fact, it is rather bandwidth dependant and since a 1Hz bandwidth is assumed the Rayleigh-Jean's approximation is employed and the power-spectral density is equivalent to $\bar{v}_n^2 = 4kTBR$ [119].

For the same detector of 1µm/0.06µm transistors, the thermal noise contribution of a single transistor of the differential pair is shown in Figure 3-15.a. This plot shows that the thermal noise peaks at 0.3µV/√Hz at the sub-threshold and threshold region and starts to roll off with gate bias. The roll-off is based on the modulation of the channel resistance which decreases with gate-bias, and in return, thermal noise decreases.

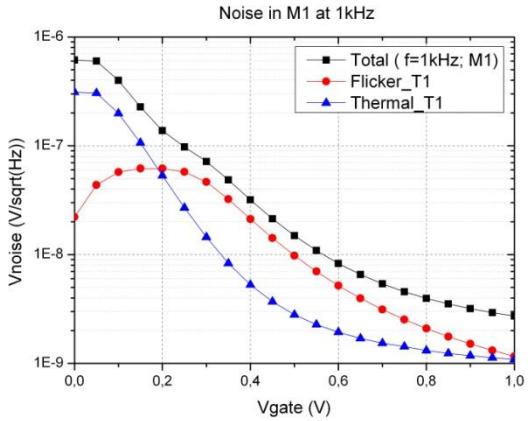
Figure 3-15.b compares the thermal noise levels with respect to three different detector sizes. The thermal noise behaviour with respect to gate bias varies due to the different channel modulation in different transistor sizes. One observation for instance shows that transistor M2 of 0.3µm/0.06µm dimensions has a worse on-resistance compared to longer and wider transistors. The channel exhibits higher resistance with smaller devices, and therefore a higher thermal noise is expected. For instance, for a V_{GS} =0.2V the thermal noise of a 0.3µm/0.06µm device is more than twice that for a 1um/0.2µm device. This is due to the fact that smaller transistors require a larger potential at the gate to open the channel.



(a)



(b)

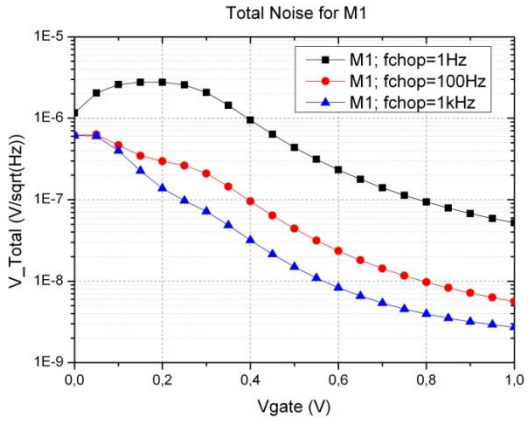


(c)

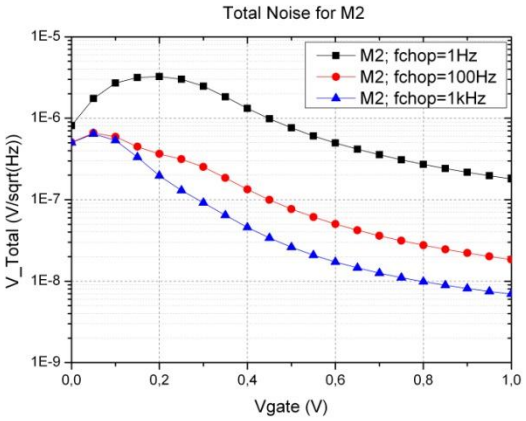
Figure 3-16: Simulated noise contributors for Terahertz-mixer M1 formed of transistors T1 and T2, with 1µ/0,06µm each at (a) 1Hz, (b) 100Hz, and (c) 1kHz. T1 is one NFET transistor operated differentially through the source. The source power is fixed at 10nW. The total noise corresponds to the total noise of the mixer, and the flicker and thermal noise correspond to one of the transistors.

But how does this flicker noise compare to the thermal noise of the transistors and how much does it contribute to the total noise? A comparison with the flicker noise levels in Figure 3-16a-c reveals that the flicker noise is significantly higher than the thermal noise at low chopping frequencies and when the input power levels are sufficient to generate this type of noise.

At 1-Hz, the 1/f noise is even higher than the channel thermal noise, and that has a direct impact on the NEP. Therefore, the impact on the total noise becomes apparent. Only chopping at around 1-kHz and beyond reduces the flicker noise with respect to the thermal noise, however this flicker contribution is still significant. The total noise level decreases substantially when chopping at 1-kHz, with the thermal noise becoming the dominant factor. The figure shows that the total noise curves lose their humps around the sub-threshold and threshold regions as the flicker noise is reduced.



(a)



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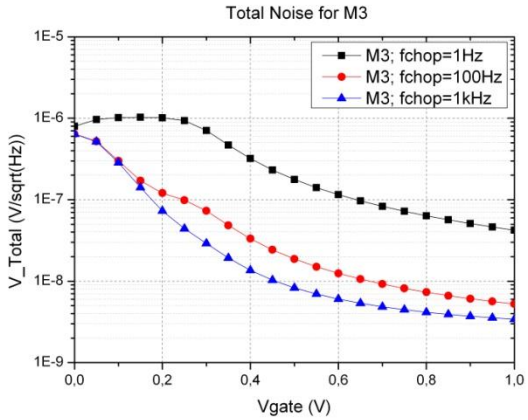


(c)

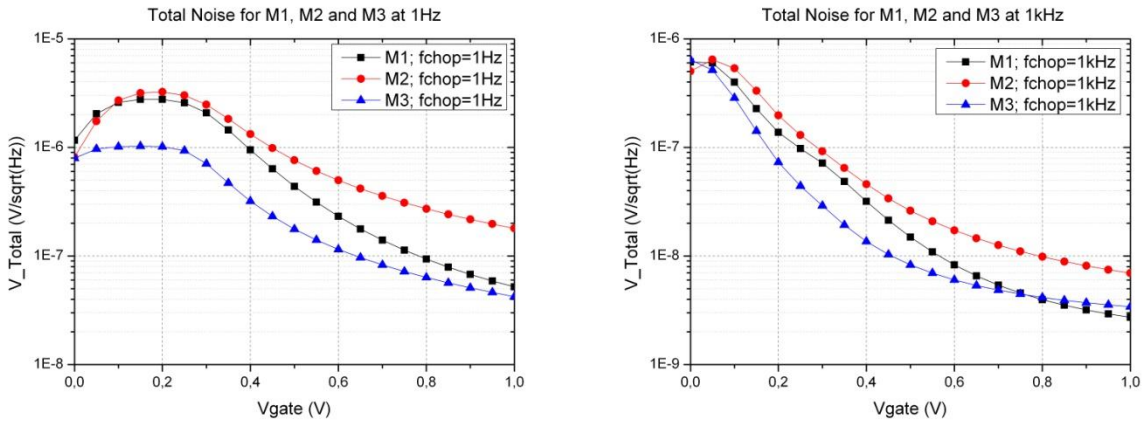
Figure 3-17 : Simulated total noise at 1Hz, 100Hz and 1kHz for (a) Mixer M1 (b) Mixer M2 and (c) Mixer M3. The source power is fixed at 10nW.

M1, M2, and M3 are differential cold-NFET mixers coupled through their sources, with device dimensions of T1=1µm/0.06µm, T2=0.3µm/0.06µm, and T3=1µm/0.2µm, respectively.

Figure 3-17.a-c compare the total noise levels per device size with respect to chopping frequency. The comparison shows that smaller transistors exhibit much higher flicker noise levels at lower chopping frequencies than larger transistors. The wider and longer devices are more immune to flicker noise. The total noise of the three different FET sizes is shown in Figure 3-18.a and Figure 3-18.b. These plots clearly show that the smallest devices exhibit the highest noise contributions mainly due to the higher mixing efficiency that generates a larger DC voltage leading to higher flicker noise.

As the chopping frequency increases the total noise level of each device tends to be only comprised of the thermal noise of the channel. In other words, for a THz mixer that is foreseen to operate at low chopping frequencies, wider and longer devices are favoured. If chopping is readily available, smaller devices are the better option. Of course, this should be decided in view of the impedance matching and the expected overall system performance as discussed in the previous and the upcoming sections.

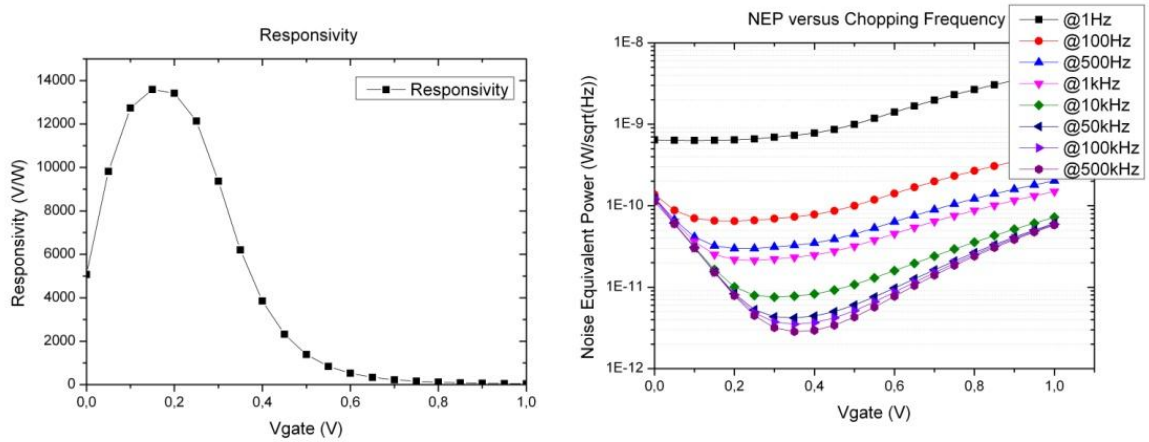
This analysis has a direct implication on the NEPs of concern. To elaborate more on this, simulation results for a 1µm/0.06µm large device reveal that even a few-fold increase in NEP may be possible whilst increasing the input power from 1nW to 100nW and chopping at appropriately low frequency.



(a) **(b)**

Figure 3-18: Comparison of total Noise for M1, M2 and M3 at (a) 1Hz and (b) 1kHz

Increasing the device length is, therefore, advantageous for low chopping frequencies and high input power levels at the detector, for example devices with W/L=1/0.2µm. For high chopping frequencies and low input power levels, however, short transistors should be comparable or even outperforming. Therefore, sizing is necessarily done in view of the foreseen input power level, chopping frequency, and load conditions to result in the optimum DC performance.



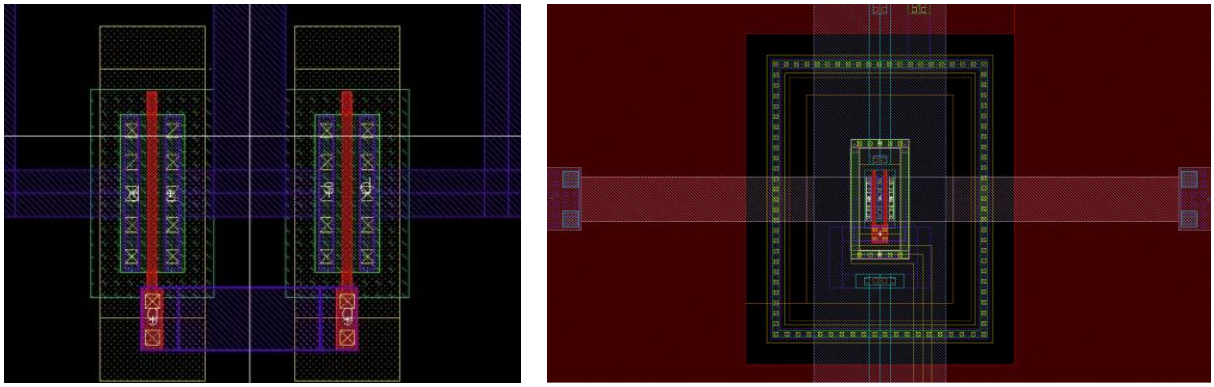
(a) **(b)**

Figure 3-19: (a) ℜv and (b) NEP versus chopping frequencies: 1µm/0.06µm NFET pair in differential source-coupling mode. Pin=100nW, Rout=100MΩ, Frequency=650GHz.

Simulations of ℜv and NEP versus chopping frequencies are shown in Figure 3-19. It clearly shows that the NEPs could be substantially improved when operating the detector at higher modulation frequencies. Whilst the responsivity remains unchanged in the case of purely resistive loads, the responsivities could drastically be degraded should cables be used for readout. Capacitive shunting will thus degrade the output signal at higher frequencies and impacts the NEP. However, the noise levels could still roll off faster than the responsivity levels.

All these findings are important to keep in mind when sizing the transistors in view of the NEP_{minima} and $\Re v_{maxima}$ alignment. It is noteworthy at this level that the chopping frequency is not only important for the devices' intrinsic 1/f-noise, but also for the readout circuitry noise. It will be more apparent in the next chapters when we discuss multipixel camera design.

3.1.5. Layout Techniques



(a) **(b)**

Figure 3-20 : (a) Layout of two separate NFETs operated differentially, (b) and layout of single double fingered transistors operated differentially through the sources (drains).

A few layout tricks to enhance the noise performance and the mixing efficiency of source-driven differential NFET Terahertz detectors is suggested here. The concept is based on utilizing a single dual-fingered NFET as a differential detector rather than two separate NFET, as shown in Figure 3-20a,b. In layout view, a double fingered 2µm wide transistor is drawn with a 1µm wide transistor equipped with two drain contacts and a source contact (or vice versa). Therefore, the 2 drains/sources are used as differential ports for the Terahertz mixer core. The top view of the differential THz detector is shown in Figure 3-21. The balanced signals are coupled to both drain contacts of the transistor, and the output signal is extracted from the common source.

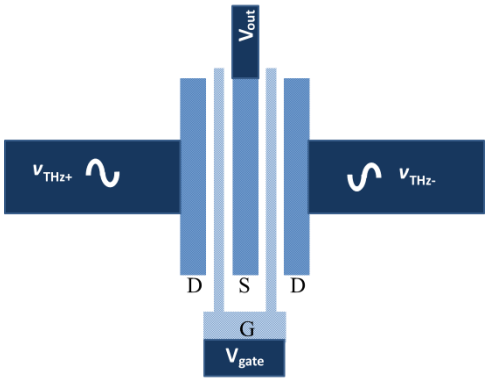


Figure 3-21: Double fingered differential THz NFET detector layout

A cross-sectional view of this differential transistor is shown in Figure 3-22. The effective differential pair created by the single transistor share a common well at the source, and therefore a better ac-ground is created across the gate and the source, enhancing the broadband behaviour.

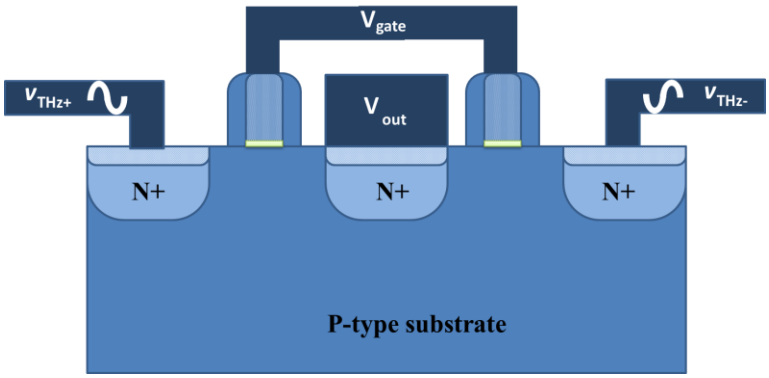


Figure 3-22: Cross-section of double fingered differential THz NFET detector

Additionally, the junction capacitances at the source are reduced and there is no need to route two individual sources externally as they are intrinsically connected, thus reducing noise and enhancing the efficiency.

3.2. CMOS Technologies Comparison

3.2.1. Circuit Level Comparison

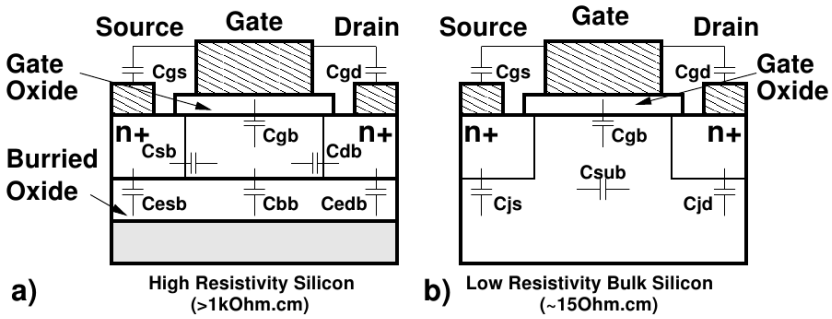
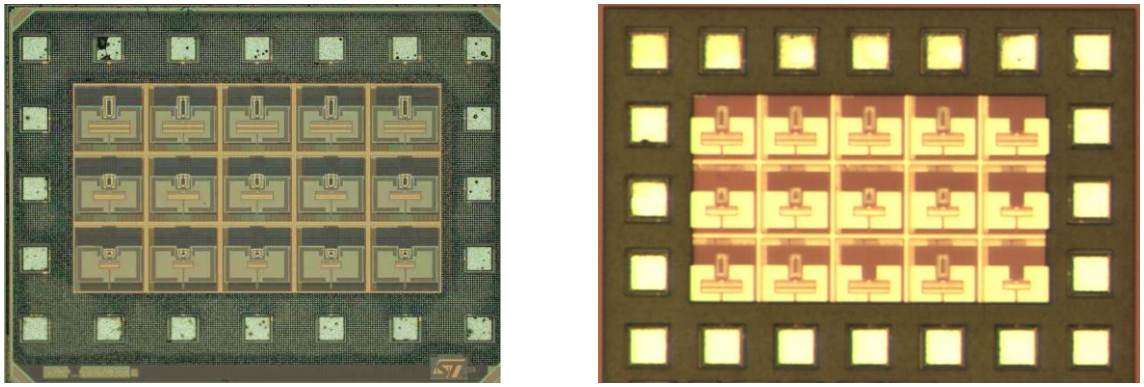


Figure 3-23: (a) CMOS bulk and (b) CMOS SOI cross-section demonstrating intrinsic parasitics [79].

To be able to compare the detector performance in bulk and partially depleted Silicon on insulator (SOI) CMOS, the device intrinsic parasitics should be analysed. Figure 3-23 shows cross-sections of NMOS transistors in (a) bulk CMOS and (b) both partially depleted SOI. The silicon on insulator exhibits a strong isolation of the active device from the silicon substrate, essentially suppressing the parasitic elements C_{jd}, and C_{sub} through the creation of a box underneath the devices.



(a) **(b)**

Figure 3-24: 5x3 test arrays of THz detector test structures. (a) 65nm CMOS SOI chip [18] and (b) 65nm CMOS bulk chip [78], [79].

In bulk CMOS these parasitic capacitances tend to shunt part of the coupled THz signals to the substrate. Thus, it can be seen that SOI transistors will perform more efficiently than bulk due to the reduction of these junction capacitances. This has been analysed [79] and SOI detectors proved to outperform those of the bulk technology for the following circuits shown in Figure 3-24. The signal to noise ratio at the output of the detectors of the same gate-driven topology with dimension of 1µm/60nm NFETs at the same distance are compared in Figure 3-25. It reveals that the SOI detector has a higher SNR compared to the Bulk detector. It shows that the silicon lens increases the SNR as compared to front-side illumination.

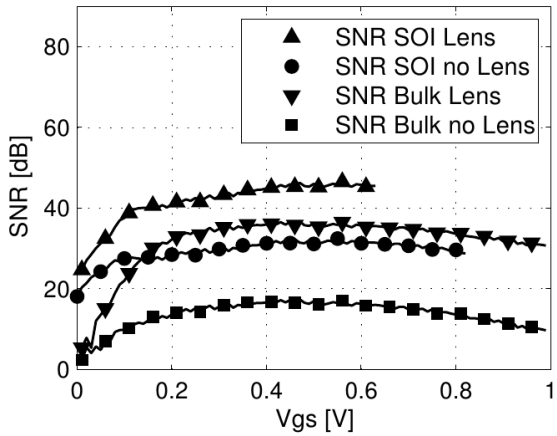


Figure 3-25: SNR comparison at a distance of 10cm for gate-drain driven detectors implemented in CMOS Bulk and SOI, with and without a Silicon Lens.

Besides, bulk transistors require isolation wells with reverse biased diodes to avoid cross talk, latch-up and signal leakage. It is important to distinguish between the performance of isolated and non-isolated transistors in terms mixing efficiency. Isolating the wells create huge capacitive diodes with their corresponding series resistances. We believe that isolating the wells could potentially degrade the signal detection by increasing the junction capacitances.

With the interest of implementing fully integrated readout analogue or digital circuitry within the focal-plane arrays, the utilization of SOI technologies saves in circuit area, increases the efficiency of mixing, reduces in power consumption as well as the noise generated by digital elements that are a major concern for THz detectors [120], [121], [122], [123].

Further transistor enhancement could be attained by utilising fully depleted devices and further scaled technologies. FDSOI technologies are quite expensive in comparison to lower technology nodes. But such technologies are quite attractive and promising with the fact that heavy investments at foundries are developing these technologies into maturity [124], [125], [126], [127]. FDSOI technologies exhibit excellent device isolation from the substrate and from neighbouring transistors and removes the history effect in PDSOI transistors. The drain-to-source capacitances are also reduced as the transistors are ultra-thin. Besides, smaller transistors with gate lengths of 22nm offer higher input impedances and therefore will have higher responsivitites.

One of the drawbacks thus far is the low-resistivity substrates used for the wafers. In essence this is needed for back-body biasing; feature made possible by creating an ultra-thin buried oxide, as well as deep trenches around the transistors. Therefore to be able to control the body levels, the substrates should exhibit low resistivity levels. However, benefits in terms of back-body control will be discussed in the following sections.

FDSOI and PDSOI are especially attractive in multi-pixel THz design, where multiple noisy digital and analogue elements comprised of switches, amplifiers, decoders and other, induce considerably more noise into the detection and readout chain. However the process fabrication cost is much higher than bulk CMOS technologies.

3.2.2. Antenna Level Comparison

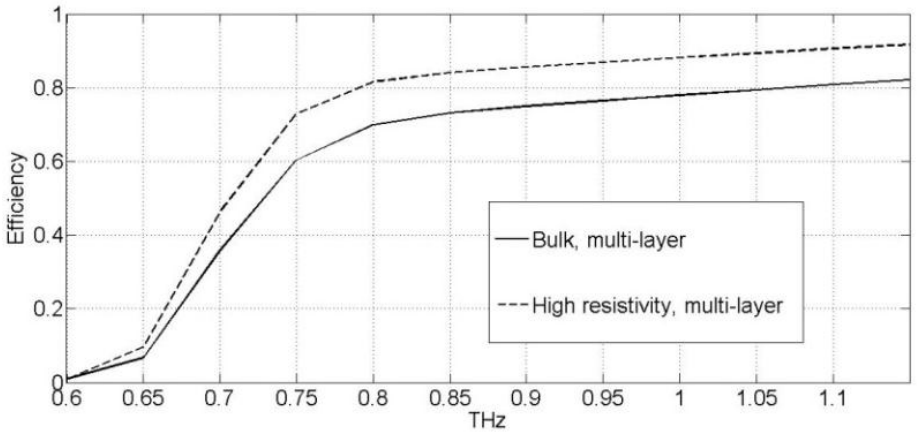


Figure 3-26: Radiation efficiency of the proposed antenna on a semi-infinite silicon substrate. The chip thickness is 150µm and the silicon resistivity is assumed to be 15 Ωcm and infinity for a bulk and high-resistivity substrate, correspondingly. The antenna is realized as a multi-layer thick metal geometry [128].

The other difficulties arise from devising appropriate antenna topology to provide the highest radiation efficiency on a silicon substrate with its layout fully compatible with complex digital CMOS design rules. The antenna should also deliver reasonable optical quality; known to be challenging for substrate-based antennas.

Choosing a wire-type antenna with no direct proximity to GND planes (floating wires) may be favourable for Ohmic loss minimization at THz frequencies when compared to standard micro-strip or slot antennas with small cross-sections of the radiating slots that induce high Ohmic loss [128]. The other remedy to minimize the overall loss of the radiating element may be the application of a high-resistivity substrate as shown in Figure 3-26. However, high-resistivity silicon is considerably more expensive than standard bulk and not fully compatible with the mainstream bulk CMOS technology. Therefore, standard bulk CMOS process is attractive, but low resistivity will lead to additional conduction losses in the substrate.

3.2.3. Passives in CMOS Technologies

As the main aim here is full integration of THz-systems on chip, it is essential to investigate the capabilities of designing the THz antennas on-chip along with the transmission lines for both sources and detectors. It is rather important to understand the characteristics and limitations of passives design for THz detection as much as it is for the detection principle itself.

3.2.3.1. Characteristics, Loss Mechanisms and Design

In spite of the considerably improved raw performance of silicon devices, there exist some important challenges in using silicon at mm-wave frequencies and beyond. The downscaling process of CMOS nodes goes in parallel with the vertical shrinkage of the back-end-of-the-line (BEOL) and a decrease of the metal and the dielectric thickness, as well as the metal pitch in order to increase the integration density. This, in turn, leads to increased Ohmic loss of passive structures, and possibly magnified influence of the substrate loss on the transmission line propagation. As it is known, with the increase in frequency, skin effects are much more significant and could no longer be neglected. The Skin depth in [m] is given by δ_s

$$\delta_s = \sqrt{\frac{2\,\rho}{2\,\pi\,f\,\mu_0\mu_r}}$$

Where

- ρ is the bulk resisitivity [Ω.m]
- f is the frequency in [Hz]
- μ_0 is the permeability constant in [H/m] and is equal to $4\,\pi\ \text{x}10^{-7}$
- μ_r is the relative permeability and is approximately equal to 1.

Figure 3-27 shows a plot of the skin depth δ_s for Copper, Gold, and Aluminum with respect to frequency from 300GHz up to 1.8THz. This reveals that the waves are much confined to the surface of the metals and do not penetrate more than 60nm from the surface of Copper lines. This effectively increases the losses of the transmission lines.

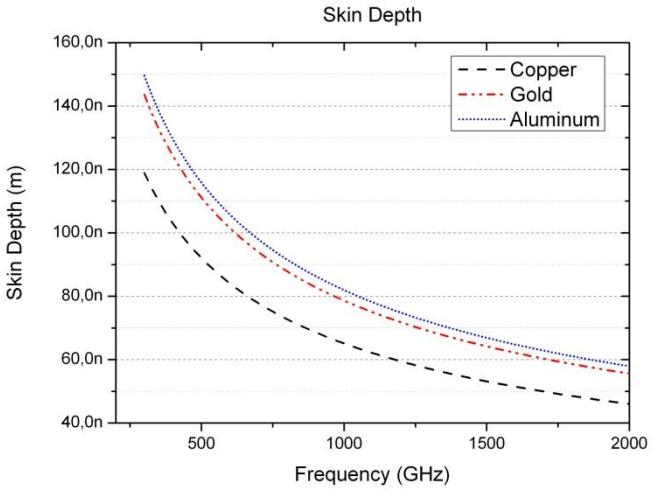


Figure 3-27: Skin depth versus frequency for Copper, Gold, and Aluminium lines.

Another important limitation related to the BEOL vertical shrinkage is that it imposes very challenging layout design rules in terms of the available metal densities; not much relevant in many other technologies. The CMP process steps used for metal deposition desire a very high level of wafer-uniformity which is only made possible when the underlying metal layer densities are homogeneous all over the wafer.

3.2.3.2. Antenna Design

Within the design constraints for designing passive elements described in the previous section, the main challenges to confront are mainly related to the antenna detector-matching, and the antenna radiation efficiency. The BEOL of CMOS technologies are relatively thin in height, therefore a ground plane necessary for patch antennas would be very close to the antenna if designed at a top metal. Therefore, folded dipole antennas as well as ring antennas were chosen and designed. Given the high dielectric constant in Silicon, the radiation therefore develops through the silicon, and the best illumination is through the back of the die.

An optimum match between detector and antenna for maximum conversion efficiency allows the detector to operate close to its maximum responsivity over a wide frequency range. As shown in section 3.1.1, the detectors exhibit high and complex input impedance at their inputs. Impedance levels are even as high as 1kΩ or beyond for some transistor sizes). The input impedance of the MOSFET is defined by its intrinsic and extrinsic parasitic capacitances and the resistance of the channel in the corresponding operation mode. This impedance is bias dependant. In the sub-threshold regime the channel resistance is much higher than the weak or strong inversion regimes. The antennas have been co-designed with the detectors and several illumination topologies were investigated [78], [128], [129]. The ring antennas are comprised of two magnetically coupled semi rings connected at the zero H field. All the wiring is routed underneath these regions. The length of each wire is approximately a wavelength in Silicon, for a centre frequency, and the width of the antenna helps expand the bandwidth. Therefore, each semi ring is a half wavelength long. The feed lines with the antenna both define the differential input impedance of the antenna, which as described above is made to complex-conjugate match the detectors at the centre frequency.

3.2.3.3. Illumination Topologies, Packaging and Loss Mechanisms:

The various losses would include reflective losses due to the discontinuities at the air/silicon/metal interface creating a mismatched dielectric level. Ohmic losses, as discussed above, are very high at THz frequencies, as the skin effect means that the THz current created on the THz antenna restricts them to travel very close to the surface. This also depends on the back-end of the line (BEOL) stack available from process design-kit (PDK), where advanced nodes such as 65nm CMOS and beyond provide at least 7 metal layers with top thick metals, and 28nm FDSOI provides a10 metal stack.

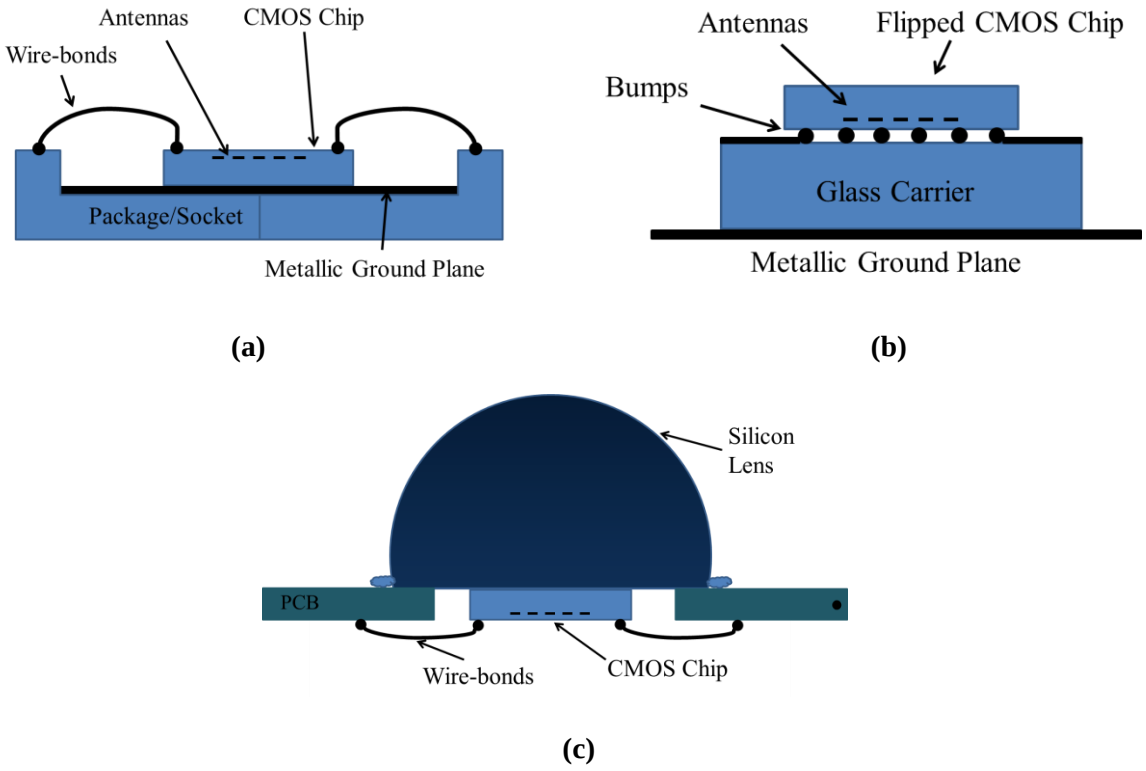


Figure 3-28: Packaging techniques: (a) front side illumination, (b) back-side illumination, and (c) back-side illumination through Silicon-lens.

Additionally, the internal reflections within a Silicon dice lead to substrate-modes. Therefore, technologies with different substrate resistivity offer varying performances. Utilization of 65nm CMOS Silicon-on-insulator (CMOS SOI) leads to higher bulk-resistivities on the order of 3kΩ.cm, compared to low resistivity Bulk CMOS, which is on the order of 15Ω.cm. However, there exists a trade-off in this case, as the high resistivity Silicon serves as a damper for the reflected waves, but should not totally damp the original THz waves propagating through the substrate medium. One solution, therefore, that works for both SOI and Bulk CMOS is to thin the substrate from typical values of 750µm down to 100-150µm. Furthermore, at THz frequencies, and as the wavelengths are quite short compared to RF and Microwaves, on-chip THz radiators utilizing the top metal layers efficiently develop their beams from the back-side of the chip, i.e. through the Silicon substrate.

Therefore, one would develop two different packaging and illumination topologies: Front-side illumination and Back-side illumination, as shown in Figure 3-28. Front-side illumination is the least favoured of two in terms of antenna efficiency, as explained above where substrate modes are dominant. However, straightforward wire-bonding techniques could easily be employed. Back-side illumination, on the other hand, enhances the antenna efficiency by reducing the substrate-modes. To

further enhance the coupling efficiency, a high resistivity Silicon lens could be attached at the back-side of the Silicon die, which both decreases the substrate-modes and guides the rays onto the corresponding pixel aperture. A comparison based on HFSS simulations across frequency of the three topologies is shown in Figure 3-29.

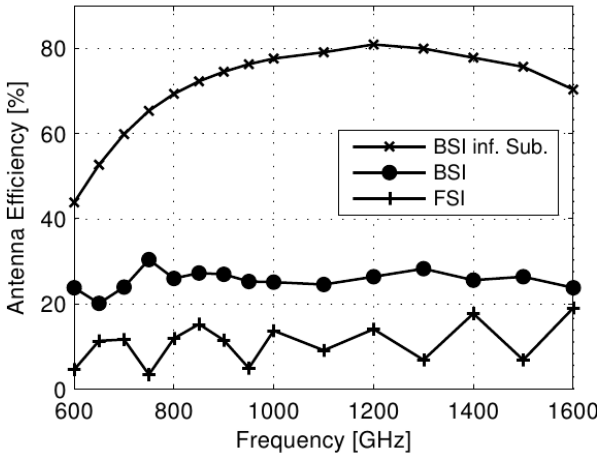


Figure 3-29: Simulated antenna efficiency in different illumination topologies: Back-side illumination, front-side illumination, and back-side through semi-infinite substrate illumination mimicking a Silicon lens [78].

Another important parameter directly impacting the coupling efficiency is the antenna alignment with source. The source/receive antennas should be aligned at their bore-site at horizontal and vertical axis, their azimuthal tilts, as well as the polarization (be it vertical or horizontal). Any mismatches would effectively lead to considerable power loss, and could be quantified according to the Friis transmission equation.

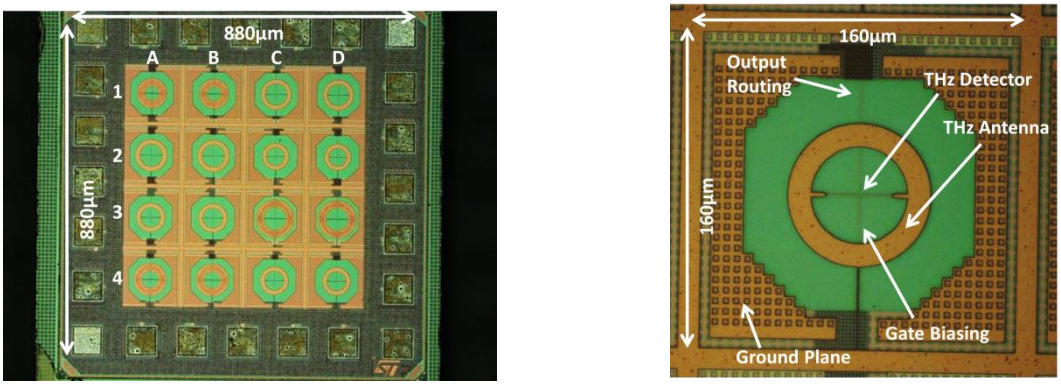
3.3. Detectors in 65nm Bulk

3.3.1. Circuit Design and Implementation

In this section the design, implementation and characterisation of various Terahertz detectors in a 65nm CMOS bulk technology from STMicroelectronics are presented. The designed chips are comprised of 4x4 pixels of different detector and antenna test structures. The test structures where co-designed between the antennas and the detectors of different sizes and impedances following the aforementioned methodology of efficient Terahertz detection in FETs in the previous sections. Following thorough analysis of the detectors in different operating conditions and topologies, the antennas were co-designed with Dr. Janusz Grzyb [129].

As described before, impedance matching at the frequencies of interest is the key to efficient detection. Impedance matching can be done in between the antenna and the detector via passive transmission-lines. Various matching structures were analysed and eventually it was to include the matching elements as intrinsic parts of the antenna. Therefore, the modifications on the feed-lines and antenna diameters and thicknesses have been chosen to match detectors of various sizes, at different bias points and frequencies. The transistor PDK models include metal one, therefore the antennas have been designed down to metal one that defines the input ports of the detectors.

The dice micrograph and a pixel micrograph are presented in Figure 3-30. The chip total size is 880µm x880µm, and the pixel pitch is 160µmx160µm. The chip is ESD protected and fulfils the design rules of the process. A global ground plane extending over the full BEOL is laid-out across the chip. Openings within the ground plane are designed to accommodate the antennas and detectors. These openings include passive and active layers blocking with a carefully adjusted opening size to allow minimal interference with the evanescent waves.

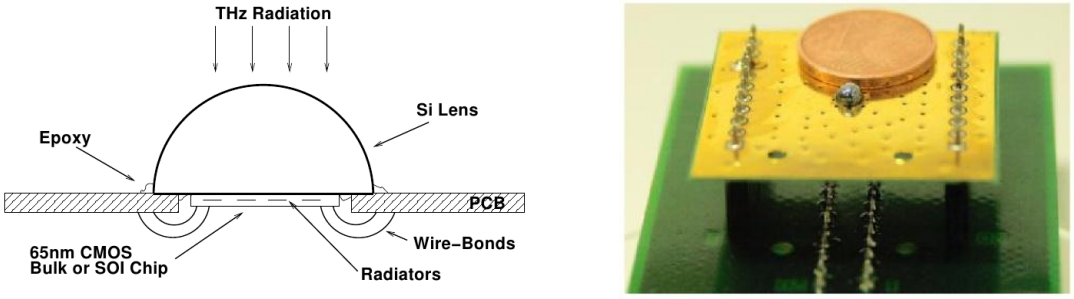


(a) **(b)**

Figure 3-30: (a) Die micrograph of implemented THz- detector test-structures in 65nm bulk CMOS and (b) image of a single pixel.

The circuits are based on the differentially fed through their sources NFET detectors. The detectors are formed by using a double-finger NMOS, as described in section 3.1.5. The gate bias and the signal outputs are routed vertically, and run through a hollow section of the antenna within the zero-field regions, at the H-plane. Each four detectors on the die are gate-biased from a separate biasing pad.

The pixels to be powered up at once are chosen in a manner to be as furthest possible from one another, to enable the examination of neighbour pixel effects such as coupling. The detectors are not isolated from the substrates, as there are no active circuits on the die. It was intended to study the effect of the isolation created underneath the transistors, as it is believed they may deteriorate the detector efficiency due to the added capacitive and resistive parasitics of the diodes created underneath the terminals and the channel.



(a) **(b)**

Figure 3-31: (a) Schematic and (b) photograph of packaging of CMOS chip with a 3mm diameter Silicon hyper-hemispherical lens.

The chip i thinned down to 150μm to increase the signal efficiency and was glued from the backside using low-shrinkage UV-cured epoxy to a 3mm diameter Silicon hyper-hemispherical lens without AR-coating. The chip was then wire-bonded to a low-cost FR4 PCB as shown in Figure 3-31. The chip was aligned to the centre of the lens with B3 being the centre pixel. Therefore, all other pixels are off-axis and their performances are thus sub-optimal.

In the next section, characterisation results of a few selected pixels are presented. As mentioned above, the off-axis pixels are suboptimal due to the reduced received power arising from reflections at the Silicon-air interface. Therefore, the actual performance of these pixels is believed to be better. Measuring them properly requires separate packaging per pixel, where the pixel would be placed exactly in the centre of the lens. Further improvements would be to use anti-reflective coating to the lens.

3.3.2. Measured Results and Analysis

Table 1 presents a list of the measured pixels with their corresponding parameters including the pixel name, device dimensions, and targeted frequency. In this section the measurement results of some selected pixels will be presented and then correlated to the simulated data. This correlation will enable the study the validity of the quasi-static/non-quasi-static analysis that this work is based on. It is worth to mention that the targeted frequency is related to the detectors' best simulated impedances; therefore as frequencies diverge away from the targeted frequency the detector/antenna impedance match starts to degrade. As for the case of broadband matching, a trade-off in the impedance match is employed to enable a wider band of operation.

Pixel name	Transistor characteristics	Targeted frequency
A2	NFET diff. pair, common well, W/L=1µm/0.06µm	850GHz
A3	NFET diff. pair, common well, W/L=1µm/0.06µm	650GHz
A4	NFET diff. pair, common well, W/L=1µm/0.2µm	650GHz
B4	NFET diff. pair, common well, W/L=1µm/0.2µm	800GHz-1THz
C3	NFET diff. pair, common well, W/L=0.3µm/0.06µm	675GHz

Table 1: List of measured test structures in 65nm bulk CMOS technology

The detectors were measured in free-space. A frequency-tuneable power source operating from 650GHz up to 1.1THz and equipped with a diagonal horn antenna was used to illuminate the detector at a distance R.

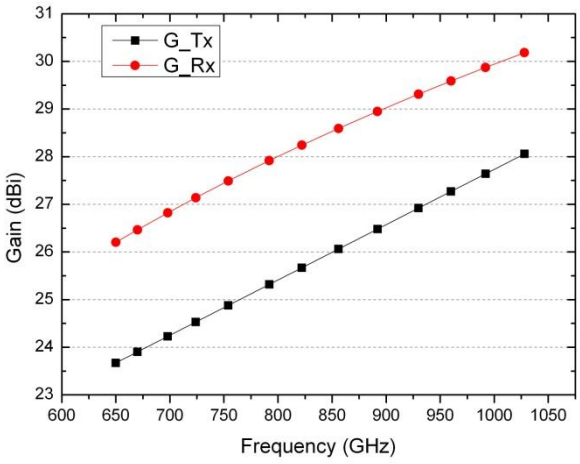
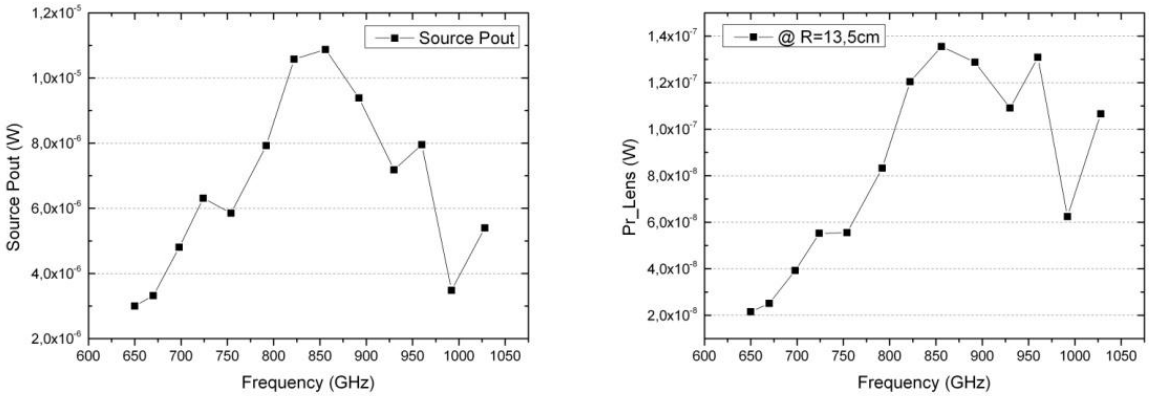


Figure 3-32: Extrapolated gain of transmit antenna based on two points provided by the manufacturer, and calculated receive antenna gain with a lens diameter of 3mm based on the theoretical effective area calculation.

The source antenna has a frequency dependant gain and two points are provided by the manufacturer. An extrapolated plot of the Tx antenna gain is shown in Figure 3-32. The detector antenna gain is shown on the same plot. The directivity has been estimated based on the effective area of the antenna considering the lens solid angle to be the aperture.



(a) **(b)**

Figure 3-33: (a) Calibrated total source output power and (b) calculated received power at a distance of 13,5cm across frequency.

The source power with respect to the bandwidth of operation is shown in Figure 3-33. The source transmits a maximum power of 10.9µW at 856GHz. This power was calibrated using an Ericsson power-meter across the indicated frequency range. According to these transmitted power values, Figure 3-33.b represents the received power at a distance of 13.5cm as calculated using the *Friis transmission equation* including the directivity values in Figure 3-32. These received power levels will be used hereafter for all detectors characterised at a distance of 13.5cm. Some detectors were measured at different distances, and will be denoted accordingly.

First, the noise measurements will be demonstrated. Then, the measurements of the selected pixel will be presented individually.

Noise measurements:

The spot-noise at various frequencies was measured for the three different detector sizes with respect to the variations in gate bias. The noise was measured using an Agilent spectrum analyser by connecting the output of a specific detector to a low-noise voltage amplifier with an amplification factor of 60dBV. The amplifier has an input impedance of around 1TΩ and an output impedance in the MΩ range. The input impedance of the spectrum analyser is 50Ω, thus creating a mismatch at the input. The effective amplification was measured to be 300X by applying a sinusoid and measuring the amplified signal on the spectrum analyser. This noise measurement does not include the device under source illumination. Therefore, the noise plots presented here represent only the device thermal noise along with the low noise amplifier noise including its 1/f noise.

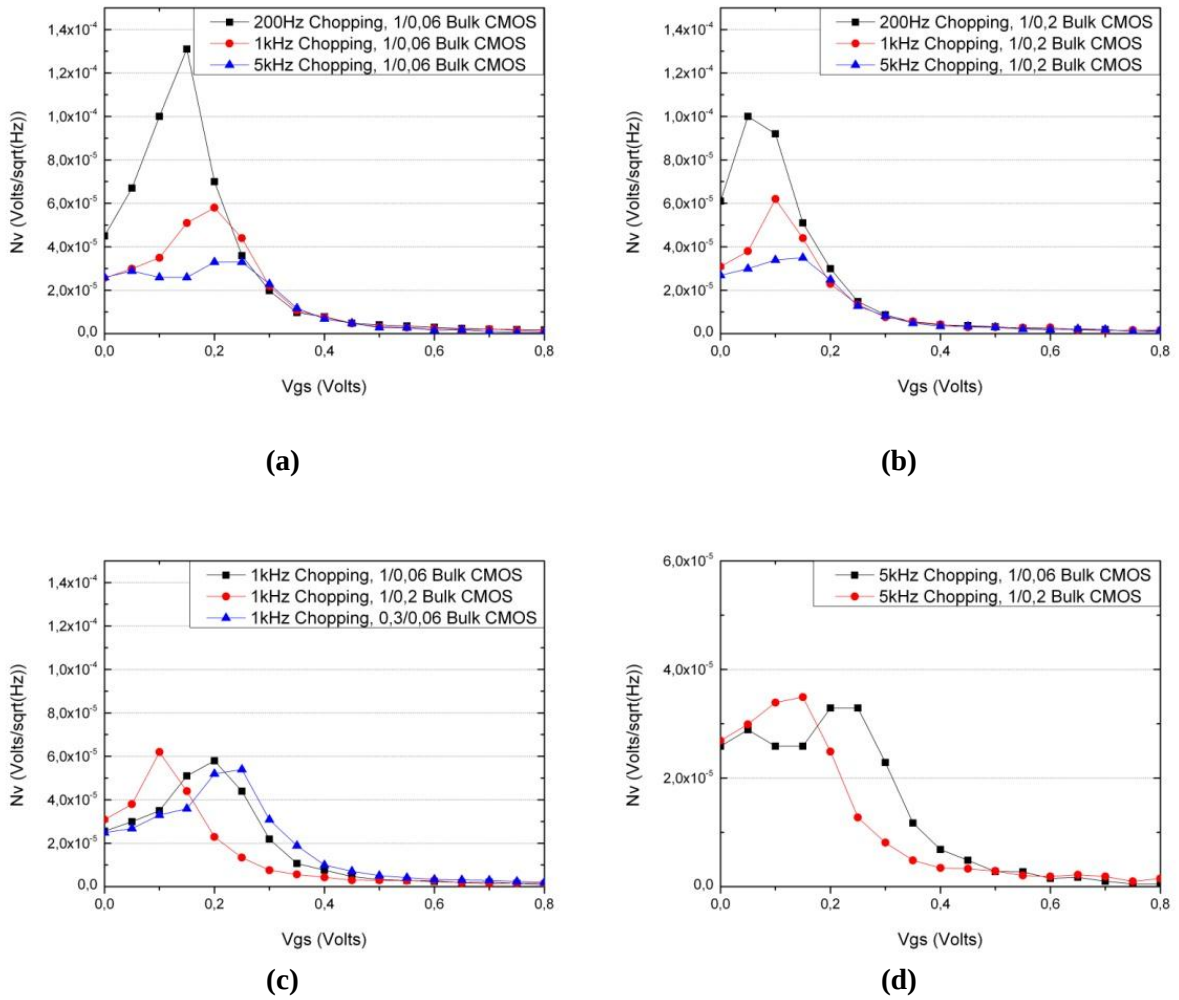


Figure 3-34: Measured output noise-voltage for various detector sizes and over different chopping frequencies

The output noise of a detector with 1µm/0.06µm device-dimensions and that of a 1µm/0.2µm device are shown in Figure 3-34 with respect to gate bias, at 200-Hz, 1-kHz and 5-kHz. As expected, the noise at lower frequencies is much higher than that a higher frequencies as the flicker noise is quite significant. It is worth nothing though that this flicker noise component arises from both the amplifier stage and the intrinsic NFET flicker noise. However, the detector flicker noise level is much lower

since there is no signal applied. As the frequency increases, the major noise contributor is the detector thermal noise which is frequency independent. The measured noise plots align well with the simulated values shown in section 3.1.4, with the exception of the additional injected noise from the external amplifiers.

A comparison between the device sizes in Figure 3-34 shows that the output noise maxima are shifted with respect to the gate bias, yet the noise values are approximately the same at higher chopping frequencies. This is due to the varying channel modulation and, consequently, channel conductance. At very low chopping frequencies, longer and wider devices are more immune to flicker noise in comparison with shorter and narrower devices.

Pixels Characterisation:

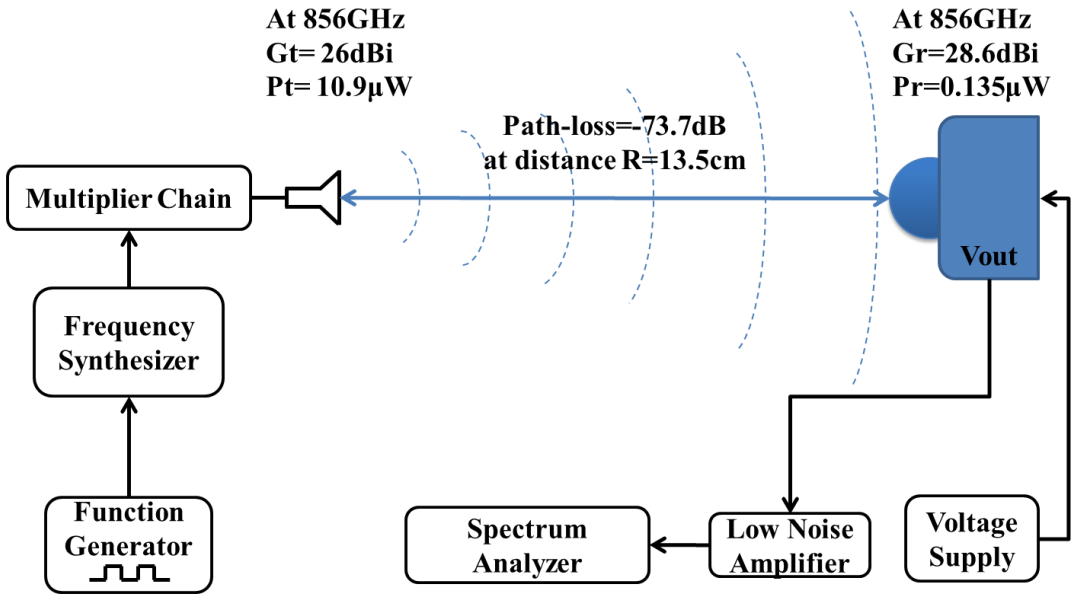


Figure 3-35: Free-space measurement setup example used for the detectors' characterization.

The pixels presented hereafter are measured and characterised in free space as shown in Figure 3-35 and the responsivities and noise equivalent powers are calculated as described in chapter 2. For instance, for a source frequency of 856GHz the source transmits a total power of 10.9µW with an antenna gain of 26dBi. The path loss at a distance of 13.5cm is -73dB, thus the received power at the lens interface is 0.135µW. The gain of the receive antenna is calculated from $G_r = \frac{4\pi A_{eff}}{\lambda^2}$ to be 28.6dBi with an effective antenna area of $A_{eff} = \pi R^2 = 7.07E^{-6}\ m^2$ for a lens radius of 1.5mm.

Below, measurements of each pixel will be presented and analysed with respect to their frequency and DC characteristics. The pixels have been measured at slightly different distances as the data has been collected in different times.

Pixel A2:

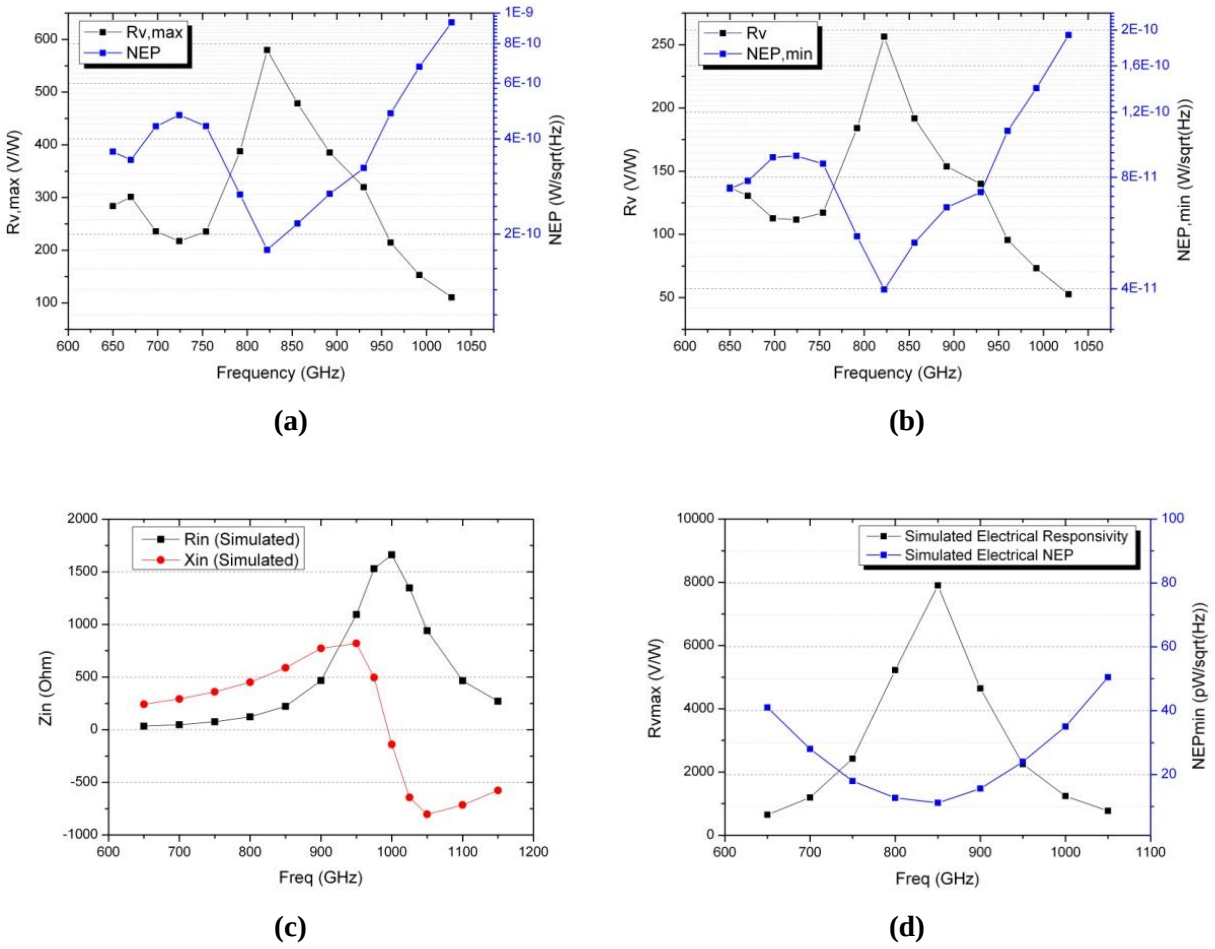


Figure 3-36: Frequency characteristics of pixel A2 where (a) ℜv maxima and their corresponding NEPs and (b) NEP minima and their corresponding ℜvs. (c) Simulated antenna impedance. (d) Simulated Electrical ℜv maxima and NEP minima using the simulated antenna impedances. This antenna has been designed for a peak at 850GHz with a device of W/L=1um/0,06µm. The frequency plot matches the intended design based on simulations using the PDK. The ℜv max is 570V/W V_{GS} = 0.23V, and the NEP_{min} is 40pw/√Hz at V_{GS} = 0.47V at 825GHz. The measurements were performed in the far-field of the Tx and Rx antennas, at a distance of at D=13.5cm. the 3dB bandwidth spans between 770GHz and 930GHz.

Figure 3-36.a-d show the characterisation results of pixel A2. Pixel A2 is designed for a centre frequency of 850GHz. The device has a W/L=1µm/0.06µm. The maximum responsivity at a gate bias of V_{GS} = 0.23V with its corresponding NEP, and the minimum NEP at V_{GS} = 0.47V with its corresponding responsivity are shown in Figure 3-36.a and Figure 3-36.b respectively.

The $\Re v_{max}$ is 570V/W at V_{GS} = 0.23V, and the NEP_{min} is $40pW/\sqrt{Hz}$ at V_{GS} = 0,47V at 825GHz. The measurements were performed in the far-field of the Tx and Rx antennas, at a distance of R=13.5cm and a source modulation frequency of 1kHz. The NEP was extracted from the measured noise shown in Figure 3-34. Antenna impedances versus frequency were simulated using HFSS, and are plotted in Figure 3-36.c. Using these impedance numbers, the responsivity and noise equivalent power were simulated and are shown in Figure 3-36.d. The measured frequency characteristics of pixel A2 present

a good level of correlation with the simulations using the PDK, with the peak responsivity and minimum NEP at 850GHz and the 3dB bandwidth spanning between 770GHz and 930GHz.

Pixel A3:

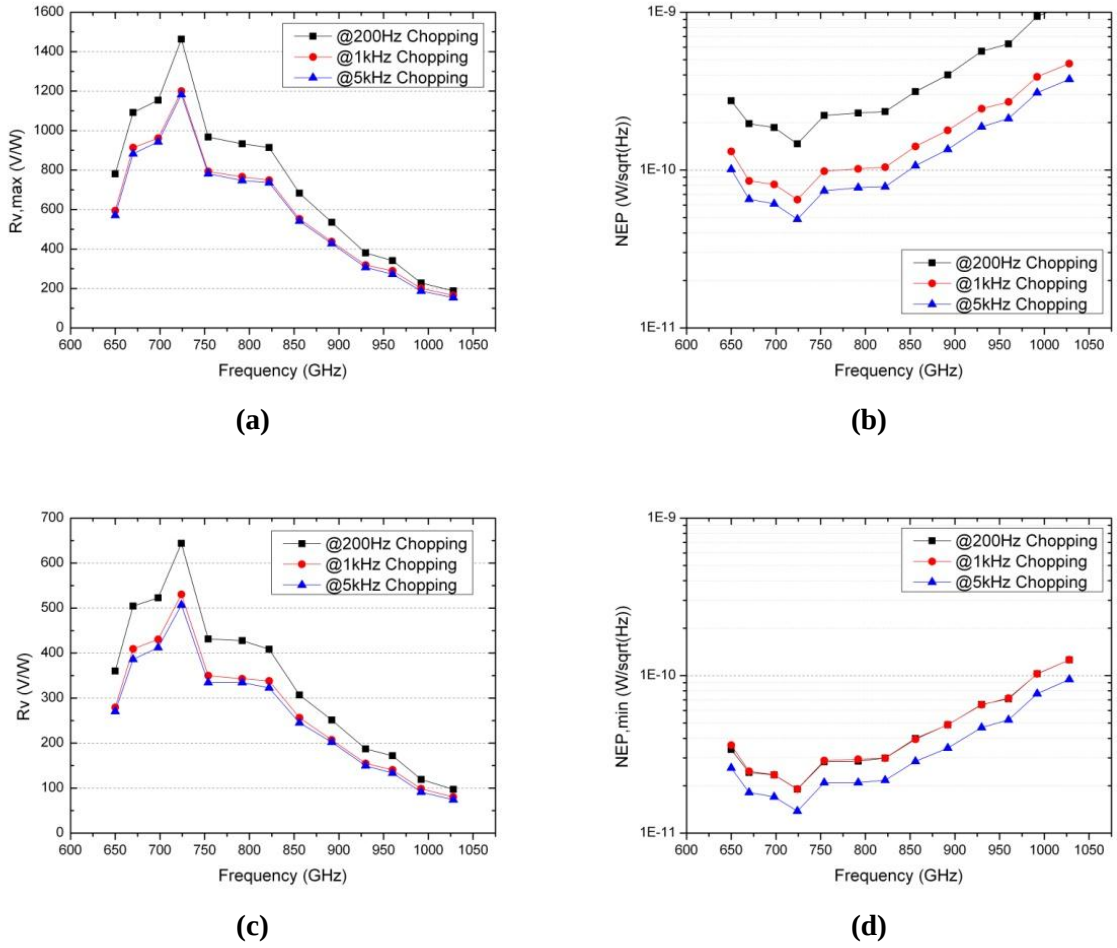


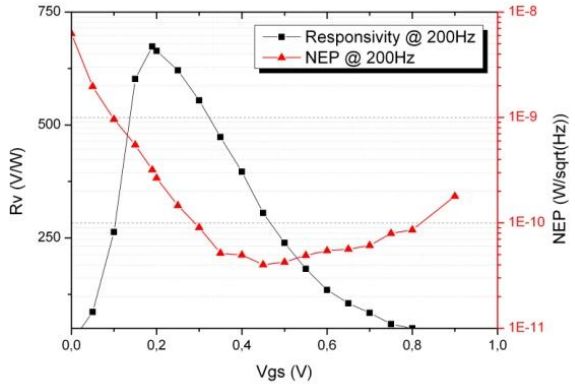
Figure 3-37: Frequency characteristics of pixel A3 at R=14,5cm showing the (a) maximum ℜvs and (b) their corresponding NEPs frequency characteristics with respect to chopping frequency. (d) Minimum NEPs and (c) their corresponding ℜvs across source frequency and with respect to chopping frequency. Key values: ℜv =1450V/W and NEP=318pW/√Hz @200Hz, at V_{GS} =0.19V. ℜv =650/W and NEP=20pW/√Hz at V_{GS} =0.45V

Pixel A3 was measured at a distance of 14.5cm from the source. The responsivity measurements were done at 200Hz, 1-kHz, and 5-kHz source modulation frequency, and the noise measurements were extracted accordingly. Figure 3-37.a represents the maximum responsivity measured at a gate bias of 0.19V across various frequencies and Figure 3-37.b represents the NEP at the same gate bias.

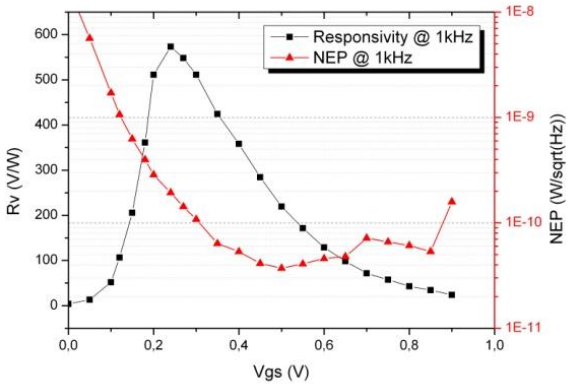
The minimum NEP with its corresponding responsivity was measured at a gate bias of 0.45V for the same source frequency range. The responsivity peaks at a source frequency of 724-GHz and is found to be around ℜv=1450V/W at a chopping frequency of 200-Hz, and is reduced to 1200V/W at a chopping of 1-kHz and above. The variation in responsivity is due to the capacitive loading of the detectors, as the capacitive cables filter shunts the signals with the increase in frequency. However, the much higher noise level at 200Hz makes it worse in terms of NEP, even though the responsivity is

higher. This is apparent also at the region of minimum NEP shown in Figure 3-37.c and Figure 3-37.d, where the NEP_{min} at a gate bias of 0.45V is 20pW at a chopping frequency of 200Hz and $14pW/\sqrt{Hz}$ at a chopping frequency of 5-kHz.

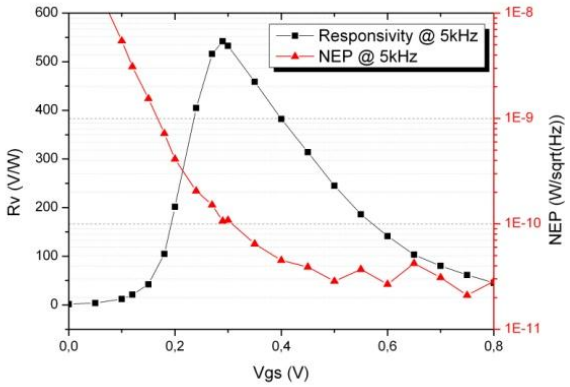
These are the best values recorded thus far in literature for CMOS based detectors and are as good as or better than the current state of the art THz direct detectors[130]. The frequency characteristics show a 3dB-bandwidth ranging from 650-GHz up to 850-GHz.



(a)



(b)



(c)

Figure 3-38: Pixel A3 at R=14.5cm versus gate bias at 856GHz at (a) 200Hz (b) 1kHz and (b) 5kHz chopping frequency

The responsivity and NEP at a frequency of 856GHz was also measured across the different operation regions of the transistors, at 200Hz, 1kHz, and 5kHz and are shown in Figure 3-38. This frequency is not that of the maximum responsivity and NEP. However, the plots show the transistor behaviour when matched properly for an increase in responsivity at the regions of minimum NEPs. These plots also show that for a proper readout circuitry design, chopping at higher frequencies may be deemed favourable as the 1/f-noise of the circuitry could play performance-changing role.

Pixel A4:

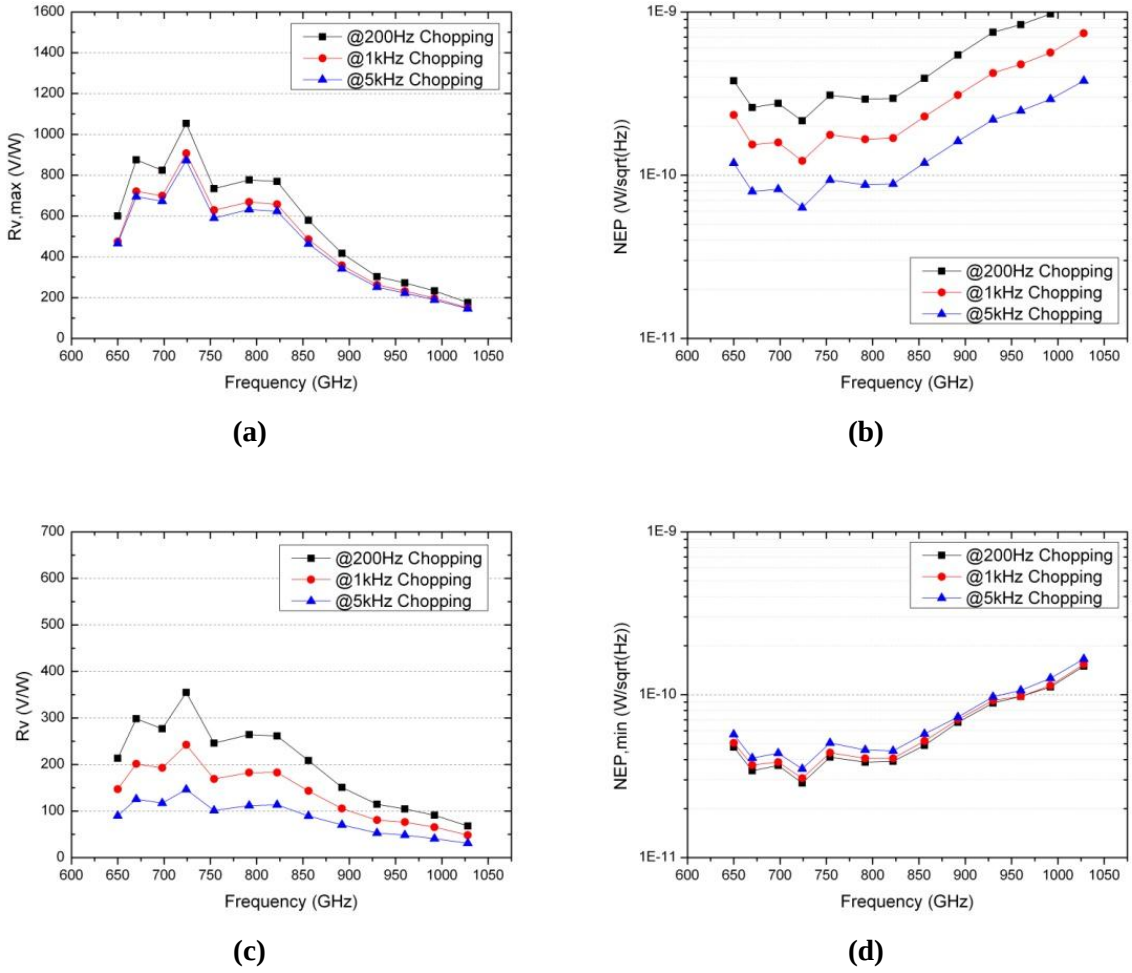


Figure 3-39: A4 pixel measured at R=14.5cm showing the (a) maximum ℜvs and (b) their corresponding NEPs frequency characteristics with respect to chopping frequency. (d) Minimum NEPs and (c) their corresponding ℜvs across source frequency and with respect to chopping frequency.

This pixel is equipped with the same ring antenna utilised for pixel A3, yet with a differential NFET pair of wider transistors, with 1um/0.2um dimensions, each. The antenna is designed to match the 60nm wide transistors; therefore this antenna is mismatched to the 200nm wide transistors. Figure 3-39 shows the measured maximum responsivities and their corresponding NEPs, as well as the minimum NEPs with their corresponding ℜvs. The measurements were carried out at a distance of R=14.5cm, over a frequency range of 650GHz up to 1.05THz, with chopping frequencies of 200Hz, 1kHz and 5kHz. In comparison with pixel A2, it is obvious that the maximum ℜvs and minimum NEPs are deteriorated across the spectrum and at all chopping frequencies.

It is also visible how the NEPs at the maximum ℜvs are widely dependant on the chopping frequencies, and likewise behaves the ℜvs at minimum NEPs. The ℜv peaks at a frequency of 724GHz with a chopping frequency of 200Hz and a value of 1100V/W, and the NEP minimum is also at 724GHz but for a chopping frequency of 5kHz, and a value of 35pW/√Hz. This is interesting because we know that the ℜv deterioration with respect to chopping frequency is only due to the

capacitive loading of the device, therefore, with proper termination at the output the ℜv essentially should remain constant.

It can be observed that the ℜv maxima shift their bias-positioning with respect to chopping frequencies. This is mainly due to the frequency-dependant match of the detector channel with the output loading. As the modulation frequency increases, the detector match at the output is deteriorated at its high-impedance at the sub-threshold regime with respect to the decreasing load-impedance due to the capacitive-effects. However, even though the ℜv decreases significantly, the enhancement in the noise performance counters and betters the NEP values. We can deduce the benefit of chopping at higher frequencies, primarily to reduce the 1/f-noise of both the detector and the readout electronics.

Pixel B4

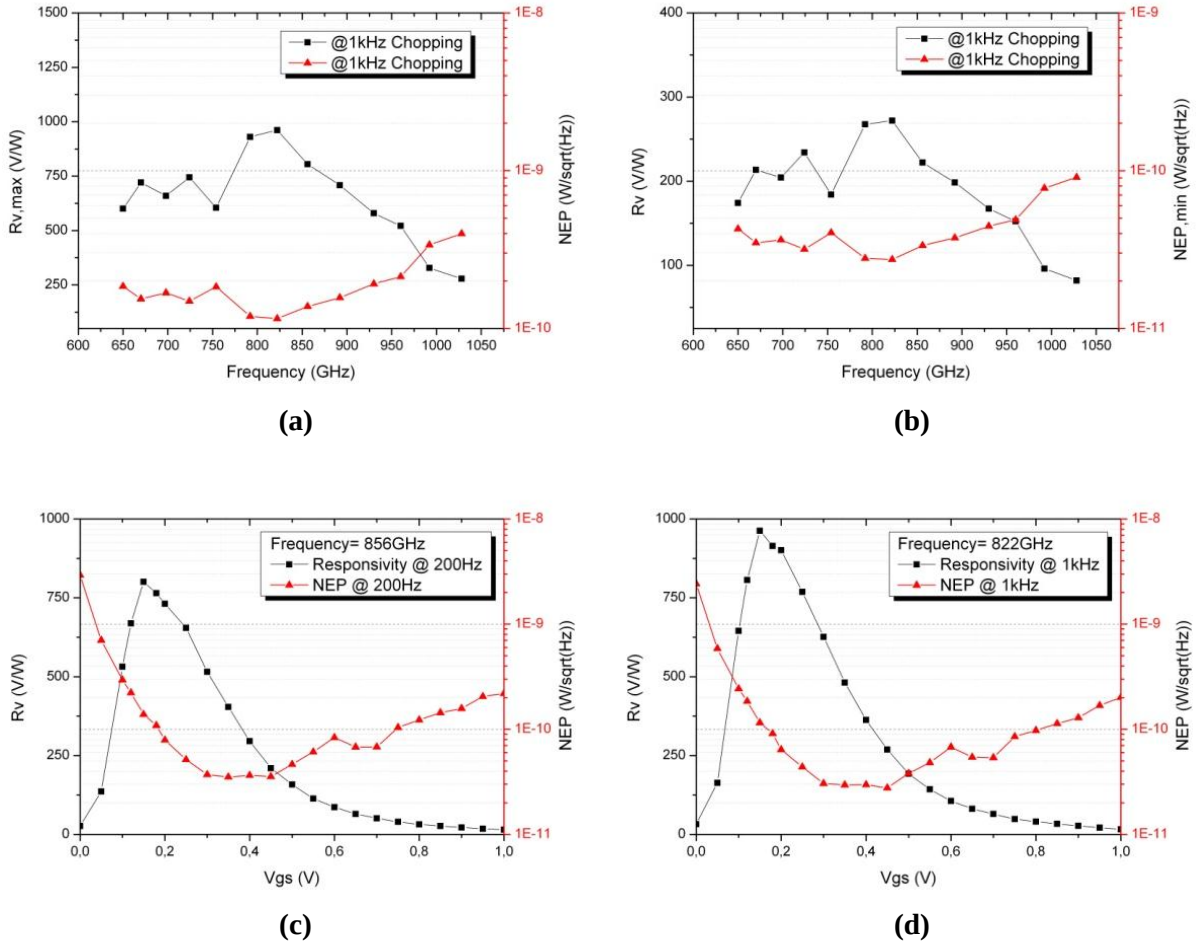


Figure 3-40 Pixel B4 measured at R=14.5cm and 1kHz chopping frequency, showing the (a) maximum ℜvs and their corresponding NEPs frequency characteristics with respect to chopping frequency; (b) minimum NEPs and their corresponding ℜvs. Responsivities and NEP DC characteristics at 856GHz source frequency at (c) 200Hz and (d) 1kHz chopping frequencies.

This pixel is equipped with an antenna matched to offer a bandwidth between 800GHz and 1THz. However the matching favours a detector of 1um/0.06µm dimensions, which is presented in pixel B3. Unfortunately B3 is not characterised yet, thus B4 shall provide a suboptimal performance as to what this antenna is capable of delivering.

Figure 3-40 shows the measured responsivities and NEPs at a distance of 14.5cm with respect to a sweep of transmitted frequency. At 1-kHz, the responsivity peaks at 822GHz with a value of 960V/W and the NEP minimum is 26pW/√Hz at the same frequency. The 3dB bandwidth spans from 650GHz to 960GHz.

Pixel C3

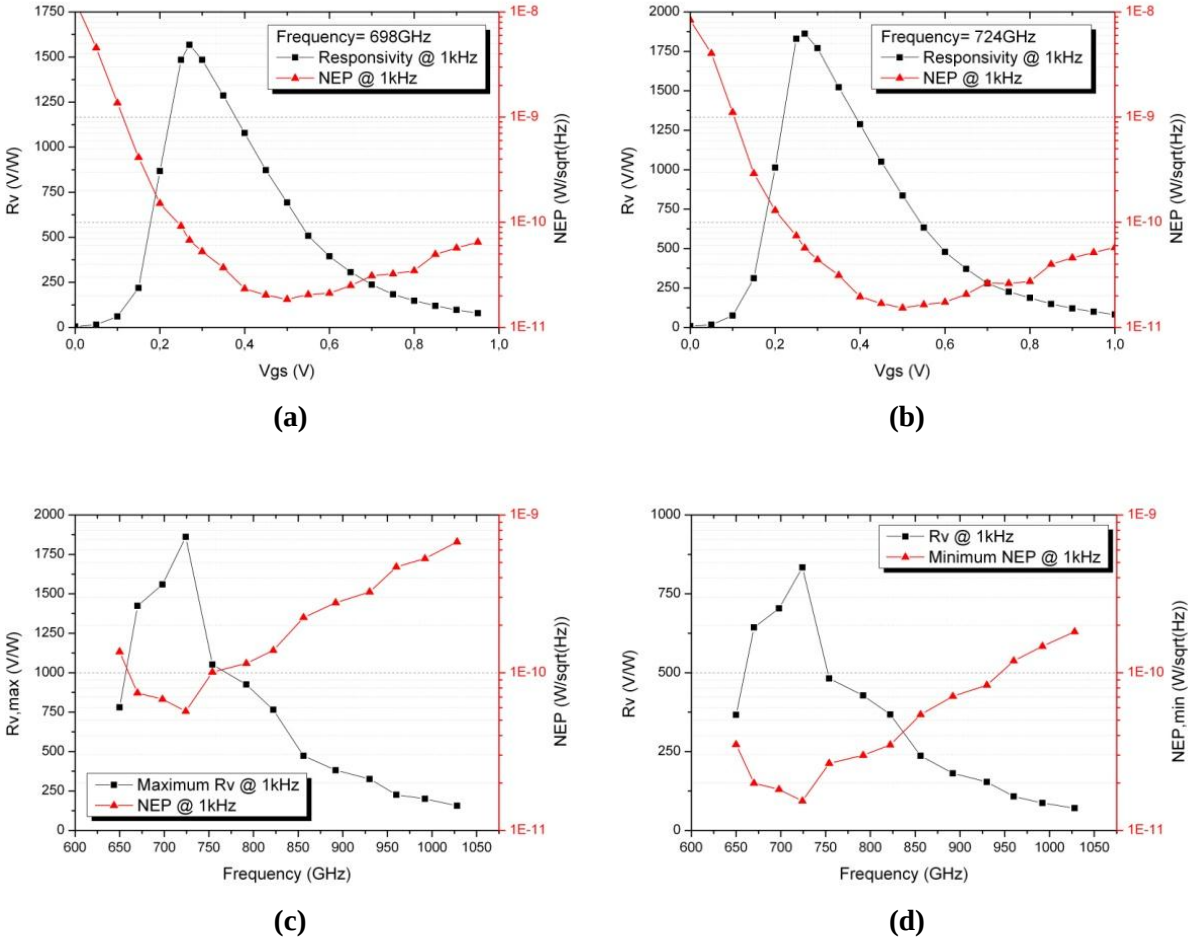


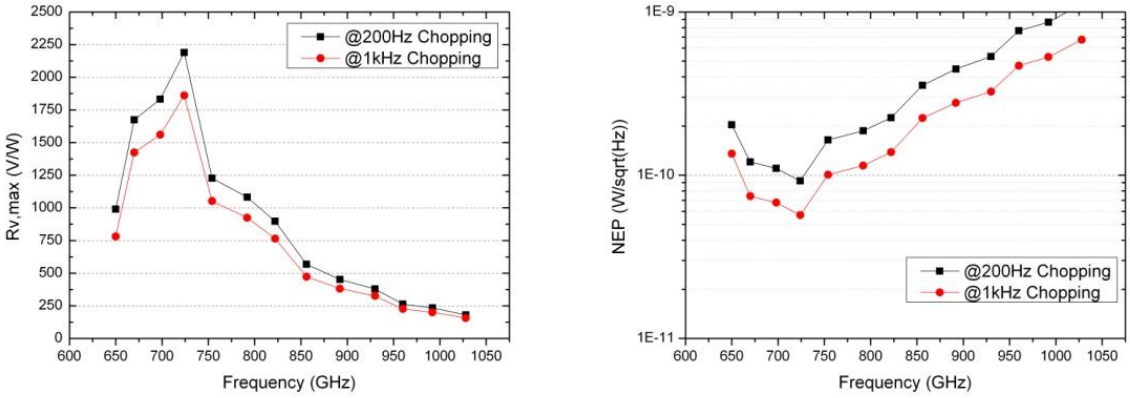
Figure 3-41 pixel C3 measured at 14.5cm and 1kHz chopping frequency, showing responsivities and NEP DC characteristics at 1kHz chopping frequencies for (a) 698GHz source frequency at (b) 724GHz source frequencies.
(c) Maximum ℜvs and their corresponding NEP at 1kHz; (b) minimum NEPs and their corresponding ℜv at 1kHz.

This pixel was measured at a distance of 14.5cm. It is equipped with an antenna designed to match best at 675GHz for a differential NFET pair of 0.3µm/0.06µm device dimensions. Figure 3-41a and b present the responsivity and NEP at 1kHz chopping with respect to gate bias at transmission frequencies of 698GHz and 724GHz respectively.

The responsivity peaks at 724GHz and attains a value of 1850V/W and a responsivity of 1650V/W at a frequency of 698GHz. The frequency characteristics are shown in Figure 3-41c and d, and show a 3dB bandwidth between 650GHz and 750GHz. The minimum NEP attained is at 724GHz, dipping to

15pW/√Hz. This could be enhanced even further by chopping at 5kHz or beyond, and the NEP values are expected to dip even further below pixel A3.

Figure 3-42 shows the chopping frequency influence. At 200Hz, the max ℜv reaches 2240V/W, and therefore we can observe that if we attain this responsivity at a higher chopping frequency, the NEP minima could be even further enhanced.



(a) **(b)**

Figure 3-42: Pixel C3 measured at 14.5cm for 200Hz and 1kHz chopping frequencies. (a) Measurement of maximum ℜvs (b) and their corresponding NEPs.

3.4. Detectors in 28nm FDSOI

In this section the design and characterisation of single-pixel THz detectors implemented in a 28nm fully-depleted silicon-on-insulator CMOS technology is presented.

3.4.1. Circuit Design and Implementation

The intention of this design is to test the capabilities of THz detection in the recently available 28nm FDSOI technology. At the time of design, no RF models of the transistors were yet available, and thus a complete co-design between the detectors and the antennas was not possible.

It is essential to mention a few notes on the antenna design. The antennas are ring antennas based on the reported antennas in the previous sections on bulk CMOS. The technology backend in the FDSOI technology is comprised of a 10metal stack. Therefore the antennas needed to be resized to include the entire metal stack, to comply with the metal-density uniformity across the chip imposed by the process rules. However, as the transistors are fully isolated from the substrates, protection diodes were obligatory to protect the transistors' terminals during the CMP process. Creating antenna-diodes at the RF path is surely not favoured as they will act as parasitic capacitances that will deteriorate the signals arriving from the antenna ports.

Several techniques including creating metals loops were employed, but diodes were still required to be placed. Thus, protection diodes at the antenna DC bias that runs across the zero-intensity fields were placed. The antenna metal loops at the feed-lines need to be further optimised in the future to include their inductive effects, which by all means could be in the benefit of countering the capacitive impedances of the detectors.

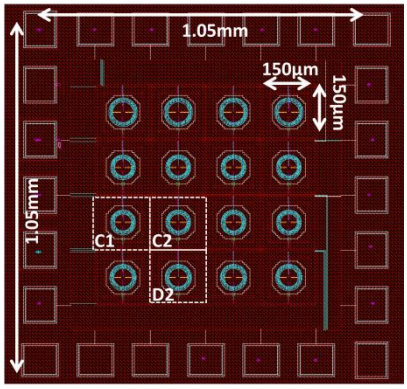


Figure 3-43: FDSOI chip micrograph

Additionally, as the tight CMP design rules were stringent at the time, as the technology is dedicated for pure digital design. Therefore, the design of antennas has included un-wanted fillers in the proximity of the antennas near-fields. Especially, an un-favoured filling of silicided poly-silicon within a region close to the antennas is single out as a main influence. EM simulations of the antennas with and without the poly-Silicon fillers have shown that the antenna efficiency have been degraded from 60-70% down to 10-15%. It is thus evident that further optimisation is vital, and thus the results that will be presented hereon are suboptimal due to the EM-influence. A solution to this problem is to

connect localized poly-silicon fillers to the antenna, and EM simulations show an improvement of efficiency back to 50%. These optimised antennas are not included in this thesis.

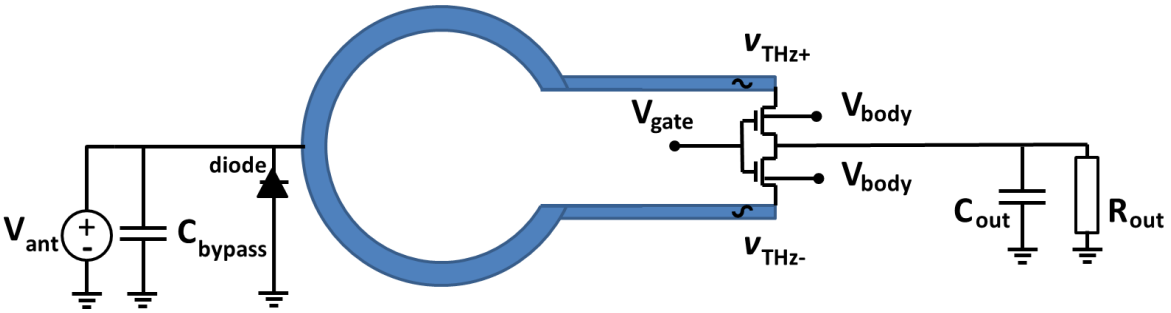


Figure 3-44: FDSOI pixel circuit design

The circuit has included a variety of detector sizes from the smallest detector sizes that include the highest input impedance, to detector sizes of the same dimensions used in the bulk CMOS design presented in the previous section. The chip micrograph is shown in Figure 3-43 with dimensions of 1.05mmx1.05mm and a pixel pitch of 150µmx150µm. All the detectors differentially fed through the sources, are biased by a single gate bias pad and a single pixel schematic is shown in Figure 3-44. The bodies of all detectors are controlled by another pad, and the mechanism is shown in Figure 3-45. The body bias acts as contact to the second gate with the buried oxide being thicker than the first gate oxide. Therefore, the gate bias modulates the threshold voltage of the transistor.

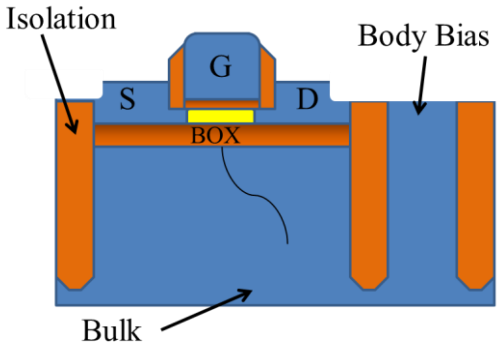


Figure 3-45: FDSOI transistor cross-section showing body access

As discussed in chapter 2, the FDSOI technology offers better isolation of the transistors from the noisy bulk. In our specific case, the full isolation from the substrate effectively enhances the noise performance and increasing the signal coupling efficiency to the detector channel due to the decreased parasitic effects underneath the terminals' junctions.

Various applications for the body bias are foreseen, such as modifying the operation regime of the transistors, or performing reset mechanisms of the detectors in the case of multi-pixel designs. However, no direct impact on the THz performance of the detectors via modifying the body voltage-level is yet observed.

3.4.2. Measured Results

Table 2 presents a list of the measured pixels with their corresponding parameters including the pixel name, device dimensions, and targeted frequency. All transistors were measured in free space at a distance of R=15cm using the same methods utilized in the previous section on 65nm bulk CMOS design.

Pixel Name	Transistor Characteristics	Targeted Frequency
C1	Fully Depleted NFET, common well, W/L=1µm/0.06µm	850GHz
C2	Fully Depleted NFET, common well, W/L=1µm/0.03µm	850GHz
D2	Fully Depleted NFET, common well, W/L=0.08µm/0.06µm	Broadband: 600-1000GHz

Table 2: list of measured pixels with their characterisitcs

The noise measurements will be presented next, and the pixel characterisation results will be subsequently demonstrated and discussed.

Noise measurements:

The noise voltage was measured at 1-kHz for the three different detector sizes, 1/0.06µm, 1/0.03µm, and 0.08µm/0.06µm. The measured plots versus the gate bias are shown in Figure 3-46. The measurements show the difference in the noise behaviour or the transistors with the change of the detector dimensions. As discussed in section 3.4.3, the increase of the noise around the sub-threshold regions is due to the increased flicker noise that adds on top of the white thermal noise. However the flicker noise seen here is mainly due to the off-chip low noise amplifier as no signal is provided tot eh THz detectors. These noise measurements will be used hereafter for the calculation of the NEP of the detectors.

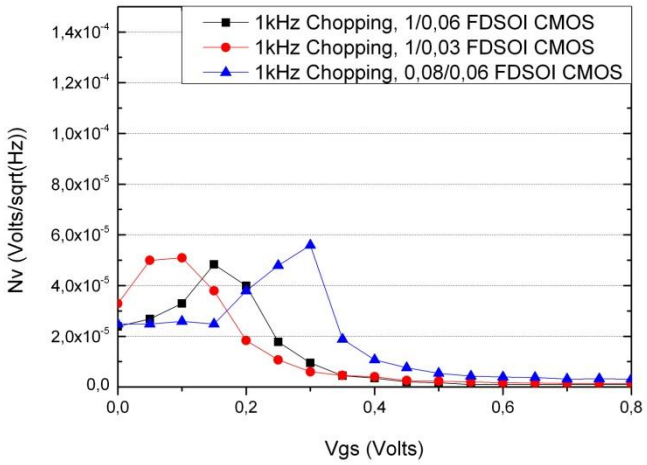
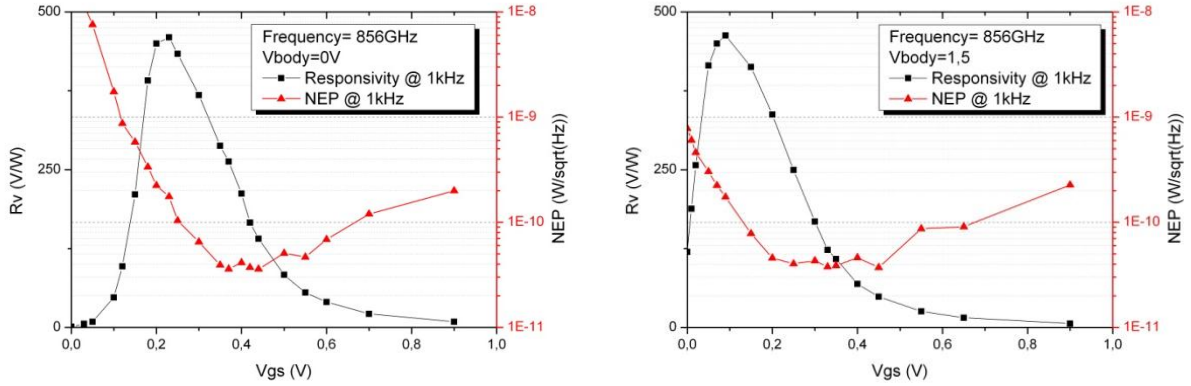


Figure 3-46: Output noise voltage at 1kHz for various detector sizes

Pixel C1:

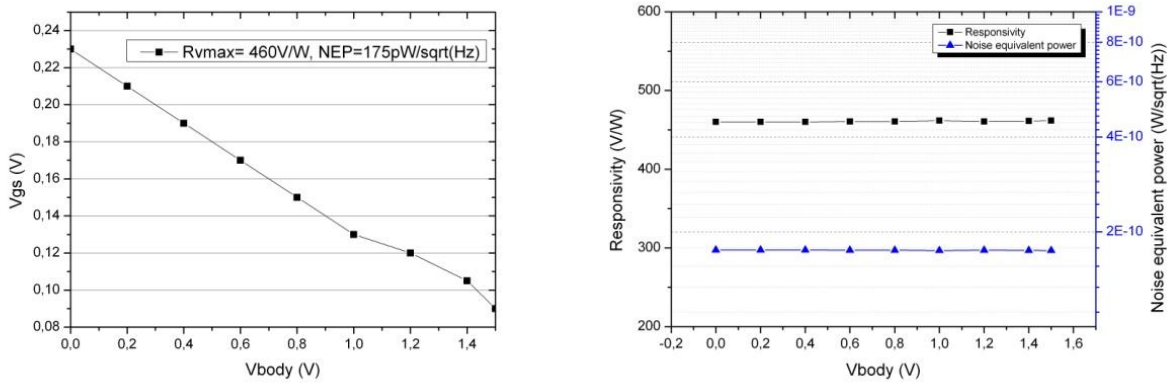
Figure 3-47 shows two plots of the responsivity and NEP at 856GHz and a 1-kHz chopping for pixel C1 at a body bias of 0V and 1.5V. For a body bias of 0V, the maximum responsivity is 460V/W at a gate bias of 0.23V, and the minimum NEP is 37pW/√Hz at a gate bias of 0.42V. When biasing the body at 1.5V, the threshold voltage moves downwards, and the entire behaviour of the detector shifts with respect gate bias. Then, the maximum responsivity is also 460V/W but is located at a gate bias of 0.09V, and the minimum NEP is also 37pW/√Hz at V_{GS} =0.33V.



(a) **(b)**

Figure 3-47 Pixel C1 measured at 856GHz and a 1kHz chopping frequency. (a) Responsivity and NEP measurements across gate bias and a body bias of 0V (b) and a body bias of 1.5V

Sweeping through the body bias and modifying the gate bias accordingly to locate the maximum responsivity shows that the ℜv max is always constant. This is shown in Figure 3-48 where the $\Re v_{max}$ is always 460V/W with its corresponding NEP being 175pW/√Hz. This NEP value is not the minimum NEP, but rather the NEP at the specific maximum ℜv. As we can see, biasing the body at a higher voltage would end up with a detector attaining a high ℜv at a zero gate voltage bias.

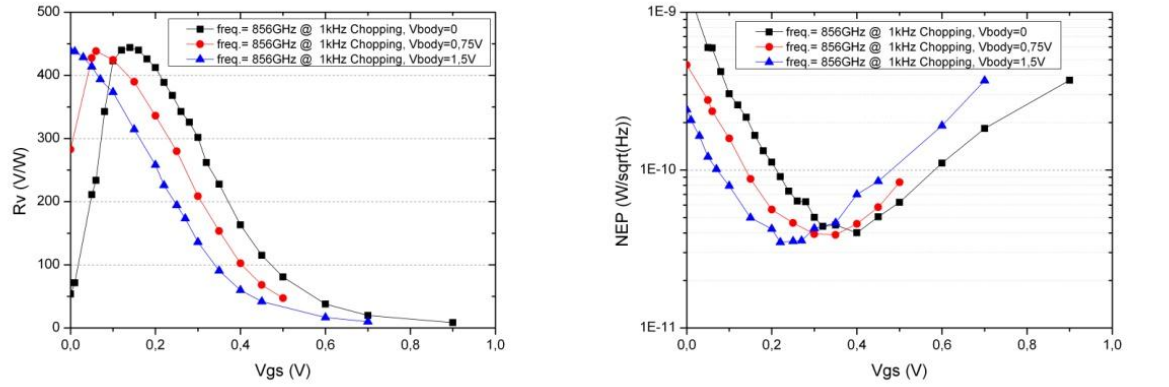


(a) **(b)**

Figure 3-48: Pixel C1 measurements show (a) the shift of the maximum ℜv of 460V/W across the gate bias corresponding NEP of 175pW/√Hz, with respect to the body bias sweep (b) which remains fixed across body bias.

Pixel C2:

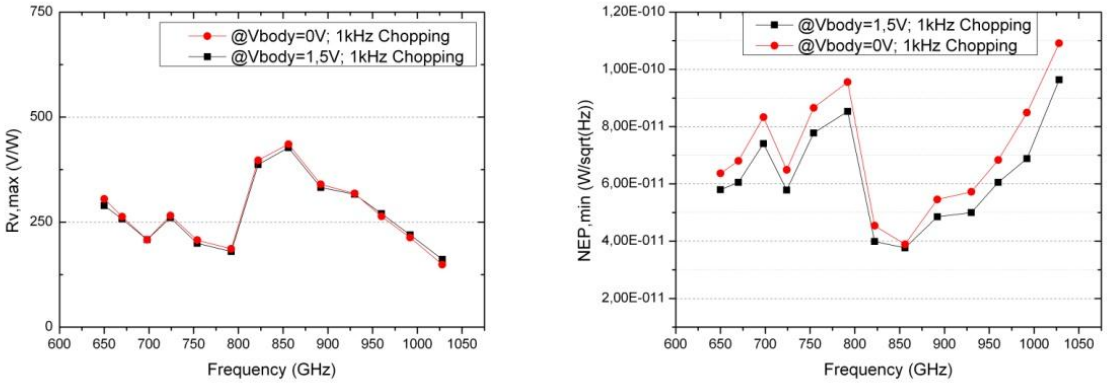
We perform the same measurement methodology employed for C1, and apply it to pixel C2. This pixel is designed with the minimum transistor gate length of 22nm. The maximum measured responsivity at 1kHz for a frequency of 856Ghz is 450V/W for a body bias of 0V, 0.75V, and 1.5V. the minimum measured NEP is 45pW/√Hz.



(a) **(b)**

Figure 3-49: Pixel C2 (a) ℜv and (b) NEP, both measured across gate bias at 1kHz, a distance of 15cm, at 856GHz source frequency, at 0V, 0.75V, and 1.5V body biases.

The frequency response of the detector at 1kHz at a body bias of 0V and 1.5V are shown in Figure 3-50. Once again, the body bias shows minimal RF impact, yet the ℜv maximas and NEP minimas shift over gate bias-level according to the body bias-level.



(a) **(b)**

Figure 3-50: Pixel C2, (a) maximum ℜv and (b) minimum NEP, measured at a 1kHz chopping frequency, a distance of 15cm, at 0V and 1.5V body bias, across various source frequencies

Pixel D2:

Pixel D2 is the smallest detector width available by the technology. Even though the detector attains high input impedance, the noise levels are significantly higher than the other transistors presented before. It is essential, however, to observe the eventual behaviour when the transistors are properly matched to the antennas. Figure 3-51 presents the $\Re v$ and NEP of the detector at 856GHz, 1kHz chopping frequency, with respect to the biasing voltage. The detector peaks at around 0.3V, with an $\Re v_{max}$=580V/W. However, the responsivity rolls off drastically in the sub-threshold domain, and this is believed to be due to the output loading conditions in view of the utterly high impedance levels in the sub-threshold domain.

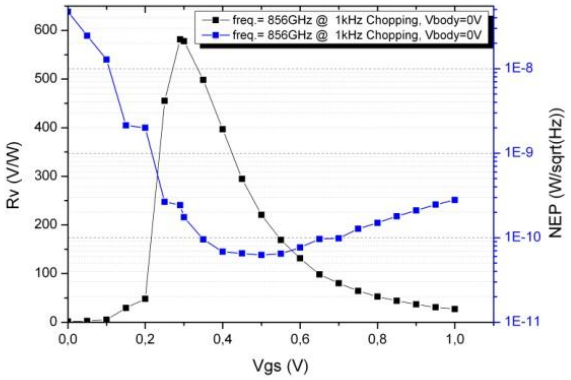
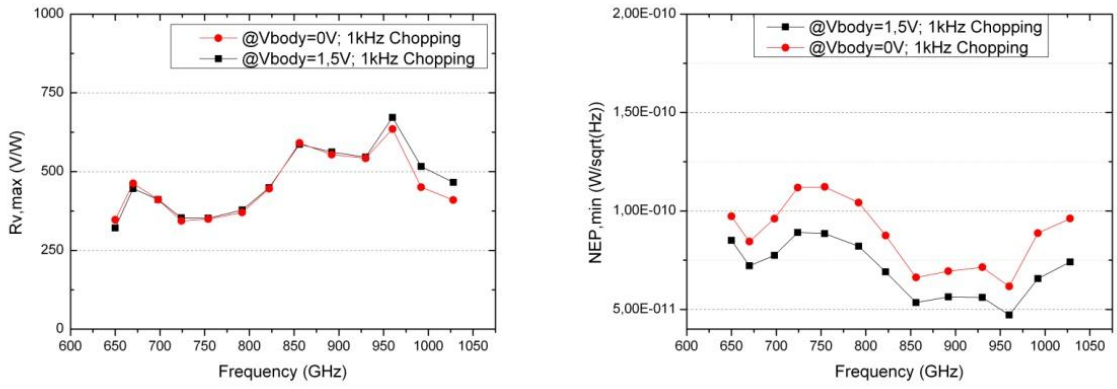


Figure 3-51: Pixel D2 $\Re v$ and NEP measured at 15cm, a 1kHz chopping frequency, at 856GHz, and V_{body} =0V.

A frequency sweep for the same detector was performed and is shown in Figure 3-52 for body biasing at 0V and 1.5V. The antenna used here is designed for a broad bandwidth, which can be observed over the entire measured spectrum. The 3dB bandwidth spans from 650GHz up to 1THz.



(a) **(b)**

Figure 3-52: (a) $\Re v$ maxima and (b) NEP minima at a distance of 15cm and 1kHz chopping frequency, across frequency

3.4.3. Analysis and Comparison

It is rather worthwhile comparing the measured noise levels of two devices of the same dimensions in the two different technologies we have presented in this work, 65nm bulk CMOS and 28nm FDSOI CMOS. We do not have measured data yet for detectors of the same size equipped with the same antennas, even-though the hardware includes a few variations that have similar antennas.

Figure 3-53 compares the measured noise voltage of two differential detectors in 65nm bulk CMOS and in 28nm FDSOI CMOS technologies, with dimensions of 1um/0.06µm each. The measurements were carried out at 1-kHz spot frequency and are amplified by 1000X using an external high impedance low noise amplifier. The FDSOI measured results show lower noise levels compared to the bulk CMOS, especially at the regions of interest defined between 0.2 and 0.4V. With the proper antenna matching to the detectors the responsivity could be further enhanced and therefore the NEP could benefit from both by the lower noise levels and the increased responsivity.

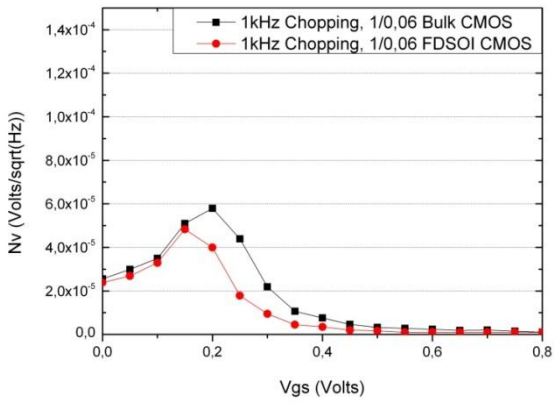


Figure 3-53: Comparison of noise from differential 1um/0.06µm transistors in 65nm Bulk and 28nm FDSOI

3.5. Circuits for Dual Polarization THz Detection

Novel ideas for mm-Wave and THz detection based on polarization diverse antennas are proposed here. This technique requires the usage of two THz sources that emit at orthogonal antenna polarizations. In the case of commercially available sources such as VDI sources, the radiation is transmitted via diagonal horns. Diagonal horns, due to their geometry, spill part of the power from the cross to the co polarization [131], [132]. Therefore, this radiation could be still utilized rather than being lost.

The main applications of such as system are shown in Figure 3-54, and are summed up as follows:

- Polarization diverse imaging could potentially present different information about the object under test. Thus, a system implemented as in Figure 3-54.a effectively leads to two different outputs corresponding to the received power at its corresponding polarization.
- Homodyne and heterodyne mixing could be enabled within the same pixels and without the implementation of on-chip local oscillators. The radiation received at the orthogonal (cross and co) polarizations could exhibit the same or different frequencies. As the signals excited the antenna at different polarizations, as in Figure 3-54.b.
- In current mode operation of THz mixers, the outputs of the mixers could be combined for a higher overall responsivity of the system. This is only beneficial in the case where the source exhibits a power spill over its co-polarization.

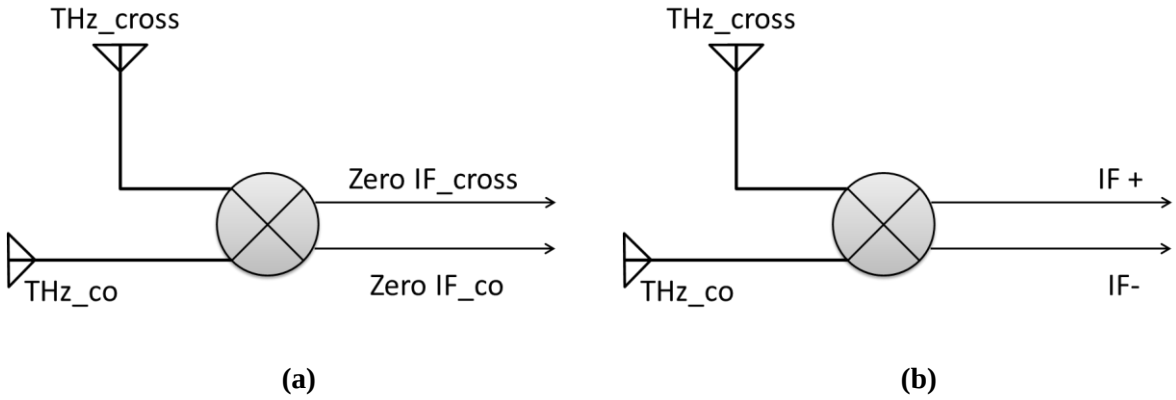


Figure 3-54: Block diagram of (a) polarization diverse THz mixer and (b) polarization diverse heterodyne mixer

3.5.1. Circuit Design and Implementation

Polarization diverse antennas and their detectors were implemented in a 65nm CMOS bulk technology. The antennas were designed by Dr. Janusz Grzyb following analysis and discussions on the concept. I have designed the circuitry and the entire chip. The circuit is comprised of two sets of differential source driven NFETs, as shown in Figure 3-55, with 1um wide and 60nm long low V_T low power RF transistors. Each pair is connected via its sources to one polarization port of the antenna.

The outputs of the transistors and the corresponding gate biases are routed diagonally, as shown in Figure 3-55.b. Measurements of these detectors have not been carried out yet at the time of writing this thesis.

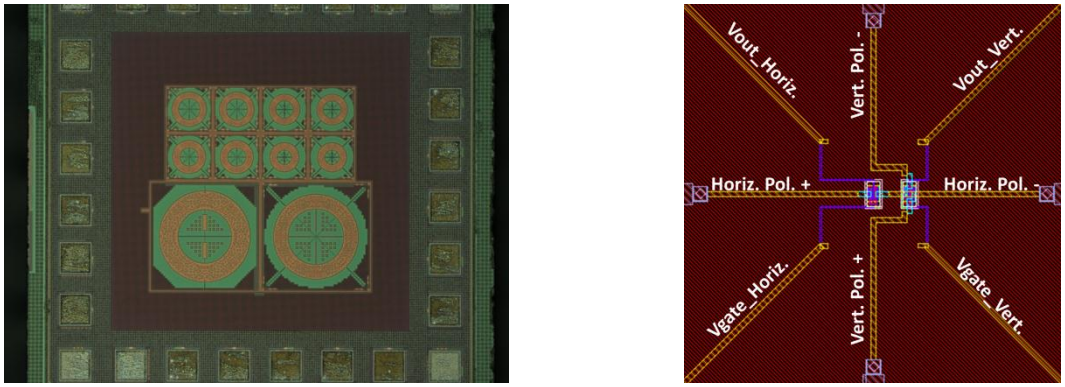


Figure 3-55: Chip micrograph of test structures with dual polarization antennas and detectors

The realised circuit schematic is shown in Figure 3-56 where the RF feeds are connected to the same antenna, receiving from a different polarisation, and the outputs are routed separately.

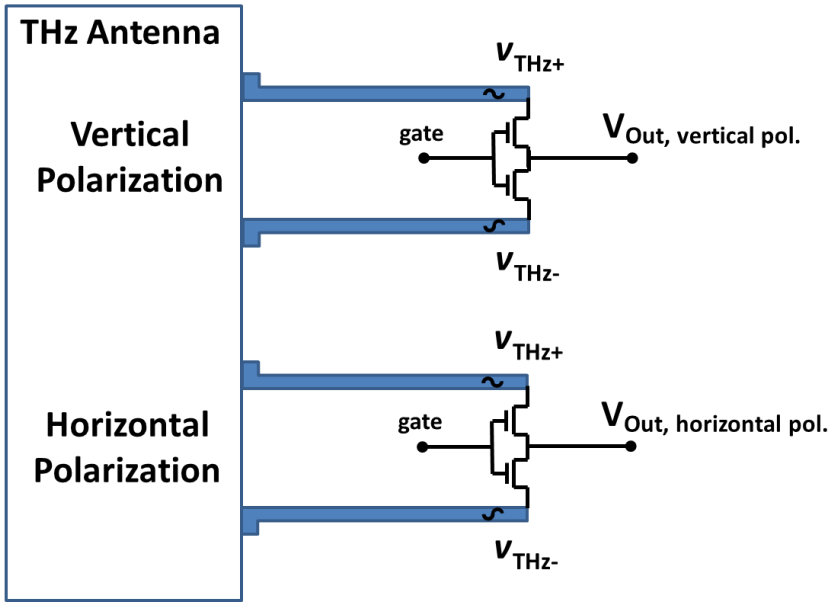


Figure 3-56: Schematic of dual polarisation circuit and antenna.

3.6. Circuits with Output Combining

Another detector topology is proposed with multiple Terahertz detectors with output combining. The topology is shown in Figure 3-57. The circuit generally comprises of N detectors equipped with their individual antennas and connected in parallel at their corresponding outputs. This topology increases the antenna effective area leading to a higher power coupling. Two main benefits arise from such a topology:

1. Field of View and Power Harvesting: In the case of single pixel imagers, increasing the antenna aperture allows for more efficient energy coupling. When using a Silicon hyper-hemispherical lens, each antenna would be looking towards a different angle according to its position with respect to the centre pixel. Therefore, the single pixel imager will be less sensitive to setup misalignments.
2. Noise Levels: connecting multiple cold transistors in parallel leads to a reduced effective channel resistance. As the noise at higher chopping frequencies is dominated the thermal noise, this topology effectively reduces the thermal noise level especially at the sub-threshold and weak-inversion regions.

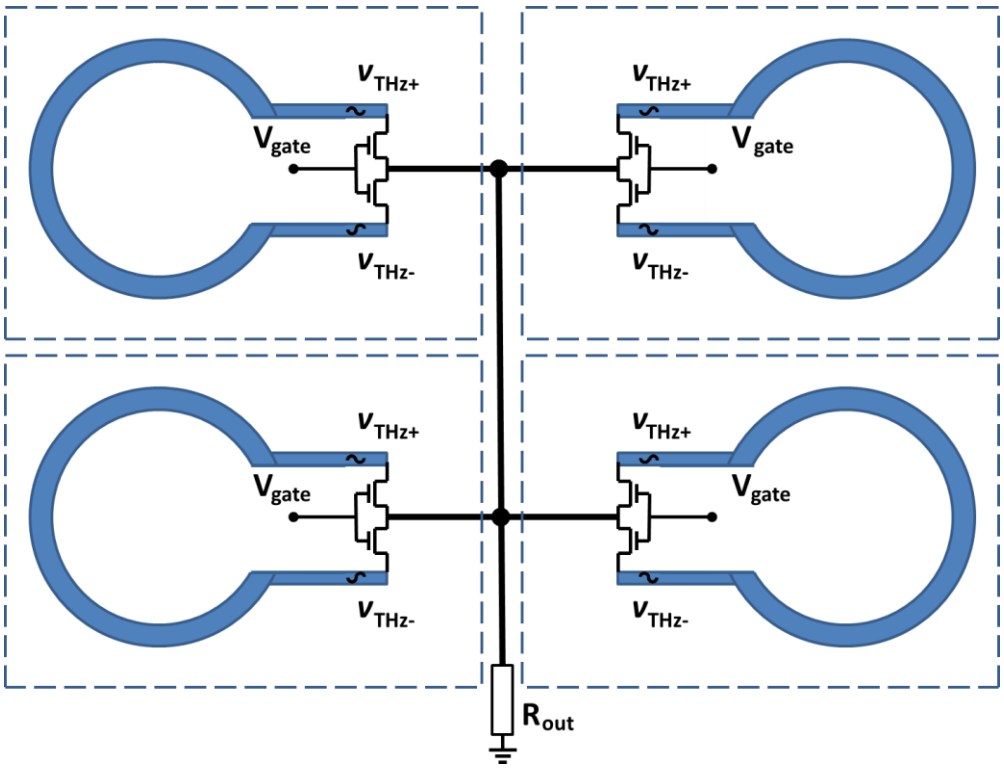


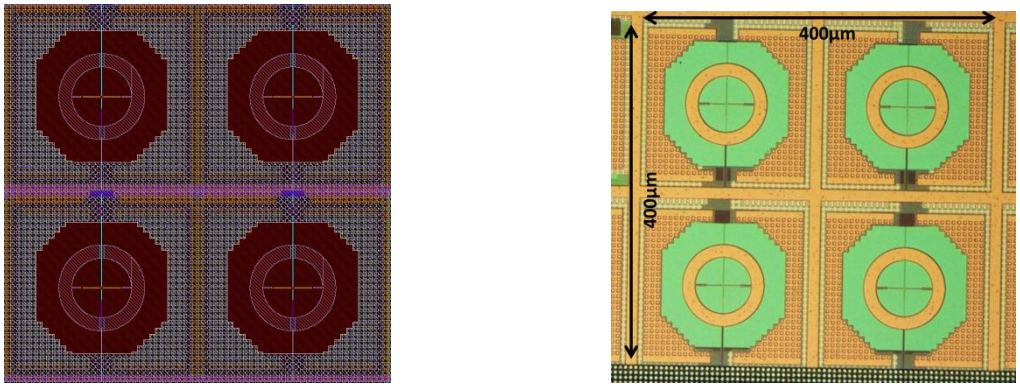
Figure 3-57: Circuit schematic of 4 pixels combined at their outputs

The performance is studied in the two different modes of operation, the *current-mode* and the *voltage-mode.* In the case of the voltage mode of operation, the voltages appearing from each detector do not add in parallel, and the highest voltage potential will dominate. Therefore, even as the power is effectively Nx $P_{in,detector}$, where $P_{in,detector}$ is the power received by a single element, the output voltage remains $V_{out,detector}$. Thus, the Responsivity decreases subsequently by N times. On the other hand, when operated in current-mode, the currents add in parallel and thus the Responsivity would remain unchanged. The NEP, on the other hand, is dependent on the number of elements. Taking for instance

four pixels in parallel with a channel resistance of R_{ch} leads to an effective resistance of $R_{eff}= R_{ch}/4$. The expression for the channel-resistance dependant thermal noise is 4kTBR.

3.6.1. Circuit Design and Implementation

A 4 element output combined circuit has been designed in CMOS 65nm bulk technology from STMicroelectronics. The circuit micrograph with the corresponding *Virtuoso* layout view is shown in Figure 3-58. The circuit comprises of 4 cold (unbiased) NFETs of 1µm/0,06µm gate width and length, respectively. A single element has a pitch of 100µm, and thus a total collecting physical aperture of 400µmx400µm is attained. The circuit has not been fully characterised at the time of writing this report.



(a) **(b)**

Figure 3-58: (a) Layout view and (b) implemented micrograph of 4 pixels combined at their outputs

3.7. Chapter Conclusions

In this chapter a detailed analysis of the design of Terahertz direct detectors was presented. This investigation is developed with respect to various electrical and electromagnetic parameters. Circuit analysis and EM analysis were examined in various CMOS technologies.

From the derived analysis and the implemented circuitry, we can conclude the following for voltage-mode FET THz power detectors:

- Technologies with substrate isolation provide higher mixing efficiency and better noise levels. Higher resistivity substrates enhance the antenna efficiency and using high resistivity Silicon lenses at the back-side of the chips is favoured for reducing substrate modes and for focal-plane array operation.
- Detectors with high input impedance will created the larger voltage drops at their input ports. Smallest FET sizes will create the highest input impedances.
- Complex conjugate matching to the antennas is necessary to properly deliver the received power.
- Despite the fact that smallest detectors will create the largest signals at their input ports, detector sizing is done in view of the power levels anticipated as well as the available chopping frequency and loading conditions.
- Large input powers, when efficiently delivered to well-matched transistors, increase the detector's internal flicker noise. Flicker noise could become substantial at certain detector sizes and power levels.
- Flicker noise is reduced by chopping at higher frequencies, or by resizing the transistors.
- Higher input powers also saturate smaller devices in a faster fashion.
- Output impedance varies the output signal, with high impedances favoured for a larger signal when the detectors are operated within their sub-threshold regions.
- Correlating the measured detectors to the simulated antennas and detectors using PSP model have revealed a good level of agreement. This reveals that the non-quasi static theory may suffice in explaining the behaviour as well as in designing the circuits.

Accordingly, a variety of test structures were designed and measured in CMOS 65nm bulk and 28nm FDSOI. Record NEPs as low as 14pW/√Hz were attained and record responsivities for non-amplified detectors of beyond 2kV/W. The low NEP values were reached due to the high responsivity levels, whilst maintaining low noise levels.

The THz detectors designed in a 28nm FDSOI technology were not optimised following the optimisation methodology described in this chapter, as there were no RF models available at the time of design. Instead, antennas were ported from 65nm Bulk CMOS that were presented in this chapter, and modified to fit the design rules of the 28nm FDSOI technology. However, the measured noise level at 1-kHz for a 1μm/60nm device show that the FDSOI detectors enjoy a lower noise level by a factor of 2 at certain biasing conditions. Furthermore, the FDSOI technology offers very small detectors of very high input impedances. It is thus expected that properly designing antennas in FDSOI will potentially lead to a much more enhanced NEP and responsivity values.

Therefore, these results do not imply that FDSOI is inferior to Bulk CMOS.

Below is a performance summary of the measured detectors.

Table 3: Performance summary of measured detectors in 65nm Bulk CMOS and in 28nm FDSOI. All detectors are differentially fed source-coupled NFETs. Detectors designed in bulk CMOS were optimised in terms of impedance. (*) FDSOI designs are not optimised, and thus the performance shown here is suboptimal. The FDSOI circuits are measured with a 0V body bias. Changing the body bias only modifies the V_T and thus the gate-bias dependent curves only shift according to the threshold voltage shift.

	Designed			Measured		
	CMOS Technology & Detector Size	**Pixel**	**Antenna Frequency**	**Optimum Frequency**	**Maximum Responsivity [V/W]**	**Minimum NEP [W/√Hz]**
Optimised Impedance Matching						
	65nm Bulk W/L=1µm/0.06µm	A3	650-750GHz	724GHz	**1460** @ V_{GS} =0.19V @200Hz	**19p** @ V_{GS} =0.45V @200Hz
				724GHz	**1200** @ V_{GS} =0.27V @1kHz	**19p** @ V_{GS} =0.47V @1kHz
				724GHz	**1180** @ V_{GS} =0.29V @5kHz	**14p** @ V_{GS} =0.5V @5kHz
	65nm Bulk W/L=1µm/0.2µm	B4	800GHz-1THz	822GHz	**960** @ V_{GS} =0.15V @1kHz	**27p** @ V_{GS} =0.45V @1kHz
	65nm Bulk W/L=0.3µm/0.06µm	C3	650-750GHz	724GHz	**1860** @ V_{GS} =0.27V @1kHz	**15p** @ V_{GS} =0.5V @1kHz
Non-optimised Impedance Matching	**28nm FDSOI (*)** W/L=1µm/0.06µm	C1	850GHz	856GHz	**460** @ V_{GS} =0.23V @1kHz	**35p** @ V_{GS} =0.44V @1kHz
	28nm FDSOI (*) W/L=1µm/0.03µm	C2	850GHz	856GHz	**430** @ V_{GS} =0.14V @1kHz	**39p** @ V_{GS} =0.4V @1kHz
	28nm FDSOI (*) W/L=0.08µm/0.06µm	D2	Broadband: 600-1000GHz	856GHz	**590** @ V_{GS} =0.23V @1kHz	**66p** @ V_{GS} =0.55V @1kHz

Chapter IV- Design of a 1kpixel Terahertz Video Camera in 65nm Bulk CMOS

The main driving interest for the heightened research in THz detection in CMOS is the large-scale benefits that these technologies provide. The niche Terahertz industry must be presented with alternatives that all other technologies suffer from: high levels of integration. For instance, 65nm CMOS is a mature industrial technology with well modelled analogue and digital building blocks. Ultimately, almost all low cost high-end consumer electronics are Silicon based. Thus, to foremost utilize CMOS capabilities for Terahertz imaging would logically mean to integrate as many pixels as possible and carry out as much signal processing on a single chip. Of course this has to come in view of maintaining competitive power consumption levels and sensitivities. There is no doubt in the capabilities of integration in CMOS, and the downscaling of the technology means that orders of magnitude could be saved on area. But will that at all cope with tough requirements of the Terahertz imaging-chain?

4.1. Multi-Pixel Challenges and Design Methodology

The main design challenges to face are related to a myriad of limitations. Primarily, the limited source power is what sets the major constraints, contrary to the single pixel topology where most of the source power is utilized for the detector at the other end of the imaging chain. In the multi-pixel case, the source power has to be divided at best by the number of pixels available. For example, for a typical source power of 10μW for a source at 1THz illuminating a camera of 1024 pixels each pixel receives a maximum of 10nW. Of course this is the upper end of signal reception, should the entire source power is squeezed onto the FPA and coupling efficiency be 100%, which is never the case.

Proper antenna design is therefore crucial. Compact pixel pitch for dense focal plane array (FPA) arrangements with low mutual coupling is important, and the FPA should be simulated with as many pixels available as possible. Beam aberrations for the lens off-axis pixel locations and antenna impedance variations in the presence of reflections from the Si-air lens interface should be considered.

On the other hand, for on-chip amplifiers and signal processing to be able to operate and extract the signals from the corresponding noise-floor of the detector circuitry, the output voltage per detector should be large enough and the noise floor should be low. A margin for imaging defined by the imaging dynamic range should also be wide enough to produce high quality images. This essentially is guided by a proper $\Re v$ and NEP design, in view of the available resources such as source power.

Additionally, all the design constraints analysed in Chapters 2 and 3 are commonly valid in the case of multi-pixel design, with more crucial requirements since the tolerance is much stringent compared to single pixel systems.

It is a true quasi-optical and electronic challenge to be addressed adequately. In this regards, a set of design approaches to tackle the above defined challenges is concluded. The lower sensitivity of direct

detectors comes for the benefit of wider operational bandwidth. Broadband match between antenna and high input impedance detector for maximum responsivity and minimum NEP according to the methodology demonstrated in Chapter 3 should be employed to achieve the system requirements. As discussed also before, radiation coupling-efficiency is enhanced on high resistivity substrates such as CMOS 65nm SOI technologies. However, for more commercial process technologies such as 65nm bulk CMOS the radiation efficiency is enhanced by thinning the substrate and gluing the Silicon die at the back of a high resistivity Silicon lens. Antenna design should provide rotationally symmetric Gaussian-like radiation patterns for all pixels; ring antennas demonstrated in chapter 3 are therefore highly favourable.

On the electronic-end, in pixel integration capacitors should be utilized for SNR improvement, as the detectors should operate with zero-IF outputs. In return, in-pixel amplification to lift the output signal voltage levels is also essential, and offset compensation circuitry should be designed to account for pixel amplification offsets. Then, each pixel differential output signal should be selected and amplified in series, to be digitized by an Analogue to digital converter, off or on chip. For Row/column addressing, decoder circuits need to work with a global shutter circuit to define the integration/reset timing for each imaging frame.

According to the aforementioned challenges and requirements, a 1kpixel camera for terahertz imaging with the necessary on-chip electronics was designed. The chip is equipped with a Silicon hyper-hemispherical lens of high resistivity and will be described in detail in the subsequent sections.

4.2. Design and Implementation of a Multi-Pixel THz Camera

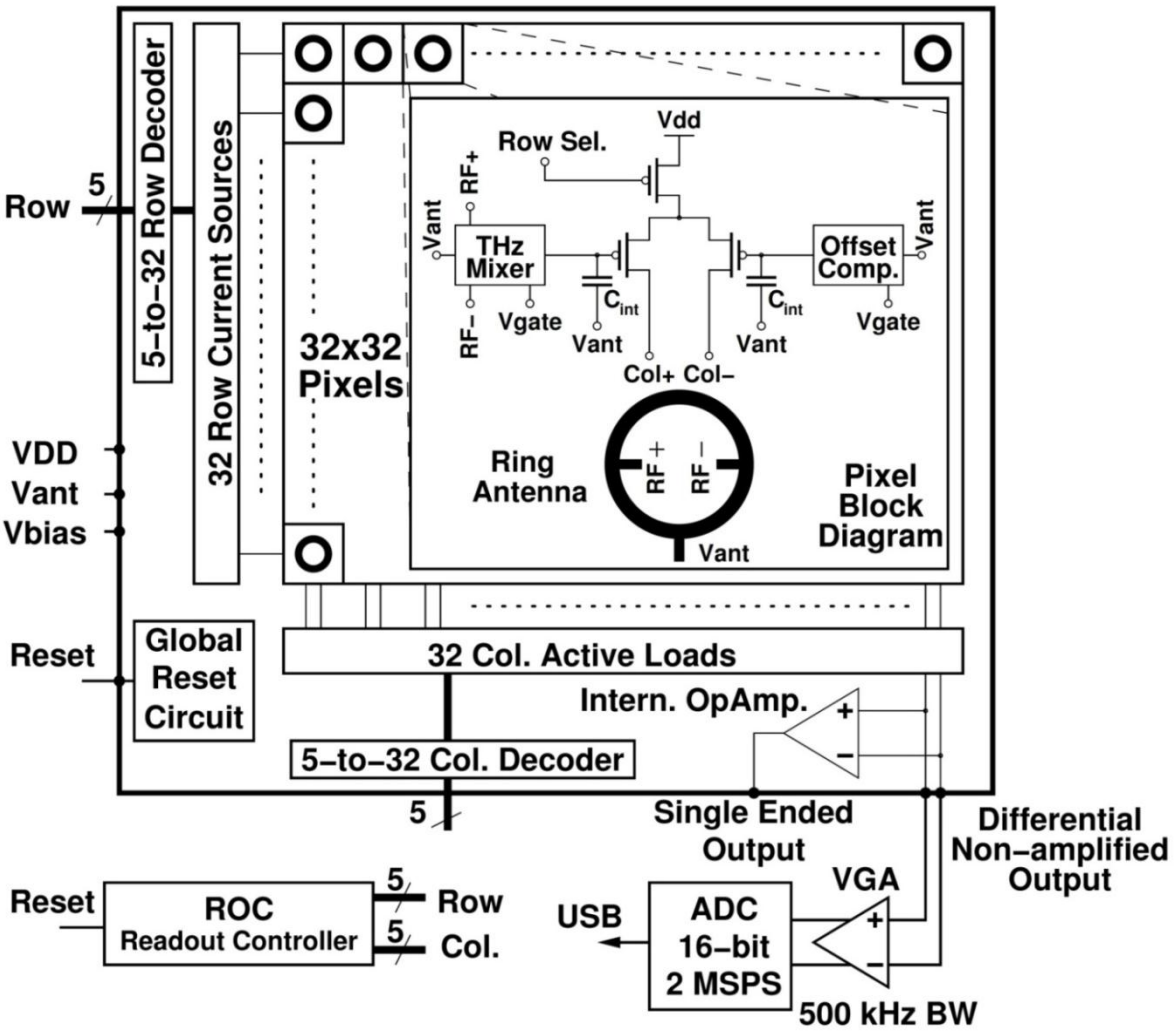


Figure 4-1: 1kpixel THz camera block diagram [80], [111]

A block diagram of the implemented camera operating at zero-IF (DC) is shown in Figure 4-1. As the diagram demonstrates, the imager follows a global shutter readout scheme. All pixels are controlled globally within each imaging-frame to integrate the signals and then reset. The core of each pixel comprises a wire ring antenna feeding a cold (non-biased) differential NMOS distributed resistive mixer; as outlined in detail in Section 2. The mixing transistors produce output voltages as per their input THz power and the charges are accumulated across an integration capacitor C_{int} connected between the output node of the mixer and the antenna DC node.

For offset compensation purposes, each detector in the array is equipped with a complementary in-pixel blind reference circuit. The offset compensation is an exact copy of the THz detector, yet not connected to the THz antenna ports. Instead, its sources are only connected to the DC level of the antenna, which also sets the DC level of the sources of the detector. This is analogous to the visible imagers that are normally equipped with a blind pixel for off-set compensation.

The difference between both the detector and the blind-reference outputs is processed by a consecutive amplifying stage consisting of a differential transistor pair with an active load. This in-pixel amplification carried out via the in-pixel differential amplifiers exhibit a 50dB open-loop gain. The differential amplifier is comprised of high performance low power RF PMOS transistors of dimensions of 100µm/1µm with 10 fingers each. Whereas the row select switch is also a PMOS transistor of 10µm/1µm W/L and 10 fingers each. Pixels of the same column share the same active loads.

Contrary to conventional visible light CMOS image sensors that normally utilize a photo-diode detector and require a separate reset transistor, the detector transistors themselves can be used to reset the accumulated charges at the integration capacitor; thus reducing the number of required circuit elements. All pixels are reset at the end of each frame.

The basic detector circuitry in the array operates fully in parallel (zero-biased detectors) but in order to achieve an overall low power operation, only the readout of a single row is biased up at-a-time by a 5bit row encoder and the differential pairs of the mentioned amplifying stages pairs in each column share a common active load. Next, a digitally controlled multiplexer selects a single pixel out of the row that is further buffered by a unity-gain amplifier and transferred to the input of an external 16-bit ADC. The fixed pattern noise is thus far treated externally by capturing a single dark frame before the camera operation.

The following section describes in detail the camera circuit design in a 65-nm CMOS process technology from STMicroelectronics in detail. This includes the RF CMOS circuit design of the detector front-end as well as the readout circuitry, which both are in line with all the industrial CMOS design rules. My main contribution was in the design of the pixels of the camera. Later on, I have worked on packaging, setting up and measuring the camera performance.

4.2.1. Pixel Design and Readout Integrated Circuit

The design of the pixels follows the reasoning set in the previous chapters. We have decided to opt for the source-driven differential NFETs due to the broadband behaviour that was explained in the previous chapter. At the detector front-end, the differential NFETs have been designed alongside with the antenna design to provide a complex conjugate match at the frequencies of operation. We targeted a BW extending roughly from 700GHz to 1THz with a centre frequency of 850GHz. A single transistor is a 1µm wide low-power and low-threshold RF NMOS transistors with a minimum gate length of 60nm. The transistor-pair share a common well, with a common source in the middle, as explained in the previous chapter. The well was isolated from the substrate to reduce the injected noise from the analogue and digital core that are continuously running. As noted before, silicon on insulator technologies are believed to offer further enhancement of this design as the transistors will be immune to any noise fluctuations.

As the camera is intended to operate with no lock-in techniques, the mixers should present a zero-IF output. Therefore, capacitors are placed at the outputs of each detector to hold the output signals, and integrate them for SNR enhancement. HB simulations have shown that capacitors of the size of around 100pF are needed to integrate within a frame rate of 25fps, over a time of 40ms. However, this is physically impossible to fit within our pixel pitch. Therefore, only 8pF was possible to integrate. We have used four poly-capacitors, placed in parallel to maximise the capacitor value, arriving at the 8pF total capacitance. It is important to note here that it is well known that poly-capacitors may be

disadvantageous due to their 1/f noise arising from the poly-silicon. This type of capacitors was used because it offered a larger capacitance value and was easier to integrate at the time. In the future, further enhancement would be to use multiple metal-oxide-metal capacitors, as well as CMIM capacitors in parallel and atop of each other, as they are designed on different metal layers.

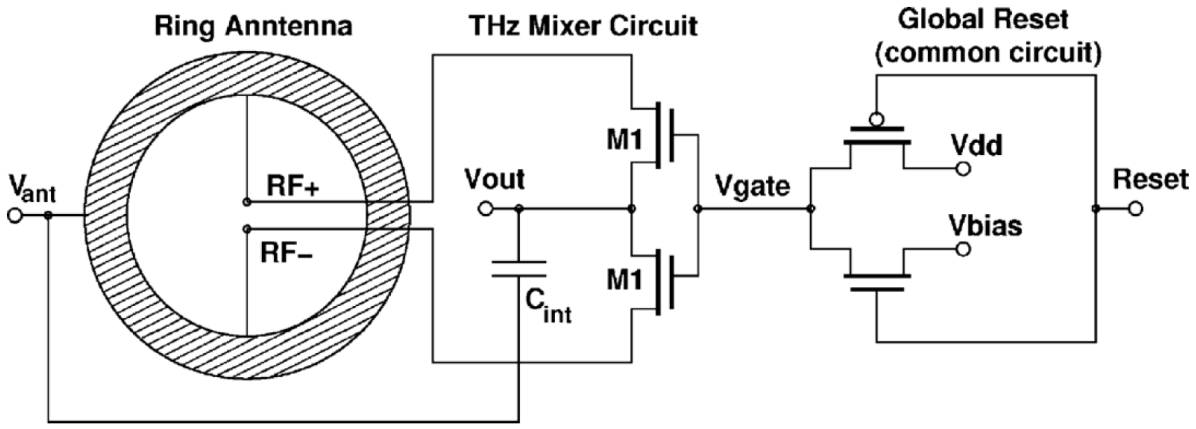


Figure 4-2: Global reset circuitry [111]

In terms of the in-pixel integration, amplification and readout circuit design, the key challenge is to achieve low power consumption levels whilst processing the detected signals with the minimum added noise. Passive pixel sensors, therefore, would be preferred, but the signal from the detector circuit is too small. As explained in the previous chapter, in voltage mode readout the detectors need to be terminated by a high output impedance. Therefore we require a trans-conductance stage. We have investigated several options regarding the ROIC. The original idea was to design sample and hold network followed by an amplifying stage. This idea was ruled out due to three main factors:

- The injected noise from the switches will degrade the overall system noise level especially before the signals are amplified
- The increase in power consumption due to the use of more switching circuits. For more noise immune sample and hold networks the power consumption is even much higher
- The area penalty due to the integration of more circuitry per pixel.

An active pixel circuit, therefore, provides better noise immunity and in-pixel amplification. In order to lower the average power consumption per pixel, only the in-pixel amplifiers of a single row are activated at a time, as will be seen in the following chapter on the complete readout chain.

Therefore, as described above, the readout circuit scheme here uses the NMOS detector transistor itself to reset the accumulated charges of the integration capacitor reducing the number of required in-pixel circuit elements. This is beneficial in reducing also the number of unwanted noisy elements connected to the detection node. The detector is seen as a current source in parallel with both the channel conductance and the integration capacitor. The channel conductance is controlled by the NFET gate bias. Therefore, the transistor channel itself could operate as a mixer or as a short circuit.

This concept is explained in Figure 4-3. At any gate bias ranging from zero up to around 0.7-0.8V the detector is in the mixing mode. In other words, the detector is efficient in detecting the THz signals

and produces an output voltage as per the theoretical explanation in chapter 2. Physically, this is due to the non-linearity of the channel created within the transistor. When the gate is biased at 1.2V the channel in the transistor is completely open and is conducting, and the responsivity is almost zero. This could be seen in the plots in chapter 3 for single pixel detectors. This phenomenon could be exploited in our benefit for the integration and then discharge of the signals. Therefore, we designed a reset/integrate global shutter, shown in Figure 4-3, that provides a bias to all pixels setting them in the specified operation mode. This global shutter comprises of an NMOS and a PMOS transistors. During the integrate mode, the PMOS transistor supplies the detector bias of interest, for example 0.3V, when presented with a low voltage at its gate. During the reset mode, the NMOS transistor supplies a 1.2V when a high voltage is supplied to its gate.

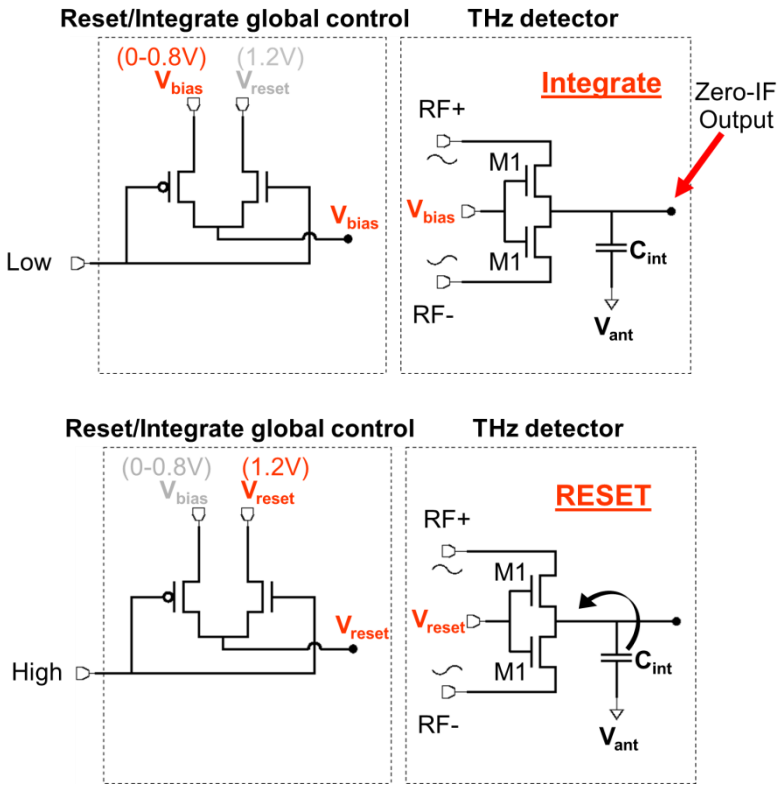


Figure 4-3: Integrate and reset scheme

Figure 4-4 shows the circuit schematic of the active part of a pixel circuit. The row select signal is being shared amongst a row of pixels, whereas the Col signal is shared among a pixel column. The detector transistor M1 is followed by a readout transistor pair M3/M4 acting as a differential pair with an attached offset compensation circuitry (blind reference pixel).

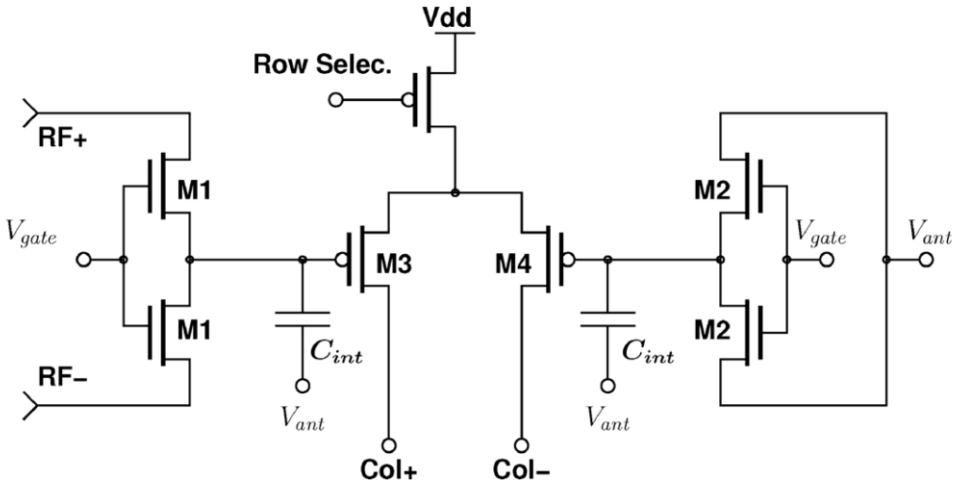


Figure 4-4: single pixel schematic

The blind reference pixel circuit is not connected to an antenna, and therefore, is used to produce a reference potential at one of the branches of the differential pair stage operated in open-loop. The gate bias of the transistor pair M3/M4 is provided by V_{ant}. This voltage is applied either through the active pixel or through the blind reference pixel. In the case of M3, this bias voltage is further applied through the common node of the antenna.

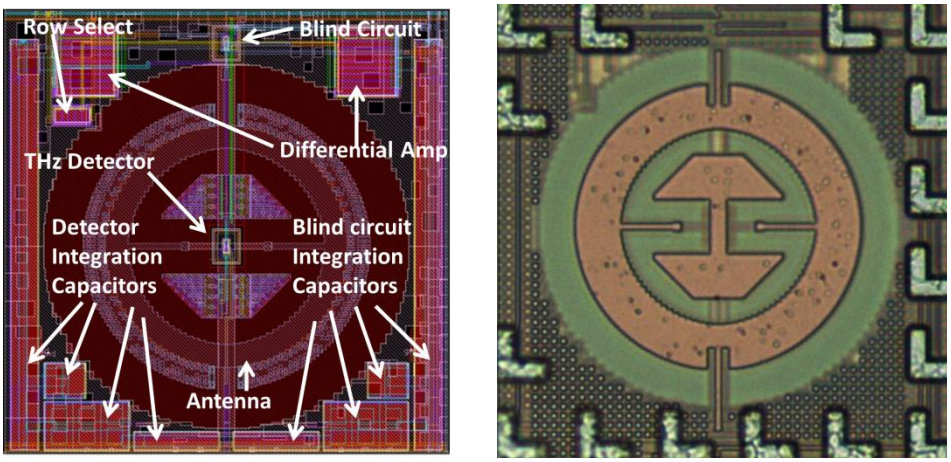


Figure 4-5: Single pixel layout and optical micrograph

The layout view and the physical design of a single pixel with its corresponding on-chip antenna are shown in Figure 4-5. The ring antenna is realized in the 7-layer copper back-end-of-the-line (BEOL) and designed to provide broadband operation while feeding a high-resistivity silicon hyper-hemispherical lens through the backside of a 150µm thick 15Ω.cm bulk silicon substrate. The 32x32 FPA exhibits a 80µm pitch. All highly doped active cells considerably interfering with radiating fields are selectively blocked to reduce incurred conductive losses. These blocking amounts to 55% of the pixel area (fill factor).

The differential amplifier, the current source, the offset-compensation circuit as well as the integration capacitors are all placed underneath the ground plane, as shown in Figure 4-5. This is important to

isolate the active circuitry from the THz radiation, and to maintain the blindness of the offset-compensation circuit. The outputs are connected to output busses as shown in the layout view, and run on metal 5 of the stack to reduce the lines resistivity, and were routed underneath the global ground plane. The NFET detectors are placed in the middle of the antenna, and are fed differentially through the antenna feeds, as shown in the figure. The PDK models of the transistors are valid up to metal one of the transistors; therefore, the EM simulations of the antennas include the feed-lines down to metal one. The feed line structures play an important role in matching the impedances of the detectors.

The symmetry provided by the pixel layout improves a rotational symmetry of radiation patterns. All required low-frequency routing into the pixel centre is realized along the antennas zero-field intensity (H-plane). The simulated antenna radiation efficiency is 70-77% from 0.8-1THz on a semi-infinite Si substrate. The antenna configuration has a low cross-coupling of -25dB among all pixels in the array, even in the absence of anti-reflection coating [128].

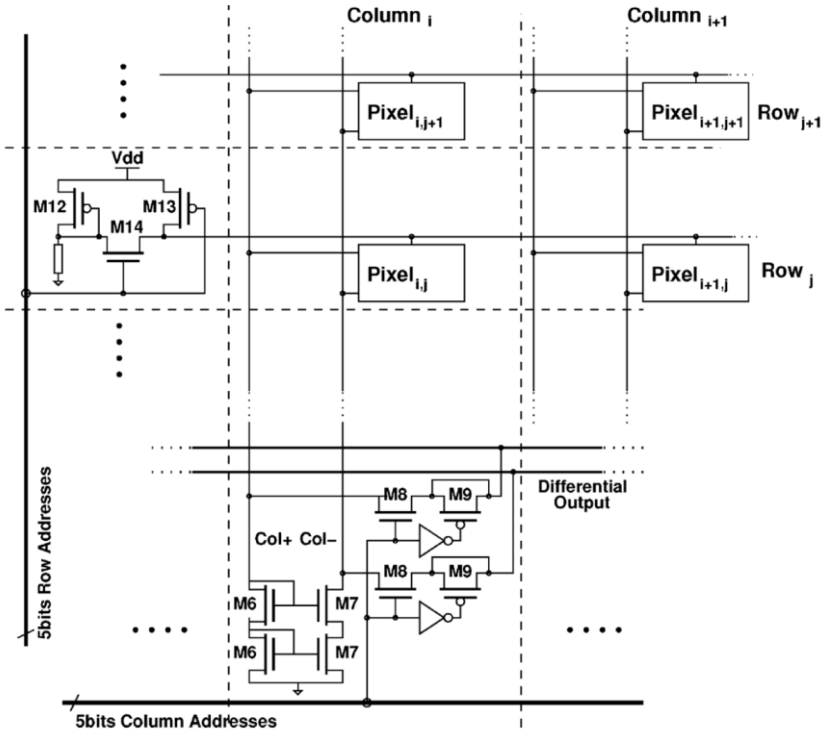


Figure 4-6: Digital control of the 1kpixel camera [111]

Figure 4-6 shows the block diagram of the digital selection unit. The row and column selection is realized by using 5-bit addresses for row and column selection. Two auxiliary enable signals switch decoders off during the charging period of the integration capacitors. A single row is biased up at-a-time and the differential pairs in each column share a common active load (M6-M7) providing a simulated open-loop gain of 50dB per pixel. A digitally controlled multiplexer selects a single pixel to be further buffered by a unity-gain amplifier. This readout scheme was controlled externally by an FPGA and enables parallel operation of 1024 pixels, while the readout circuitry activates only a single row (32elements).

4.2.2. Circuit Implementation in Bulk CMOS 65nm

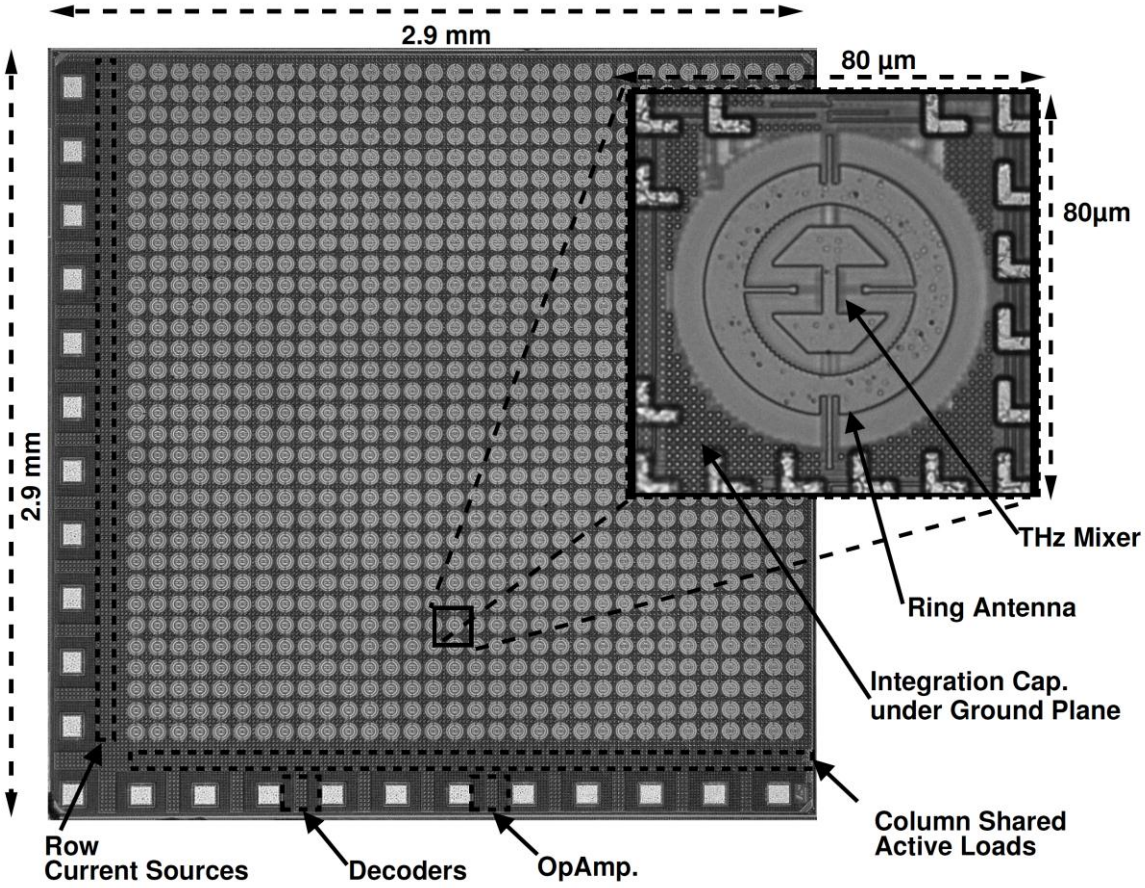


Figure 4-7: Chip micrograph of the 1kpixel camera implemented in 65nm Bulk CMOS [80], [111]

The chip was fabricated in a 65nm bulk CMOS technology from STMicroelectronics. The array micrograph is presented in Figure 4-7. The die size is 2.9x2.9 mm^2 including wire-bond pads. The chip layout includes the full metal stack (thick multi-layer metal structures) with dummy fillers to be compliant with an industrially qualified CMOS process technology.

The 32x32 on-chip antennas on the FPA chip, exhibiting an 80µm pixel pitch, feed a commercially available hyper-hemispherical silicon lens (15mm in diameter) through the backside of the silicon die as shown in Figure 4-8. The chip is aligned with the lens centre and both are fixed together using a low-shrinkage UV epoxy. No AR coating was applied at the lens aperture. The lens extension length (L) is 2.75mm, which in combination with the die thickness of 150µm, results in an overall L/R ratio of 0.366; being slightly below the elliptical position. The overall assembly shows an experimentally verified filed-of-view of about ±23 degrees, and residual reflection loss of around 2 dB at the lens aperture/air interface [111].

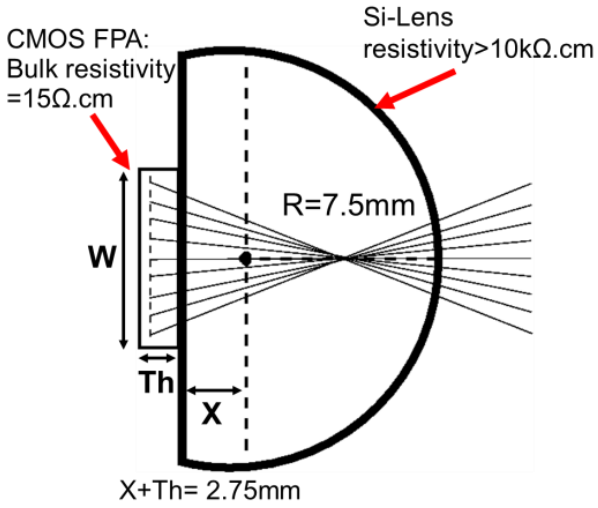


Figure 4-8: Chip-Lens assembly and demonstration of THz rays projected onto the CMOS FPA.

4.2.3. Packaging and System Implementation

To demonstrate low-power and low-cost packaging solutions for handheld applications, the lens-supported FPA chip was wire-bonded onto a low-cost FR4 PCB providing a substantial cost benefit over standard waveguide based THz technologies. The camera is configured for plug & play operation through a regular USB port.

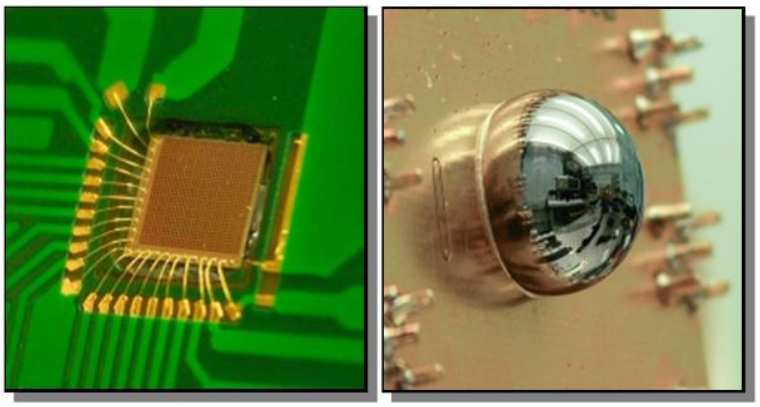


Figure 4-9: Lens and chip assembly and wire-bonding [80]

The terahertz camera, shown in Figure 4-9 and Figure 4-10 is packaged in a 5x5x5cm^3 metal box to demonstrate low-power and low-cost packaging solutions for handheld applications. It is connected to the data acquisition board via a single 8wires RJ45 cable. It consists of a silicon lens attached to the chip back-side, a readout controller (ROC) implemented in a complex programmable logic control device (CPLD) driven by a clock generator (CLK), a low noise variable gain amplifier (VGA) and a regulated power supply.

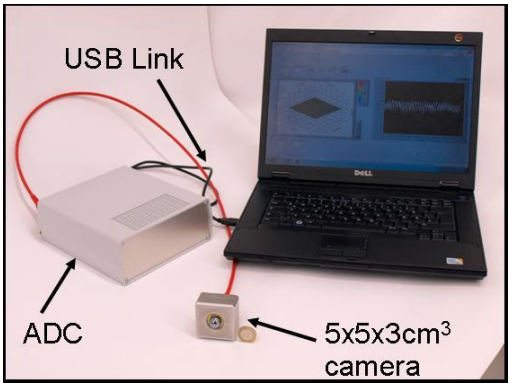


Figure 4-10: THz camera in plug and play operation

The analogue output of the compact THz camera was sampled with up to 2MSPS by an external 16-bit ADC and was sent to a computer via a USB link to be displayed on a screen. The developed software by Richard Al Hadi [111] displays a three dimensional graphic in real time of the streamed data as shown in the demonstration setup Figure 4-10. It enables basic image processing of the video stream starting with a dark calibration frame for fixed pattern noise reduction.

4.2.4. Timing Schemes

As mentioned earlier, the integration time is reduced due to the reduction in the capacitor size. This results in a faster capacitor charge up, leaving plenty of time for readout. This could be exploited in our benefit, though, to operate the camera at a higher speed. Concepts of correlated double sampling, for instance, could be employed by running the camera at double speed.

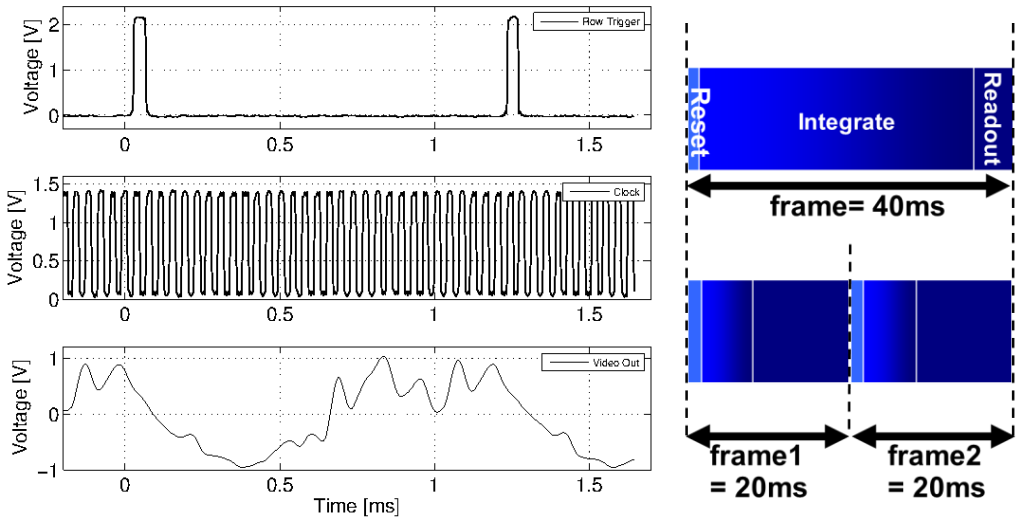


Figure 4-11: recorded video output as well as the control signals

Figure 4-11 shows a measured snapshot of the output signals across various pixels within one row. The figure also shows the row triggers that switch the readout to the next row. The trigger is synchronised to the clock, and repeats itself every 32 clocks, equivalent to 32 pixels. This mechanism repeats itself 32times (32 rows and 32 columns), after which a reset signal arrives. This timing structure was implemented and coded in VHDL on an FPGA that accordingly supplies all the

necessary biases and switching commands to the silicon chip. The video output also includes fixed patter noise, which is removed afterwards in software by subtracting a dark-image from all the upcoming active frames.

4.2.5. Camera and Detector Characterisation

A more conservative theoretical upper limit (40.2-44.2dBi) in the following A_{eff} calculation is used, assuming the lens physical aperture to be the collecting area. The directivity was also measured and calculated according to [112]. The measured directivity was 41.75dBi at 856GHz, and was repeated across 650-1028GHz. The measured directivity was found to be 39.5-43.5dBi, which is 0.75dB lower than the theoretical calculations.

The path-loss at a 1-meter distance is between -88.5 and -93dB for a frequency range from 650-1028GHz. The received power is calculated as explained in chapter 2. The source power was calibrated using an Ericsson power metre, and was found to range between 1.7-11.2µW . The directivity of the source antenna was presented in chapter 3. The received input power per pixel varies between -50 to -42dBm according to the Friis transmission formula.

The ℜv and NEP were measured at various detector bias points and chopping frequencies across the entire 650-1028GHz frequency band and are shown in Figure 4-12. This was carried out by selecting a single pixel by software externally, and chopping the source. These figures include a 5-dB VGA gain implemented off-chip. In fact, without the VGA gain, the responsivities and NEPs would still include the in-pixel amplification. At a 5-kHz chopping frequency, the minimum NEP is 100pW/√Hz at a Vbias =1.25V and the maximum ℜv is 140kV/W. The ℜv includes the 5-dB gain of the camera module and the in-pixel amplification. The NEP includes thermal detector noise, flicker noise, additional noise from the in-pixel differential stage, the active load and current sources, however, they are not representative of the camera in operation.

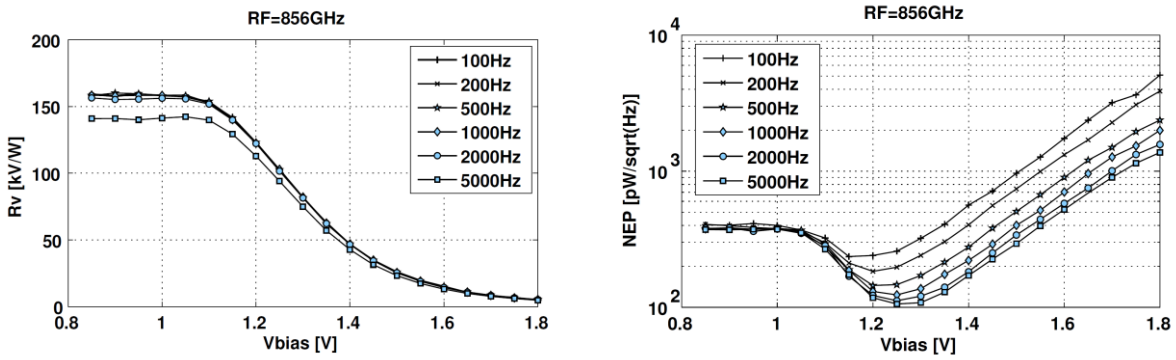


Figure 4-12: Single pixel responsivity and NEP at 856GHz with respect to chopping frequency [111]

From 0.65THz up to 1.1THz the maximum ℜv and the minimum NEP are presented in Figure 4-13 and Figure 4-14 and for different chopping frequencies, respectively. These two figures show a 3-dB bandwidth of at least 170GHz from 790-960GHz. The pixels are expected to still operate beyond 1THz. However, the measured frequency band is limited by the available measurement equipment.

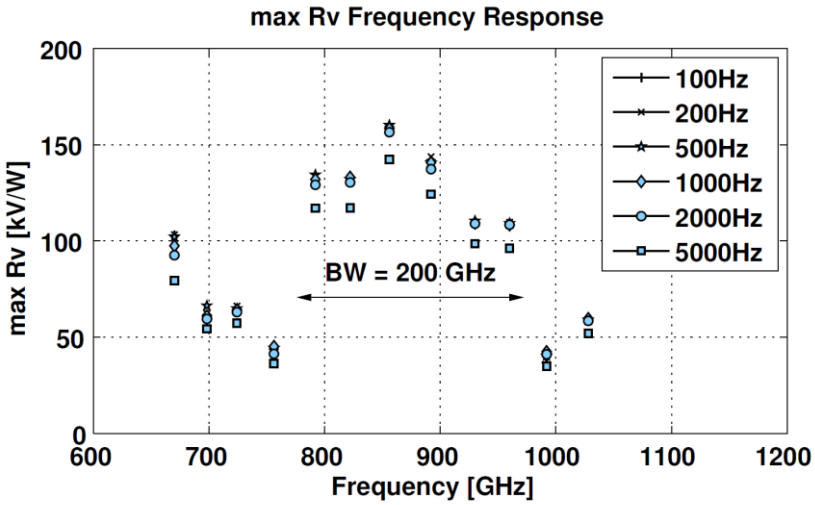


Figure 4-13: Maximum ℜv of a single pixel across the spectrum with respect to chopping frequencies [111]

The noise performance of this imager could be further improved by correlated double sampling (CDS), which substantially reduces correlated low-frequency noise of the imager. The imager would support such measurements; however, this is currently not implemented in the readout controller software. Further camera measurements in video-mode which is a relevant figure for the real operation of the camera, as well as antenna measurements were provided in [111].

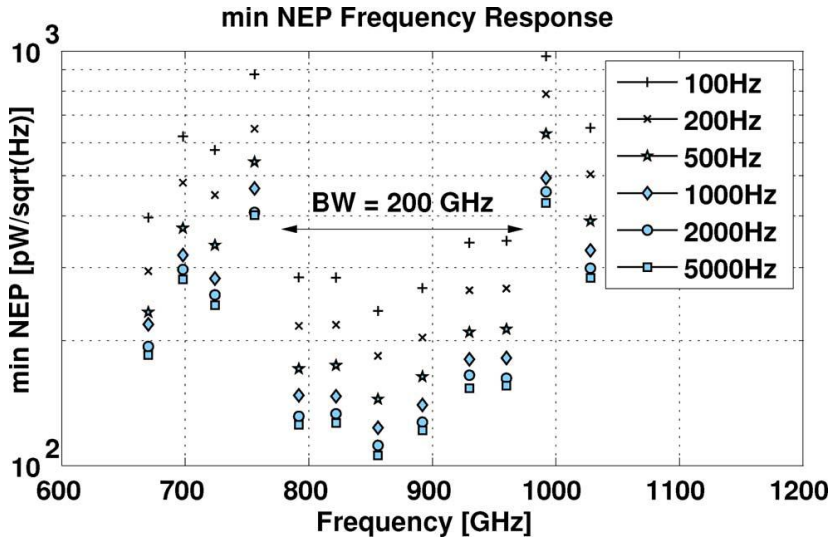


Figure 4-14: Minimum NEP of a single pixel across the spectrum with respect to chopping frequencies [111]

4.2.6. Noise Analysis

To examine the nature of the noise contributors in this design and for the sake of comparison with the previously-presented standalone-detectors, small-signal noise analysis has been performed with and

without the read-out integrated-circuitry (ROIC). The simulations have been carried out at various chopping frequencies, differential-amplifier biases, as well as varying source input-power levels.

Chopping at higher frequencies moves the signal away from the 1/f noise of the ROIC. Furthermore, the results at a 1kHz modulation-frequency including the ROIC reveal that the major noise contributors are the readout switches which account to almost 98% of the generated noise when the responsivity is not at its highest, and are of thermal nature in the order of $20fV^2/\sqrt{Hz}$ seen at each branch of the differential output. The remaining added noise is dominated by the active-loads and the current source (in the order of 0.1 $fV^2/\sqrt{Hz}$, whereas the thermal-noise contributed by the THz detector is highly bias-dependant and accounts to merely 0.01% of the total noise within the regions of low responsivity, but then rises to around 60% of the noise contribution when biased for high responsivity. This is consistent with the measured results of the standalone-detector. Additionally, the blind-reference circuit merely contributes to thermal noise as there is no signal present, yet the thermal-noise level is similar that of the THz-detector according to the various biasing conditions as explained above.

These results explain why the measured NEP of the camera-chip including the on-chip readout circuitry is higher than those of the previously published results of standalone-detectors.

4.3. Chapter Conclusions

This chapter has presented the design, implementation and characterisation of a 1kpixel THz video camera. This camera is a world's first and it demonstrates the feasibility of multi-pixel FPA design for Terahertz imaging in CMOS technologies.

The camera pixels include a THz ring antenna designed with a differential source-fed FET detector, using the methodology demonstrated in the previous chapter. The differential detectors are comprised of a single double-fingered NFET operated differentially. The detectors are isolated from the substrate to avoid noise leakage from the digital and analogue core. Integration capacitors, differential amplifiers, blind reference pixels and row-select switches acting as current sources were all integrated in a single pixel.

The full camera chip includes a digital core comprised of multiplexers that was designed by Dr. Yan Zhao. Active loads and readout switches with an on-chip op-amp were designed by Richard Al Hadi. The antennas were designed by Janusz Grzyb, with impedances and operation conditions provided by me. I have worked on the full design of the pixels of the camera.

This camera operates in video mode with frame rates exceeding 25fps up to 500fps. Responsivity and NEP were measured for single pixels with the readout circuitry switched off. Total camera responsivity and NEP were also measured for the camera in full operation over the full video bandwidth.

Further optimisations are believed to enhance the performance of the camera. Employing the design methodology shown in chapter 3 will bring about an important sensitivity improvement to the detector intrinsic performance. Therefore, the readout circuitry should manage to maintain the lowest noise levels possible to not deteriorate the excellent detector performances.

More integration is also possible, with the chance to implement the ADCs on chip, with possible $\sum \Delta$ modulators and noise cancellation techniques.

Chapter V- Terahertz Frequency Synthesis in CMOS Technologies

As described in the introduction of this thesis, there has been recent activity in the domain of frequency synthesis using Silicon technologies. Frequency multipliers or frequency oscillators are the core topologies employed. This chapter presents a 5push ring oscillator aimed at increasing the frequency of operation as much as possible. It is important to relate to the original triple push oscillators mentioned recently in the literature [99]. The main aim here is to design harmonic oscillators with as high fundamental frequencies as possible, in view of maintaining oscillation and producing sufficient power. Then with the benefit of the ring structure, efficiently combine the fifth harmonics in phase and provide them to an antenna or to a heterodyne mixer.

5.1. Five-Element Ring Oscillator Design at 600GHz and 900GHz in 65nm CMOS

5.1.1. Circuit Design and Implementation

The idea is based on the synthesis of a fundamental frequency below the technology limits and then efficiently extracting higher order harmonics. In this case, a 5-push ring oscillator was proposed. The schematic of the oscillator is depicted in Figure 5-1. Five low V_T low-power RF GO1 transistors are connected gate to drain respectively, and their sources share a common ground. The gates and drains are connected via inductors L_g. The transistors input impedance is capacitive and the transistor dimensioning and biasing conditions set the impedance level. Together with the inductor interconnects the ring-chain could be designed to oscillate at a fundamental frequency set by the parasitics of the transistors. However, to attain oscillation, the Barkhausen criterion should be satisfied, and that is by creating a phase-shift of 360degrees along the ring-chain. Consequently, each elements would exhibit a phase-shift contribution of 360/5=72degrees.

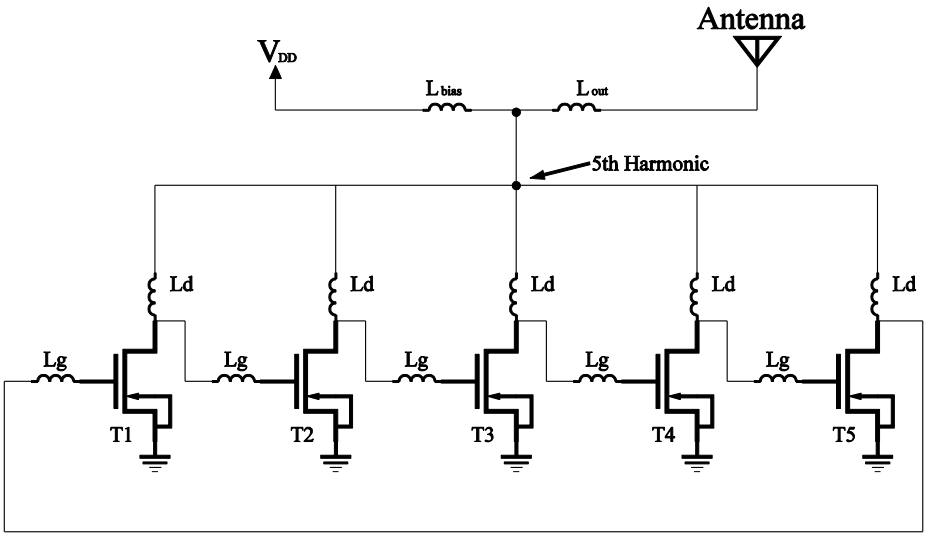


Figure 5-1: 5push circuit schematic with inductors

Analysing the various phase-shifts of the fundamental and its corresponding harmonics reveal that harmonics of the same order, including the fundamental, are out of phase, except the n*5th harmonics. For instance, the fundamental appearing at each branch node of the ring-chain would have a phase of $m * \varphi + n * 360°/5$, where n spans from 0 to 4 is the element number, m spans from 1 to 5 is the harmonic number, and φ is the initial phase of the fundamental oscillating frequency.

Similarly, the 2nd harmonic would have phases $2 * (\varphi + n * 72°)$ at each nth node, and so on for the 3rd, 4th, 6th harmonics, etc... The 5th harmonic, though, will appear at each node with phases of $5 * (\varphi + n * 360/5°)$, which means the 5th harmonics of the fundamental oscillating frequency appear to be in phase at the output nodes, whilst all other harmonics are out of phase. As a result, one could efficiently combine the outputs of the 5th harmonics, whilst the lower harmonics would be filtered intrinsically due to phase destruction.

In this case, power combining could be realized by extracting these frequencies using high frequency filters tuned to the 5th frequency component, denoted as L_d in Figure 5-1, which also serves as a output matching network for the ring oscillator.

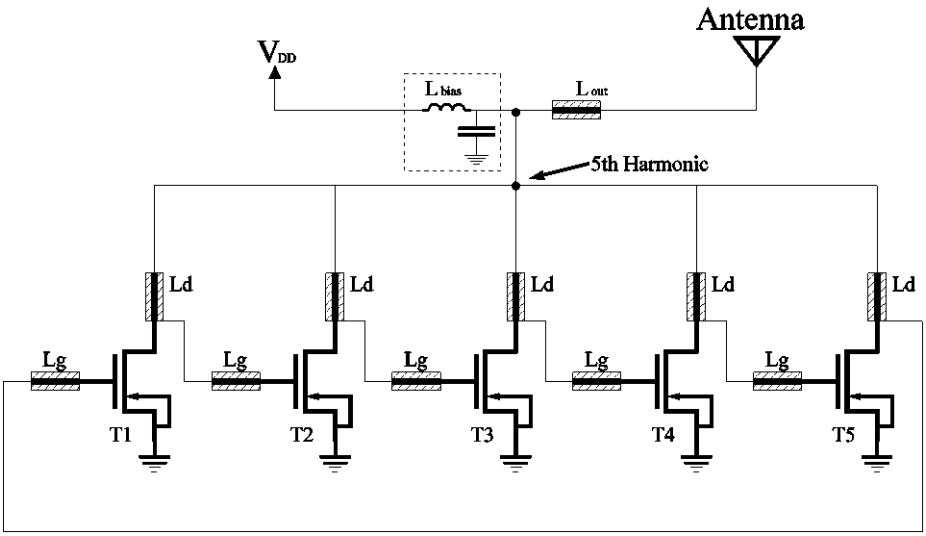
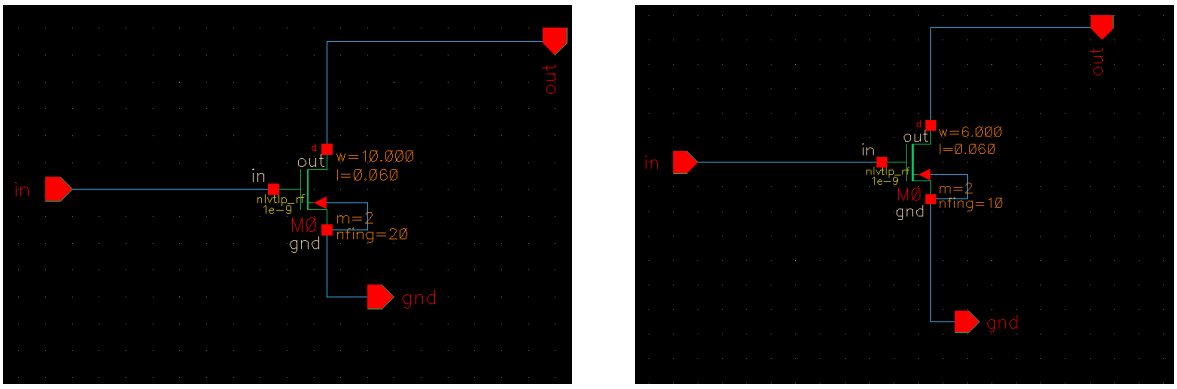


Figure 5-2: 5push circuit schematic with Microstrip lines

Physical realisation on-chip is not possible with real inductors due to the ultra-high frequencies and the size/quality-factor requirements. Furthermore, an exact phase shift of 360/5=72degrees is required between all branches; otherwise the ring-chain might not enter into oscillation. Therefore, we decided to realize the inductive interconnects by micro-strip transmission lines utilizing the lower two thin metals m1 and m2 for the ground shield, and the thick top metal M6 for signal propagation. CPW lines are much favourable for signal purity and higher propagation efficiency (quasi-TEM propagation), however for layout purposes constrained by the proximity of the oscillator elements micro-strip-based transmission lines have been designed, as shown in Figure 5-2.



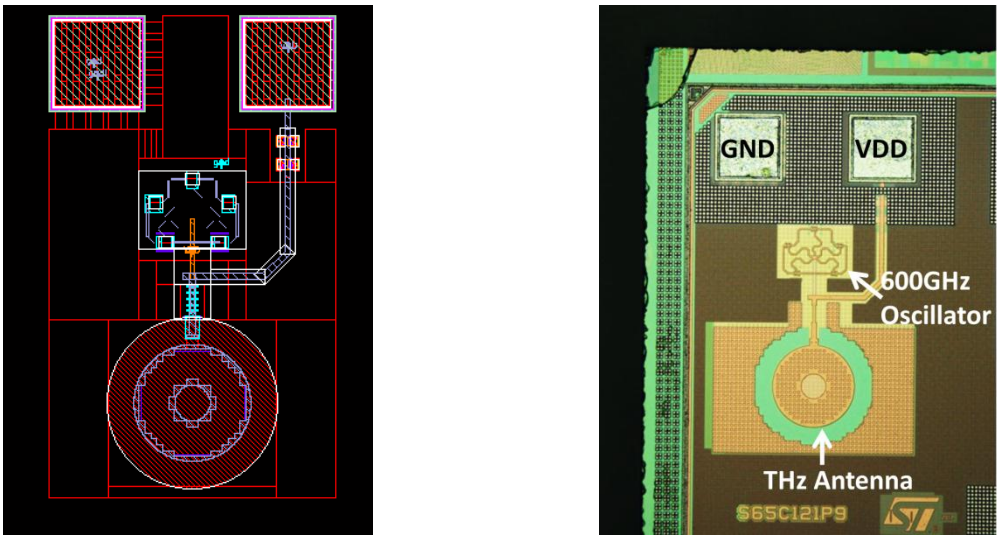
(a) **(b)**

Figure 5-3 (a) 650GHz oscillator element (b) 900GHz oscillator element

For a fundamental oscillation of 120GHz producing a 5th harmonic at 600GHz, each of the five oscillator transistor elements is comprised of two transistors in parallel with a width of W=10µm, a length of L=60nm, and 20 fingers, each, shown in Figure 5-3. a.

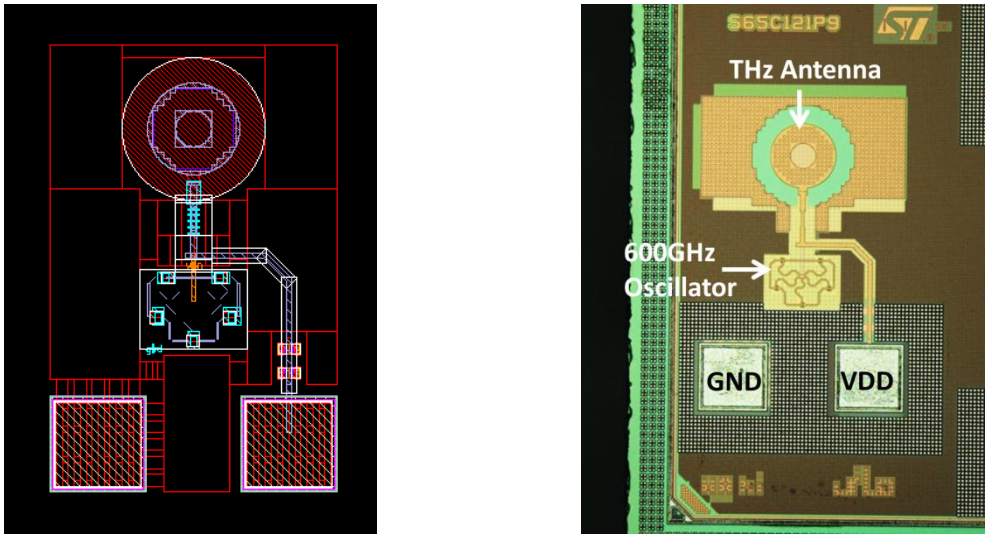
For a fundamental oscillation at 180GHz, and a 5th harmonic at 900GHz, each of the five oscillator transistor elements is comprised of two transistors in parallel with a width of W=6µm, a length of L=60nm, and 10 fingers, each, shown in Figure 5-3. b. The transistors are accessed from both ends of

the gates, and the sources are tied to the ground plane that surrounds the transistors with a strap of body contacts surrounding each element.



(a) **(b)**

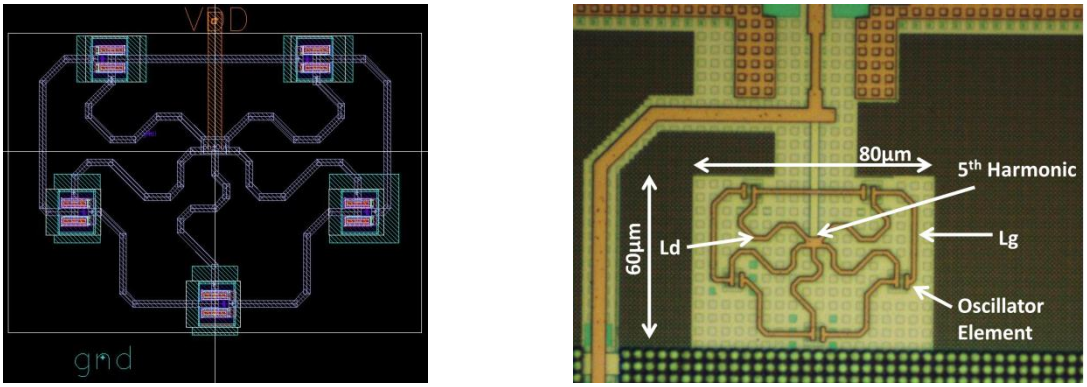
Figure 5-4: (a,b) Layout of 600GHz ring oscillator with an on-chip ring antenna



(a) **(b)**

Figure 5-5: (a,b) Layout of 900GHz ring oscillator with an on-chip ring antenna

The micro-strip lines L_g and L_d have an impedance of 77Ω and an inductance of around 20pH each. The implemented micro-strip lines were designed using the thick top metal 7 with a width of 1.5µm and L_g has a length of 40µm and L_d has a length of 35µm. The output is extracted via a 50Ω line using metal 6 of a width of 3µm.



(a) **(b)**

Figure 5-6: (a,b) 650GHz oscillator core

The layout realization is shown in Figure 5-4 for a 560GHz oscillator and Figure 5-5 for a 900GHz oscillator. The oscillator core is shown in Figure 5-6 and occupies a size of 80µmx60µm.

5.1.2. Oscillator Simulations and Measurements

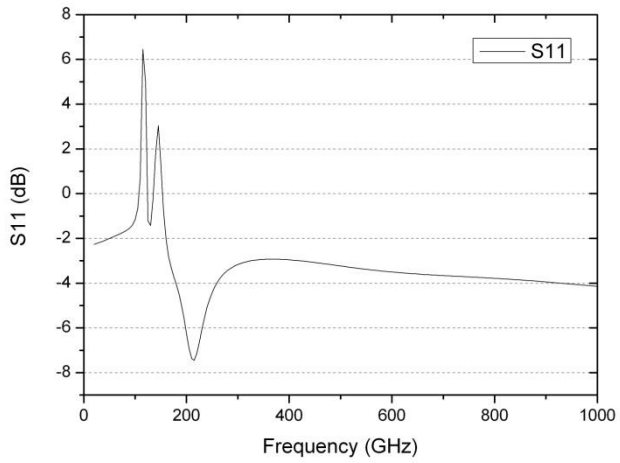


Figure 5-7: S11 plot for the 650GHz oscillator core

Figure 5-7 presents an S11 plot for the 650GHz oscillator core along the oscillator ring-patch when terminated with a 50Ω. The oscillator shows a positive S11 at 120GHz when a termination port is placed at the oscillator ring-path. Figure 5-8 shows the HB-simulated output power across the spectrum from the oscillator with the inclusion of the designed micro-strip lines. The simulation suggests a -20dBm power at 600GHz at a VDD of 1.3V, with a tuning range of 5GHz, and a power consumption of 100mW at 1.3V.

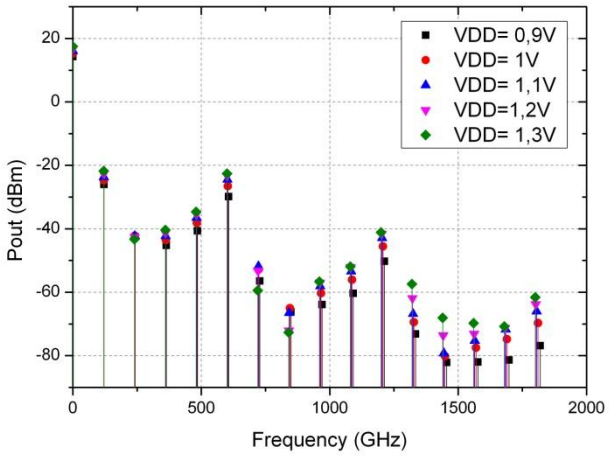
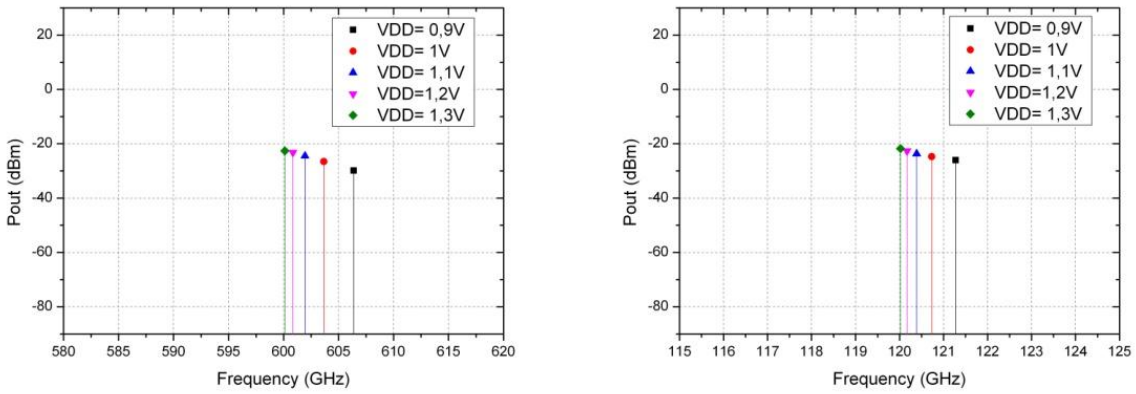


Figure 5-8: Harmonic balance simulation of the 600GHz oscillator



(a) **(b)**

Figure 5-9 (a)5th harmonic simulated output power (b) and fundamental output power

Figure 5-9.a,b suggest that the power combining did not entirely succeed in suppressing the 1st harmonic due to the transmission lines sizing and phase mismatch, and further optimisation steps need to be employed. As VDD increases, the synthesized frequency starts to decrease and the generated power increases. This Figure shows a tuning range of around 1GHz at the fundamental, corresponding to 5GHz at the 5th harmonic.

Figure 5-10 shows the time domain output signals at various VDD biases for the 600GHz oscillator. The signal has been deteriorated due to the presence of a high 1st harmonic signal. This figure shows that the amplitude of the synthesized signal is increased as the VDD is increased, mainly due to the enhanced non-linearities within the devices.

Attempts to measure the power sources were carried out. The total output power was measured using a power-metre equipped with a horn antenna with a lower cut off frequency of 300GHz to ensure the lower harmonics including the fundamental were suppressed. The total measured power was between

5 to 9 microwatts, however it was difficult to separate this measured power from any thermal power generated by the circuitry as this level approaches the sensitivity of the power meter (around 1 microwatt). Attempts to identify the frequency of oscillation using a sub-harmonic receiver equipped with a receiving horn antenna were not successful because the 5th harmonic of the designed sources lie outside the sensitive bands of the measurement equipment.

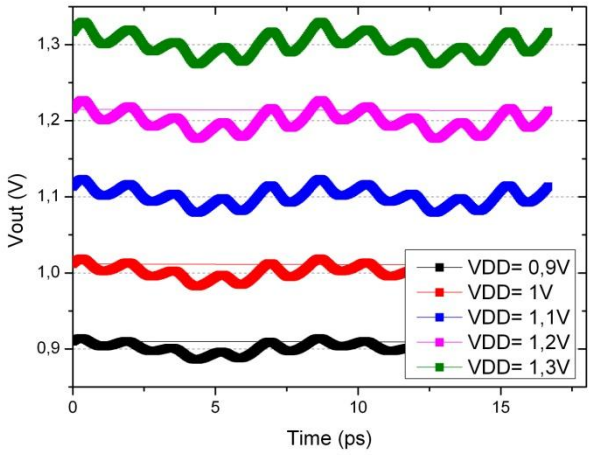


Figure 5-10: time domain of the output signals for the 600GHz oscillator

As a conclusion of this subsection, the design of 5push ring oscillators could lead to higher synthesized frequencies in comparison to all other solutions for frequency generation. However, this circuit offers little flexibility in terms of layout design, which makes it challenging to design multi-band oscillators.

Besides, the complexity of the passive-elements design leads to a number of design trade-offs that in return result in the reduction in output power or the increase in the power levels of other harmonics, as in the case described above. On the other hand, the increased number of elements in the oscillator increases the risk of detuning the circuit due to process variations. Further analysis for various process corners will be employed in the future.

5.2. Power Combining Schemes

As the output powers of harmonic oscillators in CMOS at Terahertz frequencies are limited to sub milli-Watt levels, it is thus essential to employ power-combining networks of multiple oscillators. Various power combining schemes exist in the state of the art, from spatial power-combining [133], to active and passive power combining [89], [134], [135].

We investigated passive power combining schemes based on microwave techniques. Figure 5-11 shows the basic block-diagram of a power-combining network where multiple oscillator elements are connected to the combiner-network producing a single output, ideally with a total output power of $N*P_{osc}$.

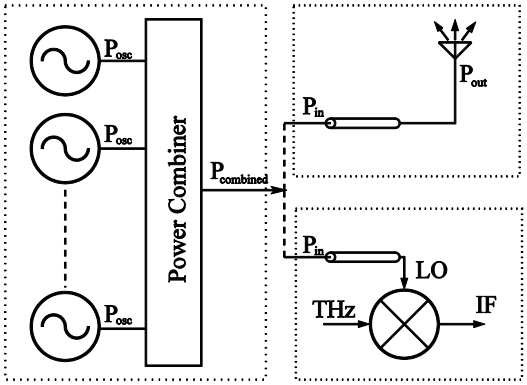


Figure 5-11: Power combining networks

However, the efficiency of power combiners is never 100%. The traveling signals are attenuated on the lossy transmission-lines especially as the frequencies increase, as explained in chapter 3. Plus, the impedance mismatch between the various oscillators and combiners, as well as the varying loading conditions of oscillators will increase the insertion loss per element. Additionally, the signals from each oscillator core have to be in-phase and must oscillate at the same frequency to add up efficiently, which is normally not the case. Each oscillator has different start up conditions and may suffer from wobbling signals and phase-noise.

Consequently, all oscillator cores have to be phase and frequency locked, either by injecting a stable signal from a strong core-oscillator, or by mutually locking the adjacent oscillators to be combined, to have a stable and efficiently combined output. In fact, the low quality factor of the lines comes at the benefit of facilitating the locking of oscillators.

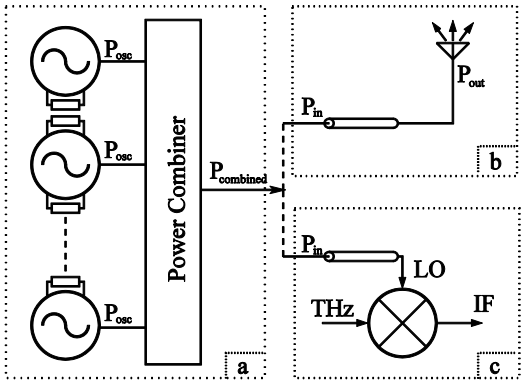


Figure 5-12: Power combining and mutual locking

Mutual locking of harmonic ring oscillators can be attained either at their fundamental frequencies or their corresponding 5th harmonics [136], [137]. Figure 5-12.a shows the block diagram of a mutually-locked power combiner scheme. Mutual locking of the chain of ring oscillators is attained by magnetically coupling part of the signals on the fundamental path of the oscillator. Luckily, the geometrical layout of the 5-element ring oscillators is of pentagonal shape, as shown in Figure 5-6, which allows for stacking of multiple oscillators back-to-back; thus mutually locking each other. Besides, the low quality factor of the transmission lines aids the frequency and phase pulling of the oscillators. Effectively, oscillators in frequency-proximity will pull each other towards a balanced state in phase and frequency. The drawback of this technique is the fact that the magnetic coupling when the lines are placed in each other's proximity will modify the lines' impedances and thus unbalance the oscillator fundamental path.

Similarly, Figure 5-13 shows an injection-locking scheme with a strong oscillator is injecting its signal into the oscillators, magnetically, whilst the oscillators are mutually dragging each other. The benefit of this scheme is the idea that the output could be controlled and steered in phase and frequency by controlling the injecting oscillator. Thus, steerable arrays could be designed utilizing this scheme.

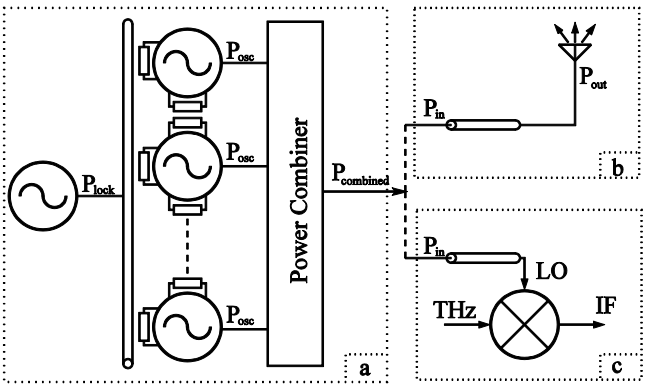


Figure 5-13: Power combining and injection locking

Regarding the passive power-combining methods, various power combiners exist for a long time. However, for lower frequencies around the RF and Microwave bands, such combiners could not be implemented on Silicon due to the huge area they require. On the other hand, due to the low power levels of Silicon-based sources described in this chapter, it is impossible to employ passive power

combining off-chip. Therefore the benefit of Terahertz frequencies arises from the fact that the wavelengths are quire short, relative to Microwaves and RF. Therefore combiners such as Wilkinson combiners are feasible for on-chip implementation.

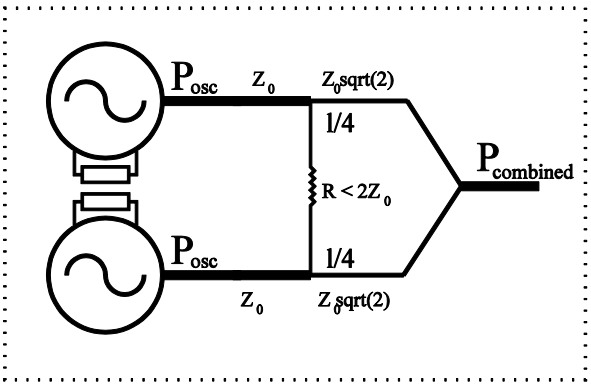


Figure 5-14: Power combining using Wilkinson combiners and fundamental mutual-locking

Figure 5-14 shows a schematic of a Wilkinson power combiner. Here, we include the technique of mutual locking through magnetic coupling as discussed above. The efficiency of the combiner here is increased with the increase of the mutual locking of oscillators.

Figure 5-15 shows an interesting method of locking on the harmonics of the oscillators, described in1982 [138]. This technique exploits the fact that a Wilkinson combiner is designed with a balancing resistor connecting the combining/dividing ports. Performing an Odd/Even analysis shows that for a minimum insertion of the signal from port 2 to port 3 and vice-versa, the termination resistor should be equal to twice the characteristic impedance of the line:

$$R = 2 \times Z_0$$

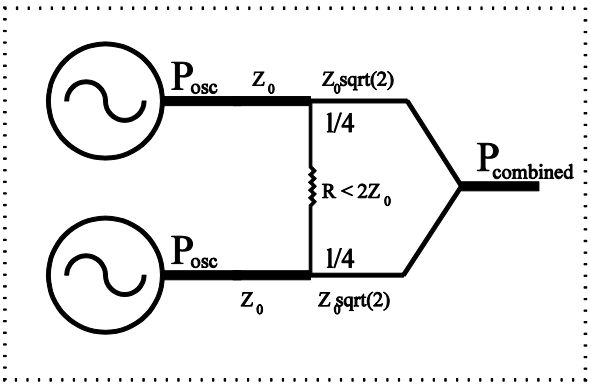


Figure 5-15: Power combining using Wilkinson combiners and harmonic mutual-locking through termination-resistor mismatch

However, if the resistor value is modified, for instance decreased below 2 x Z_0, or increased beyond, a portion of the odd signal will be injected from one port into the other. If the resistor is sufficiently reduced, the injected signals from one side into the other would effectively assist both oscillators to mutually lock at a common frequency/phase level. One the other hand, the quarter-wave line at the frequency of operation could be modified to enhance the signal injection. The benefit of this concept is that the design is relaxed on the layout level, contrary to the design shown in Figure 5-14.

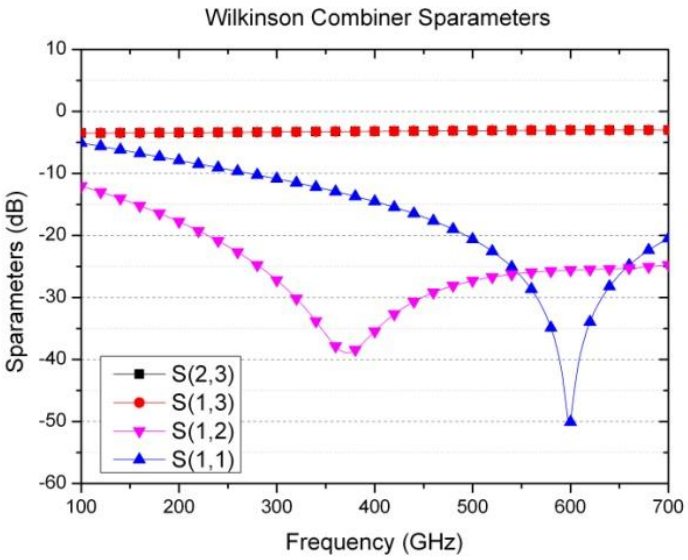


Figure 5-16: Simulated S-parameters of a 600GHz Wilkinson power combiner with a 58µm quarter-wave line showing ports 2 and 3 as the input ports and port 1 as the combined output port

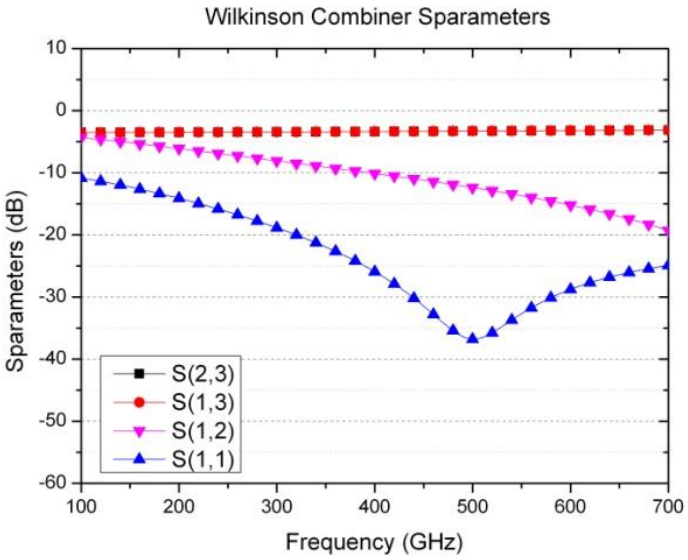


Figure 5-17: Simulated S-parameters of a 600GHz Wilkinson power combiner with a 40µm quarter-wave line (shorter than required) showing ports 2 and 3 as the input ports and port 1 as the combined output port

Furthermore, the previous subsection has shown that the implemented 5-push ring oscillators still exhibit a strong fundamental at the output. Therefore, the proposed circuit enables utilizing the first harmonic by re-injecting it from one oscillator into the other.

Simulations of the Wilkinson combiner are shown in Figure 5-16 and Figure 5-17. As mentioned above, a 100Ω resistor is necessary to damp the odd-modes of the combiner. A 90Ω resistor is used in the following simulations. For a quarter-wave line, the length of the micro-strip line was calculated to

be 58µm. Figure 5-16 shows around -25dB of signal insertion between both combining ports at 600GHz and -15dB at 120GHz. This plot shows that only a small portion of the fundamental leaks from one combining port into the other.

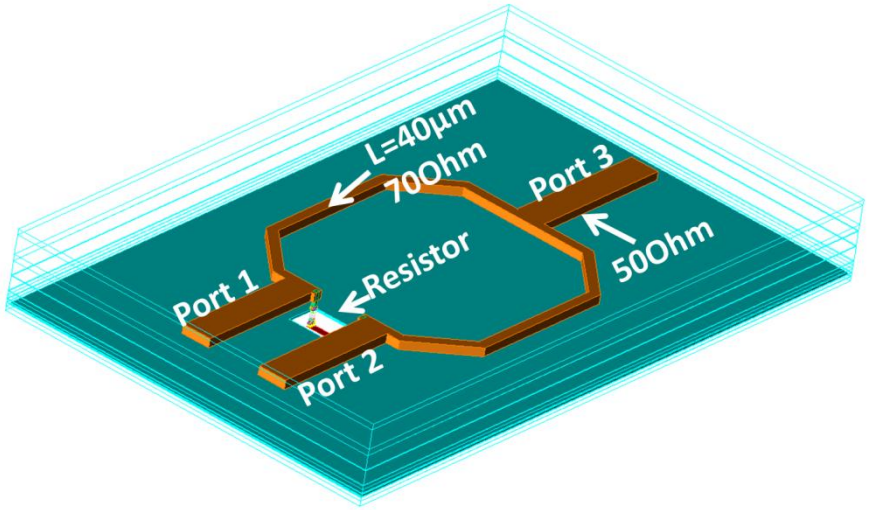
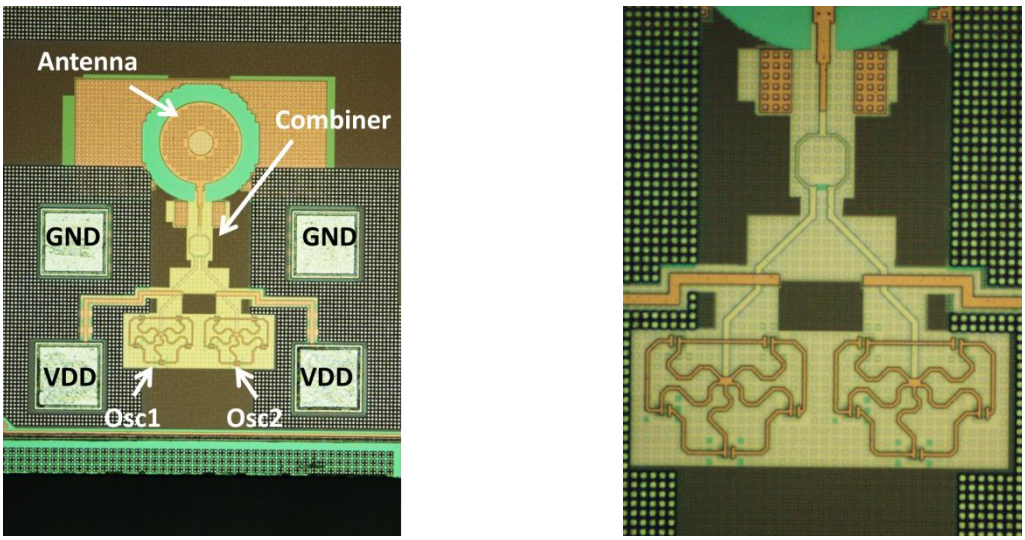


Figure 5-18: 3-Dimensional view of implemented Wilkinson power-combiner. The combiner is implemented on thick Metal-6 of a 7 metal back-end of a 65nm Bulk CMOS technology



(a) **(a)**

Figure 5-19: (a,b) Die micrograph of power combining circuit for ring oscillators using Wilkinson combiners. The circuit occupies x mm2, and was design in a 65nm bulk CMOS process technology from STMicroelectronics.

On the other hand, when the quarter-wave line is varied, the signal injection between the combining ports is increased. Figure 5-17 shows the simulations of the same Wilkinson combiner, yet with a 40µm quarter-wave line. This plot shows that S12 has increased up to -15dB at 600GHz and up to -5dB at 120GHz. This means that the fundamental signal leaks into the other port and only a portion of the 5th harmonic at 600GHz leaks into the other port.

This concept has been designed in a 65nm Bulk CMOS technology. The micro-strip Wilkinson combiner layout is shown in Figure 5-18 and the die micrograph is shown in Figure 5-19. The characteristic impedance of the micro-strip lines at the input and output ports of the combiner are 50Ω, and the quarter-wave lines have an impedance of 70Ω. The length of the quarter-wave lines was chosen to be 40µm to enhance signal injection between both combining ports. The microstrip lines were designed using thick metal 6, and the ground shield is comprised of a mesh of metals 1 and 2. The resistor value is 90Ω. The 600GHz oscillator designed and presented in the previous section was connected to the input ports of this Wilkinson combiner, and the output was connected to a ring antenna tuned at 600GHz. Measurements of this structure will follow soon.

5.3. Heterodyne Receiver Design in 65nm Bulk CMOS

One idea to increase the sensitivity of the THz detectors is to employ heterodyne techniques. A block diagram of heterodyne receiver is shown in Figure 5-20. The Terahertz radiation is provided from an antenna tuned to the frequency of choice, and is coupled to the THz mixer. A local oscillators is simultaneously coupled to the mixer-core, and an intermediate frequency (IF out) is extracted and amplified at the output.

Heterodyne detection also preserves both amplitude and phase information which could be exploited for 3D-like imaging. However, heterodyning effectively comes at the cost of increased power consumption and reduced detection bandwidth, contrary to direct detection circuits. Furthermore, the difficulty of designing frequency synthesizers operating within the THz range in addition to the challenge of injecting their signals into the mixing-chain means local-oscillators for heterodyne receivers are utterly challenging to realise.

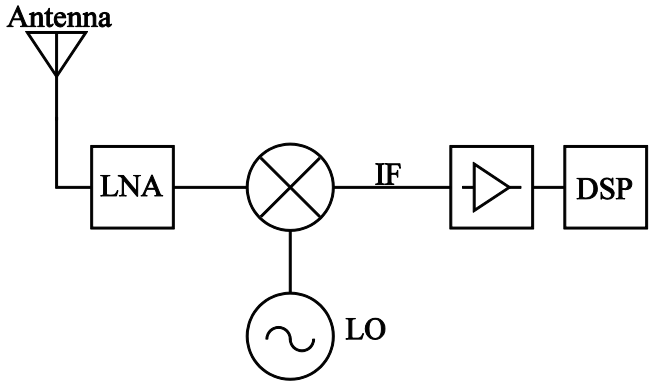


Figure 5-20: block diagram of heterodyne receiver

As shown in Figure 2-5 in chapter 2, various circuit topologies exist for heterodyne detection. We are interested in devising methodologies for realising heterodyne receivers. Heterodyne receivers provide much higher sensitivity levels than direct detectors. However, the main concern as discussed earlier is both the efficient synthesis of a stable and powerful local oscillator to drive the mixer, as well as the supply and distribution of these LO signals. Thus, this may seem utterly inappropriate for multi-pixel design as the power consumption will be unreasonably high and the integration within chips will be largely space consuming. However, some applications require only a single receiver or a few pixels, whilst sensitivities might be more important for the system requirements. Furthermore, heterodyne detectors are effectively at the heart of communication receivers. Therefore, it appears to be interesting to develop heterodyne detectors for high sensitivity THz imaging and communication using CMOS technologies.

Therefore, this section discusses various methods of implementing heterodyne mixers and of supplying the LO signals, and will demonstrate an implemented heterodyne mixer in 65nm CMOS.

5.3.1.1. Supplying LO spatially

One method to realise heterodyne receivers is to supply the local oscillator spatially as shown in Figure 5-21. In this case, two sources are required, and the illumination mechanism should be taken into account. Active illumination with a second source operating at the same frequency as the first

source, $f_{THz}=f_{LO}$ (homodyne detection), or with a slight shift in frequency, $f_{LO}=f_{THz}+\Delta f$ (heterodyne detection) enables this method of imaging.

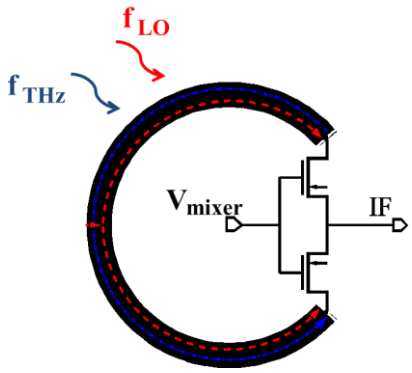


Figure 5-21: Spatially supplied local oscillator and THz signals

Another novel method of providing the local oscillator spatially is based on the dual-polarisation antennas discussed in chapter 3.5, where only one source is needed. In this case the LO and RF comprise of the vertical and horizontal polarizations of a single source, respectively.

5.3.1.2. Supplying LO On-chip or Off-Chip

Having shown in this chapter that it is yet feasible to synthesize frequencies within the Terahertz band, we have investigated the possibility of using the Ring-Oscillators as local-oscillators for heterodyning. The small size of the oscillators serve as an attractive option for compact sized heterodyne mixers.

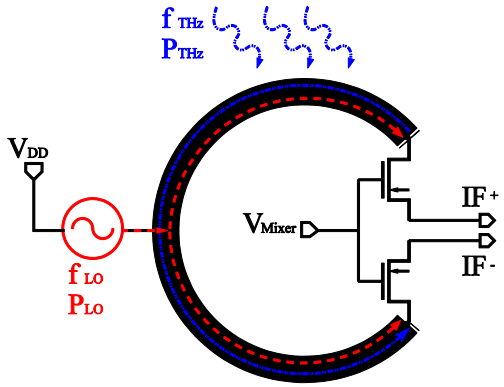


Figure 5-22: Heterodyne mixing with differential outputs.

Figure 5-22 shows a method of supplying the local oscillator to the THz heterodyne mixer. An on-chip or off-chip local oscillator provides the signals through the on-chip THz antenna at the zero-field point. In this case, the THz signal coupled by the antenna is differential at the mixer terminals, whereas the local oscillator signal splits at the antenna branch and arrives with the same phase at both terminals of the mixer. The heterodyne mixer could be built with a differential output IF as shown in Figure 5-22.

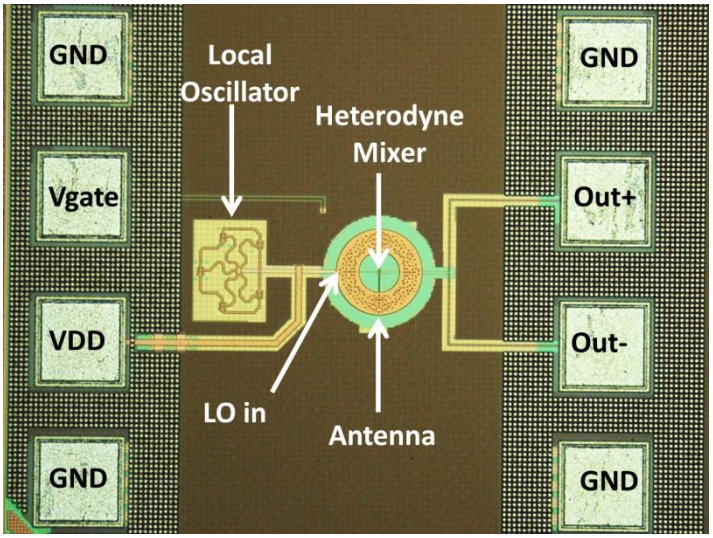


Figure 5-23: die micrograph of Terahertz heterodyne mixer

The THz mixing-core is a differential NMOS pair connected to a differential Ring-Antenna via their sources, where each source received an opposite phase THz-signal. The gates are connected to a DC bias-line. The local oscillator is provided through the antenna at the zero field intensity. The power from the LO splits in between the branches, and pumps the transistors from both ends in phase, whilst the THz radiation arrives through the antenna and balanced to the differential ports of the mixer. The gate bias is provided separately. This circuit was implemented in a 65nm bulk CMOS technology and the chip micrograph is shown in Figure 5-23. Two 1µm/0.2µm low V_T low power RF NMOS transistors were designed for a differential output. A simulated time domain of the balanced output of the mixer is shown in Figure 5-24.

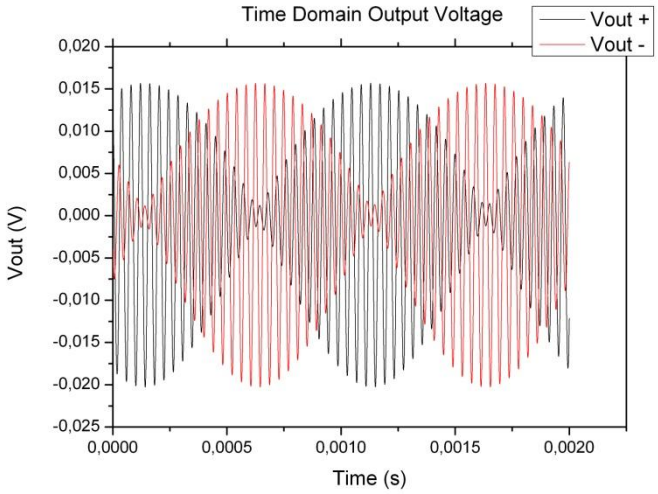


Figure 5-24: Time domain output of the heterodyne mixer

5.4. Chapter Conclusions

In this chapter implemented circuits for Terahertz frequency synthesis based on 5push ring oscillators were presented. Two oscillators at 600GHz and 900GHz with on-chip antennas were presented. The circuits are not measured yet. The concept relies on generating a high fundamental frequency in a 5 element ring chain by satisfying the Barkhausen criteria, then extracting 5^{th} order harmonics that add in phase if properly combined. The design suffers from layout restrictions so that a complete phase rotation is maintained in the chain designed hand in hand with the proper impedances of the lines. The current source is not measured yet, but simulations show that a strong fundamental still exists, thus decreasing the 5^{th} harmonic power by a few dBs. Yet, further optimisation is required and is believed to attain better output power levels.

To overcome this impediment, power combiner circuits based on Wilkinson combiners was designed. The Wilkinson combiner is designed in a manner to inject part of the odd modes from one input port into the other. This is true for both the fundamental and the 5^{th} harmonics, with higher fundamental return loss.

A heterodyne mixer using the ring oscillator as a local-oscillator was also presented. The LO provides the signal through an on-chip antenna that splits the signal along the antenna metals. The LO signals arrive in phase at both of the differential mixer ports, whilst the THz received signals arrive out of phase at the ports. This design is beneficial for heterodyne-imaging for increased sensitivity, as well as for RADAR-like phase imaging and communications.

The aim of this chapter was to explore possibilities of high-frequency synthesis. Even with the limited output power, foresee future benefits from such circuits, especially in communication and in active imaging are anticipated. With further optimisations in plans, as well as power combining techniques, target full-system integration of Silicon detectors and sources will be targeted.

Chapter VI- Terahertz Imaging Systems

Efficient design and realisation of commercially viable Terahertz systems require sufficient knowledge of both the application intended and the circuits supporting the application. As discussed earlier, certain applications such as material characterisation require the best sensitivity and dynamic range available, and they would require single pixel systems with wide bandwidths (spectroscopic measurements) to analyse absorption/reflection signatures. Applications such as security screening require a large number of pixels yet quick processing and narrow bandwidth of operation could be tolerated.

As discussed in Chapters 2 and 3, THz detectors in CMOS technologies do not exhibit the required sensitivity for passive imaging systems. That is due to the NEP levels of the current CMOS detectors that are not low enough to detect the natural radiation of objects at ambient temperature. Therefore, another important note to mention is that we are dealing with "Active Imaging" requiring active illumination of the object under test from one or many Terahertz sources, as discussed in Chapter 4, as opposed to "Passive Imaging" techniques. Active imaging could be conveyed either in "*Reflection Mode*", where the THz signals that bounce off an object-under-test are detected by the THz-detectors, or in *"Transmission Mode",* where the THz-radiation that penetrates and exits an object-under-test are detected. Accordingly, we require the proper source/object/detector alignment that produces the best images possible. In other words, the radiation from the THz-source should be guided properly towards the imaging-plane and then projected onto the detectors' collecting aperture with the highest optical and electromagnetic efficiency possible. Amongst the parameters to be taken care of are the polarizations of the sources and detectors antennas.

Moreover, as the commercially available sources are limited in power (few 10s or 100s of μWatts), it is thus apparent that integrating N pixels at the detector-end would effectively mean division of the available power, at best, by the number of receive elements N. This will be apparent shortly that the power received is impacted by more than the number of elements as the coupling efficiency is further deteriorated mainly by the detector array-geometry and by the system EM complexity. Recalling from Chapter IV, multi-pixel systems have much higher NEP levels due to the added noise-contributors, leading to a further degradation of the overall system efficiency. The dynamic range is impacted in this case, and the circuit level should be designed with the link-budget estimated beforehand. A solution would be to use multiple source-modules to increase the SNR, with a direct impact on cost.

It is essential to recall that terahertz systems are quasi-optical systems. It is essential to deal with beams that have relatively good Gaussian field and power distributions. Effectively, Gaussian-Optics could be employed when analysing and tracing the THz-beams; enabling the utilization of collimating and reflecting tools such as lenses and parabolic mirrors.

Spatial resolution is a gained factor of the increase in frequency of operation due to the shorter wavelengths compared to Microwaves and mmWaves. However, spatial resolution is not exactly the wavelength of the utilized radiation, and is rather the diffraction-limited resolution, as explained in Chapter 1, with the diffraction angle defined as:

$$\alpha_{min}=2.44\ \lambda/D \quad (42)$$

leading to a spot resolution d_{spot}, at a distance R, of

$$d_{spot}=2.44\ \lambda R/D \quad (43)$$

Imaging in reflection-mode is particular challenging because of the known issues of specular reflections. Direct detectors are more suited for transmission mode imaging because direct detectors do not provide phase information nor distance information. Because of this, this camera is intended for transmission mode imaging.

In this chapter, we demonstrate various system designs from single and multiple pixel designs. We will first analyse the link-budget requirements of the various setups in view of feasible source-detector design. Then, optical and electrical setups of each imaging-system will be demonstrated. We will also consider stacking techniques for imaging of large objects. These analyses will therefore set our reference boundary-conditions for our THz-systems' performances.

6.1. Link Budget Estimations

The very heart of Terahertz system design lies within the estimation of the link budget. The core aim is to maximize the SNR at the output of the imaging system whilst maintaining the highest sensitivity possible, defined by a lower NEP. We have observed throughout this work that the regions of maximum $\Re v$ and minimum NEP are not aligned. This has been explained to be as a result of the reduced mixing efficiency within the regions of lower channel resistance. Whereas, this channel resistance is the main noise contributor in terms of white Johnson noise, the noise thus decreases as the transistor channel is opened further. Therefore, the NEP includes both the responsivity and noise voltage factors.

The output signal to noise ratio for a direct detector is given by 44:

$$SNR_{out} = \frac{P_{in}}{NEP\sqrt{fps}} \quad (44)$$

Where

- SNR_{out} is the signal to noise ratio at the output of the detector
- P_{in} is the input power at the input of the detector
- NEP is the measured optical noise equivalent power of the detector
- $\sqrt{fps}$ is the square root of the frame rate of the imaging system, where the frame rate is the inverse of the integration time τ in seconds.

This equation shows the interrelation between the system performance and the NEP. Going back to the original definition of the NEP as the power level where SNR drops to unity at an integration time of 1s, could also be revealed in this equation.

On the other hand, the responsivity sets the output voltage dynamic range. Even for a high imaging SNR, the output dynamic range is important as it is directly related to the succeeding readout electronics. This raises the question whether the THz detector should be operated at max $\Re v$, min NEP, or somewhere in between. It seems the answer is not directly obvious, but it is apparently

application and system dependant. It may be deemed useless to design for low NEP, if the corresponding $\Re v$ at the same bias point is very low and if the resultant output voltage is lower than the sensitivity of the amplifying stage ahead. It also is dependent on how strong the input signal is anticipated to be.

For instance, in cases where the input power is quite strong and the matching is properly adjusted between the detector and antenna, the output voltage produced at the minimum NEP gate bias could be sufficient for efficient signal amplification. In the case where the peak signals are still weak enough to produce a sufficient output voltage, it may be essential to back off from the NEP minimum bias voltage onwards to the regions of higher responsivity. Of course this should be done with the certainty that the detector is still capable of detecting these week signals, again defined by the NEP at that specific gate bias.

Therefore it is valid to separate the operation of the detectors between single and multiple pixel systems. The devices could as well be dimensioned accordingly, with the readout electronics a complementary part of the entire design.

6.2. Single Pixel Imaging Setup

Imaging by single-pixel systems is probably the easiest and most straight-forward in terms of system complexity. Figure 6-1 shows the basic optical and electrical setups for single-pixel scanned-imaging in *transmission-mode*. The main electrical components are a THz source, a THz detector, an AM or Pulse modulator, voltage supplies, and a data acquisitions and processing system such as a computer. An example of a terahertz source is the Schottky-diode based multiplier-chains provided by Virginia Diodes [60] that feed to diagonal horn antennas. This type of multiplier chains typically have a multiplicity in the order of 40-60X, therefore they are typically fed by a GHz-range frequency synthesizer. The typical total radiated power is in the range of 1mW for narrow-band sources and 10s of for wide-band sources ranging from 650-1000GHz. The diagonal horn is fed by waveguides, and normally delivers nice Gaussian beams. Another option is to use the Silicon integrated-sources, as discussed in Chapter 5, with total output powers ranging from 1-10 of μW.

The THz-source is fixed at one end of the setup and is used to illuminate the object in free-space. The detector should be aligned with the source, and both source/detector antennas should be aligned properly at boresight for maximum radiation coupling (including antenna polarization).

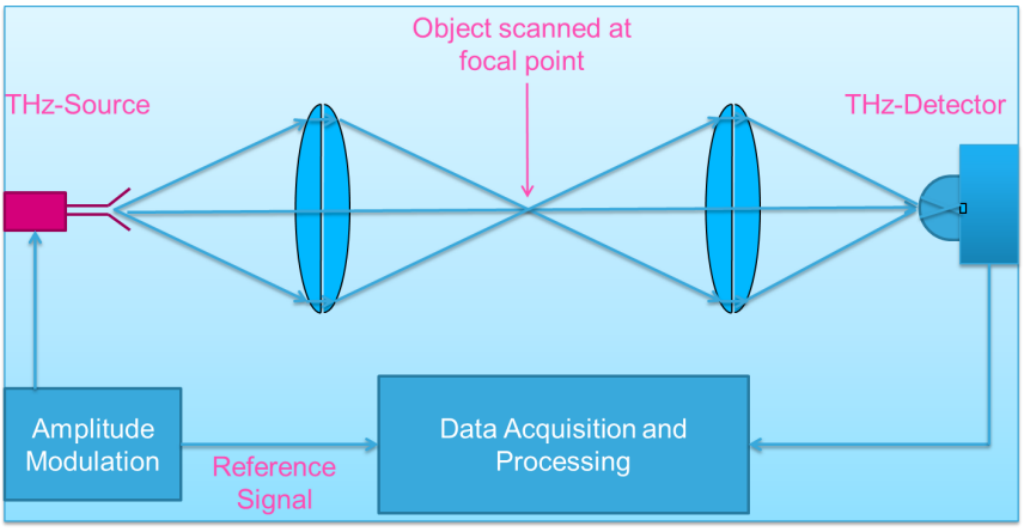
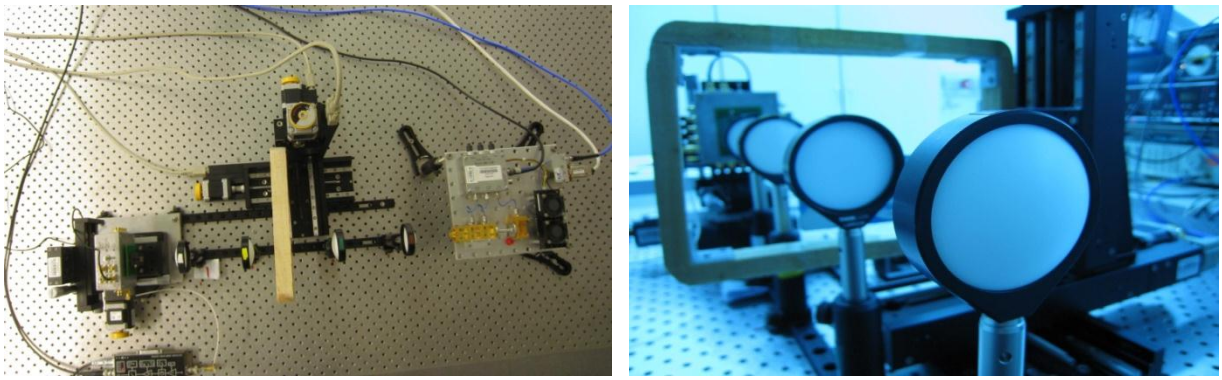


Figure 6-1: Single-pixel scanned-imaging setup

The THz source creates a diverging Gaussian beam, and to efficiently utilize the available radiated power PTFE lenses are used to collect the radiated power and converge them onto a diffraction limited spot, as shown in Figure 6-2. This spot is the exact location where the object will be placed to be imaged. The THz-beam diverges from that point on, and another set of PTFE lenses will be used to re-collect the radiation and project them on the aperture of the detector antenna.



(a) **(b)**

Figure 6-2: Photograph of (a) scanned imaging setup (b) with the corresponding plastic lenses

As mentioned above, the object to-be-imaged is placed at the focal-spot, and is scanned in the {X-Z} direction. A cross-section of the imaging plane is shown in Figure 6-3. The focal-spot is the point where the radiated power is squeezed onto the diffraction limit, and imaging at this spot provides with the highest possible dynamic-range.

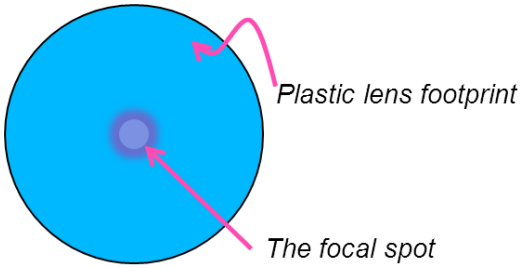
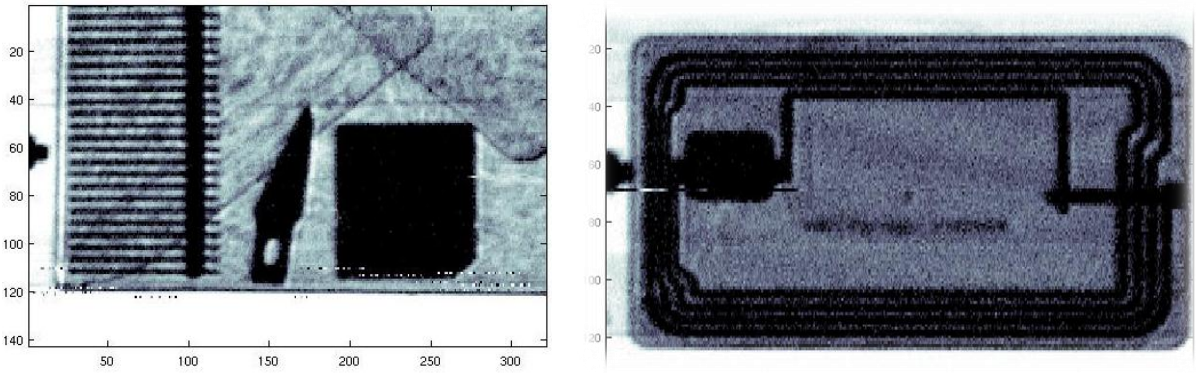


Figure 6-3: Cross-section of focal-plane showing the focal-spot and the lens footprint

As the THz-radiation illuminates the receiver, the CMOS detector converts the received power according to its characteristic $\Re_v$, and the ouput voltage would range according to $Vo= \Re_v X P_{in}$, based on the bias-dependant voltage responsivity. The maximum output voltage would correspond to the maximum power is received when there is total signal transmission through the focal-spot. The minimum output voltage corresponds to the Noise-Spectral density at the frequency of operation, and it equals N_0=NEP x $\Re_v$. Synchronously, the output voltage from the detector is digitized and processed whilst the object is being scanned in the {X-Z} direction. As the output voltage levels correspond to the various power levels transmitted through the imaged object, the THz-image will be produced accordingly.

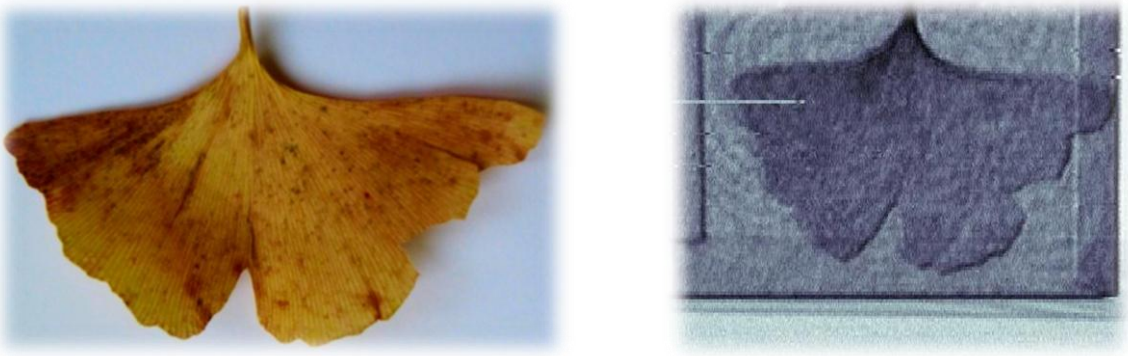
Imaging Results:

Here we present some of the imaging results that have been performed throughout this thesis. Figure 6-4 shows the first 1THz imaging results in CMOS using a source driven THz detector in CMOS 65nm bulk. The figure shows (a) an envelope with hidden objects (b) and an RFID card both scanned in transmission mode at 1THz.[78]



(a) **(b)**

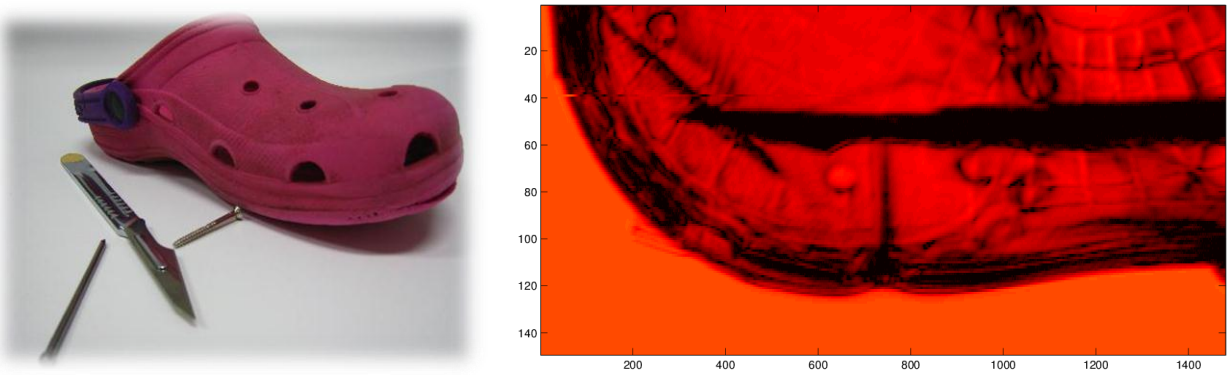
Figure 6-4: (a) An envelope with hidden objects (b) and an RFID card both scanned in transmission mode at 1THz



(a) **(b)**

Figure 6-5: (a) Optical image and (b) 650GHz image of a semi-dried leaf hidden in an envelope

Figure 6-5 shows a 650GHz image of a semi-dried leaf that was hidden inside an envelope produced by a gate-driven THz detector in 65nm CMOS SOI with a silicon lens [79]. The THz image shows the regions of dried water and the regions where water still exist



(a) **(b)**

Figure 6-6: (a) Optical image and (b) 650GHz image of a crocs shoe with hidden metallic objects

Figure 6-6 shows the image of a crocs shoe with some metallic objects hidden inside [79] scanned using a lens integrated NFET detector in 65nm SOI CMOS, operating at 650GHz. The THz image shows very high quality results with details revealing the various application domains of THz imaging, from quality control and inspection to security screening and other.

6.3. Multi-Pixel Imaging Setup

Active imaging at terahertz frequencies is commonly done by raster scanning with an image acquisition time on the order of minutes. This section, however, demonstrates the camera operation in video-mode, where video streams are recorded in real-time without the need for raster scanning and source modulation. While raster scanning focuses a terahertz beam down to a diffraction limited spot size, which transmits through the object and is then refocused onto a single detector element, this camera requires optics which illuminate a large object plane simultaneously. This substantially reduces the irradiance at the object and the image plane, reducing the available SNR per pixel. For

this reason, a higher power 0-dBm x48-multiplier chain at 650-GHz was used for object illumination in the following.

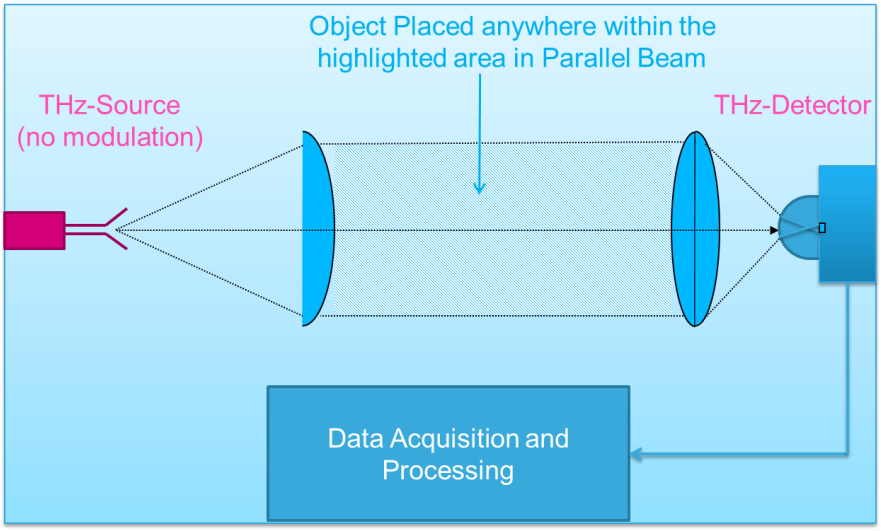
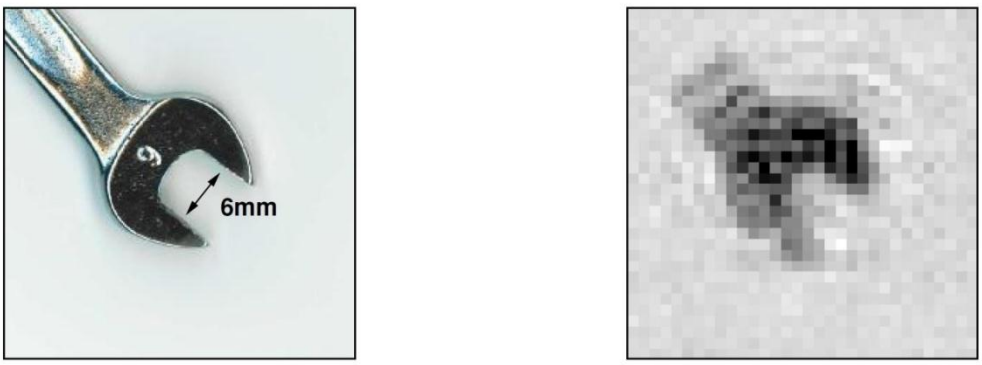


Figure 6-7: Multi-pixel imaging setup

Figure 6-5 shows the optical imaging setup used for transmission mode imaging with a single terahertz source. In order to create a parallel Gaussian beam at the object plane, a 0-dBm 650-GHz x48 multiplier source with a single-mode 25-dBi horn antenna was placed at the focal length of a plano-convex spherical PTFE lens with an f-number of f/2. The terahertz beam penetrates the object and is re-focused by a fast PTFE lens (f/0.5).

The fast lens almost matches the field-of-view of about 23° of the camera module, such that the object plane is projected onto the hyper-hemispherical silicon lens of the camera module. This basic imaging setup was designed to demonstrate imaging in video mode at 25fps. A digital still frame recorded with this setup is shown in Figure 6-8. It shows a picture of a metal wrench with a 6mm opening recorded using the 1kpixel THz video presented in chapter 5.



(a) **(b)**

Figure 6-8: 650GHz still image from the 1kpixel camera demonstrated in chapter 4 [81]

6.3.1. Stacking of multi-pixel camera modules:

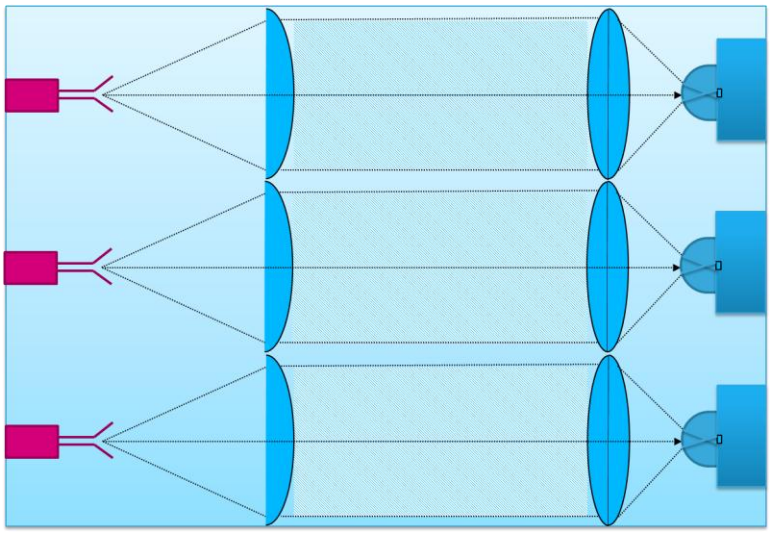


Figure 6-9: Stacking of Multi-pixel imaging setups (modular approach)

One way to increase the imaging area and to utilize best the fact that CMOS imagers are relatively cheap for mass production is to design modular THz multi-pixel imagers intended for stacking. Figure 6-6 shows a schematic of the proposed concept. It comprises stacked modules back to back to increase area of the imaging plane. Each module is made of a THz source with a diverging beam, optical lenses to create a parallel beam from the transmission end. From the detection end it is comprised of a multi-pixel THz camera equipped with a silicon lens, and a correction lens to converge back the THz radiation onto the camera, within its field of view.

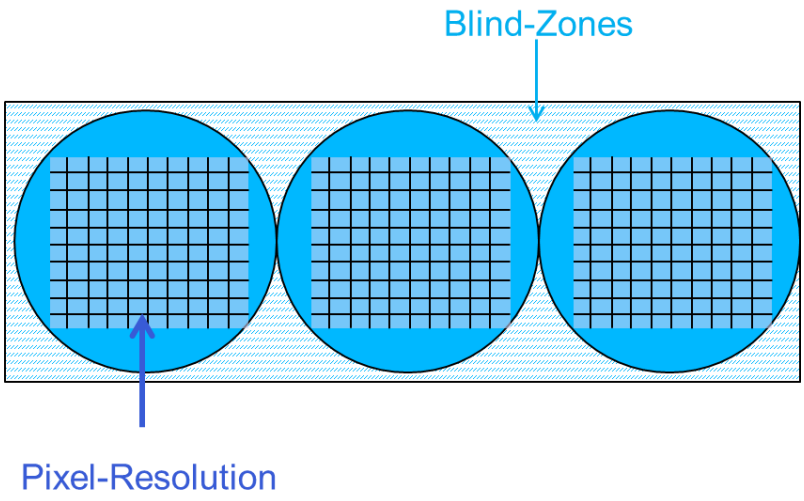


Figure 6-10: Cross-section of stacked multi-pixel modules at the imaging plane. Blind zones exist due to the physical footprint of the lenses.

This stacking of course creates blind zones as shown in Figure 6-7 due to the optical setup footprints. However, this setup is still beneficial as the optical imaging area is enlarged. Blind areas could be

corrected by mechanically moving the object or the complete setup twice, in X and Y directions. However, for moving objects, these blind zones could be corrected in software.

It is important though to discuss this setup in terms of feasibility and cost. So far, as discussed in chapter 4, sources are bulky and expensive. Therefore it is more cost efficient to invest in higher power sources and increase the pixel count on the detector side, than creating stacks of detectors.

However, as research is on-going in terms of source design using Silicon technologies, this stacking technique could prove worthwhile. In that case, the specifications of the integrated sources design could be relatively relaxed at the expense of distributing the system over a larger number of modules with lower pixel counts designed within the available power levels.

6.4. Chapter Conclusions

The aim of this chapter was to give an idea on how the designs of THz detectors and cameras discussed in the previous chapters were utilized to produce THz images. This chapter has thus presented techniques that were performed in lab for single pixel raster-scanned imaging as well as multi-pixel imaging using focal-plane arrays. Imaging results from some of the detectors and from the 1k-pixel camera designed in CMOS 65nm were also presented.

The modular concept of CMOS-based THz cameras and sources which could lead to stacking of THz detectors to increase the imaging area was also presented.

Chapter VII- Conclusion and Prospects

This thesis has reviewed, contested, derived, and designed a variety of concepts regarding THz design in CMOS. The realisation of various room-temperature THz apparatus based on CMOS FETs was discussed in view of their numerous parameters.

Design of single pixel Terahertz detectors was examined in various technology nodes, namely 65nm Bulk and SOI CMOS, and 28nm FDSOI. A wide field analyses was performed with respect to enhancing the detectors performances defined by their noise equivalent powers and responsivities. These figures of merit were shown in terms of their relation to the detector topology, device dimensioning, anticipated power levels and chopping frequencies, load conditions, noise, technology nodes and modelling, as well as the efficient electromagnetic design.

Initial trials in CMOS have tested the capabilities terahertz detection and were presented in this manuscript. Then, the single pixel design methodology that was discussed in the previous chapters was applied and optimised detectors lead to record performances with respect to Silicon based detector state of the art, as well as existent commercial products. It is expected that detection of THz in CMOS is still valid and should operate beyond the design and measured spectra that was restricted by the available equipment at the time of designing these circuits. Designs and measurements beyond 1THz could follow soon.

The architecture of a fully integrated camera chip is a normal technological and scientific inclination to make use of CMOS capabilities. Therefore, a 1k-pixel video camera for THz imaging was designed and presented here; being a world first in terms of large integration in a commercially viable technology. As naked THz detectors could reach very good performance levels, this invention tested the viability of designing with full integration. The likelihood of commercializing THz solutions based on CMOS relies on further industrial optimisations as well as proper fitting the solutions to certain application spaces.

Essentially, THz sources remain a hurdle. Cutting down on the detector cost by migrating THz solutions to Silicon technologies may be deemed insufficient should the source design lag behind endlessly. This incited the investigation of CMOS based sources in the recent years. Therefore, ideas of THz frequency synthesis were also discussed in this thesis. As the aim is to further stretch the frequency of operation of the sources, I have suggested the 5-push oscillator as a solution to synthesis tones beyond the technology limits. Even though the source power may be relatively low along with certain layout-difficulties, the concept is promising as frequencies as high as 900GHz could be reached. Full arrays of sources must be possible in CMOS as the sizes of these sources are very small compared to the current waveguide-based art.

Therefore, power combining techniques were also discussed in this dissertation. Methods include mutual and injection locking as well as a combination of both is discussed with respect to their feasibility. One concept out of many was presented, including a modified Wilkinson combiner that accommodates mutual locking within its inherent design.

To expand on the benefit of source design, heterodyne mixers were also presented. These mixers aim at increasing the imagers' sensitivities as well as providing phase information necessary for 3D imaging or RADAR-like imaging. In fact, the design of THz sources expands the application space beyond imaging. Short range communications could be made possible with on-off keying as a potential modulation technique. Communication can be seen as that with a THz carrier or that of an increased communication bandwidth. THz communication could also be exploited for security verification in communication systems where THz source/detector modules are used as hand-shake security confirmation to start other RF or mm-wave systems. Spatial, frequency, and polarisation diversity are examples of what THz short range and secure communication could employ,

Imaging results were shown with their relevant applications such security screening, safety inspection, agricultural and pharmaceutical imaging, as well as quality control. To present a futuristic insight regarding wide angle THz imaging, modular THz imagers were presented. These are comprised of THz sources and detectors with their corresponding optics, and are designed to be stacked back to back to enlarge the imaging area.

Terahertz system design in CMOS and Bi-CMOS technologies is starting to develop into its feasibility. Scaling of the technologies is steadily promoted, and more is yet to come in terms of new concepts and ideas as well as optimisation of the current solutions. Investigations of THz circuits on flexible electronics may follow and camera chips that include multi-spectral detectors including visible, infra-red and Terahertz sensors are other ideas of expanding the application space.

This collective worldwide effort may bring about technologies that could address new questions in Science, and provide pathways to novel concepts, postulations and fundamentals.

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Author's Biography

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