

FABRICATION AND CHARACTERIZATION OF
NANOMETER SCALE ORGANIC ELECTRONIC
DEVICES:
APPLICATION TO FIELD-EFFECT TRANSISTORS

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To Marilú Cedeño.

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Abstract

This thesis deals with the fabrication and electrical characterization of organic electronic devices with critical dimensions down to the sub 100-nm scale. The applications include organic field-effect transistors (OFETs) as well as molecular devices where the interelectrode separation is defined by the thickness of a self-assembled molecular layer. Electrodes are prepared using several techniques such as shadow mask evaporation, photolithography, electron-beam lithography (EBL), nanoimprint lithography (NIL) and breakdown of nanowires by controlled electromigration, depending on the application and the range of interelectrode separation. In the case of OFETs, the channel length of the devices is in the range from 70 μm down to 50 nm. Dihexyl-quaterthiophene (DH4T) is used as active material and is deposited from solution by drop casting, spin coating and self-assembly.

In the case of OFETs, a different behavior was found when comparing results on devices produced by drop casting and spin coating. In particular with respect to the presence, or not, of a saturation region at high drain-source voltage. The output characteristics of almost all of the spin-coated devices presented saturation at high drain-source voltages while for all of the drop-cast devices the drain-source current did not saturate.

Non-saturating output characteristics at short channel lengths were initially interpreted as resulting from the overlap of the depletion regions next to the metal contacts. Nevertheless, the observation of this effect at long channel lengths for devices containing relatively thick organic semiconductor layers suggested that this is the result of the current flowing through the bulk of the organic semiconductor in addition to the current through the accumulation layer at the semiconductor-insulator interface.

In order to account for this effect, the model for the output characteristics of FETs in the gradual channel approximation was modified to take into account the contribution of the mobility of the bulk of the organic semiconductor to the total channel mobility. The proposed model also incorporates the metal-semiconductor contact resistance because at short channel lengths it becomes comparable to the channel resistance. This model satisfactorily fits the results for all the fabricated devices.

An increase in the field-effect mobility was expected for devices with channel lengths in the nanometer scale caused by the increase of material homogeneity and reduction of grain boundaries in the channel at this lengthscale. Nevertheless, the field-effect mobility was found to decrease with decreasing channel length. This decrease is not due to a contact resistance limitation, as suggested in the literature, but it is most probably the result of incomplete filling of the channels for short channel length devices.

Additionally, gate voltage modulation in molecular electronic devices, where the channel length is defined by the thickness of a self-assembled DH4T layer sandwiched between gold electrodes, is demonstrated.

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Chapter 1

Introduction

The main difference between organic and inorganic electronic semiconductors resides in the charge transport mechanisms, which are related to the different types of interactions between their building blocks and the degree of order of the resulting materials. Atoms in Si crystals are bound together by strong covalent bonds while organic semiconductor molecules are weakly linked by van der Waals interactions. In the case of single-crystal inorganic semiconductors, charge transport takes place in well-defined electronic bands. On the other hand, charge transport in polycrystalline or amorphous-organic semiconductors is the result of hopping between molecular localized states. Consequently, organic semiconductors exhibit lower carrier mobility ($\mu \ll 1\text{cm}^2\text{V}^{-1}\text{s}^{-1}$) compared to their single-crystal inorganic counterparts.

The advantages of organic materials over the inorganic ones are related to the ease of processing them due to their unique mechanical properties as well as their compatibility with low-cost fabrication techniques. Low-cost applications are possible thanks to the use of solution-based processes, such as spin coating or drop casting, which simplify the fabrication steps as well as to the possibility of large area coverage. Organic semiconductors are of continued scientific interest because of the possibility

to tailor their electronic, magnetic and optical properties as well as their application prospects in low-cost electronic devices.

The main purpose of this research is to study the variation of electrical transport properties on organic FETs with respect to electrode separation. An increase in mobility is expected when the electrode separation is reduced from the micrometer scale to the sub-100 nm region caused by a decrease in the number of scattering events at grain boundaries or due to the increase in material homogeneity. Dihexylquaterthiophene was chosen as the active material because it can be deposited from solution simplifying the fabrication steps. Nano-electrodes were fabricated using EBL as well as novel fabrication techniques like NIL. The fabricated FET devices are used as tools to study the field-effect mobility on organic semiconductors.

This thesis is organized as follows. In the present chapter, we will introduce organic semiconductors, organic field-effect transistors and molecular electronic devices. The physical mechanisms leading to the semiconducting properties of conjugated molecules and polymers are considered in the section related to organic semiconductors. Later we will review the working principle of organic field-effect transistors and the differences with respect to standard inorganic devices. Finally, the field of molecular electronics is addressed.

In Chapter 2, the experimental techniques for nanofabrication and characterization of organic electronic devices are treated. These techniques include EBL and NIL, as well as SEM and AFM. The limitations of the fabrication techniques to small-scale structures (below approximately 50 nm) are studied. The results of fabrication of electrodes for nanometer-scale field-effect transistor structures are given. Next,

the methods for the deposition of organic semiconductor are reviewed. The chapter concludes with the study of the fabrication methods for molecular electronic devices and the presentation of our results in this field.

In Chapter 3 we first describe the experimental setup used for the electrical characterization of the fabricated devices. Later, the main results of the electrical characterization of DH4T OFETs as well as self-assembled molecular layer devices are given.

In Chapter 4, the most frequently used models to explain the process of charge transport in organic semiconductors and their application to the case of OFETs are studied. Finally, a model to interpret the current-voltage characteristics of the solution-processed DH4T OFETs and to extract the electrical parameter of these devices is proposed.

The results are discussed in Chapter 5. In the case of results related to OFETs the attention is given to the morphology of the organic semiconductor layer, the measured current-voltage characteristics and the field-effect mobility. Finally, the observed modulation of the current in devices based on self-assembled DH4T layers is discussed. The conclusions are given in Chapter 6.

1.1 Organic Semiconductors

Research on organic semiconductors started in the 1970s and since then several devices such as LEDs and FETs have been fabricated using organic materials [73]. The advantages of organic materials over the inorganic ones are the ease of processing due

to their unique mechanical properties. They can be vacuum deposited at low temperatures, drop cast or spin coated from solution. Additionally, they can be patterned using low-cost fabrication techniques such as NIL and self-assembly.

The main difference between organic and inorganic semiconductors is that charge transport takes place in well-defined bands in the case of inorganic crystalline semiconductors, and as a stochastic process of hopping between localized states (in a molecule or few monomeric units) in organic materials. This gives rise to the low carrier mobility ($\mu \ll 1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) in organic semiconductors compared to their single crystal inorganic counterparts.

In this chapter we start by revisiting the concept of charge delocalization in π electronic systems. This is used later as the base for understanding the conduction mechanisms in conjugated polymers and short molecules.

Polymers are macromolecular chains formed by repeated units called monomers. Polymers are commonly known as flexible and electrically insulating materials. However, there exist relatively new types of materials known as *conjugated* polymers and molecules exhibiting semiconducting and conducting properties. Conductivity in polymers was discovered accidentally in trans-polyacetylene. Doping polyacetylene varies its conductivity in a range of up to nine orders of magnitude.

Polyethylene is a typical example of insulating polymer and is formed by chains of covalently bonded C atoms with a nearly tetrahedral coordination. The molecular flexibility and weak intermolecular interaction results in macroscopic samples with the common mechanic properties of plastics. The backbone on insulating polymers such as polyethylene is formed by saturated sp^3 hybridized sigma C-C bonds. The resulting

covalent bonds are strong and the electronic excitations from the bonding orbital to the antibonding orbital require a large amount of energy. Therefore, the energy gap is large and the material is transparent.

On the other hand, in conjugated polymers like polyacetylene the backbones are formed by sp^2 hybridized C atoms. As a result, three sigma-bonding orbitals ($2s$, $2p_x$ and $2p_y$) and a bonding $2p_z$ orbital are formed. Here the coordination of the carbon atoms is not four but three. Neighboring $2p_z$ orbitals can overlap along the backbone forming π bonds where electrons are delocalized. Conjugated polymers are large-band-gap semiconductors, with an energy gap typically in the range of 1-3 eV and therefore highly colored materials.

In the next section we will review the quantum mechanical description of the phenomenon of electron delocalization in π -electron system.

1.1.1 Electron Delocalization in π -Systems

A simple example to illustrate electron delocalization in a π -system is the benzene molecule (Ref. [35]). Benzene is a ring molecule with the H and C atoms lying on the same plane. The symmetry around each C atom is trigonal with respect to the C-H bond and the neighboring C atom. There is one p_z orbital per C atom containing one electron that is left over.

Due to the fact that all p_z orbitals are equivalent an electron can in principle be in any of them. According to the Linear Combination of Atomic Orbitals (LCAO) method, the wavefunction for the electron is given by the sum

$$\Psi = \sum_{i=1}^6 c_i \pi_i \tag{1.1}$$

where c_i and π_i are the coefficients and the p_z orbitals on each C respectively. Due to the six-fold symmetry of the molecule the following relation holds

$$\Psi_{\text{rotated}} = \exp(2im\pi_i/6)\Psi_{\text{unrotated}} \quad (1.2)$$

with $m = 0, 1, \dots, 5$. In this way, after a rotation of $\pi/6$ we have

$$\begin{aligned} \pi_2 &\rightarrow \pi_1, \pi_3 \rightarrow \pi_2, \dots, \pi_1 \rightarrow \pi_6 \\ c_1\pi_6 + c_2\pi_1 + \dots + c_6\pi_5 &= e^{2im\pi/6} (c_1\pi_1 + c_2\pi_2 + \dots + c_6\pi_6), \end{aligned} \quad (1.3)$$

Taking into account that the wavefunctions π_i are linearly independent, the solutions for the coefficients are given by

$$c_j = \exp(2\pi imj/6) \quad (1.4)$$

This result represents a wave for the π electrons. Therefore, there will be delocalized electrons able to move around the entire molecule in addition to the localized ones in the C-H and C-C bonds.

1.1.2 Conjugated Polymers

The term conjugated comes from the fact that the bond length is alternated between successive C atoms. This is a general result for one-dimensional metallic systems, which are unstable against deformation (doubling of the unit cell) and the appearance of an energy gap at the Fermi level as shown by Peierls. Figure 1.1 shows the bondlength alternation in trans-polyacetylene. Both configurations are degenerate.

At high dopant densities, spinless conduction is observed in most of the conjugated polymers. This fact cannot be understood in terms of the process of dopant-induced

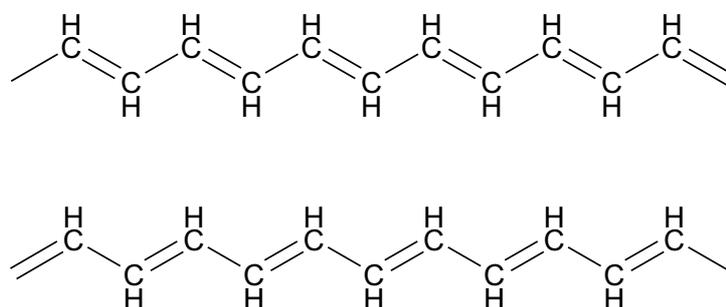


Figure 1.1: Alternation of single and double bond in trans-polyacetylene. This causes bond length alternation along the chain. Both configurations shown are isoenergetic (degenerate).

conductivity. Therefore, it is important to analyze the way charges are stored along the polymer backbone.

An oxidation process implies electron transfer from the π -system to the dopant agent. It is desirable then, to have a polymer with small ionization potential to ensure that transfer via oxidation can be easily achieved. In analogy to inorganic semiconductors, removing a charge from the π -system to a dopant would be equivalent to creating a hole in the valence band by transferring an electron to an acceptor level (See Figure 1.2). However, in the polymer, the positive charge carrier is not delocalized as in inorganic semiconductors. This charge localization comes together with a local structural rearrangement of the bonding configuration near the charge due to strong electron-phonon coupling in these quasi-one dimensional systems. Something analogous happens for the reduction process.

Some of the most common examples of conjugated polymers used in the fabrication of field-effect transistors are poly(2,5-thienylene vinylene) (PPV) and poly(3-hexylthiophene) (P3HT) and their chemical structures are given in Figure 1.3.

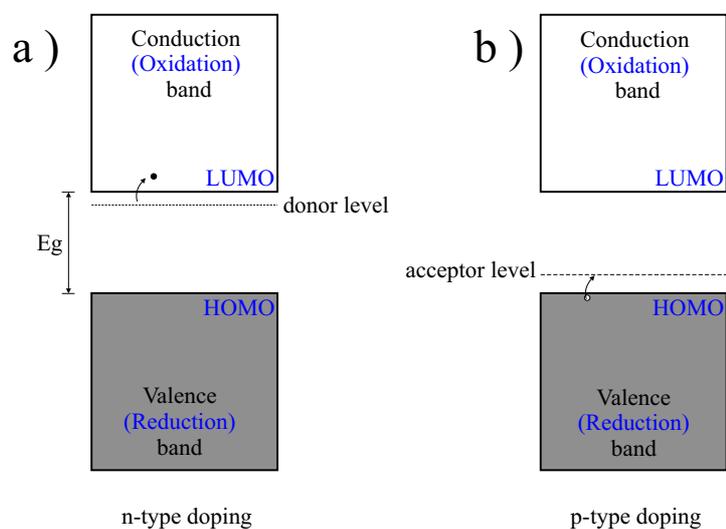


Figure 1.2: Energy band diagram for inorganic a) n-type a) p-type semiconductors. The terms in blue refer to the analogous in organic semiconductors. In inorganic crystalline semiconductors the bands represent delocalized charge carriers along the crystal. In the case of organic semiconductors the term “band” refers only to an energetic interval.

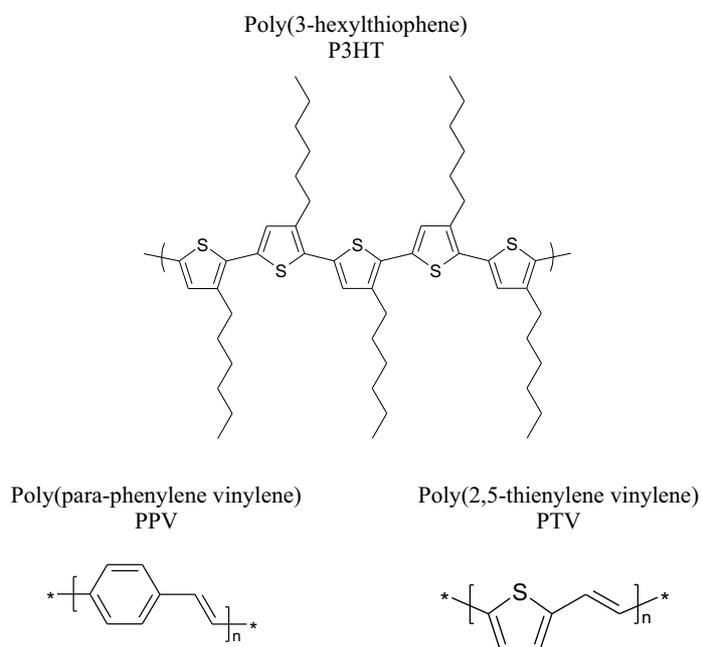


Figure 1.3: Chemical structure of poly(3-hexylthiophene) (P3HT) and poly(2,5-thienylene vinylene) (PTV), the most frequently used polymers for organic field-effect transistors; poly(2,5-thienylene vinylene) (PPV) used in organic light-emitting diodes is also shown

The different types of charged defects appearing in a polymer chain depend on the degeneracy or not of the ground state [66]. These charged defects will be treated in the following sections.

Polarons

Let us first analyze the doping process of a polymer with a non-degenerate ground state such as polythiophene. The process is illustrated in Figure 1.4. Upon chemical oxidation, an electron is removed from the π -system creating a free radical and a spinless positive charge or cation. A free radical means an unpaired electron with spin $1/2$. Radical and cation are coupled through the lattice distortion. The lattice distortion is associated with higher energy with respect to the rest of the backbone. Therefore, the extension of the distorted segment coupling these two entities is limited by energetic considerations. A *polaron* is defined as the combination of a charged site coupled to a free radical through a local lattice distortion. The existence of a polaron leads to the formation of localized states in the bandgap, where the lower energy states are occupied by single unpaired electrons.

Additional oxidation may either create an extra polaron in another part of the chain or remove an electron from the polaron. In the second case, the free radical of the polaron is removed and a dication is created. This spinless defect is called a *bipolaron*. Nevertheless, formation of a bipolaron is more energetically favorable such that two polarons on the same chain can combine to form a bipolaron.

Increasing the doping concentration, bipolaron bands arising from overlapping of

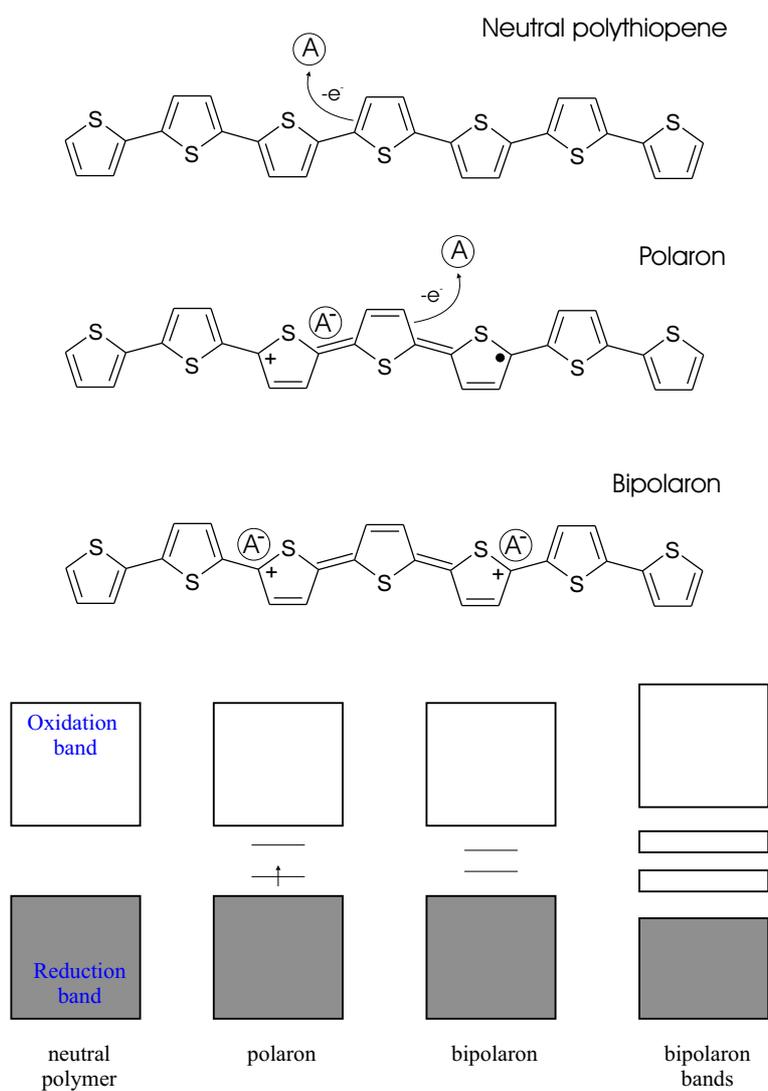


Figure 1.4: Oxidation of polythiophene. Polaron and bipolaron states are created in the process. For materials standing high doping levels, the possibility exists for the creation of bipolaron bands that may eventually merge the oxidation and reduction bands giving the possibility of metallic-like conduction. Adapted for polythiophene from Ref. [66]

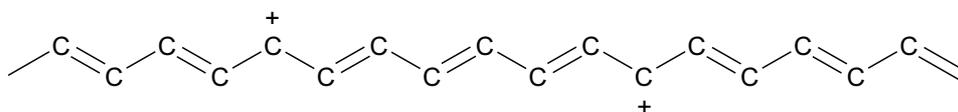


Figure 1.5: Two solitons in a trans-polyacetylene chain. Solitons create energy states in the middle of the bandgap. H atoms are not shown for clarity.

bipolaron levels at high doping densities may result. Even further, for polymers allowing high enough doping densities, this bipolaron bands have the chance to merge the valence and conduction band together in such a way to produce metallic-like conductivity.

Solitons

In the case of conjugated polymers with degenerate ground state such as trans-polyacetylene structural defects corresponding to interfaces between different configurations may appear. These defects are called *solitons* and because of the degenerate structure, the cations may move freely along the chain giving a possibility for charge transport (See Figure 1.5). Moreover, in the case of neutral systems they will carry spin because of the unpaired electron. On the other hand, injected charge may localize at such defects giving rise to a defect with charge but no spin. The presence of solitons results in the formation of energy levels in the middle of the gap. At high enough doping levels, the solitons will form a soliton band, which can eventually merge with the band edges.

Experimental evidence of the existence of these electronic states has been found in the results of optical spectra of thin films of conjugated polymers before and after doping. The spectra of the doped materials show electronic transitions with energies

lower than the bandgap. In addition, the number of low-energy optical transitions agrees with the predictions from theory, giving three transitions when polarons are present, two for bipolarons and one for solitons.

1.1.3 Short Molecules

In addition to polymers, several short molecules are considered as organic semiconductors when there exist energy levels for electron or holes that can be populated by thermal excitation of the order of kT provided by the environment. Additionally, a minimum level of intermolecular interaction is needed to permit local charge transfer to neighboring molecules. As a result, charge transport will occur as (i) hopping transport, or (ii) delocalized spreading out across several molecules depending on temperature and interaction strength (See Karl in Ref. [28]).

Molecules fulfilling these conditions are the ones containing carbon- $2p_z$ orbitals with a suitable intermolecular distance as in the case of conjugated polymers. Organic crystals and polycrystalline films of conjugated molecules can be formed depending on the deposition procedure. Induced charge carriers are localized along sections of the molecule or the whole molecule as in the case of conjugated polymers.

Three types of excited states can appear in organic crystals: (i) neutral excited states, (ii) ionic pair states and (iii) ionic single charge states. Excitations from ionic pairs involve charge transfer (CT) to neighboring molecules and the electron and hole are correlated due to Coulomb interaction. These states are called charge transfer states.

The chemical structures of the most frequently used semiconducting molecules for

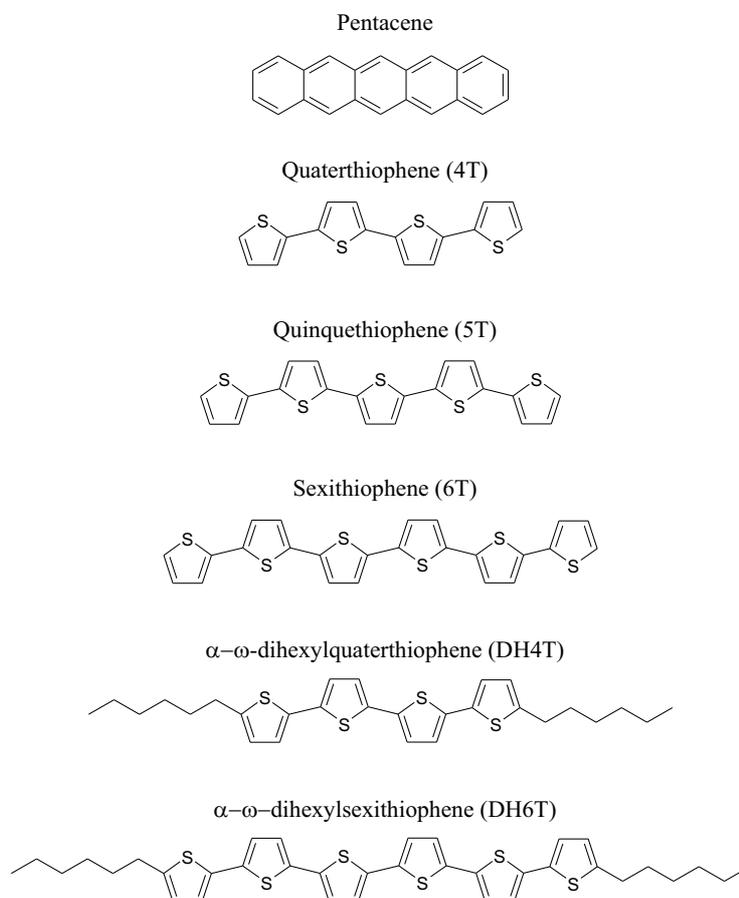


Figure 1.6: Chemical structure of the most frequently used molecules for the fabrication of organic field-effect transistors.

the fabrication of organic field-effect transistors are shown in Figure 1.6.

1.1.4 Transport in organic semiconductors

In this section we will first summarize the most important issues about organic semiconductors and their differences with respect to their inorganic counterparts. Later, we will give a qualitative explanation of the mechanisms of charge transport in organic semiconductors. A quantitative analysis of the models used to rationalize charge transport in organic semiconductors and the dependence of mobility on temperature and

electric field intensity is given in Chapter 4.

Organic semiconductors are constituted by molecules or polymers (macromolecules) containing π orbital systems that are rings of atoms (C, H, S) bound with alternating bond lengths. An additional condition is that the distance between neighboring π -orbital systems in the molecules is below certain threshold to guarantee the overlap of their wavefunctions.

Comparing organic and inorganic semiconductors we find out that one of the most important differences is the nature of their building blocks and the type of chemical bond that keeps them together. Molecules and polymers in organic semiconductors are bound together by means of weak van der Waals bonds that are orders of magnitude weaker than the covalent bonds of atoms in crystalline inorganic semiconductors. This difference results in orders of magnitude of difference in the mobilities of charge carriers.

In general, organic semiconductors are unintentionally doped because of the charge transfer processes under oxidation in ambient as well as because of the impurities remaining after the synthesis of the material. In the charge transfer process under oxidation shown in Figure 1.4, an electron is removed from the π system in such a way that a free radical and a positive charge (or cation) are created. Charge carriers in organic semiconductors are molecular polarons that consist in an electron or hole and the associated distortion of the position of the neighboring atoms in the molecule.

There are two limiting situations for the mechanisms of charge transport in organic semiconductors. First, for highly ordered molecular crystals and at low temperatures band-like conduction is observed. Band-like transport refers to transport across delocalized or extended energy states as for crystalline inorganic semiconductors. Due

to the weak intermolecular coupling, energy bands of molecular crystals are narrow and the mean free path of the carriers is of the order of the lattice constant at room temperature.

Second, in disordered materials the energy states are localized on the molecules or molecular segments of polymers separated by topological defects. In these systems, transport occurs by charge carrier hopping across localized states.

The intermediate situation is found in partially ordered organic semiconductors. Examples of these systems are films of organic semiconductors composed by a collection of grains or crystallites. Inside the grains and crystallites, the material is highly ordered but grain boundaries represent defects of the crystal structure and traps for charge carriers. For a system of these characteristics the Multiple Trapping and Release (MTR) model (Ref. [20]) is used to explain charge transport in organic semiconductors as an interaction of charge carriers moving along bands, inside grains, with localized levels that represent traps, along grain boundaries.

Hopping transport has been extensively studied. One of the most important examples is the work by Bäessler et al. (Ref. [5]) using Monte Carlo simulations. In a hopping system the energy states are localized on the molecules or molecular segments of polymers separated by topological defects. The organic semiconductor material is considered as an energetically disordered and positionally random system. These two types of disorder are correlated because the presence of positional disorder will induce energetic disorder via the potential energy of the interaction, which depends on the relative position of neighboring molecules. The origins of energetic disorder are the fluctuations in polarization energy and the distribution of molecular segments in

polymers.

The hopping rate is given by a factor that contains a wavefunction overlap factor and a Boltzmann factor for jumps upward in energy. The energy barrier is the difference in energy levels between the guest and the target molecules. These factors together are contained in the so-called Miller-Abraham factor. Therefore, the application of an electric field modifies the hopping transport reducing the average energy barrier for upward jumps in energy in the direction of the field. If the material contains a high density of traps the transport becomes dispersive, i.e. the velocity of a sheet of carriers injected at one electrode at a certain time will decrease as the packet traverses the sample. Both, experimental results and Monte Carlo simulations show an Arrhenius temperature dependence of the mobility ($u \propto \exp(-c/T^2)$).

1.2 Organic Electronic Devices

1.2.1 Introduction

Since the demonstration of field effect in an OFET made up of polyacetylene in 1983 many different materials such as conjugated polymers, oligomers and other molecules have been used and the mobilities have been increased by five orders or magnitude [73]. Fabrication of a variety of electronic devices based on organic semiconductors such as rectifiers, organic light emitting diodes (OLEDs) [8] and organic field-effect transistors (OFETs) [24] has been reported in the literature. Devices with increased complexity, such as active-matrix light-emitting displays (AMLEDs) and plastic transistors in active-matrix displays [44], have been demonstrated as well.

Organic field-effect transistors (OFETs), based on both oligomers and polymers, are subjects of research due to their application prospects in low-cost electronic devices. Low-cost applications are possible thanks to the use of solution-based processes that simplify the fabrication steps. Moreover, organic semiconductors are interesting because of the possibility to manipulate their electronic, magnetic and optical properties [29].

Several important advances in the field of OFETs have been reported recently including synthesis of new n-type thiophene derivatives [27], replacement of SiO₂ gate-insulating layers and metal contacts by polymers [36], fabrication of nanometer-channel-length OFETs by nanoimprint lithography (NIL) [3], and plastic transistors in active-matrix displays [44], among others. As far as electronic properties is concerned, Vissenberg and Matters [79] have deduced an analytical expression for the field-effect mobility in amorphous organic transistors which is based on a percolation model of hopping between localized states. This model was used successfully to fit the experimental temperature dependence of the field-effect mobility μ_{FE} of pentacene and polythienylene (PTV) OFETs.

In this section, we will introduce OLEDs and OFETs. The basic structure and operation of a standard FET will be reviewed before introducing OFETs. Additionally, the crucial aspect of electrical contacts to organic semiconductors will be addressed. Finally, molecular electronic devices will be considered.

1.2.2 Organic Light Emitting Diodes

OLEDs have unique properties that make them very attractive for new applications. For instance, the fabrication of cheap flexible displays based on OLEDs has been demonstrated [38]. Moreover, OLEDs are easily tunable using fluorescent dyes. These devices have already reached the level of industrial production.

Light emission is obtained from radiative recombination of electrons and holes. The physical processes involved in the operation of OLEDs are injection, transport, capture and radiative recombination of free carriers [8]. The key for the optimization of the yield of an OLED is to have high and nearly equal densities of carriers of opposite charge at the interface between the electroluminescent and the hole conductor layer. Considering this, some heterolayer devices have been fabricated.

The structure of the simplest heterolayer OLED is shown in Figure 1.7. It consists of an electroluminescent layer such as tris(8-hydroxyquinolato)aluminum (Alq_3) sandwiched between an electron injection layer (cathode) such as Mg/Ag and a hole injection layer (anode) like N,N'-di(naphthalene-1-yl)-N,N'-diphenyl-benzidine (NPB) for example. The NPB layer is deposited on an indium-tin oxide (ITO) layer on glass substrate. The Alq_3 layer, where electroluminescence takes place, can be doped with fluorescent dyes for color tuning and to increase the efficiency. The NPB layer is a hole conductor used to reduce the mismatch between the energy levels of the Alq layer and the ITO hole injector layer and to balance the number of injected carriers of opposite sign. In this way, the operating voltage of the OLED is also reduced.

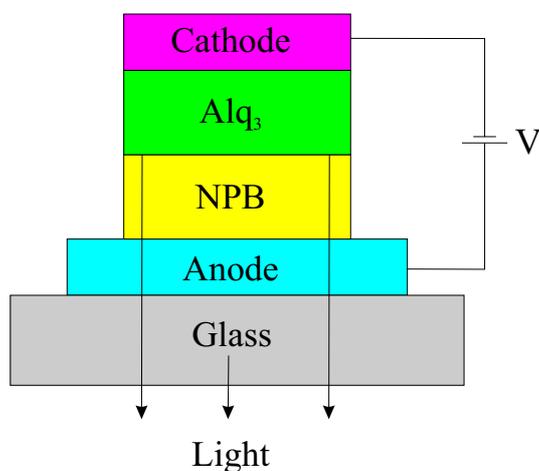


Figure 1.7: Schematic of a heterostructure OLED based on Alq₃ and NPB as hole conductor layer.

1.2.3 Field-Effect Transistors: Basic Structure and Operation

The basic structure of a FET is shown in Figure 1.8a. It consists of three electrodes called *source*, *drain* and *gate*. In the bottom contact configuration, source and drain are deposited on an insulating layer that covers the gate electrode. The most common example is the system composed of a thermally-oxidized layer grown on a highly doped Si substrate (SiO₂/Si). The gate electrode is contacted through the conducting part of the substrate. Next, a layer of a semiconducting material is deposited or grown on top. The region between the electrodes is called *channel*. The interfaces of the organic semiconductor and the gate, with the SiO₂ insulator, and below the channel, work as the plates of a capacitor. An alternative fabrication structure is the construction of source and drain on top of the semiconducting film/substrate depicted in Figure 1.8b. The performance of these two configurations is different especially in the case of organic FETs. A variant of the top contact transistor is achieved when the gate electrode is

evaporated on top of an insulating layer covering the channel as shown in Figure 1.8c.

Let us consider a p -type semiconductor, i.e. one for which the majority charge carriers are holes. Most of the organic semiconductors are p -type but the synthesis of several stable n -type semiconductors has been reported recently [27]. If a negative voltage is applied to the gate, with respect to the source, the generated electric field will cause charge carriers to accumulate in the channel region. When the gate voltage reaches certain value, the threshold voltage V_t , the channel starts to conduct because of the accumulation of free carriers. This is the so-called *accumulation mode*. Two regimes can be clearly distinguished in the accumulation mode. For low drain-source voltages (V_{ds}), the field created by the gate is uniformly distributed along the channel, giving rise to a uniform distribution of charge carriers. Consequently, the drain current is directly proportional to the applied drain voltage. This is known as the *linear regime*.

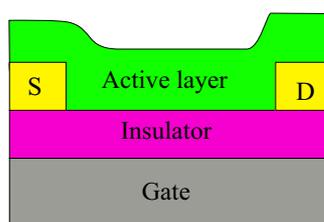
In general, in the region $0 < |V_{ds}| < |V_g - V_t|$, the drain-source current (I_{ds}) is given by the standard MOSFET equation [76]

$$I_{ds} = \frac{WC_i}{L} \mu \left(V_g - V_t - \frac{V_{ds}}{2} \right) V_{ds} , \quad (1.5)$$

where L is the channel length, W the channel width, C_i the capacitance per unit area of the insulating layer, and μ the field-effect mobility.

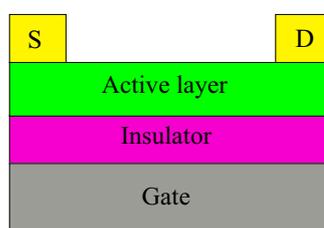
Increasing $|V_{ds}|$ above $|V_g - V_t|$ causes the electric field created by the gate at the drain contact to become zero. Therefore, there appears a depletion area in the channel around the drain contact. This phenomenon is called *pinch-off*. In this regime, called saturation regime, increasing of the drain voltage will not produce an increase of the

a) Bottom contacts



b, c) Top contacts

b)



c)

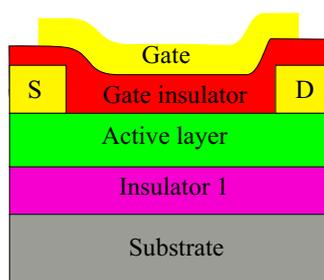


Figure 1.8: FET electrode configurations (a) Bottom contact and (b,c) top contact.

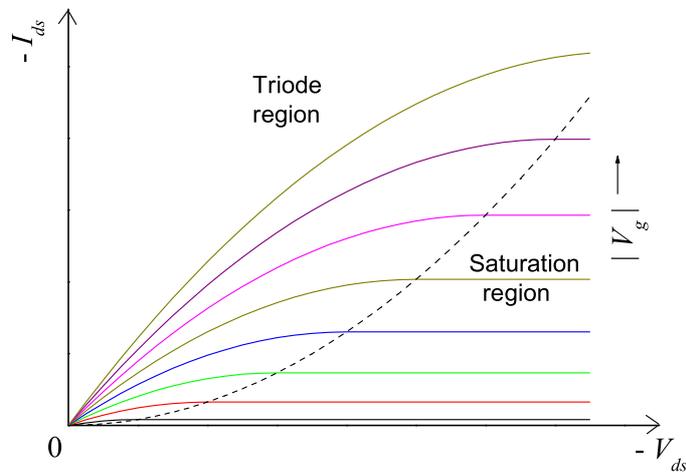


Figure 1.9: Output characteristics predicted by the standard MOSFET equations. The linear and saturation regions can be observed.

drain current. The saturation value of the current is given by

$$I_{ds} = \frac{WC_i}{2L} \mu (V_g - V_t)^2 . \quad (1.6)$$

For gate voltages (V_g) above the threshold voltage V_t , the charge carriers will be depleted from the channel and this becomes an insulator. This is known as the *depletion mode*. The *on-off ratio* is the ratio of the current in the accumulation mode over the current in the depletion mode I_{on}/I_{off} . Figure 1.9 shows the drain current as a function of drain voltage for different gate voltages as predicted by the standard MOSFET Equations 1.5 and 1.6.

Several organic FETs present the same type of current-voltage characteristics as the inorganic FETs. Therefore, many of the relations derived for inorganic FETs may be applicable to organic FETs as well. Nevertheless, care should be taken in the interpretation of the parameters because of the fundamental difference in conduction

Material	Deposition method	μ [cm ² V ⁻¹ s ⁻¹]	Ref.
PTV	s	0.002	[57]
P3HT	s	6×10^{-4}	[57]
pentacene	v	1.5	[50]
4T	v	0.025	[31]
5T	v	0.02	[58]
6T	v	0.03	[71]
DH4T	v	0.23	[48]
	s	0.012	[31]
	c	0.008	[11]
DH5T	v	0.10	[47]
DH6T	v	0.013	[23]
DFH-4T	v	0.048	[27]
DFH-5T	v	0.026	[27]
DFH-6T	v	0.001	[27]

Table 1.1: Field-effect mobility of the most commonly used organic semiconductors in OFET fabrication. In the deposition method column: *s* denotes spin coating, *c* drop casting and *v* vacuum evaporation. Also shown some new n-type organic semiconductors DFH-*n*T (perfluorohexyl-substituted *n*-thiophenes [27]).

mechanisms of these two kinds of semiconductors.

1.2.4 Organic Field-Effect Transistors

The chemical structure of some of the most frequently used organic semiconductors in the fabrication of OFETs is shown in Figure 1.3 for polymers and Figure 1.6 for short molecules and their mobilities are given in Table 1.1.

The degree of order of the active organic layer is crucial for device performance and

it can generally vary from highly ordered polycrystalline films, when thermal evaporation is used, to amorphous films when solution processes are employed. Solution-processed organic semiconductors can be spin coated or cast. In the case of oligomers an additional improvement of the molecular order has been achieved by grafting alkyl substituents to the terminal alpha sites of the molecules. This modification has proven to lead to self-organization of the molecules on the film due to molecular recognition [34, 31]. Remarkably, this approach leads to highly polycrystalline films even in the case of solution-processed films [31].

Highly-ordered films of pentacene have achieved mobilities comparable to that of amorphous Silicon (of the order of $10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$). Nevertheless, OFETs cannot compete with single-crystal inorganic semiconductors, which have mobilities three orders of magnitude higher, in high-speed applications [24]. However, OFETs can compete in novel applications thanks to their unique mechanical properties and their ease of processing. Research in OFETs is mainly concerned with the increase of the field-effect mobility.

Energy band structure

Although the band picture is valid only for crystalline systems (with translational symmetry), it is also a very important representation for the understanding of the working principle of FETs based on disordered organic semiconductors. In the case of OFETs the conduction and valence bands are replaced by the lowest unoccupied and highest occupied molecular orbitals of the organic semiconductor respectively. Figure 1.10 shows the energy band structure of an OFET based on a p-type organic semiconductor. The

cross-section of a device is shown in a) where the metal-semiconductor-metal (MSM) junction along A-A' and the metal-insulator-semiconductor (MIS) junction along B-B' are indicated. Figure 1.10b) represents the band structure of the device seen along AA', as example the values of gold and pentacene are used. Gold is chosen because its work function is similar to the energy of the HOMO of most of the p-type organic semiconductors leading to the formation of ohmic contacts. In the case a small energy barrier would exists between the contacts and the semiconductor, the application of a negative voltage to the gate will lower this energy barrier. Figures 1.10c), d) and e) show the band structure along the metal-insulator-semiconductor (MIS) junction for different values of applied voltage (Ref. [39]). Figure 1.10c) represent the situation when no voltage is applied to the gate in the ideal case (neglecting the small flat-band voltage). If a negative voltage is applied to the metal, as shown in d), the bands will bend upwards and the energy of the HOMO level will move closer to the Fermi level and an accumulation of positive charge carriers (holes) will form at the semiconductor-insulator interface. When a positive voltage is applied to the metal, the opposite band bending occurs causing a depletion of majority carriers (holes) to occur at the semiconductor-insulator interface as shown in Figure 1.10e). Contrary to the case of Si MOSFETs where an inversion regime is reached under the increase of the gate voltage, in (p-type) OFETs no inversion is reached because of the high energy barrier for electron injection at the metal-semiconductor contacts. An additional discussion of the nature of the metal-semiconductor contacts is given in Section 1.2.5.

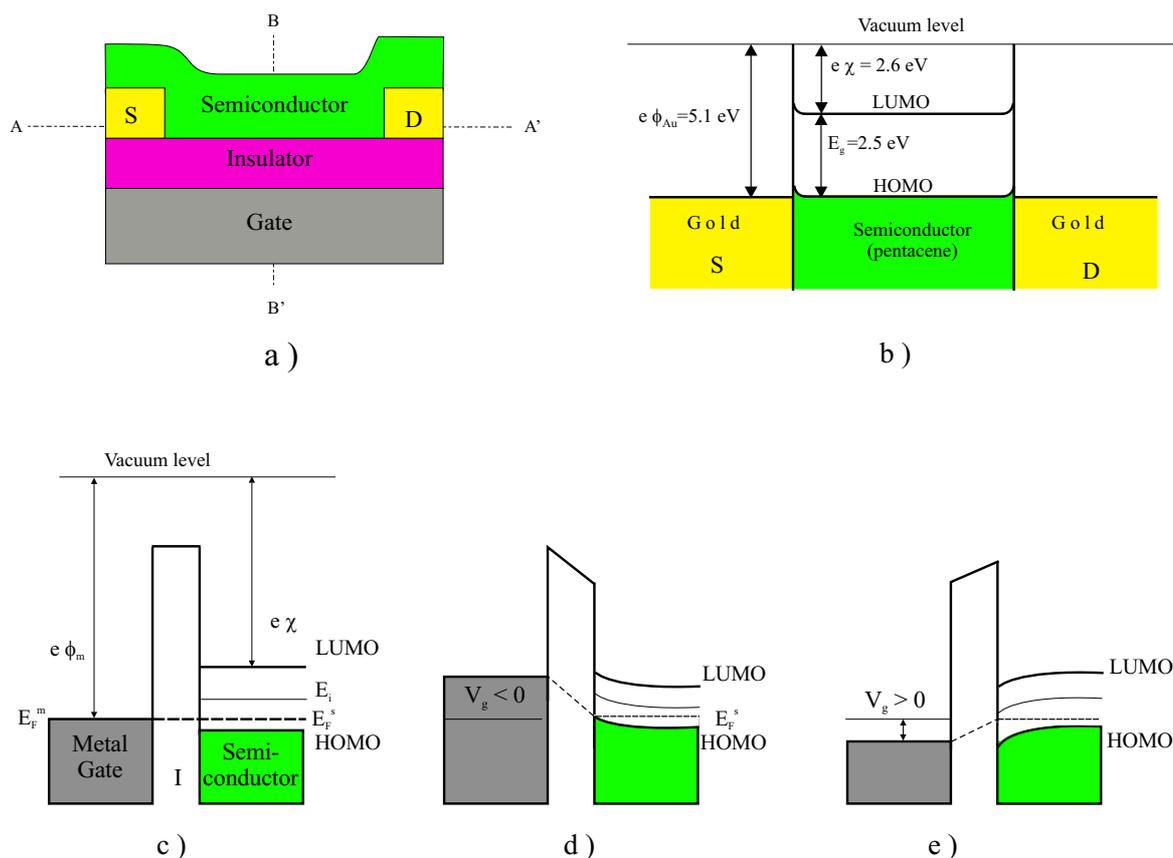


Figure 1.10: Energy band structure in organic field-effect transistors. a) Device structure showing the metal-semiconductor-metal (MSM) junction along A-A' and metal-insulator-semiconductor (MIS) junction along B-B'. Band structure for the MSM a) and MIS junctions c), d), e). The values of gold and pentacene are used in b). The band structures for different values of gate voltage are shown: c) zero gate voltage, d) negative gate voltage and e) positive gate voltage. Inversion is not reached in OFETs because the metal-organic semiconductor contacts are non ohmic for electron injection.

Device operation

The basic operation of an organic FET is described in the works of Brown et al. in Ref. [7] and Horowitz in Ref. [39, 41] the following explanation is based on these works. The device structure is shown in Figure 1.11a and consists of a highly doped silicon substrate with an insulating oxide layer grown on the surface. Source and drain gold electrodes separated a distance L of each other, defining a channel of width W , are deposited on top of the oxide layer. Finally, an organic semiconductor layer, assumed to be p-type, is deposited on top. One of these electrodes is called source while the other drain. The third electrode is the highly doped silicon substrate and is called gate. The materials mentioned here are the most commonly used in practice. However, other materials can be used as substrates, insulators and for electrode fabrication. The term thin-film-transistors (TFT) emphasizes the idea of the fabrication procedure and was used originally with amorphous silicon [76]. OFETs usually have the same structure than TFTs.

Let us consider first the case when all terminals are connected to ground, as shown in Figure 1.11b. The positive charges resulting from doping of the organic semiconductor and their associated positive counter ions, produced by charge transfer doping, are uniformly distributed on the film. Next, a small negative voltage applied to the gate as shown in Figure 1.11c. The negative voltage will induce the formation of an accumulation layer of positive charges at the semiconductor next to the insulator-semiconductor interface. These positive charges are supplied by the source and drain ohmic contacts. In this way, the opposite interfaces of the insulator behave as capacitor plates. In

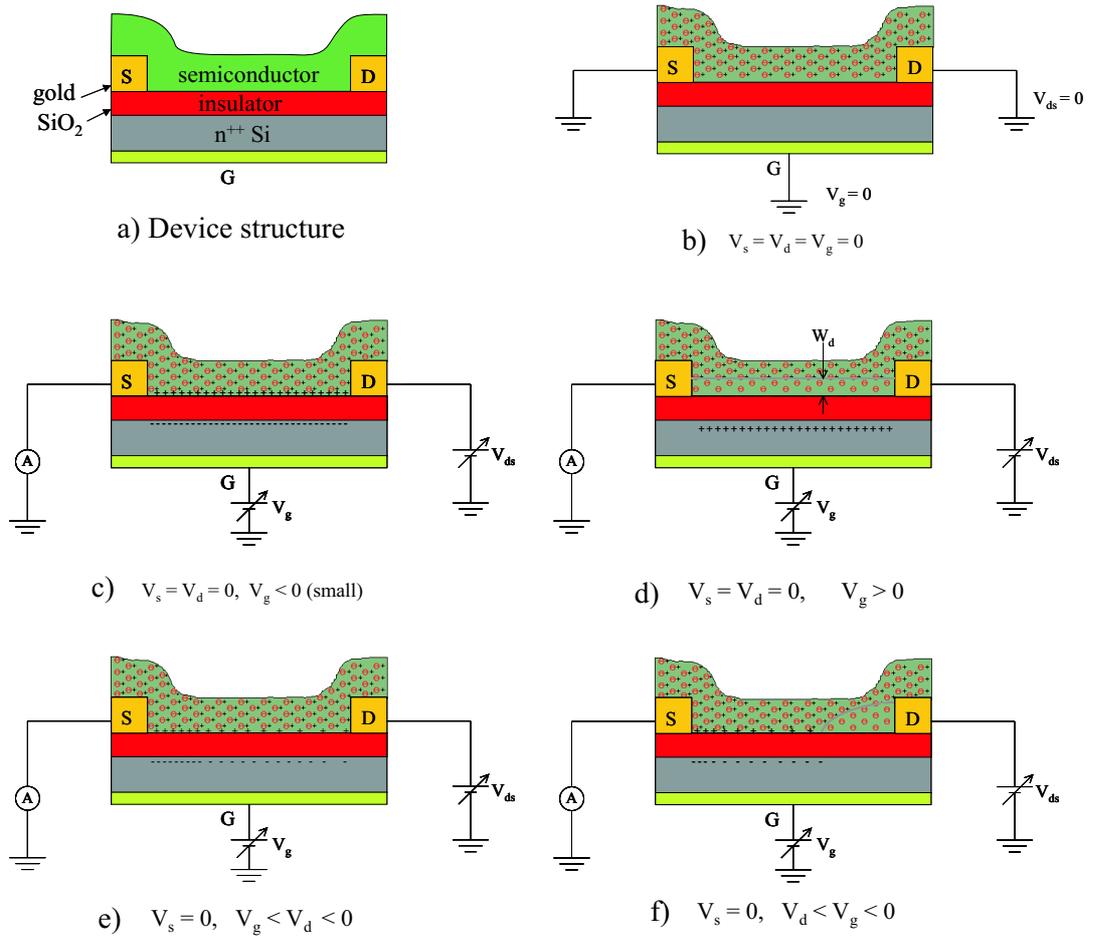


Figure 1.11: Principle of operation of an OFET. a) Device structure, b) all electrodes connected to ground, c) small negative voltage applied to the gate, d) positive gate voltage, e) $V_g < V_d < 0$ and f) $V_d < V_g < 0$ (Adapted from Ref. [7]).

this case it can be easily demonstrated that the mobility of the semiconductor layer (different from the field-effect mobility) is given by the following expression

$$\mu = \left(\frac{L}{WC_i V_{ds}} \right) \frac{\partial I_{ds}}{\partial V_g} \Big|_{V_{ds} \rightarrow 0} \quad (1.7)$$

Conversely, application of a positive voltage to the gate will produce a depletion region next to the insulator-semiconductor interface as shown in Figure 1.11d. The thickness of the depletion layer (W_{depl}) is modulated by the gate voltage according to [76]:

$$W_{\text{depl}} = \frac{\epsilon_0 \epsilon_{\text{semi}}}{C_i} \left[\sqrt{1 + \frac{2C_i^2 (V_g - V_{so})}{qN_A \epsilon_0 \epsilon_{\text{semi}}}} - 1 \right], \quad (1.8)$$

where ϵ_{semi} and N_A are the dielectric constant and the dopant (acceptor) concentration of the organic semiconductor and V_{so} is the switch on voltage of the device.

Next, let us consider the case when a negative voltage is applied to the drain and gate in such a way that $V_g < V_d < 0$ as shown in Figure 1.11e. In this case too, an accumulation layer of positive charge carriers will form but with a non uniform distribution, the charge density being higher close to the source electrode. If the drain voltage is increased in absolute value such that $V_d < V_g < 0$ as shown in Figure 1.11f, a depletion region will appear next to the drain contact. The voltage at the end of the depletion region remains constant causing saturation of the device current. Later, it will become clear that only under certain conditions this model describes accurately the behavior of OFETs.

Additional differences in the properties and the related parameters of OFETs with respect to inorganic FETs will be discussed in the remaining part of this section. As mentioned earlier, standard MOSFET equations [76] are commonly used to interpret

data from OFETs and to extract device parameters such as field-effect mobility. However, at least two important differences between these two types of devices should be taken into account:

- Generally, metal-semiconductor contacts are ohmic in OFETs while in the case of MOSFETs the contacts behave as Schottky diodes.
- OFETs lack a depletion layer to insulate contacts and conducting channel from the substrate, as in MOSFETs.

These two points imply that a finite conduction at zero gate voltage is observed in OFETs while for MOSFETs the channel forms only after a minimum gate voltage equal to the threshold voltage is applied. Therefore, the threshold voltage, in principle, should be zero for OFETs.

The concept of “threshold voltage” in organic field-effect transistors has been discussed by Horowitz in Ref. [41]. In analogy to amorphous silicon TFTs, where the presence of a threshold voltage has been associated to a gate-bias dependent mobility, it is suggested that if the mobility is considered as constant a threshold voltage cannot be defined. Instead, a model was developed in which the bulk conductance is considered [41]. The resulting relationship resembles the standard equation under certain conditions but where V_t is substituted by a zero voltage V_0 . In general, V_0 accounts for the flat-band potential, fixed charges in the insulator and the conductivity of the bulk.

Other authors [57] suggest that a more meaningful parameter to describe disordered organic field-effect transistors is the *switch-on* voltage. This in turn is defined in terms

of the *flat-band potential* which is the work function difference between the semiconductor and the gate. The *switch-on* voltage is then defined as the flat band potential, i.e. the voltage at which there is no band bending in the semiconductor [57]. For gate voltages below the switch on voltage, the drain-source current remains constant while for higher voltages I_{ds} starts to increase.

Finally, doping in organic semiconductors is an issue that deserves some attention because in generally it occurs unintentionally. Chemical methods to synthesize organic semiconductors do not allow high purity materials to be prepared efficiently as for the inorganic counterparts. For instance, DH4T the material used in this thesis, was obtained from Syncom with a purity of 94%. Therefore, doping is the result of impurities originating from chemical synthesis of the material and oxygen doping.

The dopant concentration in the active layer of organic field-effect transistors can be determined following the procedure developed by Meijer et al. in Ref. [55]. The method is based in measuring the pinch-off voltage and a model for the depletion-layer width which contains the dopant concentration as a parameter (Equation 1.8).

Due to the ohmic character of the source-drain contacts in OFETs, relatively low bulk mobilities are required in order to ensure low off-currents and high on-off ratios which are desirable in practical applications. A crossover from field-effect dominated (for $V_g < 0$) to bulk-dominated current (for $V_g > 0$) in the transfer characteristics of spin-coated poly(2,5-thienylene vinylene) (PPV) and poly(3-hexylthiophene) (P3HT) FETs was demonstrated by Meijer et al. [55]. Under certain conditions, the output characteristics of OFETs may lack a saturation region at high drain voltages caused

when the bulk of the organic semiconductor offers an alternative current channel comparable to the saturation region. The bulk mobility needs to be taken into account for low mobility materials since it can modify drastically the response of the devices even for $V_g < 0$ in p-type OFETs.

New types of OFETs devices have been demonstrated. One example is ambipolar FETs. Dodabalapur et al. [25] have reported the fabrication of a bipolar FET consisting of an organic heterostructure. Their device exhibits both n- and/or p-channel operation depending on the bias conditions. Additionally, X. Chen et al. [15] have fabricated FETs with a gate-modulated electrochemical doping based on amorphous polymers, showing ambipolar operation and high current output.

1.2.5 Electrical Contacts

Important issues in the fabrication and operation of OFETs are the type and configuration of the electrodes. Matching the material properties of the electrodes to those of the organic semiconductors will permit to obtain improved device performance. Configuration of the electrodes on the other hand will influence the electric field distribution and channel formation.

In this section, we review the physical models used to describe metals-semiconductor junctions. Moreover, from an equivalent circuit approach, we study some ways to extract or account for the series contact resistance. Additionally, the influence of the top and bottom contact configurations on the performance of organic devices is treated.

The fabrication techniques for nanometer-size metal electrodes will be treated in Chapter 2.

Models for Charge Injection in Metal-Semiconductor Contacts

The nature of the metals-semiconductor contacts is of crucial importance for device fabrication either using them as rectifiers or as ohmic contacts. Metal-semiconductor contacts were studied extensively by Rhoderic in Ref. [65].

Mott and Schottky proposed the first models to explain rectification in metal semiconductor junctions. Both were based on the idea that electrons passed through the barrier by the drift-diffusion processes. The difference between these models is that in the former the barrier region does not contain impurities as assumed for the later. As a consequence the electric field is constant and the electrostatic potential linearly increasing along the barrier region in Mott's model. On the other hand, the Schottky model assumes a linearly increasing electric field and a quadratic electrostatic potential through the barrier. In the diffusion model the current density through the junction is given by

$$J = eN_C\mu E_{\max} \exp\left(-\frac{e\varphi_b}{kT}\right) \left[\exp\left(\frac{eV}{kT}\right) - 1\right] \quad (1.9)$$

where $E_{\max} = 2kTa^2w/e$. An additional model developed by Bethe assumes that the actual process limiting conduction is the charge emission from the semiconductor to the metal. In the thermionic emission model of Bethe, the current density is expressed as

$$J = AT^2 \exp\left(-\frac{e\varphi_b}{kT}\right) \left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \quad (1.10)$$

where A is the Richardson constant and n is the ideality factor.

The process of formation of Schottky contacts is portrayed in Figure 1.12. Figure 1.12a shows the energy diagram of metal and semiconductor when they are separated. φ_m and φ_s are the *work functions* of the metal and semiconductor respectively, measured from the vacuum level. χ_s is the *electron affinity* of the semiconductor. An n-type semiconductor is considered and $\varphi_s < \varphi_m$ is assumed. The Fermi levels of metal and semiconductor will coincide when connected through an ideal wire as shown in Figure 1.12b. An electric field will appear as a result of induced surface charges on the metal and semiconductor surfaces. A thin layer of the order of 0.5 \AA accumulating extra conduction electrons on the metal will form. On the other hand, for the n-type semiconductor, a layer depleted of electrons, with positive charges and with thickness w will form. As a consequence, the bands in the semiconductor bend upwards as shown in Figure 1.12b. A difference of potential $V_i = E_i d$, will appear between metal and semiconductor. Here d is the separation and E_i the induced field in the gap. When the metal and semiconductor are put close together, V_i tends to zero as shown in Figure 1.12c. In most of the cases there is a thin interfacial layer that the carriers need to tunnel. An ideal metal-semiconductor contact is obtained when metal and semiconductor are put in contact (Figure 1.12d) because the barrier due to vacuum vanishes. The barrier height φ_b in the Mott limit is given by

$$\varphi_b = \varphi_m - \chi_s \quad (1.11)$$

Let us consider now the rectification process in a Schottky barrier which is illustrated in Figure 1.13. Assuming an n-type semiconductor in contact with a metal. Figure 1.13a shows the initial Schottky barrier when no voltage is applied. In this

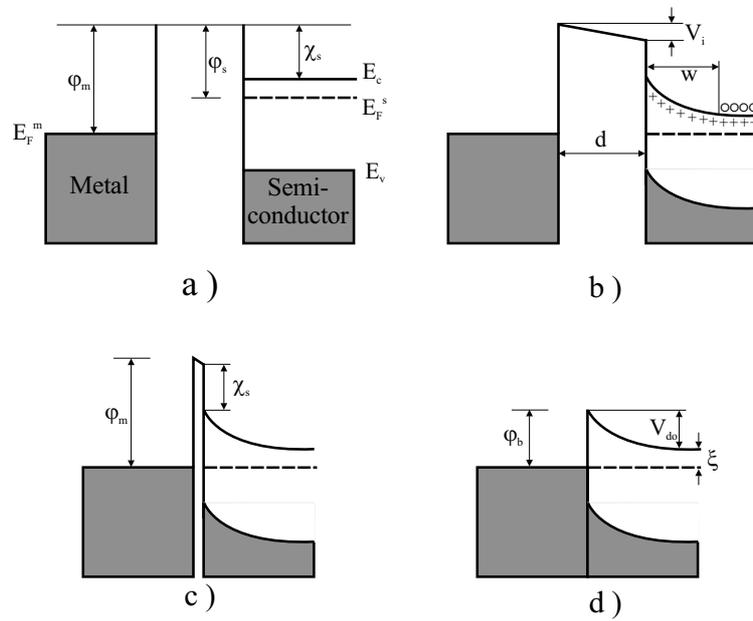


Figure 1.12: Formation of a Schottky barrier. a) Energy diagram of independent metal and semiconductor. b) Electrical connection of metal and semiconductor through an ideal wire. c) Metal and semiconductor are put close to each other. d) Close contact. Adapted from Ref [65].

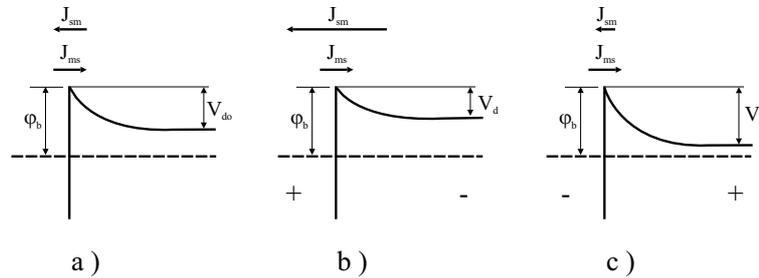


Figure 1.13: Rectification process. a) Zero bias. b) Forward and c) reverse bias. Adapted from Ref [65].

case the current flowing from the semiconductor to the metal and the opposite one will be equal and no net current will cross the barrier. When a negative voltage is applied to the semiconductor with respect to the metal (Figure 1.13b), the bands in the semiconductor are raised in energy and the electric field in the barrier is reduced. As a consequence, more electrons coming from the semiconductor will be able to cross the barrier and there will be a net electronic current from the metal to the semiconductor. When the polarity of the applied bias is reversed, the semiconductor will have a negative potential with respect to the metal and therefore the energy bands will be lowered in energy as shown in Figure 1.13c. In this case, the energy barrier of electrons coming from the metal will be increased and the current in this direction will be reduced. When the magnitude of the voltage is increased the current saturates at a value independent of the applied voltage but it is negligible in comparison to the previous case.

In addition to rectifying contacts, ohmic contacts may be formed. A contact is called *ohmic* when its resistance is low enough for the current to be determined by the bulk of the semiconductor rather than by the contact properties. Depending on the

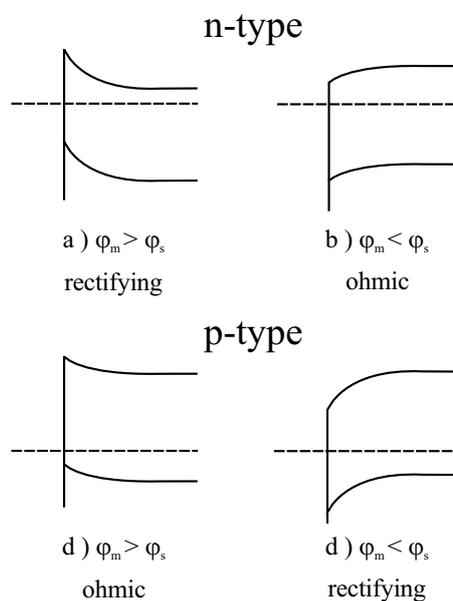


Figure 1.14: Nature of the resulting metal-semiconductor contacts for different semiconductor types and work function relations between metal and semiconductor. Adapted from Ref [65].

semiconductor type and the relation between φ_m and φ_s , different types of contacts can be obtained. Figure 1.14 shows the nature, rectifying or ohmic, of the resulting metal-semiconductor contact.

Ohmic contacts are required for device fabrication in order for the contacts not to affect the current voltage characteristics of the device. As mentioned above, most of the stable organic semiconductors used for OFET fabrication are p-type. Then high work function metals are required for the fabrication of ohmic contacts.

Contact Resistance

Calculation methods to extract OFET parameters such as the field-effect mobility, which include the effects of a contact resistance have been proposed by Horowitz et

al. [43] and Meijer et al. [56]. These methods do not consider the bulk resistance because they were proposed for devices with a negligible contribution from the bulk conductance to the device current. Both methods require measurement of the transfer characteristics in addition to the output characteristics.

Horowitz's method [43] is based on the low-voltage approximation of Equation 1.5 for I_{ds} where the quadratic term in V_{ds} is neglected. However, the voltage drop across the contact resistance is taken into account by substituting V_d by $(V_d - I_d R_s)$. Horowitz's method [43] is valid in the range of low V_{ds} and requires R_s to be voltage independent. This condition is valid for devices of channel lengths in the order of 50 μm . In this method, the drain conductance g_d and the transconductance g_m are calculated. The mobility μ can be calculated with the help of the following expression

$$\frac{g_d}{\sqrt{g_m}} \sqrt{\frac{L}{W} \frac{V_d}{C_i}} = \sqrt{\mu(V_g - V_0)} , \quad (1.12)$$

by derivation with respect to V_g with the additional assumption that μ is a slowly varying function of V_g .

On the other hand, Meijer's procedure [56] needs the output and transfer characteristics be measured for a set of similar devices based on the same semiconductor with varying L . This method assumes that the field-effect mobility is independent of channel length and that the contact resistance is the same for all devices. Therefore, the channel resistance is assumed to depend on channel length while the contact resistance to remain constant. Finally, the contact resistance was calculated from the extrapolation of a plot of the total resistance of the devices as a function of channel length at $L = 0$. The scaling behavior of the mobility shows that the contact resistance limits the

performance of the devices [56] and higher mobilities at short channel lengths cannot be attained. The limitations of this method are that several devices, assumed to have the same contact resistance, are required. This is difficult to ensure when working with organic semiconductors due to the random arrangement of the material with respect to the electrodes. Additionally, the requirement that all devices should have the same channel width may result impractical for short channel lengths. Our results concerning the channel length dependence of mobility will be given in Section 5.4.

In Section 4.3, a method to extract the contact resistance from measurements made on a single device and requiring only the output characteristics is proposed. The implicit assumption is that μ remains constant in the range of the applied V_{ds} . This method considers the quadratic term in Equation 1.5 at expense of having a non-linear equation that is solved numerically.

Surface Area Limitation

The effect of the surface area of the metal-semiconductor contacts was demonstrated on transistors based on single grains of Sexithiophene (6T) in Ref. [17]. In that work gold electrodes of different sizes were used and a reduction of the drain-source current was found when the smallest surface area electrode corresponded to the source injecting electrode. For the analysis, the metal-6T contacts were considered as Schottky diodes connected back to back. It was found that the drain-source current was limited by the reverse-biased, hole injecting source contact. The hole injection mechanism was best described in those devices by a drift-diffusion process with a field dependent mobility. The contact area was determined from AFM measurements and the normalized device

current for both configurations coincided.

In principle, the metal-semiconductor contact resistance is expected to decrease with increasing contact area but this will depend on the contact configuration that will be treated next.

Influence of the Contact Configuration

As was shown in Figure 1.8 there exist two possible configurations for the contacts in a TFT. The bottom contact configuration is the most commonly employed because the electrodes can be fabricated using established techniques such as photolithography and electron-beam lithography (EBL) as well as alternative lithography techniques such as NIL and micro-contact printing (μ CP). Nevertheless, bottom-contact devices are associated with lower mobilities compared to top-contact ones, explained as a consequence of the formation of trap-infested regions around the contacts in devices based on evaporated organic semiconductors [24].

For the top-contact electrode configuration the contacts lie on top of the evaporated film. Which in principle is free of defects because it is evaporated on a flat surface. Nevertheless, for the bottom contact configuration, the organic material is deposited on top of a patterned substrate and its morphology will be altered with respect to the flat film. Under the last conditions a region containing defects is formed around the electrodes. The defects in the channel and close to the electrodes constitute traps for charge carriers. Traps have been found responsible for both the low apparent mobility and the gate voltage dependence of the mobility found for pentacene FET with the bottom contact configuration in [70].

An alternative explanation for lower mobilities in bottom-contact devices is their smaller effective contact area compared to top-contact devices [75]. In the case of bottom contacts the metal thickness and the channel width determine the effective contact area while for top-contact devices it is given by the source contact area. An additional disadvantage of bottom-contact electrodes is their fabrication. It usually requires the deposition of thin layers of Ti or Ni to improve the adhesion of gold on the SiO₂ substrate. Ti and Ni have poor charge injection properties and are located close to the semiconductor-insulator interface where good carrier injection is necessary.

In general top contact devices exhibit higher mobilities as compared to bottom contact ones. Top contacts are usually deposited using shadow masks. Unfortunately, in order to scale down the device dimensions, the use of the shadow mask technique becomes somewhat complicated. For instance, sub-micron stencil membranes are fragile considering the configurations and filling factors required in the fabrication of nano-electrodes for OFETs. Other lithographic techniques to fabricate top contacts for organic-based devices are usually incompatible since the resist deposition and subsequent steps such as UV or electron-beam irradiation, high temperature and pressure and immersion in organic solvents, will probably cause damage to the active layer.

Therefore, bottom-contact electrodes are the best choice for downscaling device dimensions.

1.2.6 Nanometer Channel Length Devices

Several authors [73, 24] have suggested decreasing the channel length to the size of the electronic domains to reduce scattering at grain boundaries or even to the size of

the molecule in order to have intramolecular conduction. This is expected from the well known fact that the mobility in a single conjugated chain can have values of $1000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ or more.

Following this idea Schön [69] reported the fabrication of molecular scale transistors using a self assembled monolayers. This paper has been retracted and several groups are working to produce a device of similar characteristics. In Section 1.2.7 we give an introduction to molecular electronic devices.

α -T6 FETs with channel lengths varying between 500 and 30 nm were reported by Collet et al. [18]. They divided their results into two groups according to channel length. First, for channel lengths above 200 nm the output characteristics were of the usual way for OFETs. The calculated mobility values for these devices were in the range of the reported in the literature. Second, for channel lengths below 200 nm and down to 30 nm, the output characteristics did not correspond to the usual OFET characteristics because the current increased with drain voltage following a power law.

These results were ascribed to Fowler-Nordheim tunnel conduction between source and drain. In this process, the drain-source current is controlled by the gate-voltage modulated barrier at the interface source-organic semiconductor rather than by the field-induced charge layer at the insulator semiconductor interface. The reason for this is that below 200 nm the lateral electric field is too high and the energy barrier for holes at the α -6T/Au too low for the normal process of accumulation to take place.

Recently, Zhang et al. [81] reported the fabrication of pentacene FETs with $L = 30 \text{ nm}$ (single gap electrodes). The extracted mobility was in the same order of magnitude of the obtained for polycrystalline devices with $L = 20 \text{ }\mu\text{m}$. As opposed to

the results of Collet et al., no short channel effects were found for those devices. In other words, the current-voltage characteristics for the 30 nm channel length devices agree with the standard equations for FETs (Ref. [76]). As mentioned above, Meijer et al. [56] proposed that short channel devices are normally limited by the contact resistance. Therefore, these results were probably possible thanks to the improvement of the charge injecting properties of the metal-semiconductor junction. The contact resistance in these short channel length devices was reduced using Pt instead of Au because of its higher work function as well as by burying the Ti adhesion layer using a CF_4 plasma. They find no short channel effects as is the case for our $L < 200$ nm devices.

1.2.7 Molecular Electronic Devices

In order to keep the miniaturization trend of the semiconductor industry, soon it will be required that the electronic active elements should have molecular dimensions. In principle, molecular electronics deals with electronic devices fabricated using molecular materials. A more general definition of molecular electronics includes devices characterized by having active components with molecular dimensions, devices for which charge transport takes place along few molecular units of organic semiconductor, and monomolecular devices. Towards the realization of a monomolecular electronics several experiments have been reported, including molecular wires, molecular rectifiers, and switches [45]. The main obstacle is that currently there exist no reliable techniques to address single molecules. Several ways of contacting single molecules, or a small quantity of them, have been reported in the literature and will be reviewed in Section 2.7.

These approaches can be divided into two categories regarding the kind of contacts that are used. The techniques using adjustable contacts are based either on scanning probes or break junctions. On the other hand contacting of molecules can be carried out using fixed contacts for which molecules are trapped on prefabricated contacts or depositing metal contacts on a SAM.

1.3 Summary

In summary, conjugated polymers are generally semiconducting because of the instability of linear metals against deformation and opening of a bandgap ($E_g \gtrsim 1.5$ eV) at the Fermi level (Peierls instability). This is usually reflected as length and single-double bond alternation. The extension of the delocalization of charge along the backbone only reaches several conjugated units. Charged defects coupled to lattice distortion or associated to domain walls may appear under the presence of dopant agents. The extra charges created on conjugated polymers by oxidation or reduction lead to localized electronic states within the bandgap. Therefore, charge carriers are essentially localized. Something similar occurs for short molecules.

Organic semiconductors, as their inorganic counterparts, can be used for the fabrication of devices such as FETs and LEDs. There are some applications where the use of organic semiconductors is so attractive that they have passed from a scientific curiosity to industrial production. This is the case of OLEDs. The structure of an OLED consists of an electroluminescent layer sandwiched between an electron injection layer and a hole injection layer. Light emission is the result of radiative recombination

of electrons and holes. In addition to their interesting properties, such as mechanical flexibility and chemical tunability of their electroluminescent properties, low-cost production is possible thanks to the use of solution processes and large-area coverage.

Organic field-effect transistors (OFETs) are three-terminal devices in which the current flowing between two of them, called source and drain, can be controlled by a voltage applied to the gate. These devices use an organic semiconductor layer as active material filling the channel between source and drain. Under certain conditions the standard MOSFET equations for inorganic devices predict the form of the current-voltage characteristics.

Some deviations of this model arise mainly due to the difference in the nature of the metal-semiconductor contacts. In the case of standard MOSFETs the metal-semiconductor junctions are of the Schottky type while for OFETs they are better described as ohmic contacts. These differences are reflected in the definition of threshold voltage and in the role of the bulk of the organic semiconductor as a conduction channel for the device current.

The device performance is determined mainly by the magnitude of its field-effect mobility. A strategy to increase the mobility, and thereby the switching speed of devices, relies on decreasing the channel length down to the nanometer range.

The most important similarities and differences between organic and inorganic semiconductors and devices based on them are summarized in Table 1.2.

Devices with dimensions down to the molecular level will be needed soon if the current trend in miniaturization of the active elements of electronic circuits is to be kept. Several methods to contact single molecules as well as various electronic devices

Property	Organic		Inorganic Crystalline
	Crystalline	Disordered	
Building blocks/ type of bonds	(macro)molecules/ van der Waals		Atoms/ covalent
Charge carriers	Polarons		Electrons, holes
Energy states	Delocalized	Localized in molec. or molecular units	Delocalized
Energy structure/ transport mechan.	Bands	Molecular orbitals/ hopping	Bands
Thermal behavior	T. activated		T. limited by phonon scattering
Mobility [cm ² V ⁻¹ s ⁻¹]	~ 10 ³ at low T	≲ 1	1000
Metal-Semicond. contacts in FETs	Ohmic for holes (electrons) in p-type (n-type) semiconductors		Non-ohmic (back-to- back Schottky diodes)
FET operating regimes	Accumulation, no inversion		Accumulation, inversion

Table 1.2: Summary of the main similarities and differences between the properties of organic and inorganic semiconductors and field-effect transistors.

based on self-assembled monolayers have been reported in the literature. For a review see Ref. [82, 45].

Therefore, in this thesis we take up the challenge to design, fabricate and characterize organic FETs with critical dimensions ranging from the micrometer down to the nanometer level. Furthermore, the study of the influence of the channel dimensions and the morphology of the organic semiconductor on the transport properties of the devices is an important part of this work.

Chapter 2

Fabrication and Microscopic Characterization of Organic NanoFETs

2.1 Introduction

The aim of this thesis is the fabrication and characterization of nanometer scale organic FETs. The structure of a FET was described in Section 1.2.3 and the crucial step in the fabrication process is the definition of source and drain electrodes with nanometer separation. Multiple interdigitated source and drain electrodes were used in order to reduce the size of the channels. In this way, it is ensured that the deposited organic material filling the channels is as homogeneous as possible while keeping a reasonable output current level for the devices. The most reliable and versatile method to fabricate nanodevices is with the combination of EBL and the planar process.

The planar process consists in patterning a polymer layer deposited on a substrate, known as *resist*, using some kind of irradiation as UV light or electron beam. Next, using a chemical step of development, some cavities are carved into the resist on the irradiated regions leaving the unexposed areas on the substrate. The resist can be used

as a mask for different kinds of processes such as metallization and lift-off, etching and implantation. From the mentioned variants of the planar processes we used in this work metallization and lift-off. In addition to EBL there are other alternative techniques, such as NIL, which are also capable of nanometer resolution.

In the first three sections of this chapter we will study the techniques for the fabrication of the source and drain interdigitated electrodes with dimensions in the nanometer region. First, the nanofabrication techniques of electron-beam lithography (EBL) and nanoimprint lithography (NIL) for patterning of polymers with nanostructures will be introduced. Second, the metal lift-off process to transfer the nanostructured films into metallic structures will be explained.

Several characterization techniques employed to check and extract the parameters of the fabricated nanostructures are studied here. These techniques are related to the characterization of the morphology and the dimensions of the structures. SEM and AFM are used for morphology studies like size and roughness of the electrodes and of the organic layer. The performance of the finished devices (FETs) is studied by electrical characterization and this will be treated in Chapter 3.

The main deposition techniques used in the fabrication of organic semiconductor devices and the morphology of the resulting films are studied in this chapter. The techniques covered in this section are thermal evaporation and solution process. Additionally, the influence of the surface treatment of the substrate on the properties of the deposited films is treated.

Finally, fabrication of molecular electronic devices is considered. First, several

methods for fabrication of molecular electronic devices that have appeared in the literature are reviewed. Second, our experimental results in this field are presented.

2.2 Electron-Beam Lithography

Since we are concerned with the study of transport properties in organic semiconductors along characteristic lengths of the order 100 nm or below, the most practical and versatile way to fabricate nanoelectrodes with a separation in such range is EBL. Minimum feature sizes of 3 nm after lift-off have been reported using this technique [9]. EBL has a much higher resolution than photolithography because the electron wavelength is negligible compared to light wavelengths (at typical energies used in lithography). Consequently, diffraction does not play a limiting role as in photolithography. For instance, the spot size of the electron beam in the S FEG microscope used in this work has typical dimensions below 4 nm using an accelerating voltage of 30 kV. Another technique that offers the same resolution as EBL is NIL. Nevertheless, NIL requires a stamp that is usually fabricated by EBL. After the lithography steps we are left with a patterned resist which is used as a mask for metal deposition and lift-off.

Electron-beam lithography is based in the definition of patterns on a resist by means of modification of the resist solubility by electron-beam exposure. The electron beam breaks the exposed polymer chains in smaller fragments. Shorter polymer fragments of PMMA have higher solubility than longer ones. Long polymer chains are usually entangled. There is a critical number of monomers units below which polymers do not entangle. Later, when the sample is immersed in a developer solution molecules in the

exposed areas flow away leaving cavities in the resist layer. This is the *positive* resist mode. The initial molecular weight is preferable to be high for high resolution. For high enough electron energies the exposed polymer chains cross link with each other making the polymer less soluble. In this case the exposed parts will remain, i.e. we have the *negative* resist mode.

A typical EBL system is very similar to a SEM, in fact the system used along this work is composed of an electron microscope Philips XL30 S FEG and a Raith ELPHY-Plus attachment. In general, the electron gun is formed by a filament, an anode and a wehnelt. EBL machines can have a Gaussian beam or a shaped. Gaussian beam is advisable when high throughput is needed while shaped one is the choice for high resolution machines. The XL30 S FEG works with a shaped beam. During exposure the electron beam is scanned across the sample surface in order to irradiate the resist in desired areas only. Consequently, a deflecting system as well as a blanking system are needed.

W. Chen [14] produced 5 nm lines and concluded that the resolution limit of EBL is around 4 nm. Due to the high energy of the electron beam (80 keV) and to the high quality of the electron lenses of the state of the art equipment, the beam diameter can usually reach diameters below 1 nm. For accelerating voltages of around 80 kV the back-scattered electrons from the substrate do not play a role because their dose exposure is below the threshold. The real limit for resolution is given by the size of the PMMA fragments after exposure and to the intermolecular forces during development. Nevertheless our system operates at a maximum accelerating voltage of 30 kV for which proximity effect of backscattered electrons from the substrate causes low contrast

exposure limiting the resolution to ~ 40 nm.

2.2.1 Exposure

During exposure the resist is irradiated with an electron beam on selected regions according to a predefined pattern. In addition to chemical changes on the polymer, the electron beam causes the polymer chains to break down reducing in this way the local average molecular weight (MW) of the resist. It is known that the solubility of PMMA in organic solvents increases when the molecular length is below certain entanglement threshold, above which the PMMA molecules entangle.

The design of the structures was done using a Raith ELPHY Plus system. The format of the layout was GDSII and designs written in ASC format can also be loaded. The computer sends the design to the pattern generator, which in turn controls the deflection of the electron beam in the microscope column. The relevant parameters for exposure, that are related to the microscope, are *acceleration voltage*, *spot size*, and *write field size*. The beam current is defined both by the accelerating voltage and the spot size of the beam. For the pattern generator the parameters are *step size* and *dwell time* which in combination with the beam current define the dose of the exposure.

Exposure can be performed in three ways: (i) area exposure, adequate for relatively big structures, (ii) exposure with single pixel lines and (iii) single dot exposure. A sample coated with a film of resist is loaded in the microscope chamber. The resist surface is focused and the free working distance is adjusted to be equal to the one that was used for write-field size calibration, typically 5 mm. Later, the beam is blanked and the stage is moved to the position where the structure is going to be written.

2.2.2 Proximity Effect

Proximity effect is the degradation of the pattern during exposure due to scattering of electrons [62]. For the electron system used in this work, the diameter of the electron beam on the sample surface is 0.4 nm for spot size 1 and an accelerating voltage of 20 kV. Nevertheless, the scattering of electrons in resist and substrate, and secondary electrons can cause the extension of the exposed resist to be larger than intended. There is forward scattering of electrons on their path through the resist and backscattering from the substrate.

The scattered and secondary electrons expose unwanted parts of the resist that are partly removed during development. This effect becomes more prominent when there are features close together. Increasing the accelerating voltage (electron energy) and reducing the thickness of the resist as well as the substrate reduces proximity effects.

For instance, proximity effect is not a limiting factor in the fabrication of gratings with dimensions around 10 nm when using accelerating voltages of around 80 kV or above and standard PMMA-coated Si substrates. The reason is that at this energy, forward scattering is minimal and secondary electrons are generated from deeper regions of the substrate. On the other hand, for a 30 kV electron system proximity effects limit the minimum linewidth of metal lines to 20 nm.

For general structure designs there exist several algorithms to calculate the proximity effect correction for the dose distribution in order to minimize the proximity effect distortion. On the other hand, in the case of periodic structures it is easier to determine the dose value experimentally by exposing with variable dose and later choosing

the value that gives the best results. It is shown in the next part of this section how proximity effect plays a role in the fabrication of gratings. First, the period of the gratings is changed and the filling factor (line width/period) is kept constant at 50 %. Secondly, the period is constant and dose and line thickness are varied.

Relation dose-period for 50 % filling factor

Here we summarize experimental results about the fabrication of periodic metal lines (gratings) with a line thickness equal to the spacing. The lines were produced by electron-beam lithography and Cr lift-off. The electron-beam resist was PMMA 950 K MW and 200 K MW. Si and thermally-oxidized Si were used as substrates. The necessary dose decreases with decreasing period as expected. The results are shown in Figure 2.1. The relation dose-period can be adjusted to a linear function in the region under study.

We found out that only 90 % of the dose is necessary to produce the same structures when using thermally-oxidized Si compared to Si when using the same type of polymer. Additionally, different resist sensitivities were evident when comparing the doses for 200 K and 950 K MW PMMA. 200 K MW PMMA being approximately 1.3 times more sensitive than 950 K.

Line thickness variation with dose for constant period

The results in this section show the fabrication of periodic arrays of lines with a given periodicity and variable dose. A variable dose produces variable line thickness. Electron-beam lithography and Cr lift-off were used as fabrication techniques. The

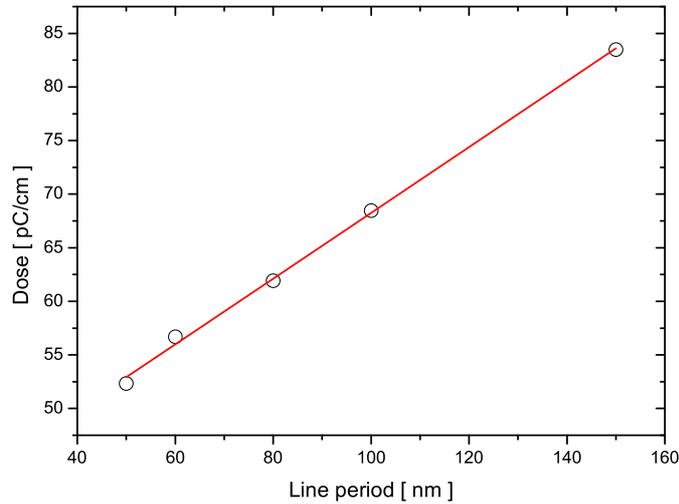


Figure 2.1: Electron-beam irradiation dose necessary to write lines as a function of line period for a filling factor of 50% on PMMA 950 K MW.

electron-beam resist was PMMA of 950 K MW on a thermally-oxidized Si substrate.

The accelerating voltage was 30 kV and the spot size was 4. The design consisted of an array of lines with 300 nm period. The increase in line thickness with increasing dose is shown in Figure 2.2. Another manifestation of the proximity effect was that the tendency of the width to increase with dose did not hold at the borders of the line array (for dose 444 and 457 $\mu\text{C}/\text{cm}$). Line thicknesses were extracted from SEM images.

2.2.3 Development

All EBL experiments in this work were performed using poly(methyl methacrylate) (PMMA) with different molecular weights as electron-beam resist. PMMA is a positive resist for moderate exposure dose, which means that the exposed regions are removed

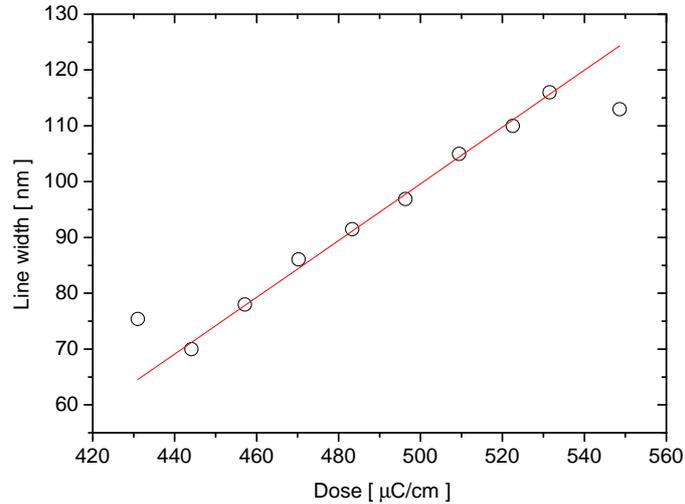


Figure 2.2: Line width obtained as a function of electron-beam dose for 300 nm period on a film of PMMA 950 K MW.

during development. The electron beam breaks the exposed polymer chains decreasing the molecular weight and increasing the solubility of PMMA. Short polymer chains do not entangle which is favorable for dissolution during development. For higher doses the electron beam produces cross-linking of the polymer chains and a decrease in solubility.

In order to develop exposed samples of PMMA, a solution of methyl isobutyl ketone : isopropanol (MIBK:IPA) in the proportion 3:1 was used. Samples are dipped into the solution at room temperature for 30 s after which they are rinsed in isopropanol and dried with Nitrogen gas. In our experiments, samples were stirred while immersed in the developer solution.

The minimum feature size attainable with EBL is below 10 nm. 7-5 nm lines after lift-off have been demonstrated in Refs. [14] and [9] but these lines were not continuous.

W. Chen suggested that intermolecular forces and resist swelling define the limits of resolution of EBL [13, 14]. Chen proposed a new development procedure in order to minimize the influence of these limiting factors. The key issues in the new process are the use of ultrasonic agitation and short development times. Ultrasonic agitation is important to provide the exposed molecules with extra energy necessary to escape from an attractive potential created by the neighboring unexposed molecules. Faster development times can be achieved using faster developer solutions and ultrasonic agitation. The reduction of the immersion time will reduce significantly the degree of swelling of the polymer, which could prevent nanometer size lines to be opened in the resist.

As was mentioned before, the system used in this work has a maximum accelerating voltage of 30 kV that makes it possible to fabricate metal lines down to 20 nm. Nevertheless, lines in this range are not exempt of failures. The minimum line width and line spacing that can be made reproducibly with the system described is 50 nm. The incorporation of ultrasonic agitation at this scale does not improve the results because the potential energy barrier for the molecules to be dissolved decreases with increasing line width [13].

In general it is difficult to make good SEM images of the patterned polymer due to charging effects and in some cases due to melting. For this reason a thin metal layer is usually deposited on top of the film to facilitate inspection with the electron beam. An alternative way consists in scanning the beam relatively fast after adjusting it in a neighboring area. This method was used to make the SEM image of Figure 2.3. The figure shows a 950 K PMMA film on Si after exposure and development. The

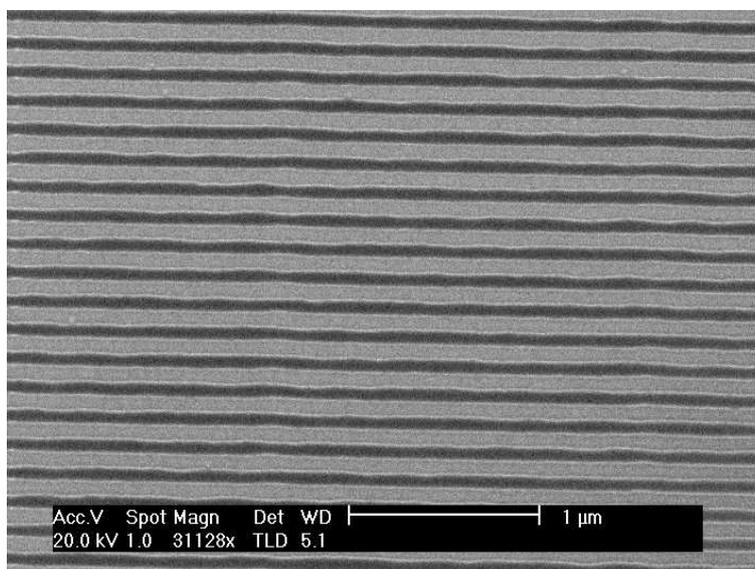


Figure 2.3: SEM image of a 950 K PMMA film on Si after exposure and development of 150 nm -period lines.

periodicity of the lines was 150 nm.

2.2.4 Bilayer Resist

In order to improve the lift-off process a bilayer resist can be used. The idea to use a bilayer resist is to produce an under etch on the resist in order to eliminate the contact between the metal layer and the resist on the substrate. This is possible thanks to the use of PMMA of different molecular weights and electron beam sensitivities. Consequently, under the same exposure conditions the cavity opened on the bottom layer is smaller than the one on the top layer. In this way, the roughness of PMMA does not affect the shape of the lines. The resist is then composed of a stack of two layers of PMMA with different molecular weight where the less sensitive resist on top as shown in Figure 2.4. Preparation of bilayer resists was performed as follows. The

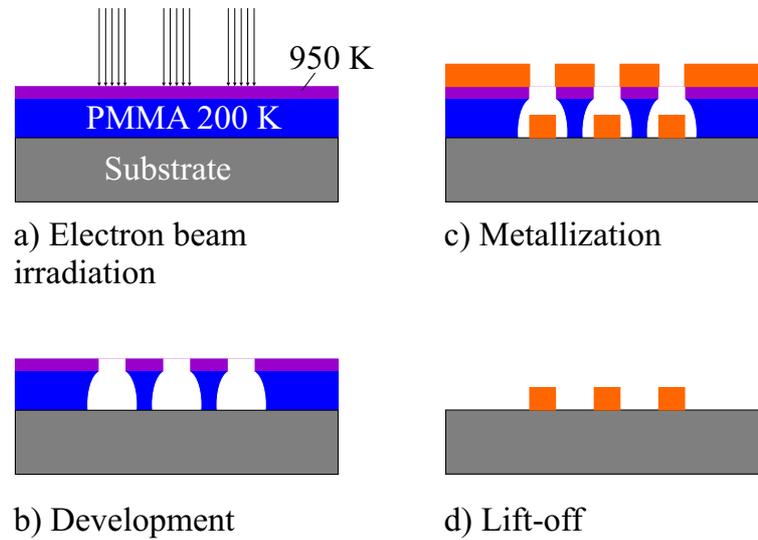


Figure 2.4: Schematics of the EBL process using a bilayer PMMA resist.

first layer of higher molecular weight PMMA is spin-coated and the sample is backed for 15 min. at 125 °C. Then, the second layer is spin-coated on top and the sample is backed again.

SEM images of interdigitated electrodes fabricated using EBL on bilayer resists on a thermally-oxidized Si substrate and Ti/Au lift-off are shown in Section 2.4.2, Figure 2.10 for electrode separation down to ~ 100 nm and in Section 2.4.3, Figure 2.14 for separation down to 50 nm.

2.3 Nanoimprint Lithography

Highly sophisticated optical lithography is the current industrial fabrication technique but it has an estimated resolution limit of 70 nm. EBL is the fabrication technique for structures with feature sizes down to approximately 1 nm (at 80 kV) [62], but it is a sequential technique limited by its low throughput. This technique is used for the

fabrication of masks for UV and X-ray lithography.

Permanent miniaturization of electronic devices and the search for low-cost processes are the driving forces for the invention of new fabrication techniques such as nanoimprint lithography (NIL). NIL is a fabrication technique with potential for sub 10 nm resolution [16] possessing high throughput due to its parallel nature. NIL is part of the group of emerging imprint-based lithography techniques [67], where we can also find mold assisted lithography, and microcontact printing. Furthermore, NIL presents several advantages for the fabrication of nanometer scale organic electronic devices [10].

In this section we describe the process of nanoimprint lithography. After the introduction to the method, the key issues in stamp fabrication are considered. Next, some details of the imprinting step are given and finally removal of the residual layer is discussed.

2.3.1 Process

The NIL process is illustrated in Figure 2.5. A sample, a stamp, and a press are needed. The sample can be any flat substrate such as Si, thermally-oxidized Si or glass coated with a thin polymer film (typically PMMA). The stamp is another substrate with a patterned face containing the structures we wish to replicate. The patterns can be made up of the same material as the substrate or can be made up of metal.

Sample and stamp are put together and are then heated from room temperature T_0 to T_1 , the heating temperature. From this moment, the temperature is kept constant during an interval ΔT_1 and a pressure p is applied. As a next step, sample and stamp are cooled down until the separation temperature T_2 and the pressure is kept constant.

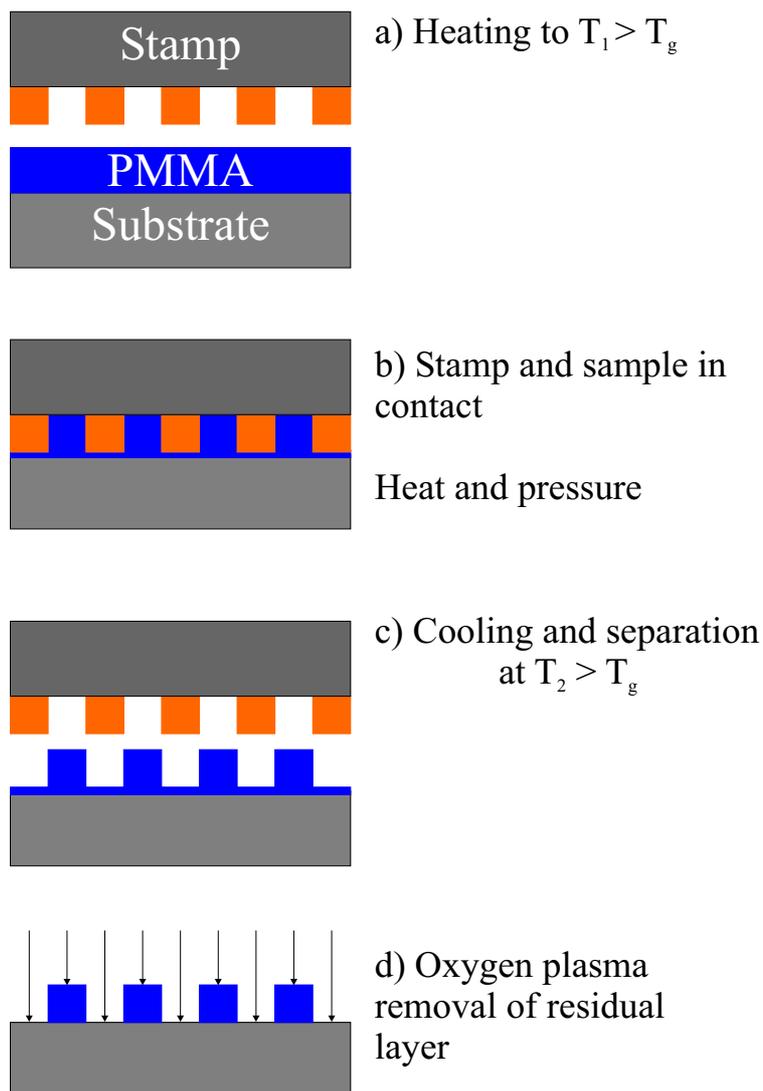


Figure 2.5: NIL process. Typical values for PMMA are $T_1 = 185\text{ }^\circ\text{C}$, $T_2 = 95\text{ }^\circ\text{C}$, and $p = 30\text{ bar}$.

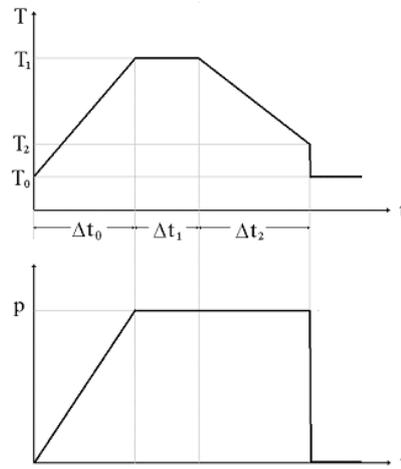


Figure 2.6: Time diagram of temperature and pressure during NIL.

Cooling takes place during a time interval ΔT_2 . Figure 2.6 shows a time diagram of temperature and pressure during the process.

2.3.2 Stamp Fabrication

In practice, the resolution of NIL is given by the minimum feature size of the stamp features. High resolution stamps are made either by EBL and dry etching, or using metal lift-off. The stamps described in this thesis were produced by metal lift-off.

In view of the device applications, substrates for the imprinted polymers are made up of thermally-oxidized Si wafers (electrically insulating layer). Consequently, Silicon was used as substrate because its surface energy is higher than that of SiO_2 preventing the polymer to stick to the stamp during stamp-imprint separation. Additionally, proximity effects during EBL are less important than in SiO_2 . The metal roughness resulting from the granularity of the deposited metal is a limitation for the smallest stamp features (See Section 2.4.1).

Parameter	Value
T_1	185 °C
T_2	95 °C
p	30 bar
Δt_1	60 s
Δt_2	160 s

Table 2.1: NIL parameters

High-aspect-ratio features are necessary to get the required metal line thickness for the transferred structures needed for device applications. Nevertheless, it is difficult to achieve this for sub-micrometer linewidths using EBL on a single layer resist. Better results were obtained using a bilayer electron-beam resist (Section 2.2.4).

The overall stamp size was usually 2×2 cm². EBL process was treated in Section 2.2 and metal lift-off will be covered in Section 2.4.

2.3.3 Imprinting

This section deals with the issues concerning the process of imprinting using a metal/Si stamp on a PMMA film spun on a thermally-oxidized Si substrate. Imprinting was performed using an Obducat press (model NIL-2-OB-1) with the parameters given in Table 2.1.

Polymer flow during imprinting has been studied in Ref. [33, 67]. It has been observed that the molecular weight of the polymer and the rate of application of temperature and pressure influence strongly the flow during imprinting. This is caused by the change on polymer viscosity over several orders of magnitude around T_g [77].

A common problem of NIL is polymer sticking to the stamp after imprint-stamp

separation. The use of several types of anti-sticking layers has been reported [67]. Even though sticking during replication of nanometer sized structures is less important, anti-sticking lead to better results.

Figure 2.7 shows SEM micrographs of a) electron-beam written stamp after Au and Ti lift-off containing interdigitated electrodes. The interdigitated region is 4 μm long and the channel length is approximately 90 nm and b) part of the imprinted 950 K molecular weight PMMA.

2.3.4 Residual Layer Removal

After imprinting, a residual layer remains at the bottom of the cavities produced by the stamp features. In order for the imprinted polymer film to be used as mask for further metallization, the residual layer should be removed. This is usually done in an oxygen plasma etcher. An anisotropic plasma etcher is preferred in order to obtain verticals sidewalls for successful lift-off.

The thickness of the residual layer is determined by the stamp design, the NIL parameters and the viscoelastic properties of the polymer [77].

Low radio-frequency (rf) power is needed to etch the residual PMMA layer because the process takes normally just few seconds that are difficult to control if a reproducible process is desired. Unfortunately, some etching machines do not work reproducibly at low rf power. In addition, an over etched film would limit the maximum thickness of a metal layer that can be deposited for lift-off (See Section 2.4.3).

Typical conditions are: rf power $P = 20$ W, oxygen flow = 20 ccm/min, pressure = 10 mT, and etching rate ~ 30 nm/min.

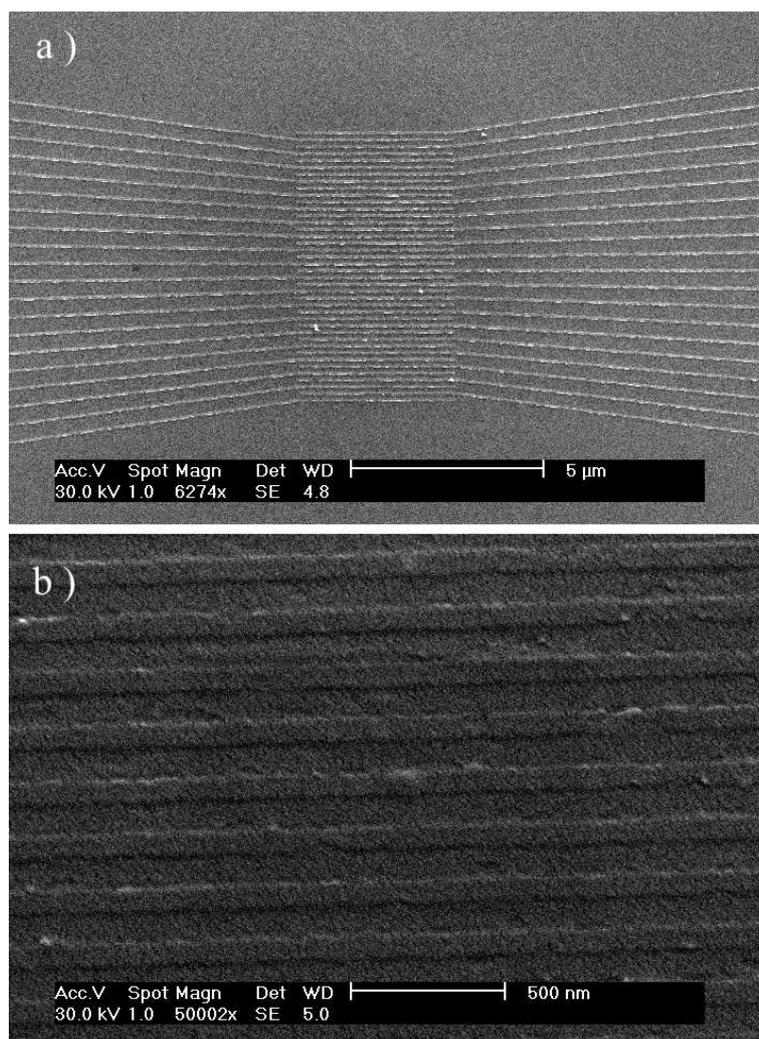


Figure 2.7: SEM micrographs of a) electron-beam written stamp after Au and Ti lift-off containing interdigitated electrodes. The interdigitated region is 4 μm long and the channel length is approximately 90 nm and b) part of the imprinted 950 K molecular weight PMMA.

2.4 Metal Nanoelectrodes

Metal lift-off is the process of transferring the pattern from the resist mask to a metal structure on the substrate as illustrated in Figure 2.8. A thin metal film is deposited on top of the sample after development of (i) EBL written samples or (ii) oxygen plasma removal of the residual layer on an imprint. During the process, metal is deposited either on top of the resist or directly on the substrate. The next step is to dip the sample in acetone (for PMMA) during several minutes with the metallized side facing downwards to dissolve the resist. Carcenac et al. [9] reported the use of trichloroethylene at 50 °C to lift off on PMMA. In all our experiments we used ultrasonic agitation during 10 minutes. The metal layer on top of the substrate is peeled-off while the metal parts deposited directly on the substrate, corresponding to the designed structure, remain attached to the substrate.

The surface treatment of the sample is very important for a successful lift-off. To prevent sticking of the metal to the substrate the RCA method can be used. An additional method is to pre-coat the sample with PMMA before cutting and then dissolving the coating in acetone. Only then the film to be used as resist is spun and backed. Otherwise, some gaps may appear on the metal-polymer film, which cause the metal to stick to the substrate.

Metal evaporation was performed using a UNIVEX experimental system from Leybold. This system has a vacuum chamber equipped with rotary and turbo pumps to get pressures of $\sim 10^{-5}$ in 20 minutes. The automatic current source supplies a variable current of maximum 400 A. Some of the experiments were done using the

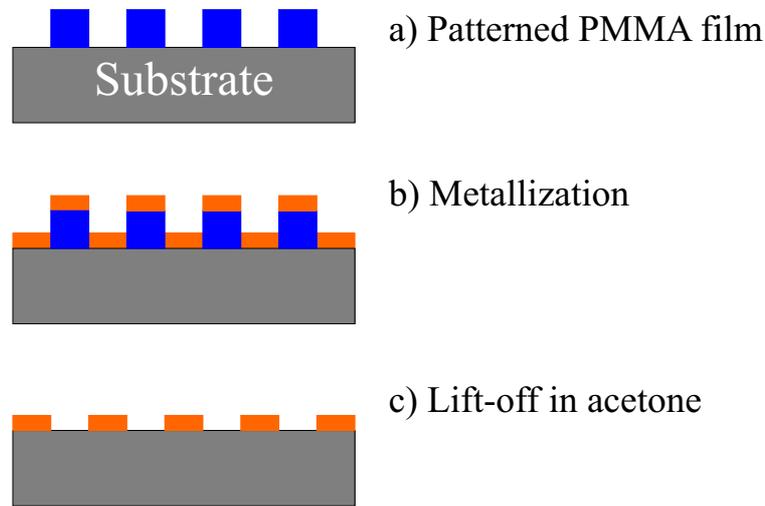


Figure 2.8: Schematics of the lift-off process with a single-layer resist.

electron-beam evaporator “e-flux” from Tectra, installed in an ITO deposition system. The limitations of the electron-beam evaporator system are that it is only possible to evaporate Cr and the time to evacuate the chamber until the required pressure is about 2 hours.

2.4.1 Choice of Metal

In this section, the use of different metals for lift-off and some aspects related to their evaporation are discussed. The surface roughness of metal lines, made up from different materials, is compared qualitatively. The lateral line thickness for the samples shown here is similar (~ 70 nm).

First, let us consider Chromium. It can be sublimated easily using both, the thermal evaporator or the electron-beam evaporator. It does not react with the source boats of the metal evaporator. Unfortunately, the grain size is comparable to the line width and gives a very irregular shape to the lines. Figure 2.9a shows a SEM image of 75 nm

Cr lines and spaces. The electron-beam resist used for this example was PMMA 200 K MW.

Second, Aluminum can be evaporated at lower temperature (Melting point = 660 °C) in the thermal evaporator. However, in the electron-beam evaporator Al melts and forms a short circuit. On the other hand, Al forms an alloy with the W source boats of the metal evaporator, which are broken after few depositions. The granularity on top of the lines is even worse than for Cr. Figure 2.9b shows a SEM image of 62 nm Al lines with a period of 300 nm. The electron-beam resist used for this example was PMMA 200 K MW.

Nickel shows the lowest surface roughness of the three metals. The lateral wiggling of the lines is mainly due to the electron-beam resist used and not to the properties of Ni. The only problem is that Ni reacts with the W boats forming an alloy, which cause the boat to break if the amount of Ni is higher than 9% of the boat mass. Using only the amount of metal necessary for each evaporation the same source boat can be used up to ~ 5 times. Figure 2.9c shows a SEM image of 75 nm Ni lines and spaces.

From the results of SEM analysis, we can conclude that the top surface seems to be smoother for Ni than for Cr and Al. Later experiments gave similar results for Ti. The drawback of Ti or Ni is that when contacted to p-type organic semiconductors they form blocking contacts for holes while Au generally leads to the formation ohmic contacts. Therefore, we decided to use Ni and Ti only for the fabrication of stamps for NIL because in this case, only the shape of the structures and the hardness of the material are important.

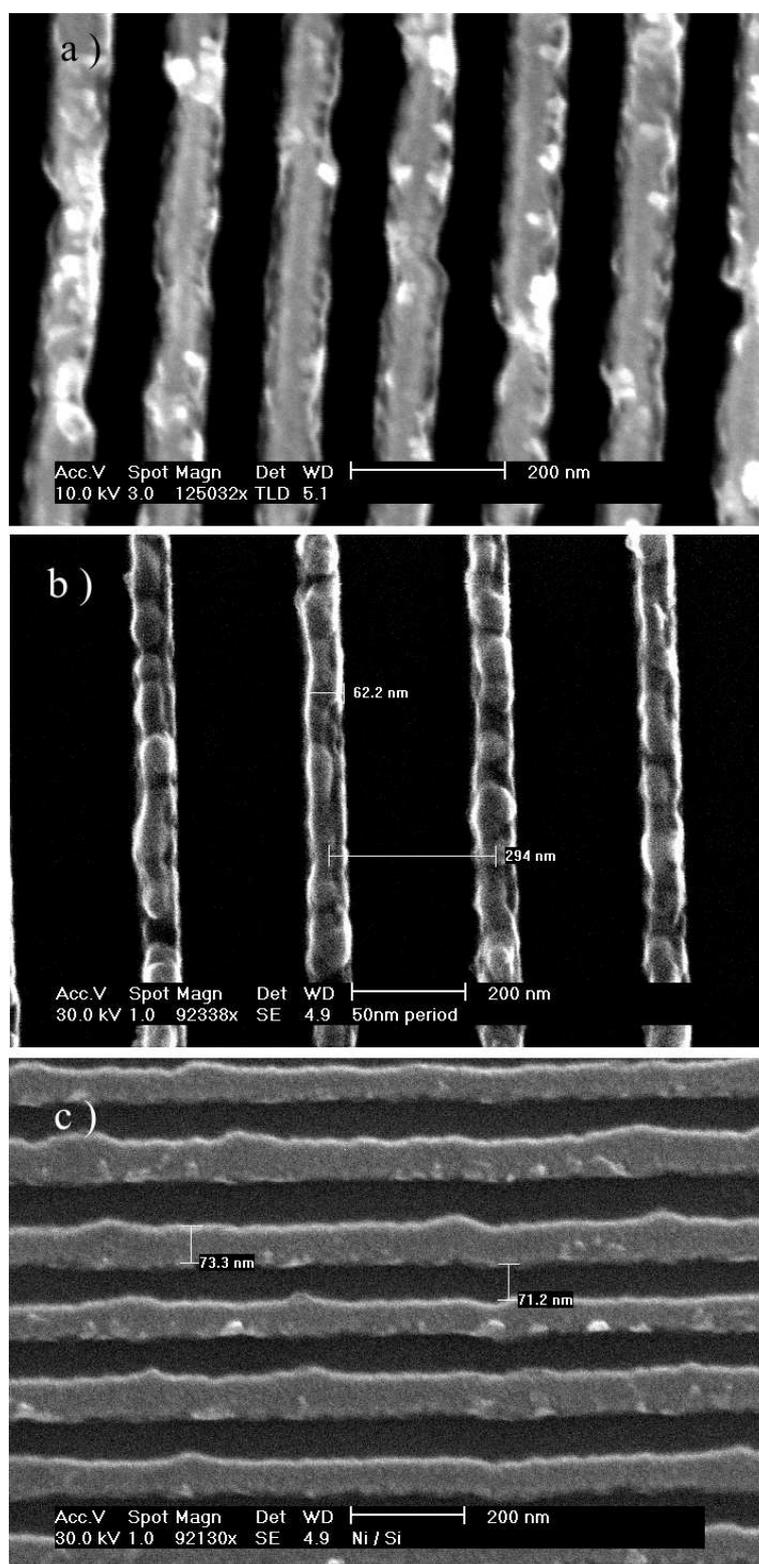


Figure 2.9: SEM images of lines produced using different metals. a) 75 nm Cr lines and spaces, b) 62 nm Al lines with 300 nm period and c) 75 nm-wide Ni lines and spaces.

2.4.2 Results for Linewidths and Spacings Down to 100 nm

Several results obtained after lift-off on samples containing PMMA films patterned either by EBL or NIL are shown in this section. Here we show only metal lines with separations down to ~ 100 nm while in Section 2.4.3 we go down to 50 nm. The displayed structures are interdigitated electrodes for the fabrication of field-effect transistors (Section 1.2.3).

An important observation is that in preliminary experiments using NIL it was found that the final transferred metal lines after lift-off were thinner than the respective lines on the stamp ($\sim 10\%$ at 75 nm line width). Polymer relaxation after imprinting is probably the reason for this effect.

SEM images of interdigitated electrodes fabricated by combination of EBL and metal lift-off are shown in Figure 2.10. The substrate was Si with a thermally-oxidized layer and a bilayer PMMA resist was used as described in Section 2.2.4. The inter-electrode spacing (channel length) was a, b) 104 nm, c, d) 390 nm, e, f) 780 nm, and g, h) 1.78 μm . Figures b, d, f and h) are close-up images of the ones on the left. The samples were metallized using 3.5 nm of Ti and 50 nm of Au.

On the other hand, SEM images of interdigitated electrodes prepared by combination of NIL and metal lift-off are depicted in Figure 2.11. Ti (2 nm) and Au (8 nm) were used during metallization. Figure a) 100 nm line width and 300 nm spacing and b) is a close up on the overlapping region.

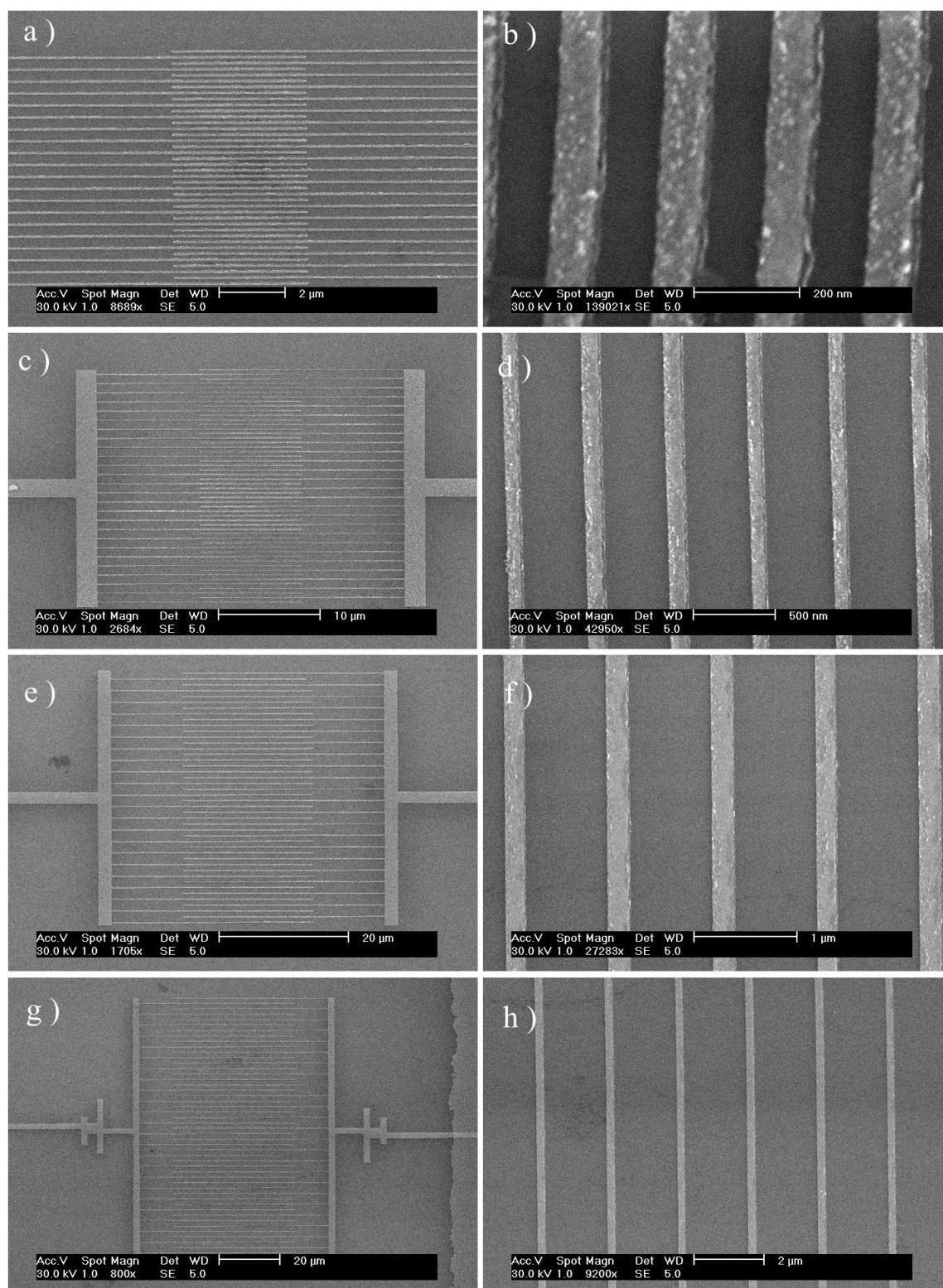


Figure 2.10: Interdigitated electrodes fabricated using EBL and metal lift-off. The substrate was thermally-oxidized Si and a bilayer PMMA resist was used. The spacing (channel length) was a, b) 104 nm, c, d) 390 nm, e, f) 780 nm, and g, h) 1.78 μm . Figures b, d, f and h) are close-up images of the ones on the left. from.

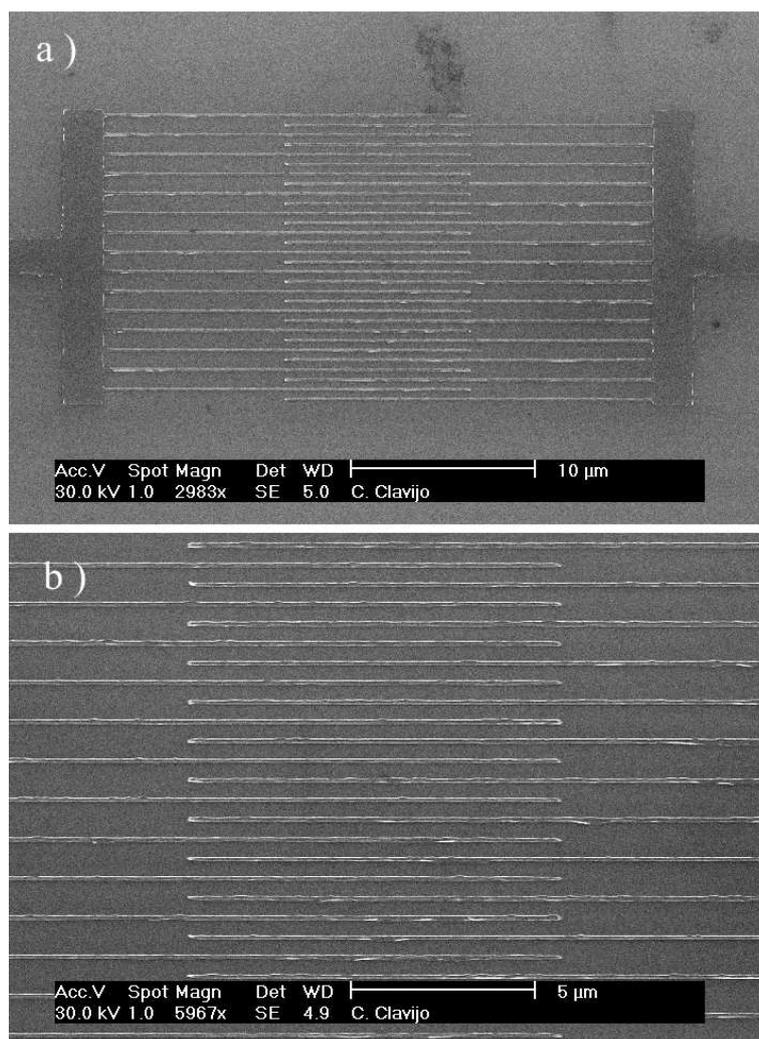


Figure 2.11: SEM images of interdigitated electrodes with 100 nm linewidth and 300 nm separation produced by NIL and Ti and Au lift-off (a). b) Close-up on the overlapping region.

2.4.3 Challenges Below Approximately 50 nm

For features with dimensions below approximately 50 nm the resist cannot be considered as a homogeneous medium because the entangled polymer chains form some kind of ball structure that starts to be visible at this length scale. This has been observed in AFM images of PMMA before and after electron-beam writing.

After exposure and development the edges of the polymer will be rounded due to scattering of electrons, inhomogeneity of the resist and resist swelling. Furthermore, the height of the trenches will be smaller than the original film thickness as shown in the Figure 2.12a.

The reduction in height and the rounding of the edges cause several problems during lift-off. First, when working with relatively thin polymer films (as it is normally the case) the amount of metal that can be deposited is reduced. Second, the round edges will produce a non-sharp discontinuity of the metal film from the top to the bottom parts. The result after lift-off will depend on the thickness of the evaporated metal. For a thickness larger than a critical value the lines will be contacted by metal bridges between them, as shown in Figure 2.12d. On the other hand, for a metal layer thickness below the critical value the result will be the expected metal structure Figure 2.12e.

Metal Gratings with line width ≤ 50 nm

The next figures show examples of gratings with line thickness ranging from 75 nm to 29 nm. Cr was used for lift off and the substrate was Si in all cases.

SEM images of the fabricated gratings with decreasing periodicity and 50% filling factor are shown in Figure 2.13. The periodicity of the lines varies from a) 100 nm,

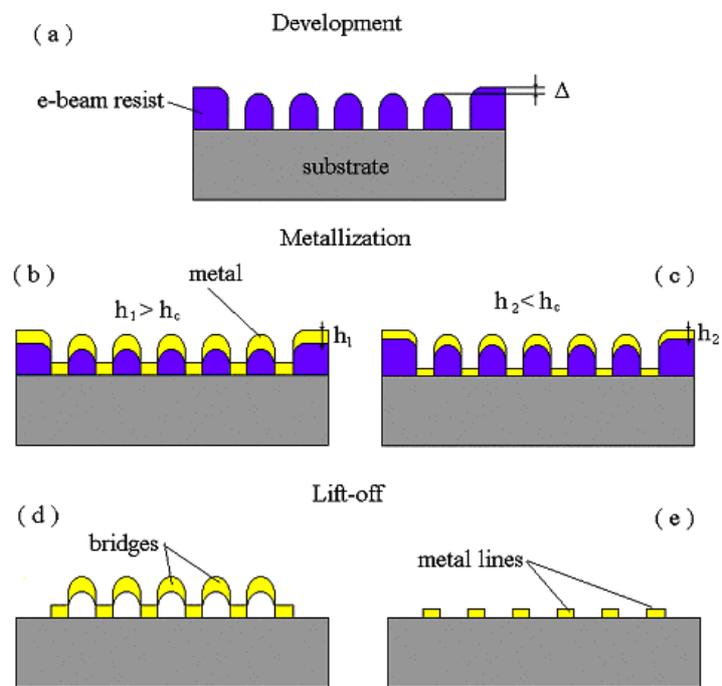


Figure 2.12: Schematics of the lift-off process for feature sizes < 50 nm. (a) Sample after exposure and development showing round edges and reduction of film thickness. Metallization with thickness higher than h_c (b), and smaller than h_c (c). Sample after dissolution of the resist with (d) formation of bridges between lines and (e) isolated metal lines.

b) 80 nm to c) 60 nm. The actual average linewidth is 50, 36 and 30 nm respectively. These gratings were produced using as a resist a thin film of 950 K PMMA with a thickness of 50 nm. The writing field was $10 \times 100 \text{ nm}^2$. It is clear in Figure 2.13 that we are reaching the limits of the fabrication process and materials properties. For instance, in c) some parts of the lines are missing. The results at this length scale can be improved using Ti or Ni instead of Cr for lift-off (See Section 2.4.1).

Next we show the results of fabrication of the smallest functional interdigitated electrodes achieved in this work. First, we show the results using EBL and then using NIL.

Combination of EBL and metal lift-off allowed to fabricate interdigitated structures with line widths and spaces down to 50 nm. Figure 2.14 displays a SEM image of the electrodes. The metals layers used were 3.5 nm of Ti and 50 nm Au. It is observed that the lateral roughness of the electrodes is comparable to the linewidth.

The minimum inter-electrode spacing attained with the combination of NIL and metal lift-off was 50 nm¹. Figure 2.15 depicts SEM images of interdigitated electrodes with a linewidth of 150 nm and 50 nm spacing fabricated by NIL and metal lift-off. During metallization, 7 nm of Ti and 16 nm of Au were evaporated. NanoRemover AG and acetone were used for lift-off.

2.5 Microscopic Characterization

In this section we will review the main microscopy techniques used in this work for the characterization of the morphology of the fabricated nanoelectrodes as well as the

¹This imprint was performed by A. Kam

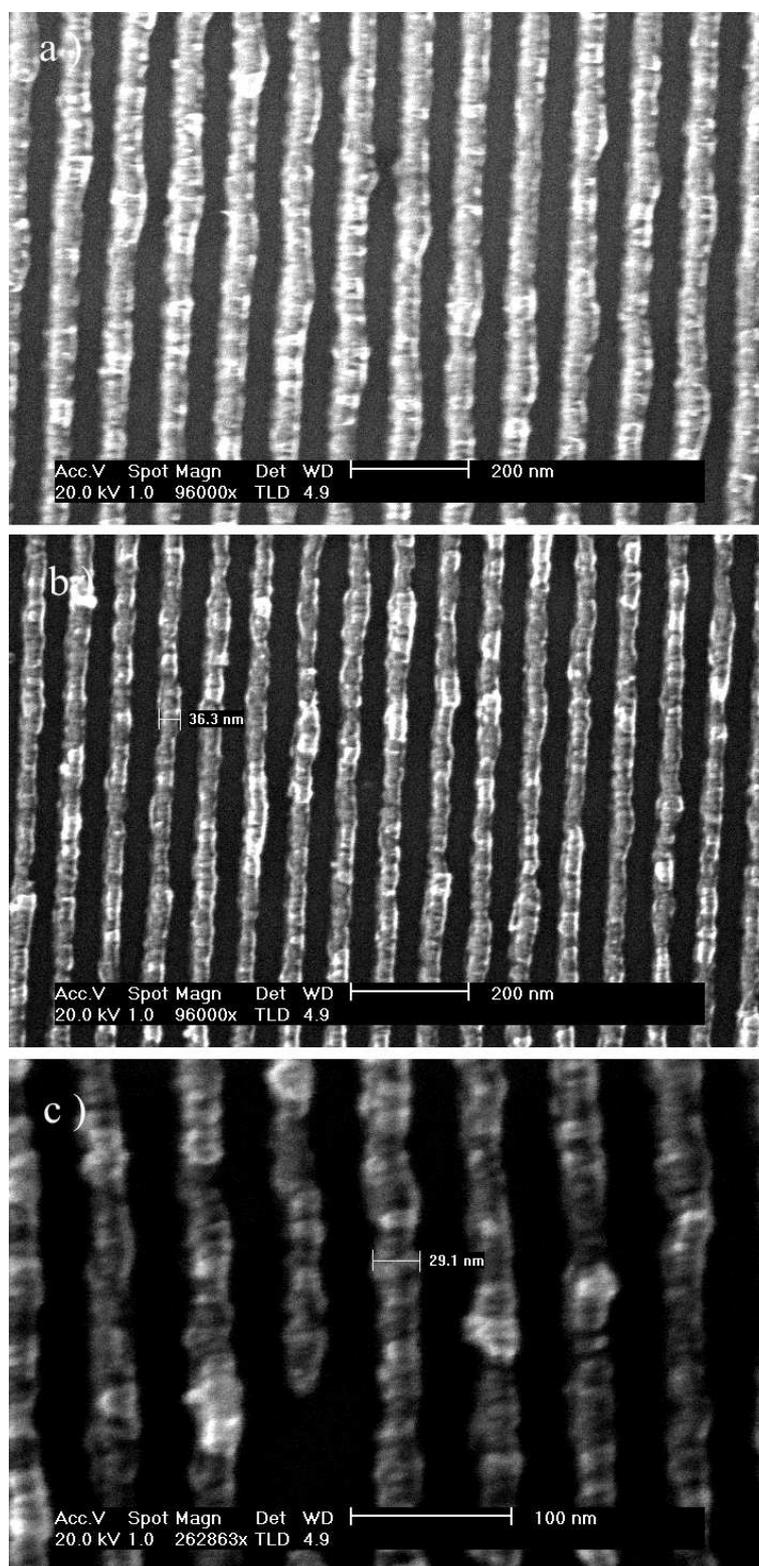


Figure 2.13: SEM images showing arrays of lines produced by EBL and Cr lift-off. a) 50 nm width and 50 nm spacing. b) 36 nm width and 80 nm period. c) 30 nm width and 60 nm period.

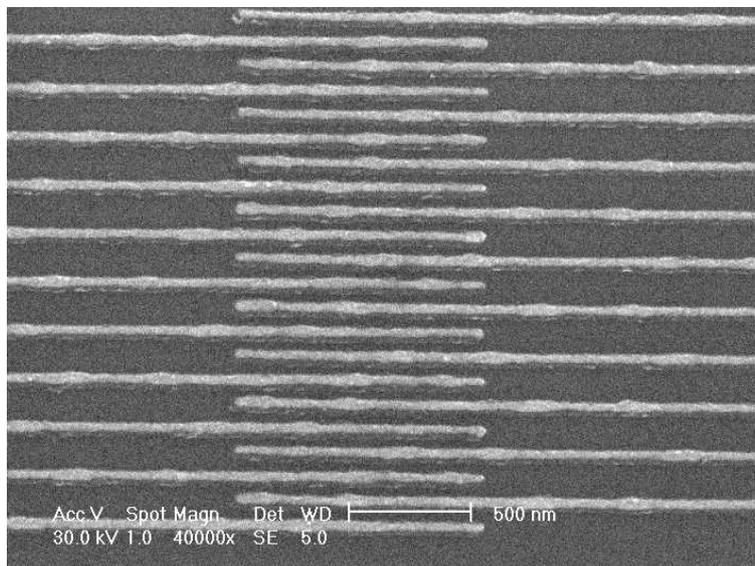


Figure 2.14: SEM image of interdigitated electrodes with a separation (L) of 50 nm fabricated by EBL and Ti/Au lift-off.

deposited organic semiconductor layers with a resolution down to the nanometer level.

2.5.1 Scanning Electron Microscopy

Scanning electron microscopy is a fast and reliable technique for imaging with a resolution down to 1 nm. It consists on scanning an electron beam across a sample surface and displaying a signal proportional to the number of secondary electrons emitted from the surface after the interaction of the electrons with the sample. The signal measured by the secondary-electron detector is displayed on a screen synchronized with the electron-beam scanner using a gray level scale. The region of the specimen where most of the electron interactions with matter take place is called *interaction volume*.

Therefore, SEM is more useful for samples where the generation of secondary electrons from electronic excitation is important and can be related to morphology. Here it

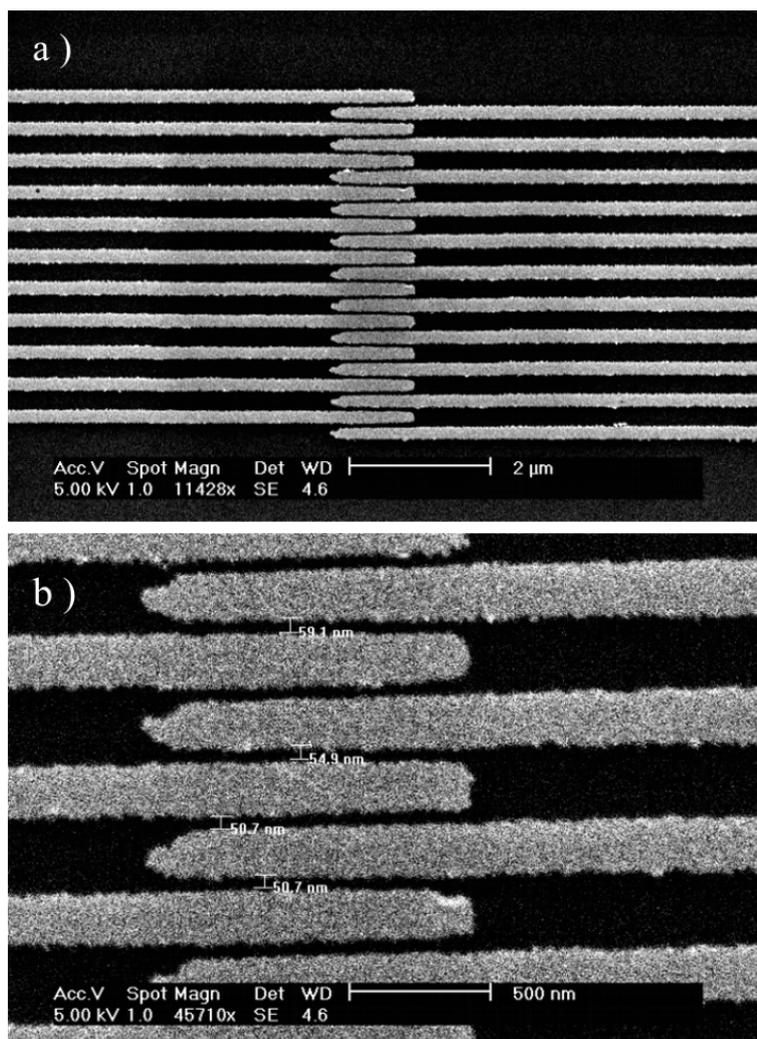


Figure 2.15: SEM images of interdigitated electrode with $L = 50$ nm fabricated by NIL and Ti/Au lift-off. Photos courtesy of A. Kam.

is used to measure the actual dimensions of the fabricated devices as well as for quality control.

In inhomogeneous materials the contrast of a SEM image comes mainly from the difference in beam penetration depth, which is directly related to the atomic number of the element. On the other hand, in homogeneous materials, topography influences the secondary electron emission because increasing the angle of incidence produces more secondary electrons. A high angle of incidence causes the interaction volume to be closer to the sample surface.

SEM is an ideal technique for conductive materials. In the case of insulating materials, an internal charge builds up a charge cloud close to the surface that makes it difficult to produce clear images. A possible solution to this problem is coating of the sample with a thin metal film but obviously this is a destructive method.

2.5.2 Atomic Force Microscopy

AFM belongs to the family of scanning probe microscopy (SPM) techniques where a sharp probe is scanned across the sample surface and some probe-sample interaction is monitored [1]. The resulting AFM image is directly related to the surface topography because it is based on scanning the atomic force between a sharp tip attached to a cantilever and the atoms on the sample surface. Another form of SPM is scanning tunneling microscopy (STM).

In STM, the tunneling current between a conductive tip and a sample is measured and a feedback loop maintains the tunneling current constant by a vertical displacement of the tip. A plot of the vertical position of the tip as a function of the plane coordinates

scanned across the sample surface constitutes the STM image. STM is capable of atomic resolution but can only be applied to conductive or semiconducting samples.

AFM uses a sharp tip attached to the end of a cantilever and can operate in three operation modes. In *contact mode* AFM the change in cantilever deflection is monitored by the system and the feedback loop maintains a constant cantilever deflection. The vertical displacement to keep the cantilever deflection is recorded to produce the topographic image. This is the only AFM technique capable of atomic resolution. In *tapping mode* AFM the cantilever oscillates at a frequency around resonance with an amplitude in the range between 20 and 100 nm. The tip contacts the sample surface at the bottom end of the oscillation. The feedback maintains constant the amplitude of the oscillation and the vertical position is recorded. Finally, in *non-contact mode* AFM the cantilever oscillates at a frequency slightly above the resonance frequency with an amplitude shorter than 10 nm. The tip oscillates above the adsorbed fluid layer on the surface. The feedback loop maintains constant the amplitude or the frequency of the oscillation by moving the tip vertically. The resonance frequency of the cantilever is decreased due to the van der Waals and other long-range forces that act 1 to 10 nm above the adsorbed fluid layer.

The scanning speed of SPM techniques is very low given as a result low throughput compared to SEM. Nevertheless, it is the best choice when analyzing electron-beam sensitive materials like organic semiconductors.

2.6 Deposition Methods for Organic-Semiconductors and Resulting Morphology

Several methods exist for the deposition of organic semiconductors. Vacuum evaporation at relatively low temperatures and deposition from solution either by drop casting or spin coating of soluble organic semiconductors. The physical properties of the resulting organic semiconductor layer such as morphology and charge transport are strongly influenced by the details of the deposition procedure. Additionally, the substrate properties are very important to determine the morphology of the deposited film. The main reasons why organic semiconductors are attractive for applications is the relatively simple and/or inexpensive deposition methods required for these materials in contrast to their inorganic counterparts.

Dihexylquaterthiophene was chosen as the main material for the experiments in this thesis because in addition to be commercially available² requires extremely simple processing conditions. The use of DH4T on properly prepared electrodes lead almost always to working devices. DH4T is a short molecule from the group of the oligothiophenes with hexyl end groups attached to it. Addition of the end groups give the molecule its soluble character in certain organic solvents. One of the drawbacks of using DH4T is its instability in ambient conditions. Which usually lead to a total loose of the device properties over periods of time of one week. Instability as well as the disordered nature of the solution processed films produce scatter of the results.

²Syncom, Groningen

2.6.1 Surface Treatment of Substrates

When using inorganic substrates such as SiO_2 a surface treatment is necessary to match the properties of the organic semiconductor to the inorganic substrate. This is generally accomplished by formation of a self-assembled monolayer (SAM). In our case we formed a monolayer from hexamethyldisilazane (HMDS) from the gas phase. In general alkyltrichlorosilanes can be used to form SAMs on hydroxylated surfaces such as glass, SiO_2 and Al_2O_3 giving rise to in situ formation of polysiloxane bounded to surface -Si-OH groups via Si-O-Si bonds [78]. Prior to SAM formation the substrates are cleaned in a solution of H_2SO_4 98% and H_2O_2 30% (3:1 volume) for one minute. Alternatively, organic semiconductors can be deposited directly (without substrate treatment) on plastic substrates such as PMMA.

2.6.2 Thermal Evaporation

Organic electronic devices based on short molecules such as acenes and thiophenes are usually fabricated by thermal evaporation in vacuum because of the insolubility of these materials. An electrically heated boat containing the molecular material is placed inside a vacuum chamber, at certain distance from the boat a substrate is placed. A careful control of the evaporation and substrate temperatures as well as the evaporation rate allows depositing highly ordered films, or even single crystals. For instance, the grain size has been found to depend critically on the substrate temperature. Evaporation temperatures for organic semiconductors are lower than the required for inorganic semiconductors. The only drawback is that it is a time consuming process because

of the time required to pump the evaporation chamber. Due to the high degree of order that can be achieved with the evaporation process the mobilities associated with devices using this method are in general higher than with solution processes.

2.6.3 Solution Process

Solution-processed organic semiconductors are expected to make an impact on manufacturing costs. High-vacuum chambers are not needed and processing times for spin coating or casting are considerably lower. Additionally, they can be processed using NIL. In general, solution processed organic semiconductors exhibit lower mobilities compared to highly ordered organic semiconductors. The model of charge motion in bands breaks down and the conduction mechanism is predominantly hopping between localized states in individual molecules or few monomeric units. Nevertheless, highly oriented microscopic regions, defined as electronic domains, on the solution processed conjugated polymer can still be found. T. Hassenkam et al. [37] used electric force microscopy (EFM) to map the potential drop on a self-assembled monolayer of conducting polythiophene deposited between two gold electrodes. The potential profile along the direction of the current presents step-like features, which are associated to electronic domains.

Sirringhaus et al. [74] demonstrated mobility enhancement of polyfluorene copolymer based OFETs through liquid-crystalline self organization with polymer chains aligned parallel to the transport direction using an alignment layer. Field-effect mobilities on devices with aligned chains in the charge transport direction are in the range of 0.01 to 0.02 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ while for the non-aligned ones $\mu < 10^{-3} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

The experiments described in this thesis were performed mainly with dihexylquaterthiophene (DH4T). DH4T with 96% purity was bought from Syncom and was dissolved in high purity ($> 99\%$) chloroform. The impurity is probably monohexylquaterthiophene. DH4T was dissolved in chloroform with concentrations 6×10^{-2} M and 2×10^{-3} M by magnetic stirring at $50\text{ }^{\circ}\text{C}$ for two hours. Substrates containing source and drain electrodes were coated with a thin film of DH4T by drop casting, using the 6×10^{-2} M solution or by spin coating using the 2×10^{-3} M solution. Solvent evaporation after casting takes approximately between 10 to 20 min. Spin coating was performed at 2000 rpm during 30 s. Film thickness was measured from cross-section SEM images of cleaved samples after evaporating a thin metal film of Ti on top of the DH4T films.

The morphology of the cast-deposited DH4T films on top of the source-drain electrodes was studied by optical microscopy and tapping mode atomic force microscopy (AFM). Optical microscopy was used to check that the coverage of the devices by the organic layer was full in all cases. Moreover, it has been observed under the optical microscope that DH4T crystallites form already in solution after drop casting. Usually, crystallites, or groups of them, slide around until their final position when the solvent is evaporated. In contrast, the spin-coated films are homogeneous and have a uniform thickness of approximately 25 nm. Figure 2.16 shows microscopy images of DH4T films a) drop cast and b) spin coated from chloroform solution on SiO_2 substrates. The thickness of drop-cast DH4T films is highly irregular as a result of the presence of some three-dimensional features and an accurate value cannot be assigned to it. From cross-section SEM images of cleaved samples a mean layer thickness of $1.7\text{ }\mu\text{m}$ was

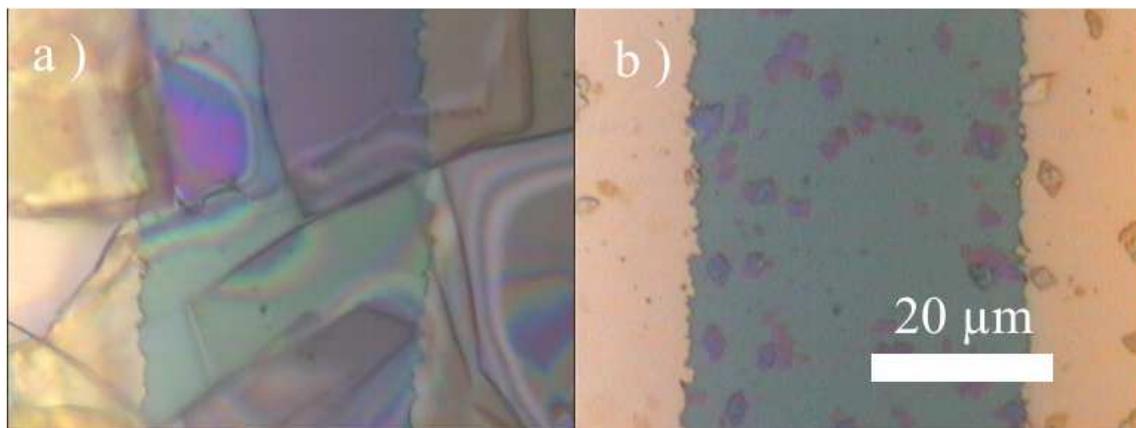


Figure 2.16: Optical microscopy images of a) drop-cast and b) spin-coated DH4T from chloroform solution on SiO_2 substrate.

measured. Nevertheless, the 3D features can reach heights up to $50 \mu\text{m}$.

Figure 2.17 shows an AFM image of a drop-cast DH4T film on SiO_2 . It shows a stack of layers covered by a top layer that adopts the form of the steps. This is supported by the cross-section images where the covered layer edges appear rounded while in the corner they appear sharp. Figure 2.17b is a $5 \times 5 \mu\text{m}^2$ close up image of the bottom-right part of 2.17a where the stack is not covered. The measured terrace height was approximately 3 nm which shows that the 3.2 nm-long DH4T molecules align in a direction nearly perpendicular to the substrate [31].

Role of the Solvent

Some organic semiconductors are soluble in certain types of organic solvents. Generally, they belong to the group of polymers but a number of small molecules can be dissolved as well. In particular the end-substituted form of some oligothiophenes.

The evaporation rate of the solvent is crucial for the process of mutual arrangement

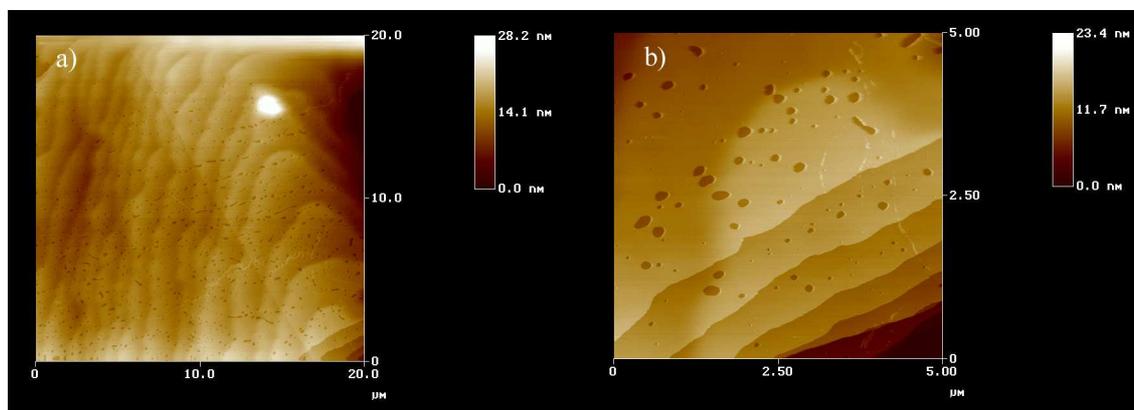


Figure 2.17: Tapping mode AFM images of a DH4T film deposited on SiO_2 . Figure b) is a close up of the lower right part of Figure a). This image shows the layered structure of the film and a cross section analysis gave an average layer thickness of 3 nm.

of the molecules and their resulting morphology. In general, solution evaporation speed will depend on the solvent and on the deposition method. For spin coated devices it was found that in addition to the type of solvent, the concentration plays a role. Too diluted solutions may prevent film deposition while too concentrated ones may result in highly inhomogeneous and thick films.

Local morphology is very sensitive to the preparation procedure. Therefore, materials of the same chemical structure may have very different electronic properties depending on the solvents used (Epstein in Ref. [28]). For DH4T it has been found that chloroform gives the highest mobility both for spin coating and drop casting. Other solvents are hexane, toluene-hexane, THF but the associated mobilities are orders of magnitude smaller. An study of the effects of different solvents and their purity used for DH4T is given in Ref. [46].

2.7 Fabrication of Molecular Electronic Devices

In this section we will review different methods to electrically contact single molecules, or a small quantity of them, that have appeared in the literature. As we saw in the introduction to molecular electronic devices (Section 1.2.7), these methods can be divided into two categories regarding the type of contacts used. Namely, using adjustable contacts and fixed contacts.

Later, we will present results on the fabrication of molecular electronic devices using two methods. First, we will consider SAM devices. Second, we will show preliminary results on few molecule devices using the gap produced by electromigration breakdown of nanowires. Results concerning electrical characterization of self-assembled layer devices will be given in Section 3.3.

2.7.1 Adjustable Contacts

In reference [21], Cui et al. used tunable contact to molecules by means of scanning probes. Similar experiments are reported in Ref [26, 22]. A porous SAM of octanethiol on Au (111) was used as molecular insulator. The investigated molecules 1,8-octanedithiol occupy the porous of the octanethiol SAM with one of the sulfur atoms bonded to the Au(111) surface. The resulting monolayer was incubated with a suspension of gold nanoparticles which bond chemically to the the second Sulfur atoms of the 1,8-octadithiol molecules. Finally, a gold-coated AFM tip was used to contact the individual particles bounded to the monolayer and to measure the current-voltage characteristics of the circuit.

Another type of tunable contact consists in using metallic break junctions [64, 49]. In reference [64], the metal junction was fabricated using EBL on an insulating layer of polyamide on a polished phosphor-bronze substrate. The metal junction consisted of a 100 nm thick gold layer deposited on top of a 0.2 nm thick Ti adhesion layer and protected by a 5 nm thick Al layer. Anisotropic RIE of the substrate below the junction region produced a suspended junctions which was broken using a three-point bending configuration by applying pressure with a screw on the center on the back of the sample. The breakdown was registered as a change to infinite resistance across the junction. Then the active molecules, bisthiolterthiophene (T3), were assembled on both sides of the junction by immersion of the suspended junction in a droplet of a 5×10^{-4} M solution of T3 in trichloro-1,1,1-ethane. Finally, the distance between the opposite contacts containing the molecules was reduced using a piezoelectric actuator until conduction was registered. They measured the current-voltage (I-V) characteristics of the junction at room temperature containing step-like features from which the transmission function of the molecules was calculated.

2.7.2 Fixed Contacts

The methods to contact single molecules based on fixed electrodes use either electrostatic trapping or deposition of small metal contacts on SAMs. In the technique of electrostatic trapping [61, 6] a fabrication process similar to break junctions is used but in this case the initial electrodes are already separated by around 20 nm. The decrease in size of the electrode separation is achieved by sputtering of Pt on top of the electrodes. The electric field created between the tips polarizes the particles which are

driven to the regions of higher electric fields and depending on the size of the molecules and the electrode spacing the positive parts of the dipole will contact the negative potential contact and vice versa. In order to trap a finite number of particles the circuit contains a limiting resistor which will cause the electric field to decrease drastically once the first particles are contacted. This technique has been used to measure I-V characteristics of Pd nanoparticles [6] and DNA molecules [61].

SAMs can be contacted by depositing small metal contacts in the nanopore geometry [12] or using shadow masks [69, 19, 68]. When using shadow masks to prepare the contacts to SAMs, the SAM thickness defines the electrode separation. This fact was used in [68] in the fabrication of a molecular FETs in a vertical configuration where the channel length was defined by the monolayer thickness. The molecules used in that work were 1,4-dithiolbenzene and 4,4'-dithiolbiphenylene. The first fabrication step consisted in the deposition of a 15 nm-thick gold contact on a SiO₂/Si substrate using lithography or a shadow mask. Subsequently, the substrate was immersed in a 0.3 mM ethanol solution of the active molecules for 24 h and cleaned afterwards using ethanol. The second gold electrode partially overlaps the first one and it was deposited using a shadow mask while the sample was cooled at temperatures between -172 °C and -30 °C to protect the SAM.

An alternative way of contacting SAM is by means of nanopores fabricated using standard lithography and etching techniques [12]. The fabrication process starts by depositing a low-stress SiN₃ layer on both polished sides of a Si(100) substrate by means of low-temperature chemical vapor deposition. On one of the sides of the substrate a window was opened using photolithography and RIE. A cavity was then anisotropically

etched using a KOH solution in such a way that a suspended SiN_3 membrane was formed. Thermal oxidation is used to grow SiO_2 on the lateral walls of the cavity for insulation purposes. EBL and RIE were used to make a hole around 30 nm in diameter through the SiN_3 membrane. The cross section of the bottom of the hole was semispherical due to a substantial reduction of the RIE rate on SiN_3 . As a result the end opening has a considerably smaller diameter than the initial. A gold contact was then evaporated on top of the upper cavity, blocking one end of the porous. The sample was then immersed in a solution of 2'-amino-4-ethynylphenyl-4'-ethynylphenyl-5'-nitro-1-benzenethiolate for 48 h and cleaned. A second gold contact was deposited through the cavity at very slow deposition rate and keeping the sample at 77 K. The current-voltage characteristics of the resulting device showed negative-differential resistance.

2.7.3 Combined Approach

Zhitenev et al. [82] used a combination of the previously mentioned approaches to measure the conductance of small molecular junctions. The fabrication steps are shown in Figure 2.18. Using this method they measured the conductance of different conjugated molecules which shows sharp steps periodic in source-drain voltage at low temperature. The gate potential controls the position of the steps.

2.7.4 Results

The results of our experiments related to the fabrication of molecular electronic devices are presented in this section. First, we will explain the structure and fabrication procedure of a self-assembled layer device. We do not use the term *monolayer* because

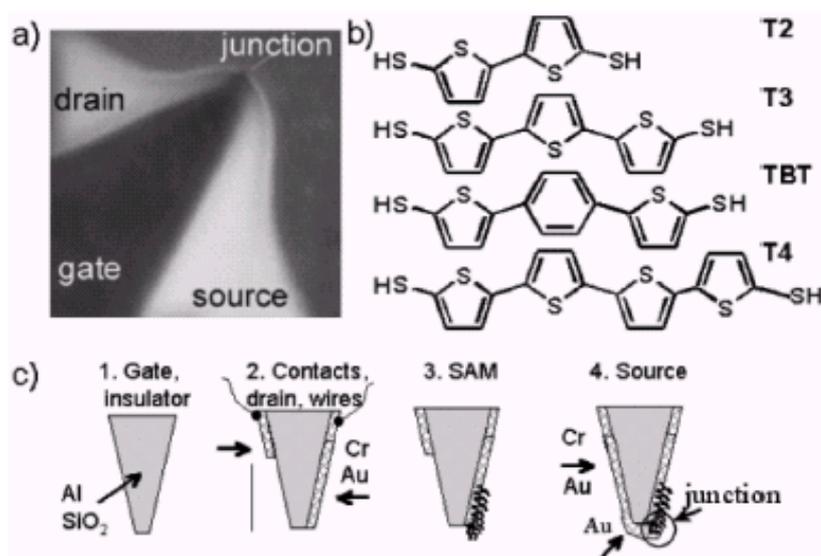


Figure 2.18: a) SEM image of the molecular junction, b) chemical structure of the molecules used, and c) sample preparation steps. Reprinted figure with permission from N.B. Zhitenev, H. Meng and Z. Bao, *Physical Review Letters*, 88, 22, 226801 (2002).

these self-assembled films are most probably disordered multilayers of DH4T molecules.

Finally, we show results of the fabrication of nanoelectrodes with a separation of 13 nm by means of EBL and electromigration breakdown.

Self-Assembled Layer Devices

Using a SAM sandwiched between two metal layers, rectifiers have been demonstrated. Several devices of this type have been reported in the Literature [32, 59]. A three-terminal self-assembled monolayer field-effect transistor SAMFET device was reported by Schön [68] but this paper has been retracted.

The device structure of the three-terminal device fabricated in this work is shown schematically in Figure 2.19. The fabrication procedure is as follows. First a metal

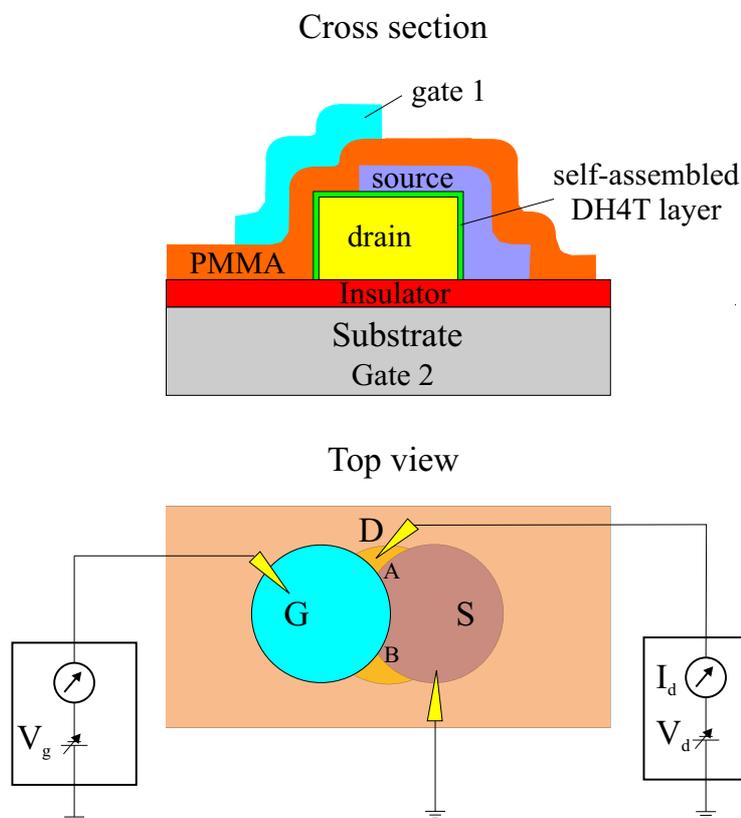


Figure 2.19: Device based on a self-assembled layer of DH4T as active material. DH4T was self-assembled on the *drain* gold electrode and sandwiched between this and a second evaporated *source* electrode. A 50 nm thin film of PMMA was coated and finally a third gold layer, the gate was deposited on top. The measurement circuit is shown in the top view. The transparency of PMMA allows contacting source and drain.

electrode ($1 \mu\text{m}$ thick) was deposited on an insulating layer by metal evaporation. The sample was then immersed during 24 or 48 hours in a 1 mM Ethanol solution of DH4T. After removing the sample from the solution it was cleaned by spinning it at 6000 rpm while pouring Ethanol. Then a second electrode with an overlapping region was deposited as shown in Figure 2.19. The sample was then coated with a 50 nm film of PMMA 950 K. Finally, a third metal contact was deposited on top, overlapping regions of the previous contacts as shown in Figure 2.19.

The first contact needs to be thick for the insulating PMMA layer, separating the third contact from the SAM molecules on the edges of the overlapping region of the contacts, to be as thin as possible. Several devices were prepared in parallel using a shadow mask with an array of holes.

The experiment was carried out twice. Immersion times were 48 and 24 hours for the first and second experiments respectively. The results of the measurements on these devices will be given in Section 3.3.

Few-molecule Devices

One of the main issues for the fabrication of mono molecular electronic devices is how to address a single molecule. Here we propose the fabrication of molecular field-effect transistors using electrostatic trapping of molecules between prefabricated contacts made by electromigration and monolayers created both by self-assembly and Langmuir-Blodgett deposition. Recently, Austin et al. [4] have reported the fabrication of nanoelectrodes using NIL and electromigration.

The first step of the method consists in the fabricating of a stamp containing pairs of electrodes connected through a thin line approximately 20 nm wide. The stamp was used for pattern transfer to metallic structures on a SiO₂ substrate. The nanowires are subsequently broken using electromigration. Electromigration refers to material transport caused by the presence of strong current densities. In order to produce a small gap the process should include heating of the substrate and slow increase of the current density. This procedure was performed on EBL written structures that were metallized using Ti/Au lift-off. The Ti layer was only 1 nm thick. For electromigration

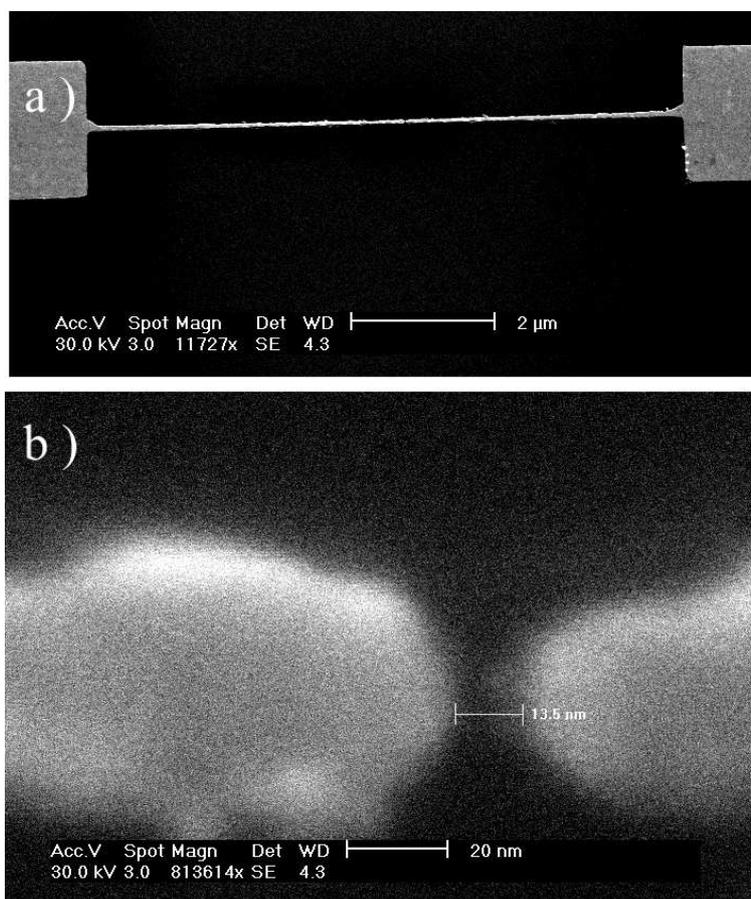


Figure 2.20: SEM image of a nanowire fabricated using EBL. a) The nanowire was broken using electromigration. b) Close-up of the broken part of the nanowire showing a gap of ~ 13 nm.

the sample was heated at 180 °C. A SEM image of the obtained contacts is shown in Figure 2.20. The measured line width was 60 nm and the gap was ~ 13 nm that is very close to 8 nm the value obtained by Austin et al. [4]. Shorter gaps are expected by using narrower nanowires.

The device has not been used for because of the lack of a suitable material to be attached between the electrodes. A suitable material should consist of a conjugated structure with end groups capable of attachment to the gold electrodes.

2.8 Discussion

Several techniques for nanostructure fabrication and characterization were considered in this chapter. The factors limiting the resolution of EBL were studied and it was found that for our experimental EBL system, limited in the acceleration voltage to 30 kV, the minimum feature size and spacing that can be made reproducibly is 50 nm. On the other hand, the resolution of NIL is mainly limited by the resolution of the stamps, which are usually made by EBL. Therefore, the minimum features obtained with this technique are the same as for EBL namely 50 nm.

Nanoelectrodes for device application are commonly made by metallization and lift-off, consequently, the granularity of the metal used for lift-off is an important issue affecting the resolution of the final nanoelectrodes. Ti and Ni give the best results, as far as stamp fabrication is concerned, because of their low roughness when deposited by thermal evaporation. The use of a bilayer resist for EBL allowed circumventing the lift-off problems for lines with dimensions down to 50 nm.

For metallic nanostructures the most suitable characterization technique is SEM for evaluation of device dimensions and lateral roughness of the metal structures. Additionally, SEM is a tool used in the process of EBL. Organic semiconductors are very sensitive to the electron beams used in SEM. When this technique is applied to the analysis of organic semiconductor films, is a destructive method that does not give a complete information on the morphology of the organic layer. AFM is an alternative in this case because it is based on scanning the atomic force between a sharp tip and the surface atoms of a sample. AFM was used in this work to provide evidence of the

layered structure of DH4T films deposited by drop casting and to determine the size of a single layer of the material.

The morphology of the deposited DH4T films was found to be strongly dependent on the deposition method used. Spin coating gives thinner and more homogeneous films than drop casting. In the experiments reported here, a 2×10^{-3} M DH4T solution in chloroform was used for spin-coating producing uniform films of around 25 nm thickness using 2000 rpm during 30 s.

The method of drop casting is simpler, films are polycrystalline and the crystallite size can be as high as 50 μm . Nevertheless, the layer thickness cannot be controlled and the solvent evaporation time is longer. In this case the concentration of the DH4T solution was 6×10^{-2} M.

Around 50 OFETs were fabricated using the HMDS treatment. The field-effect mobility was extracted from the current-voltage characteristics. The channel dimensions for some representative devices are given in Table 5.1.

The fabrication of molecular electronic devices was tried with two different methods. The first method consisted in using a self-assembled layer of DH4T sandwiched between two metal contacts deposited by vacuum evaporation through shadow masks. In this case, the self-assembled layer defines the channel length. A very important fabrication issue in this type of devices is to ensure that the organic layer is free of pinholes. The second method uses electromigration breakdown of a nanowire fabricated by EBL, which could be produced by NIL as well. The fabrication process is relatively simple and a gap of approximately 13 nm was obtained in this way. In this case, the results are preliminary because the technique needs further improvement to reduce the size of

the gap to around one or two nanometers. Additionally, a suitable molecular material to attach on the opposite ends of the nanoelectrodes such as long thiol-terminated conjugated chains needs to be used. These materials cannot be obtained commercially but only from few research laboratories on synthetic chemistry.

2.9 Summary

In summary, the techniques for fabrication and characterization of OFETs with critical dimensions ranging from the micrometer down to the nanometer scale and the main results of fabrication in this work were treated in this chapter. Metal nanoelectrodes with a minimum channel length of 50 nm were produced by both EBL and NIL. The limitations were due to the maximum available 30 kV for the accelerating voltage of the EBL system and from the roughness of the evaporated metals. The principles of SEM and AFM were studied in view of their application in the characterization of the morphology of the nanoelectrodes and the organic semiconductor films. Several deposition methods were studied and the results obtained using different variants of the solution process for DH4T were given. Finally, several approaches for the fabrication of molecular electronic devices were studied and the results of this work were given. In particular, fabrication nanoelectrodes using EBL and controlled electromigration as well as gated devices based on self-assembled DH4T layers.

Chapter 3

Electrical Characterization

In this chapter we describe the experimental set-up used for current-voltage characterization of the fabricated organic electronic devices. Later, results of the results of these measurements are given.

In the case of DH4T OFETs, output and transfer characteristics are measured for devices in a range of channel lengths from 70 μm down to 50 nm. The device stability is also studied by recording the time dependence of the device current.

Furthermore, the results of electrical characterization for gated molecular electronic devices based on self-assembled layers of DH4T are given.

3.1 Experimental Set-up

Electrical characterization was performed using a 6517A electrometer for the source-drain circuit and a K237 source-measure unit to supply the gate voltage, both from Keithley. These instruments were computer controlled. Measurements were made in darkness inside a copper shield box, at room temperature, in air and right after deposition of DH4T. The integration time for the electrometer was set to 200 ms (high

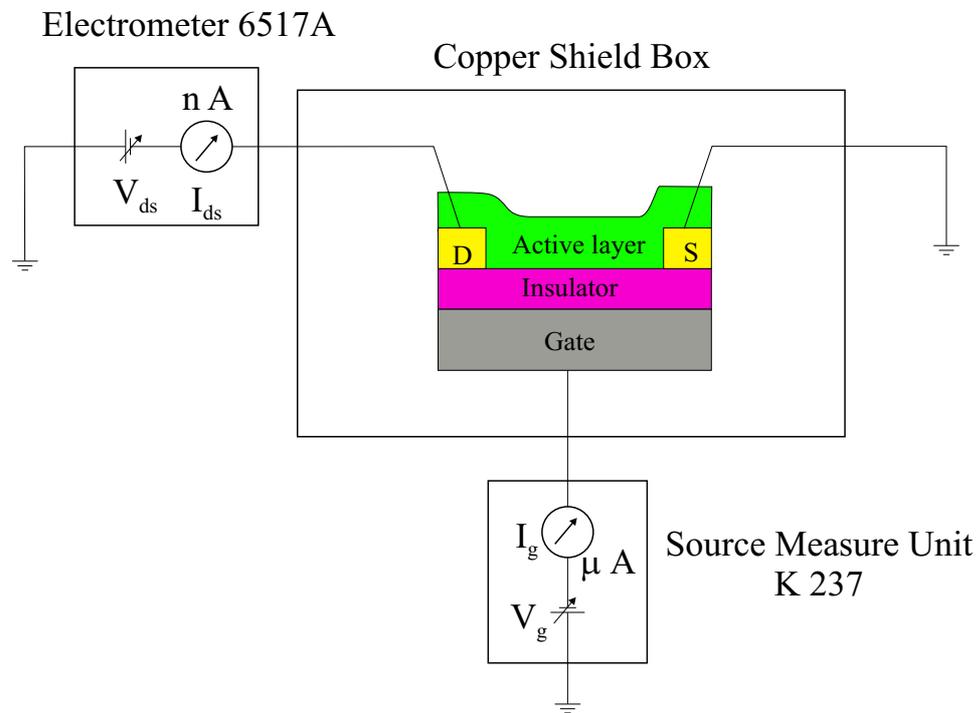


Figure 3.1: Current-voltage characterization set-up. The electrometer 6517A supplies V_{ds} and measures I_{ds} while the K337 unit supplies V_g and measures I_g . Contacts to source and drain are made using micro-manipulated tips

accuracy) and a delay time of 1 s was used between measurements. The experimental set-up is shown in Figure 3.1. A photograph of the set-up to contact electrically the devices is shown in Figure 3.2. Two types of measurements were performed:

Output characteristics drain-source current versus drain-source voltage for several gate voltages.

Transfer characteristics drain-source current versus gate voltage for a fixed value of drain-source voltage.

The fixed V_{ds} value for the transfer characteristics is usually chosen to be low typically between 1 and 2 V.

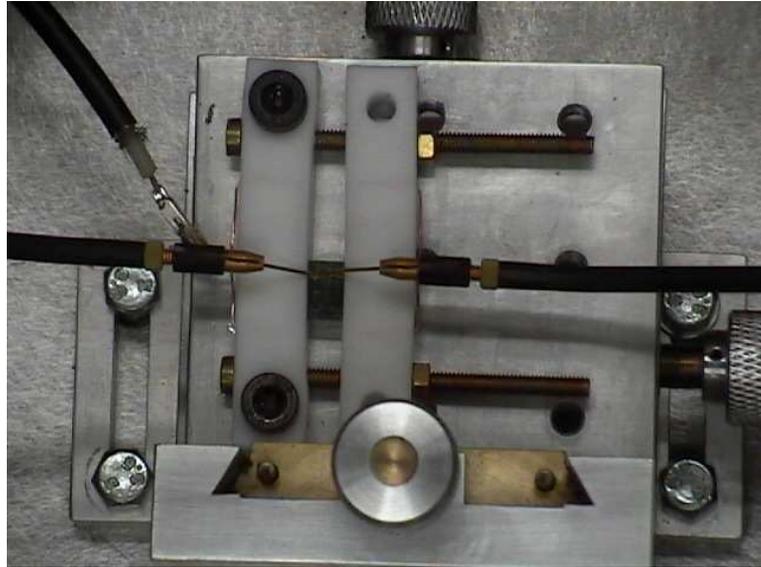


Figure 3.2: Photography of the tips to provide electrical connection of the device to external measurement devices.

3.2 Current-voltage characteristics of DH4T OFETs

In this section we present the results from electrical characterization of solution-processed DH4T OFETs. The devices considered in this section have channel lengths in the range from $70\ \mu\text{m}$ down to $50\ \text{nm}$. The techniques for device fabrication were treated in Chapter 2 and the specific parameters of the considered devices are give next.

Si wafers with a thermally-grown $400\ \text{nm}$ thick SiO_2 layer were used as substrates. Metal contacts were made by thermal evaporation of Ti ($3.5\ \text{nm}$) and Au ($30\ \text{nm}$) on SiO_2 substrates coated with lithographically patterned resist. Ti was used as an adhesion layer between gold and SiO_2 . Table 5.1 shows the channel length (L) and width (W) for each device. The substrates were treated according to the procedure described in Section 2.6.1. EBL was used in the definition of the source and drain electrodes using as resist a bi-layer composed of $950\ \text{K}$ and $200\ \text{K}$ molecular weight PMMA. Electrodes

Table 3.1: Channel dimensions of the devices.

N	1	2	3	4	5	6	7	8	9	10
L [μm]	0.050	0.145	4	10	15	20	30	39	45	70
W [μm]	20	156	1260	1260	1260	500	500	980	5000	980

for devices 8, 9 and 10 ($L > 30 \mu\text{m}$) were defined by photolithography.

The current-voltage characteristics for drop-cast devices with channel length between 145 nm and 30 μm are shown in Figure 3.3. The figure also shows the fit to Equations 4.26 and 4.32 that will be derived in Section 4.3. Leakage currents from source-drain contacts to the gate through the oxide layer are responsible for curve shifts at $V_{ds} = 0$. Curves were shifted in such a way that $I_{ds}(V_{ds} = 0) = 0$ for each value of V_g . The magnitude of the shift was below 1 nA and for most of the devices negligible.

In addition to drop casting we also prepared devices by spin coating. The output characteristics of spin-coated devices with $L = 50 \text{ nm}$, 39 μm , 45 μm and $L = 70 \mu\text{m}$ are shown in Figure 3.4. For the $L = 50 \text{ nm}$ device, the high voltage region $|V_{ds}| > 4 \text{ V}$ is not shown because the effects of the high electric field intensity ($E > 80 \times 10^6 \text{ Vm}^{-1}$) present at those V_{ds} values such as fast increase in mobility as well as strong deviation from the gradual channel approximation condition ($E_{\text{longitudinal}} < E_{\text{transversal}}$) are not included in our analysis. Higher gate voltages were supplied in order to minimize the departure from the $E_{\text{longitudinal}} < E_{\text{transversal}}$ condition. Table 3.1 contains the relevant parameters of some representative devices.

Figure 3.5a shows the output characteristics for device 2 measured at ambient conditions. For this measurement, V_{ds} was swept back and forth. The hysteresis was

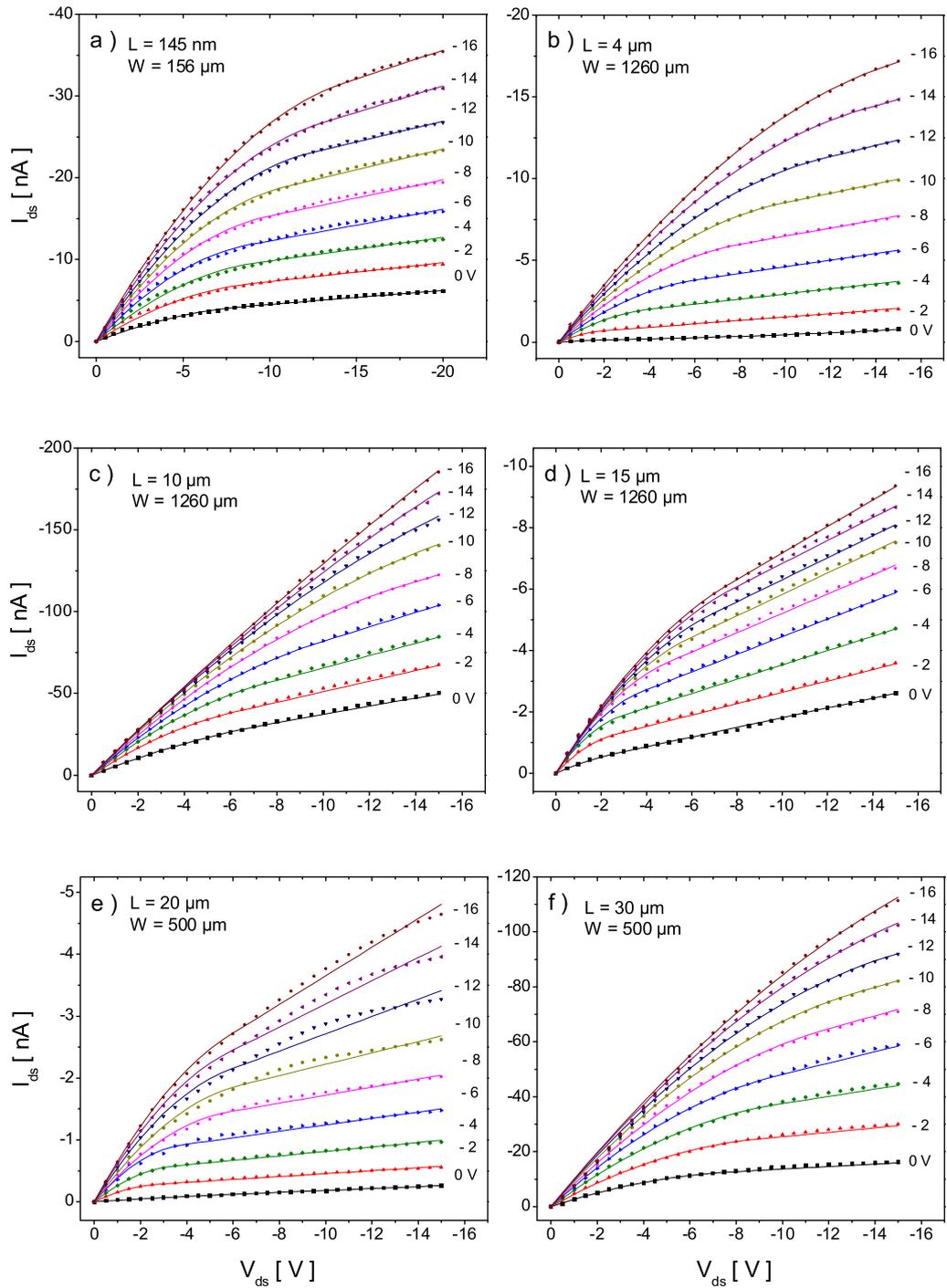


Figure 3.3: Measured output characteristics and fit to Equations 4.26 and 1.6 for drop-cast DH4T FETs with a) $L = 0.145 \text{ }\mu\text{m}$, b) $L = 4 \text{ }\mu\text{m}$, c) $L = 10 \text{ }\mu\text{m}$, d) $L = 15 \text{ }\mu\text{m}$, e) $L = 20 \text{ }\mu\text{m}$, and f) $L = 30 \text{ }\mu\text{m}$.

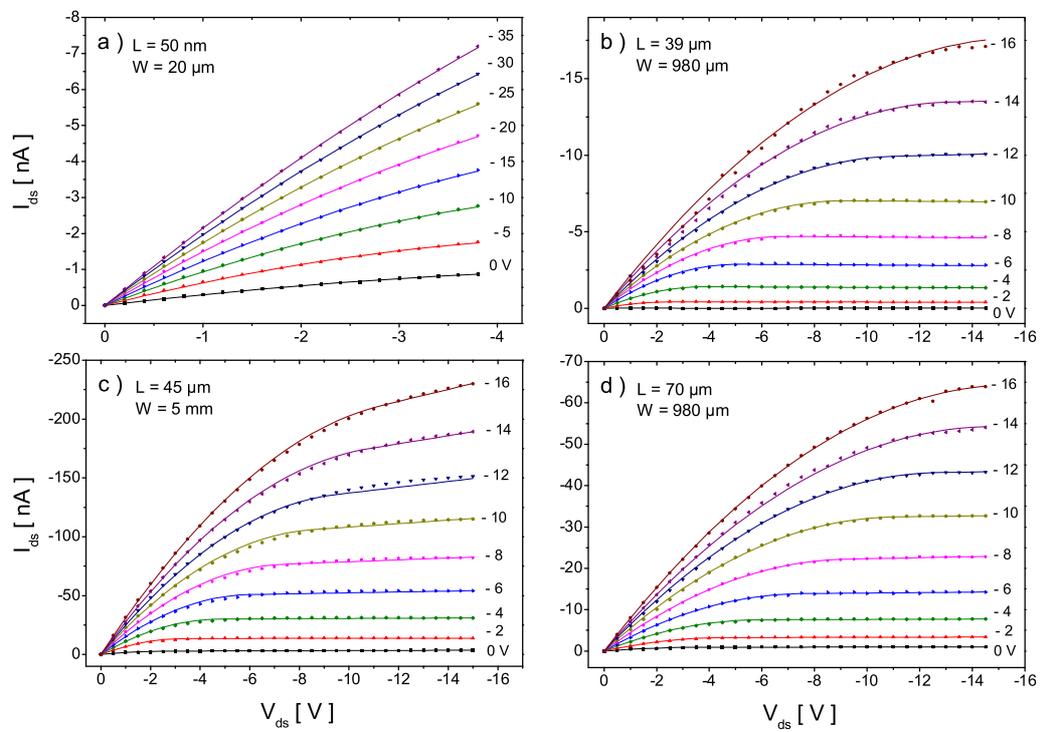


Figure 3.4: Output characteristics of DH4T FETs prepared by spin coating. a) $L = 50$ nm, b) $L = 39$ μm , c) $L = 45$ μm and d) $L = 70$ μm .

clockwise and minimal with a mean relative error of 8% for $V_{ds} < 0$. In addition to $I_{ds} - V_{ds}$ curves, the transfer characteristics were measured in the linear region. Figure 3.5b shows the transfer curve for the same device measured at $V_{ds} = -4$ V.

The stability in ambient conditions was monitored in a device with $L = 26$ μm and $W = 980$ μm prepared by drop casting. The time evolution of I_{ds} was measured for applied V_{ds} and V_g in the form of square pulses as shown in Figure 3.6. The maximum bias voltages were $V_{ds} = V_g = -16$ V and were applied during 5 s before the measurement with a period of approximately 30 s as shown in the inset. The measurement was started 18 hours after casting and was performed during 80 hours (with a pause of 3 hours).

3.3 Gated Self-Assembled Layer Devices

We present here results for two devices in each of the experiments. The devices were electrically characterized at room temperature. Figure 3.7 shows the measured current-voltage characteristics of devices 1. Figures 3.8 shows results for a second measurement on the same device where the current has been decreased with respect to the first measurement. The next measurement was performed with positive gate voltages and as shown in the Figure 3.9 the same effect as for negative gate voltages was found. A second type of curves was obtained for device 2 and is shown in Figure 3.10. Here we observe low modulation and the presence of peaks.

Figure 3.11 shows the I-V characteristics of device 3 prepared with the same conditions than the previous, except that the immersion time for self-assembly was 24

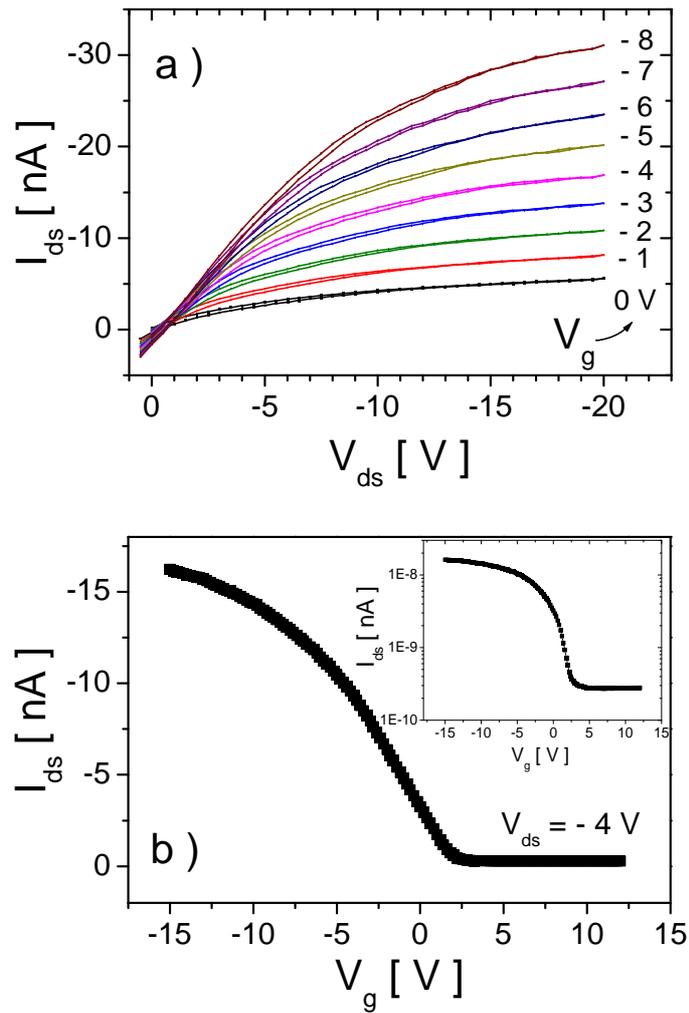


Figure 3.5: Current voltage characteristics for device 2. a) Bi-directional scan of the drain-source voltage for each gate voltage showing clockwise hysteresis and b) transfer characteristics of the same device measured at $V_{ds} = -4$ V in the linear region. The inset on b) shows the data in logarithmic scale.

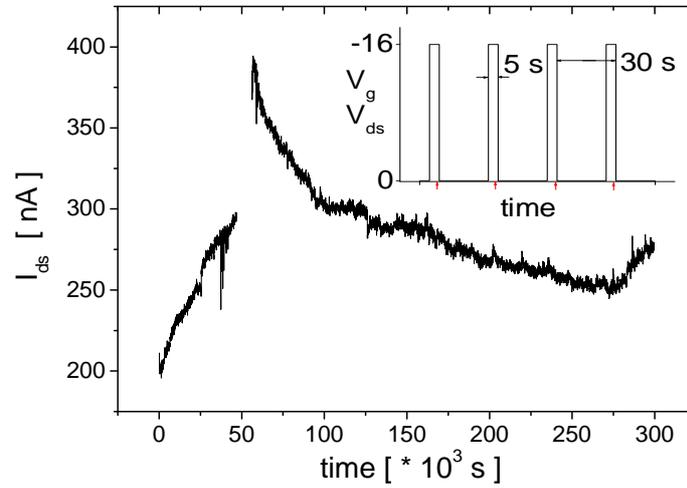


Figure 3.6: Time dependence of the drain-source current of a device with $L = 26 \mu\text{m}$ and $W = 980 \mu\text{m}$ prepared by drop casting. V_{ds} and V_g were applied as square waveforms as shown in the inset. A maximum voltage of -16 V for both V_{ds} and V_g was applied during 5 s before measurement (the measurement was interrupted during 3 hours).

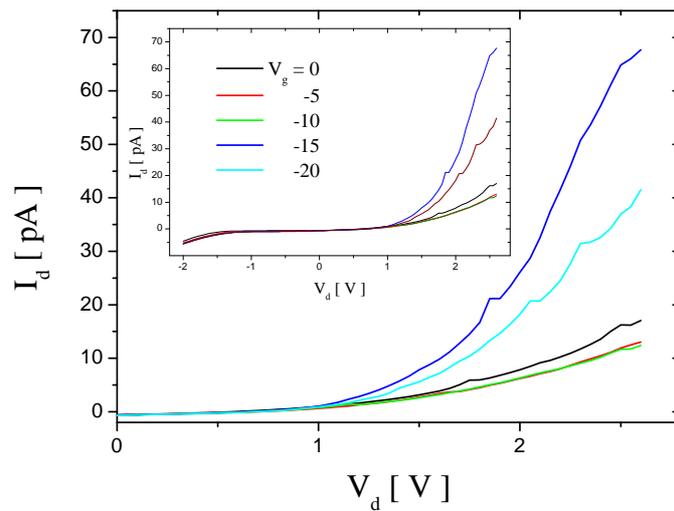


Figure 3.7: Modulation of the current-voltage characteristics of device 1 for several negative gate voltages.

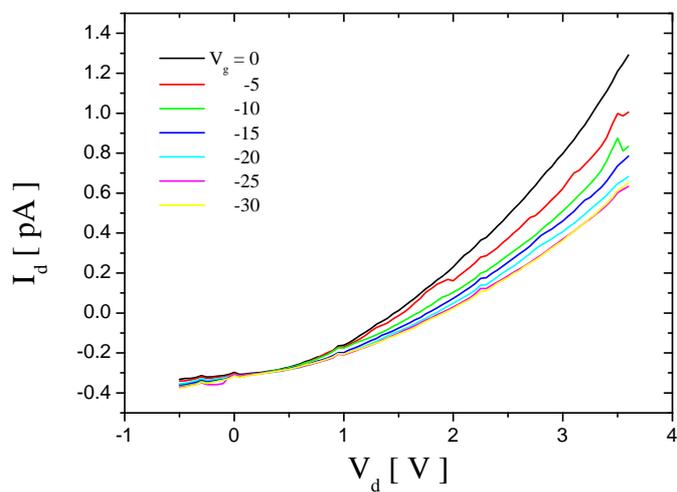


Figure 3.8: Second measurement of the current-voltage characteristics of device 1. The gate voltages were negative.

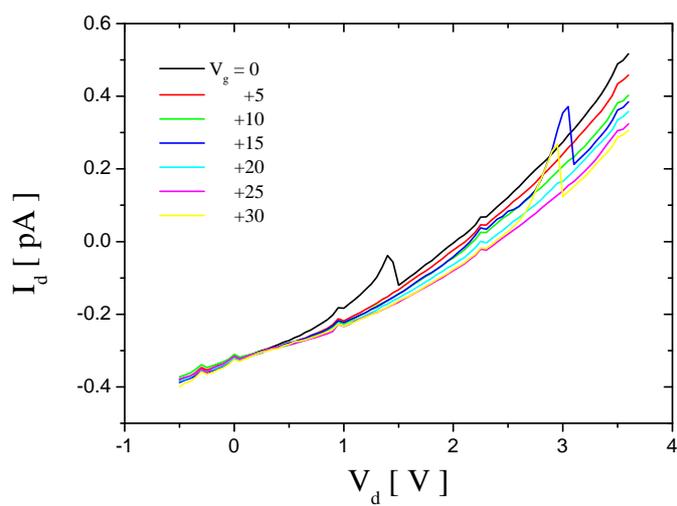


Figure 3.9: Current-voltage characteristics of device 1. This measurement was performed with positive gate voltages.

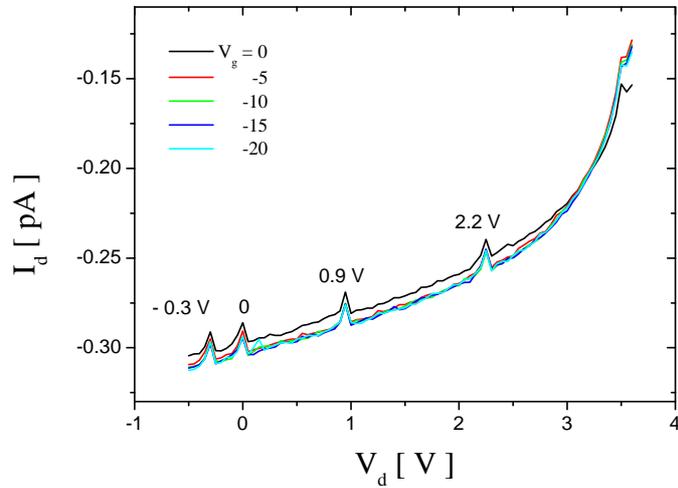


Figure 3.10: Current-voltage characteristics of device 2 with negative gate voltages applied to the gate.

hours only. It is observed that a high current, in the range of mA, flows through the device leading to breakdown of the high conductivity channel. Figure 3.12, shows the current after breakdown where it can be seen that it is of the same type than for device 1. Finally, Figure 3.13 shows the I-V characteristics for device 4 where peaks can be observed over a noisy background as for device 2.

3.4 Discussion

The experimental results from the electrical characterization of solution-processed DH4T OFETs and of devices based on self-assembled films of DH4T will be discussed here.

Non-saturating output characteristics at high V_{ds} were obtained for drop cast OFETs as opposed to the case of most of the spin coated devices. When using spin coating,

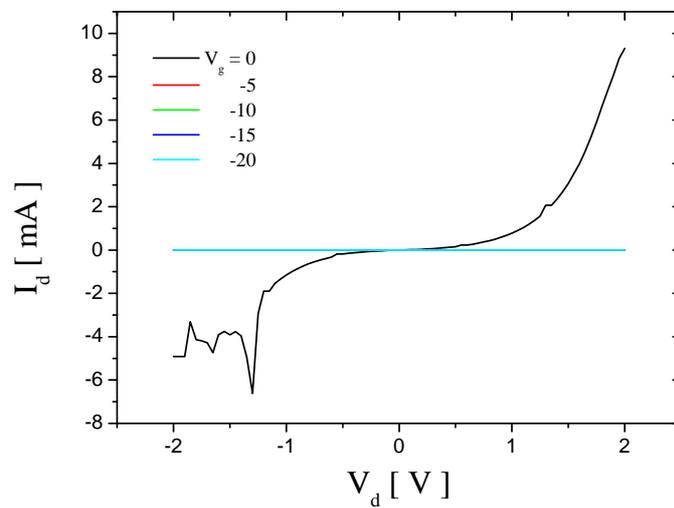


Figure 3.11: I-V characteristics of device 3. Breakdown of a high conductivity channel is observed.

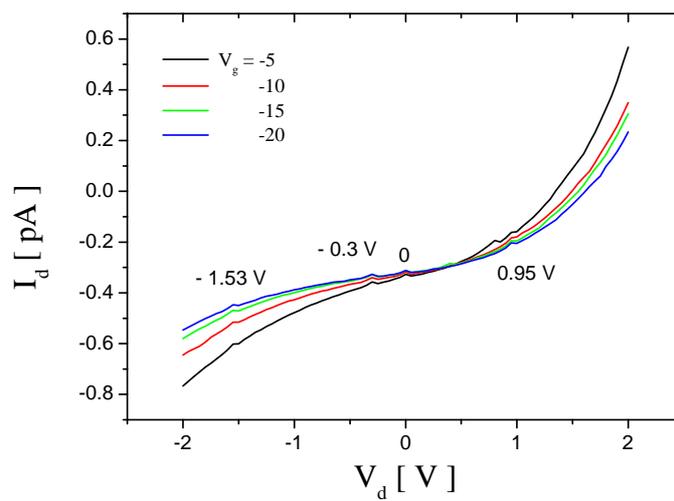


Figure 3.12: I-V characteristics of device 3 after breakdown.

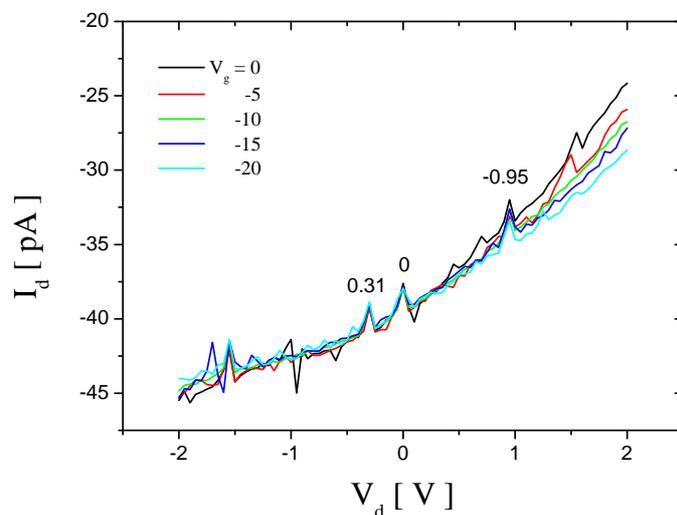


Figure 3.13: I-V characteristics of device 4. This is similar to what was observed for device 2.

only the shortest channel length device exhibited non-saturating current-voltage characteristics. We proposed that this phenomenon is caused by the interplay between the contributions to the total device current from the currents flowing through i) the accumulation layer at the semiconductor-insulator interface and ii) through the bulk of the organic semiconductor. Therefore, thin films prepared by spin coating lead to devices with current-voltage characteristics dominated by field effect, i.e. the current flowing through the accumulation layer. This is true for devices where the channel length is much higher than the film thickness. On the other hand, for the thick drop-cast devices, the contribution from the bulk of the semiconductor is always comparable to the one of the accumulation layer.

The output characteristics of the molecular devices based on self-assembled films of DH4T are discussed next. Few devices presented short circuits probably because of

the presence of pinholes on the organic layer. The I-V characteristics are asymmetric and some of them show nearly rectification properties: the current flows only in one direction but it is not linear and it is noisy. In this case, the equivalent of the anode is the electrode where molecules are self-assembled. A modulation of the current flowing through the DH4T layer by the voltage applied to the gate terminal was observed in a first group of devices. The modulated current depended on the absolute value of V_g and not on its sign. For a second group of devices, some peaks in the current-voltage characteristics appear at certain values of V_{ds} and no modulation was observed.

The modulation of the device current $\partial I_{ds}/\partial V_g$ is probably the result of changes on the electronic states of molecules close to the edges of the overlapping source, drain and gate electrodes (from point A to C in Figure 2.19). One of the reasons for the low gain is the low ratio between the length of the arc AC to the surface of the area sandwiched between source and drain. An improvement is expected from optimization of the device geometry, for example, using thin rectangular metal strips with increased perimeter to area ratio. Moreover, additional improvement of the modulation is expected by using a thinner insulator.

The reason for the dependence of the source-drain current on the absolute value of V_g and not on its sign is that this type of devices does not work by means of an accumulation layer but by modification of the molecular electronic levels under the application of an external field. The dips observed in some cases are probably related to electron reduction processes that take place when the external potential equals the molecular electron affinity [52].

3.5 Summary

In summary, this chapter treats the electrical characterization of the fabricated organic electronic devices. First, the experimental set-up and the conditions used in this work were described. Then, the results of the measurements of the current-voltage characteristics of solution-processed DH4T OFETs with channel lengths ranging from 70 μm down to 50 nm were given. Non-saturating output characteristics were found for devices with thick organic semiconductor layers compared to the channel length. This is observed for all drop cast devices as well as for the 50 nm channel length spin coated device. Finally, the measured current-voltage characteristics of gated self-assembled DH4T layer devices were presented. In this case, modulation of the current flowing through a self-assembled layer of DH4T by a gate voltage was observed.

Chapter 4

Models for Transport and Current-Voltage Characteristics

Several models for the physical processes involved in the operation of the organic field-effect transistors are considered in this chapter. First, the models for charge transport in organic semiconductors and their application to the understanding of the temperature and electric field dependence of the mobility in OFETs are reviewed. Finally, a model to explain the occurrence of non-saturating output characteristics of OFETs (Section 3.2) is proposed.

A modified model is necessary because the output characteristics of the fabricated devices are influenced by the contribution of the bulk of the semiconductor in addition to the accumulation layer to the total device current. This fact is not accounted for in the standard MOSFET model (Section 1.2.3). The model also includes explicitly a contact resistance.

4.1 Models for Charge Transport in films of organic semiconductors

Charge transport in organic semiconductors is a very complex phenomenon. The behavior of organic semiconductors may vary drastically depending on the range of the physical parameters such as temperature, charge carrier density, electric field intensity, energy distribution of carriers, correlation of charge carriers and filling of energy bands. Moreover, it can be further complicated by experimental factors such as presence of charge traps and material inhomogeneity.

The transport mechanisms may vary from band-like transport for highly ordered single-crystal organic semiconductors to hopping transport for amorphous ones, depending on the material and its preparation. Nevertheless, from the application point of view the obtained films can be divided in a) partially ordered, obtained from careful vacuum deposition, and b) amorphous films from solution process.

We will start by summarizing the main ideas and results of general transport models for disordered semiconductors. Some of them were originally proposed to describe amorphous silicon, while more recent publications have used them to explain the experimentally observed dependences of mobility on electric field and temperature on organic electronic devices.

First, we will review the model of hopping transport in an energetically disordered and positionally random system by Bässler and coworkers based on Monte Carlo simulations. Next, we will review the small polaron model of Holstein and the Poole-Frenkel model for the electric field dependence of mobility. Finally, the Multiple trapping and

release (MTR) of Le Comber and the Variable range hopping (VRH) of Mott.

4.1.1 Monte Carlo Simulations of Hopping Transport in a Disordered System

Bässler et al. [5] developed a model for charge transport in disordered organic semiconductors that predicts temperature and electric field dependence of mobility using Monte Carlo (MC) simulations. This model is suitable for molecular and polymeric materials. The energy states are supposed to be localized on the molecules or segments of polymers separated by topological defects.

The existence of positional disorder will induce energetic disorder as well, because the potential energy of interaction depends on the relative distances of neighboring particles. Energetic disorder, known as *diagonal* disorder, is originated from fluctuations in polarization energies and the distribution of molecular-segment lengths in polymers. The density of states (DOS) distribution is chosen to be Gaussian and this is motivated by the observed Gaussian profile of absorption bands.

$$\varrho(\varepsilon) = \frac{1}{2\pi\sigma^2} \exp\left(-\frac{\varepsilon^2}{2\sigma^2}\right), \quad (4.1)$$

where ε is measured with respect to the center of the DOS and σ is the width of the distribution. Equation 4.1 assumes that the self-energies of neighboring sites are uncorrelated.

The hopping rate from site i to j (with energies ε_i and ε_j respectively) is given by

the Miller-Abrahams factor

$$\nu_{ij} = \nu_0 \exp\left(-\frac{\Gamma}{a}\Delta R_{ij}\right) \begin{cases} \exp\left(-\frac{\varepsilon_j - \varepsilon_i}{kT}\right); & \varepsilon_j > \varepsilon_i, \\ 1 & \varepsilon_j < \varepsilon_i. \end{cases} \quad (4.2)$$

which contains a wavefunction overlap factor, and a Boltzmann factor for jumps upward in energy. Here a represents the average lattice distance, Γ the wavefunction overlap parameter and ΔR_{ij} the distance from site i to j . Equation 4.2 assumes that electron-phonon coupling is weak enough to make polaronic effects negligible.

The disorder associated with the distribution of the wavefunction overlap parameter, $\Gamma = 2\gamma a$, is known as *off-diagonal* disorder.

First, we will consider the temperature dependence of the mobility. Experimental studies of the temperature dependence of mobility show an Arrhenius temperature dependence

$$\mu(T) = \mu_0 \exp\left[-\left(\frac{\sigma}{kT}\right)^2\right] \quad (4.3)$$

This temperature dependence is also found with MC simulations except for the factor in the exponent. This is a better approximation for the temperature dependence of mobility because the extrapolation of μ at $T \rightarrow \infty$ gives more realistic values than with the Arrhenius relationship:

$$\mu(T) = \mu_0 \exp\left[-\left(\frac{2}{3}\hat{\sigma}\right)^2\right]. \quad (4.4)$$

Here $\hat{\sigma} = \sigma/kT$. The numerical factor $2/3$ accounts for uncertainties in occupational energies and energy barriers.

Second, the results for the field dependence of mobility will be summarized. The application of an electric field modifies the hopping transport characteristics because

the DOS is tilted by the applied potential reducing the average energy barrier for upward jumps in energy in the direction of the field.

The variation of μ with E for a hopping system, affected only by energetic disorder, has the following characteristics.

- The $\ln \mu$ versus $E^{1/2}$ plot has an S shape for a finite $\hat{\sigma}$ ($\hat{\sigma} = \sigma/kT$).
- Mobility saturates at low E and increases following the Poole-Frenkel law ($\ln \mu \propto E^{1/2}$) with small deviations at higher fields.
- For vanishing disorder, μ decreases with E at large values of E . This is related to the saturation of the drift velocity with field in a hopping system with isoenergetic sites where the jump rates are not affected by the field.

The presence of energetic disorder (Gaussian DOS) in the hopping system is sufficient to reproduce the Poole-Frenkel behavior in a limited field interval.

Incorporation of off-diagonal disorder modifies the shape of the field dependence of mobility in the following way:

- The low-field part of the $\mu(E)$ plot tends to bend upwards for increasing Σ (variance of the overlap parameter, $\Sigma = 2\sqrt{\sigma_{\Gamma}}$) leading to a mobility that decreases with increasing field.
- In the Poole-Frenkel regime the slope of the curve decreases and eventually becomes negative.

Fluctuations of the overlap parameter give rise to an asymmetric variation of the factor controlling the exchange rate of carriers. This phenomenon is similar to percolation

where certain direct transport routes will be less favorable due to poor inter-site coupling but are compensated by the opening of easy channels.

The effect of decreasing μ with increasing E is compensated at larger fields by the field effect on the energy barriers along the direction of the field. A weaker increase of μ with E than in the absence of off-diagonal disorder is recovered but keeping the $\ln \mu \propto E^{1/2}$ dependence. At the very high field limit, the disorder seen by the carriers vanishes. In this case a pure hopping system with excluding backward jumps is obtained where $\mu \propto E^{-1}$.

4.1.2 The Small Polaron

An important model to describe charge transport in organic semiconductors is the *small polaron* model from Holstein [39]. It is a one dimensional, single electron model for the problem of electron conduction coupled to lattice vibrations. In this model the total Hamiltonian is expressed as the sum of three contributions

$$H = T + EP + H_L , \quad (4.5)$$

where T is the electron kinetic energy, EP the electron-phonon coupling energy and H_L is the lattice Hamiltonian. In the second quantization notation, i.e. making use of

creation (c_i^\dagger, b_i^\dagger) and annihilation (c_i, b_i) operators (for electrons and phonons respectively), the terms in Equation 4.5 can be expressed as

$$T = -t \sum_{i,j} \left(c_i^\dagger c_j + c_j^\dagger c_i \right) \quad (4.6)$$

$$EP = -\sqrt{\varepsilon_n \hbar \omega} \sum_i \left(b_i^\dagger + b_i \right) c_i^\dagger c_i \quad (4.7)$$

$$H_L = \hbar \omega \sum_i \left(b_i^\dagger b_i + \frac{1}{2} \right) \quad (4.8)$$

where ε_n is the electron-phonon coupling constant. The following assumptions are made:

- Electron transfer is restricted to nearest neighbors.
- Charge carriers are locally coupled to a dispersionless optical phonon mode.
- Phonons are treated in the harmonic approximation.

For comparison, the lattice hamiltonian in the spacial coordinate u_n , the atomic (molecular) displacement from the equilibrium position at site n , is given by

$$H_L = \sum_{n=1}^N \frac{1}{2M} \left(\frac{\hbar}{i} \frac{\partial}{\partial u_n} \right)^2 + \frac{1}{2} M \omega_0^2 u_n^2, \quad (4.9)$$

where M is the reduced atomic (molecular) mass.

The tight-binding approximation is used for the electronic kinetic energy. The resulting dispersion relation is given by

$$E_k = E_0 - 2J \cos(ka), \quad (4.10)$$

where a is the lattice parameter and J the electron transfer energy constant. The electron-lattice coupling is given by

$$\varepsilon_n = -A u_n, \quad (4.11)$$

where A is a constant.

An important parameter appearing in the Holstein model is the polaron binding energy that is given by

$$E_b = \frac{A^2}{2M\omega_0^2} \quad (4.12)$$

The small polaron limit corresponds to the case when the electronic bandwidth $2J$ is small compared to the polaron binding energy. In this case the electronic term can be treated as a perturbation. The solution of the time-dependent Schrödinger equation in the high temperature limit $T > \Theta$ ($\Theta = \hbar\omega_0/k$ is the Debye temperature) is given by

$$\mu = \sqrt{\frac{\pi}{2}} \frac{e a^2}{\hbar} \frac{J^2}{\sqrt{E_b}} (k T)^{-3/2} \exp\left(-\frac{E_b}{2kT}\right) \quad (4.13)$$

4.1.3 Poole-Frenkel Model

The field dependence of the mobility at electric fields higher than approximately 10^5 V/cm can be explained by the Poole-Frenkel model [30, 60]. The model considers ionized electrons moving in a medium composed of neutral polarizable atoms in the field of the remaining positive ion. It is assumed that under the application of an electric field F , the potential energy is decreased by the dipolar energy and the attractive Coulomb energy

$$\Delta U = eFr_0 + \frac{e^2}{\epsilon\epsilon_0 r_0} \quad (4.14)$$

Here, r_0 is the distance from the ion to the maximum of the curve energy versus distance (U vs. r). The value of r_0 can be calculated using the Coulomb law assuming the electron is at the mentioned maximum. If the density of thermally excited carriers has an ionization energy U_0 when the applied field is zero, then under the application

of F we have

$$\mu(F) \propto \exp[-(U_0 - \Delta U)/2kT] . \quad (4.15)$$

Finally, the temperature dependence of the mobility can be expressed as

$$\begin{aligned} \mu(F) &= \mu(0) \exp\left(\frac{\beta}{kT} \sqrt{F}\right) \\ \beta &= \sqrt{\frac{e^3}{\epsilon\epsilon_0}} \end{aligned} \quad (4.16)$$

where $\mu(0)$ is the zero-field mobility and β is the Poole-Frenkel factor. The effect of U_0 has been neglected in comparison to ΔU because this energy is reduced by screening.

In summary, the Poole-Frenkel mechanism results from a decrease on the thermal ionization energy (by the factor ΔU) due to the modification of the electric potential near the localized level caused by the applied electric field.

4.1.4 Multiple Trapping and Release

In the Multiple Trapping and Release (MTR) model [20] transport results from conduction of carriers in a narrow-delocalized band interacting with some associated localized levels that act as traps. The assumption is made that most of the charge carriers are trapped in localized states, and that the quantity of temporally released carriers to extended-state transport levels depends on the energy level of the localized states, temperature and gate voltage.

The expression relating the drift mobility μ_D in this kind of system to the band mobility μ_0 is given by

$$\mu_D = \mu_0 \alpha \exp\left(-\frac{E_t}{kT}\right) \quad (4.17)$$

where a is the ratio of the effective density of states at the delocalized band edge to the concentration of traps, and E_t is the energy difference between the delocalized band edge and the trapping level.

4.1.5 Variable Range Hopping

Here we will present the Mott's concept of variable range hopping of localized electrons. This model is based in phonon-assisted tunneling of localized electrons between different sites. It was found that at low temperatures the typical hopping length R_M increases with decreasing temperature. This is the origin of the term "variable range hopping".

In crystalline systems the periodic potentials imply that electrons are delocalized (Bloch waves). The presence of impurities and lattice defects in disordered systems introduce backward scattering of the electron waves resulting in Anderson localization.

Energy fluctuation in random potentials broadens the electronic bandwidth and creates smooth "band tails" which may overlap closing the original bandgap. This results in a finite density of states at the Fermi level $N(E_F)$. This model is applicable to systems with strong disorder such that the disorder energy is much greater than the bandwidth.

According to the model the temperature dependent conductivity for a three-dimensional system can be expressed as

$$\sigma = \sigma_0 \exp \left[-(T_0/T)^{1/4} \right] \quad (4.18)$$

and

$$T_0 = c/(kN(E_F)L^3) \quad (4.19)$$

where c is a proportionality constant, k the Boltzmann constant, L the localization length, and σ_0 is a temperature independent factor.

4.2 Application of the Transport Models to Organic Field-Effect Transistors

The most important models to describe charge transport in organic semiconductors were studied in Section 4.1. Here we deal with the application of these models to the case of OFETs. The treatment is split in temperature and field dependence of the mobility. Even though the practical devices are expected to work at room temperature, the temperature dependence of the mobility is important to determine whether or not a transport mechanism is playing a role for certain material and processing conditions. On the other hand, in the OFET configuration, the material is exposed to varying electric fields created by the gate and drain biases.

4.2.1 Temperature Dependence

Organic semiconductor layers prepared on a first series of devices when the deposition techniques were not refined were disordered and the results were compatible with a thermally activated mobility and the transport mechanism was well described by the hopping through localized states model [5, 80, 79].

Waragai et al. [80] tried several models for the temperature dependence of mobility on evaporated end-substituted oligothiophenes (DM4T, DM5T, DM6T) FETs. They first investigated the temperature dependence of the mobility using the Arrhenius, super-Arrhenius relationships and the variable-range-hopping model to fit their experimental data from which the simple Arrhenius relationship proved to explain the results more accurately. The complete expression used to model the mobility was

$$\mu = \mu_0 \exp\left(-\frac{W_0 - \beta^* \sqrt{F}}{kT}\right) \quad (4.20)$$

where W_0 is the zero field activation energy and μ_0 the mobility extrapolated at $T \rightarrow \infty$.

A relationship between transport and optical properties was derived based on the polaron theory of conduction

$$4W_0 \approx \omega_{photon} \quad (4.21)$$

W_0 is the zero-field activation energy and ω_{photon} is the peak energy of the lowest-energy optical transition in the subgap region. The relation $4W_0 \approx \hbar\omega_{photon}$ was approximately satisfied experimentally for the oligothiophenes from DM4T to DM6T in that work. This is considered as evidence that hopping of polarons is the mechanism underlying charge transport in those materials.

The development of new techniques for refinement and growth make it possible to prepare molecular single crystals. For these highly ordered organic semiconductors, the mobility depends on temperature as conventional semiconductors do, decreasing with temperature following a negative power law. Band-like transport was assumed to be the important mechanism of conduction in highly ordered organic semiconductors and low temperatures. Under these conditions (below 250 K) mobilities as high as 1000

$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ have been reported.

As the temperature increases, phonon scattering becomes dominant because the binding energy of the molecules is comparable to the thermal energy. Therefore, the contribution of the band mechanism to transport becomes very small and hopping of carriers from site to site becomes the dominant mechanism. At room temperature, the upper limit for the mobility of highly ordered organic semiconductors, determined by time-of-flight measurements, is between 1 and $10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [24]. The combination of band-like and hopping mechanisms of conduction, explain the experimentally observed temperature dependence of mobility in OFETs made up of highly ordered organic semiconductors. Horowitz used the MTR model [42] to explain that two different mechanisms, involving localized and delocalized states, account for the experimentally observed temperature dependence of the mobility. In that model, charge transport occurs in delocalized bands that are associated to localized levels that behave as shallow traps. Charges in the delocalized bands interact with the localized levels through trapping and thermal release. Even though the MTR model predicts satisfactorily the magnitude of the mobility, it cannot predict the experimentally observed temperature independent mobility at low temperatures.

In order to explain the temperature dependence of mobility at low temperatures, Horowitz [40] proposed a model based on a tunneling current in polycrystalline OFETs. The model considers the polycrystalline film as a composite of crystalline grains and grain boundaries. At high temperatures, the grain boundaries are considered as resistors that dominate charge transport. On the other hand, at low temperatures, the grain boundaries are considered as Schottky barriers connected back to back . This

model explains the temperature independence of mobility at low temperatures because in this regime tunneling becomes dominant.

4.2.2 Electric-Field Dependence

Several interpretations have been given to explain the mobility dependence on gate bias and more generally its dependence on electric field. For instance, according to these interpretations, gate bias dependant mobility appears as a result of charge transport limited by traps [42], variation in carrier concentration in the accumulation layer [43, 72] or by a variable range hopping mechanism [79]. The last seems to be the most adequate for solution processed organic semiconductors and predicts $\mu \propto V_g^{2T_0/(T-1)}$ [79]. Alternatively, it has been shown in the framework of the model for hopping in a Gaussian DOS [5] that a Poole-Frenkel or $\ln \mu \propto E^{1/2}$ behavior is found in a restricted range of applied fields and degrees of disorder. Nevertheless, for vanishing disorder and high electric fields decreasing mobility with increasing electric field was found. This behavior was ascribed to saturation of the drift velocity [5] with field.

Holstein Model

In highly ordered semiconductor films of oligothiophenes for example or molecular crystals in general, charge transport can be described in terms of small polarons (Section 4.1.2). In this model electrons and holes become self-trapped polarons due to their strong coupling to the molecule vibrations. and the mobility increases with electric field as $\mu \propto \sqrt{F}$.

Multiple trapping and release model

The MTR model of Horowitz Ref. [42] is based on Le Comber's model (Section 4.1.4). In this model, gate-voltage dependence of mobility arises from the amount of released charges localized in traps. The quantity of released charge depends on the Fermi level at the insulator semiconductor interface that is modulated by the gate voltage. The drawback of this model is that the required extended states are not likely to occur in polycrystalline molecular materials.

Variable range hopping

Vissemberg and Matters [79] obtained an analytical expression for the field-effect mobility in transistors made up of amorphous organic semiconductors based on percolation model of hopping between localized states. Charge transport is described by a variable range hopping mechanism (Section 4.1.5) through an exponential density of states (DOS).

$$\mu = \frac{\sigma_0}{e} \left(\frac{\pi (T_0/T)^3}{(2\alpha)^3 B_c \Gamma(1 - T/T_0) \Gamma(1 + T/T_0)} \right)^{T_0/T} \left[\frac{(C_i V_g)^2}{2k_B T_0 \epsilon_s} \right]^{T_0/T-1}, \quad (4.22)$$

The fitting parameters are the preexponential factor to the conductivity σ_0 , the overlap parameter α^{-1} , and the width of the exponential distribution of localized states T_0 . This model was used to analyze transfer characteristics of pentacene and PTV OFETs. The experimental temperature dependence of the field-effect mobility follows the Arrhenius relationship and the considered model fits well to the data. The experimentally observed differences between pentacene and PTV are reflected mainly in the value of the overlap parameter (2.2 Å for pentacene and 0.8 Å for PTV). It is concluded that

the difference in magnitude and temperature dependence of the mobility of pentacene and PTV comes from differences in the structural order of the organic films (α^{-1}) rather than from σ_0 or T_0 .

Charge-carrier concentration dependence of mobility

An alternative explanation for the gate-voltage dependence of mobility is based on the fact that charge carrier concentration in the accumulation layer is controlled by the gate voltage.

Horowitz in Ref. [43] found that the mobility of oligothiophene field-effect transistors increased quasilinearly with gate voltage. The thickness of the accumulation layer is around one Debye length. Therefore, most of the charge is contained in one or two monolayers close to the insulator even at high gate voltages. An increase in gate voltage leads to a linearly increasing charge carrier concentration. Therefore, the apparent mobility dependence is in fact a charge carrier concentration dependence.

In a similar way, Shaked et al. [72] explain the gate voltage dependence of mobility on poly(2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylenevinylene) (MEH-PPV) in terms of charge carrier density variation. They used a Monte Carlo model of hopping transport in a disordered system from Rakhmanova et al. [63] where a short-range correlation between the energies of the hopping sites is introduced.

The analytical model developed by Arkhipov et al. in Ref. [2] considers the effect of deep traps and partly filled DOS and predicts a charge density dependence of the mobility. If in the semiconductor material there exist high densities of charge carriers and doping levels, as in the case of the accumulation layer of OFETs, the energy states

on the tail of the DOS distribution are fully filled by carriers. Filling modifies the energy distribution of localized carriers and vacant hopping sites in such a way that μ will depend on the density of charge carriers.

4.3 Model for the output characteristics of OFETs

In general, the field-effect mobility of OFETs is estimated from the transconductance (g_m) at low drain-source voltages in the constant mobility regime

$$g_m = \left(\frac{\partial I_{ds}}{\partial V_g} \right)_{V_{ds}=\text{const.}} = \frac{W}{L} \mu C_i V_{ds} , \quad (4.23)$$

Nevertheless, this simplified method may give wrong values for μ_{FE} in devices with relative high bulk conductance.

In this section we develop a model for the output characteristics of OFETs in which the bulk of the organic semiconductor, in addition to the accumulation layer, contributes to the total device current. Additionally, the metal-semiconductor contact resistance is considered explicitly.

The behavior of this type of devices can be understood assuming two contributions to the total mobility. First, the field-effect mobility (μ_{FE}) due to accumulation and transport of carriers on the semiconductor-insulator interface, and second, the bulk mobility. The accumulation layer is so thin, for the typical conditions used in device fabrication, that it is contained in the first DH4T monolayer next to the insulator [40]. The effect of the bulk mobility can be accounted for by representing the bulk by a resistor (R_b) connected in parallel to the accumulation layer as shown in Figure 4.1. The contact resistance is also taken into account in the model and is represented by

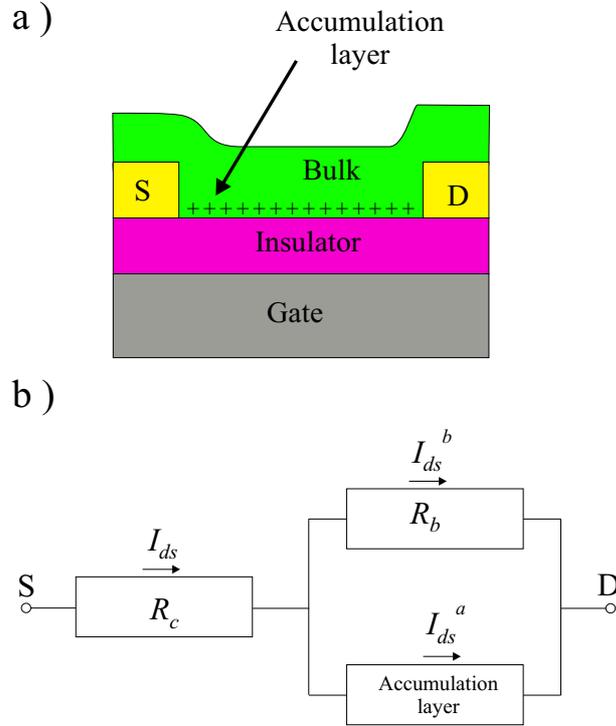


Figure 4.1: a) OFET structure where the organic semiconductor is split into the accumulation layer at the insulator-semiconductor interface and the bulk. b) The equivalent circuit for constant V_g showing the bulk (R_b) and contact (R_c) resistances.

R_c . Under these assumptions, the total drain-source current (I_{ds}) is the sum of the current through the accumulation layer (I_{ds}^a) plus the current across the bulk (I_{ds}^b).

$$I_{ds} = I_{ds}^a + I_{ds}^b \quad (4.24)$$

For the current along the accumulation layer, the standard equations for FETs in the gradual-channel approximation and at low drain-source bias holds

$$I_{ds}^a = \frac{W}{L} C_i \mu \left(V_g - V_0 - \frac{1}{2} (V_{ds} - I_{ds} R_c) \right) (V_{ds} - I_{ds} R_c) , \quad (4.25)$$

where L is the channel length, W the channel width, C_i the capacitance per unit area of the insulating layer, μ_{FE} the field-effect mobility, V_g the gate voltage and V_t is the

threshold voltage. The voltage drop on the contact resistance is accounted for by writing $V_{ds} - I_{ds}R_c$ instead of V_{ds} .

Using Equations 4.24 and 4.25 and solving for I_{ds} , we find an expression for the output characteristics in the low-drain-source voltage regime of operation that includes the bulk conductance, and the contact resistance:

$$I_{ds} = a_1 + a_2V_{ds} - \sqrt{a_1^2 + a_3V_{ds}} , \quad (4.26)$$

$$a_1 = -\frac{L + LR_c/R_b + CR_c(V_g - V_0)W\mu_{FE}}{CR_c^2W\mu_{FE}} , \quad (4.27)$$

$$a_2 = \frac{1}{R_c} , \quad (4.28)$$

$$a_3 = -\frac{2L}{CR_c^3W\mu_{FE}} . \quad (4.29)$$

Coefficients a_i can be found from a nonlinear fit ¹ of the experimental data to Equation 4.26.

The contact resistance and μ_{FE} can be calculated from Equations 4.28 and 4.29

$$R_c = \frac{1}{a_2} , \quad (4.30)$$

$$\mu_{FE} = -\frac{2La_2^3}{C_iWa_3} . \quad (4.31)$$

In a similar way, for the region that would normally correspond to saturation we have

$$\begin{aligned} I_{ds}^{\text{sat}} &= \frac{1}{1 + R_c/R_b} \left(\frac{V_{ds}}{R_b} + \frac{C_i(V_g - V_0)^2W\mu_{FE}}{2L} \right) , \\ &= b_1V_{ds} + b_0 , \end{aligned} \quad (4.32)$$

¹Nonlinear fits were performed using the MATHEMATICA software © Wolfram Research

from which the remaining parameters can be calculated as:

$$R_b = b_1^{-1} - R_c, \quad (4.33)$$

$$V_0 = V_g + R_c a_1 + \frac{L + LR_c/R_b}{CR_c W \mu_{FE}}. \quad (4.34)$$

Alternative calculation methods including the effects of the contact resistance in OFETs have been proposed by Horowitz et al. [43] and Meijer et al. [56]. These methods were treated in Section 4.3.

4.4 Discussion

A number of models have been proposed in order to describe the process of charge transport in organic semiconductor samples. While all of them take into account the inherent disorder of the resulting organic semiconductor films, none of them is able to explain the complex dependence of the mobility on temperature and field in their entire ranges. The difficulty arises from the fact that the physical processes involved in transport depend on the details of the materials employed as well as on their deposition method. Nevertheless, the models reviewed in this chapter are the most successful in their application to the analysis of the temperature and electric field dependence of the mobility in the range of device applications and for the most commonly used materials in OFETs.

The analysis of the current-voltage characteristics of OFETs based on solution-processed DH4T requires that the current flowing through the bulk of the organic semiconductor be considered. The mobility of the bulk of the semiconductor film is an important issue for low mobility materials since it can modify drastically the response

of the devices even for $V_g < 0$ in p-type OFETs.

The model developed in this chapter is based on the idea of subtracting the current flowing through the bulk of the organic semiconductor from the measured drain-source current in order to extract the mobility related only to field effect. Furthermore, the contact resistance is considered explicitly because at short channel lengths it becomes comparable to the channel resistance.

Fitting the measured output characteristics to this model will allow extracting the model parameters for the devices as will be shown in Chapter 5. The model parameters are: field-effect mobility, threshold voltage, contact and bulk resistances.

4.5 Summary

Different models to explain the charge transport mechanisms in organic semiconductors were considered in this chapter. For solution processed organic semiconductors the most probable mechanism is hopping through localized states. The predictions of the temperature and electric field dependence given by these models were considered as well as their application to the OFET configuration. Finally, a modified model for the output characteristics of solution processed DH4T OFETs was proposed. This was necessary because in this type of devices, conduction through the bulk of the organic semiconductor plays an important role that needs to be considered. The current flowing through the bulk of the organic semiconductor adds to the current flowing through the accumulation layer and produces non-saturating output characteristics. The model also includes the contact resistance, which becomes important for short channel length

devices.

Chapter 5

Discussion

The objective of this thesis concerns the fabrication and characterization of DH4T OFETs with channel lengths ranging from tens of micrometers down to sub-100 nm.

The main differences in the operation of organic FETs with respect to their inorganic counterparts are the nature of the metal-semiconductor contacts and the role of the bulk of the organic semiconductor. Source and drain contacts to the organic semiconductors in OFETs are generally ohmic for hole injection [7] as opposed to standard Si metal-oxide-silicon FETs (MOSFETs) where only negligible reverse leakage of the back-to-back p-n junctions currents can flow [76]. Therefore, relatively low bulk mobilities are required in order to achieve low off-currents and high on-off, ratios important parameters in circuit applications [7, 55]. Meijer et al. [55] showed the existence of a crossover from field-effect dominated (for $V_g < 0$) to bulk-dominated current (for $V_g > 0$) in the transfer characteristics of spin-coated FETs. Therefore, the mobility of the bulk of the organic semiconductor is an important issue for low mobility materials since it can modify drastically the response of the devices even for $V_g < 0$ in p-type OFETs. Consequently, it was shown in Section 4.3 that the analysis of the current-voltage characteristics of OFETs based on solution-processed DH4T requires that the

current related to the bulk mobility is subtracted from the measured drain-source current in order to extract the mobility related only to field effect.

The results obtained from the fabricated OFETs and the extracted physical parameters are discussed in this section. The discussion will be split in three parts: i) surface treatment and morphology, ii) current-voltage characteristics and iii) field-effect mobility. Finally, the results of the electrical characterization of gated self-assembled layer devices are discussed.

5.1 Surface Treatment and Morphology

Surface treatment has been demonstrated to be crucial to improve device performance. Preliminary results on devices prepared without surface treatment were highly unpredictable and irreproducible. Cast-deposited DH4T films on untreated substrates were amorphous, presented 3D features, non-uniform thickness and coverage. Some of these devices did not show any field effect, and in general, the zero-gate-voltage current was relatively high and the on-off ratios low.

The performance of the OFETs was improved after incorporation of a surface treatment step with hexamethyldisilazane (HMDS) in the preparation procedure as explained in Section 2.6.1. Reaction of HMDS with the SiO_2 substrate leads to the formation of a SAM with methyl end groups. In particular, 100% of the devices prepared with the surface treatment showed field effect in contrast with approximately 60% for untreated samples. Additionally, the on-off ratios increased by approximately one order of magnitude. The improvement is related to an increase in the degree of

order of the semiconductor at the metal-semiconductor interface. Upon deposition of the DH4T molecules the hexyl groups interact with the methyl groups of the monolayer inducing self-organization.

DH4T films produced by spin coating have a uniform thickness of 25 nm for the conditions used in this work. On the other hand, the resulting cast films of DH4T can be described as a collection of layers that can form either ordered stacks or just overlap. The microcrystals can reach lengths of the order of 50 μm and reflect the tendency of anisotropic molecules to order with their most densely packed planes parallel to the substrate surface [29]. A condition for this kind of growth is that intermolecular forces are higher than interactions with the substrate surface [29]. In addition to the layered film, some three-dimensional features may appear. As a result, the thickness of drop-cast DH4T films is highly irregular and can vary between 1 and 50 μm . From AFM investigations, the layer thickness was found to be approximately 3 nm which implies that the 3.2 nm-long DH4T molecules are lying nearly perpendicular to the substrate [31]. This is the optimal orientation with respect to electrical transport in the OFET geometry because transport takes place along the packing direction of the π -orbital systems.

5.2 Current-Voltage Characteristics

A discussion of the current-voltage characteristics for the DH4T OFETs is given in this section. First, we discuss the observation of absence of a saturation region in the output characteristics of certain devices and the existence of non-ohmic contacts for

few of them. Next, the observed gate-voltage dependence of the device parameters is analyzed. Finally, the device instability in ambient conditions is treated.

For a wide enough V_{ds} measurement range, the output characteristics show a gradual change from a linear region at $V_{ds} \rightarrow 0$ to a saturation region ($dI_{ds}/dV_{ds} \approx 0$) at higher voltages. However, for some of the devices the slope dI_{ds}/dV_{ds} is not negligible. In order to classify the measured output characteristics we will make use of the device resistance R_{ON} defined in Ref. [51] as

$$R_{ON} = \left. \frac{\partial V_{ds}}{\partial I_{ds}} \right|_{V_{ds} \rightarrow 0, V_g = \text{const}}, \quad (5.1)$$

and

$$R_s = \left. \frac{\partial V_{ds}}{\partial I_{ds}} \right|_{V_{ds} \rightarrow V_{ds, \text{max}}, V_g = \text{const}}. \quad (5.2)$$

which is practically equal to R_b .

Therefore, the measured $I_{ds} - V_{ds}$ characteristics can be grouped into two types according to their shape (or the relation between R_{ON} and R_s at a given V_g). (I) Curves with $|R_{ON}/R_s| \ll 1$. This type of curves is well described by the MOSFET equation in the gradual channel approximation [76]. Devices 8, 9 and 10 belong to this group. (II) Curves exhibiting $|R_s|$ of the same order of $|R_{ON}|$. Devices in this category show relatively high off-currents. Devices numbered 1 to 6 are type II. In practice we used a threshold value of $|R_{ON}/R_b| = 2.6 \times 10^{-2}$ to classify the devices. In addition, concave $I_{ds} - V_{ds}$ characteristics for low V_{ds} changing to linear and evolving as type (I) or (II) were found for devices 7 and 8. In some devices, this behavior appears only for $|V_g|$ above certain value.

Non-ohmic contacts on devices are probably the result of a high charge-injection

barrier from exposed regions of the Ti adhesion layer (between Au contacts and SiO₂ substrate) to the organic semiconductor. Exposed parts of Ti not covered by gold may appear close to the channel because of defects during lift-off for example. An alternative explanation for cast devices is that in some cases a reduced contact area between metal and organic semiconductor [75] can occur because of the random disposition of the crystallites with respect to the contacts. The $I_{ds} - V_{ds}$ curves of these devices were fit by discarding the data at low $|V_{ds}|$ where the nonlinearity appears.

The model developed in Section 4.3 was used to extract the field-effect mobility of devices of type I and II from the output characteristics of drop-cast devices (Figure 3.3) and spin-coated devices (Figure 3.4). The model parameters appearing in Equation 4.26 are in general gate-voltage dependent as shown in Figure 5.1 for the $L = 4 \mu\text{m}$ and $L = 70 \mu\text{m}$ devices.

Table 5.1 contains the relevant parameters of some representative devices, the average mobility value for each L is included together with its threshold voltage. The table also contains the contact R_c and bulk R_b resistances introduced in Section 4.3 at $V_g = -2$. The fitting error was calculated as the average of the squared relative deviations of the fit with respect to the data. The first letter under the type column indicates whether the device was prepared by drop casting (c) or spin coating (s). The additional number indicates the type of output characteristics. Devices marked with * showed non-Ohmic features at low V_{ds} and for $|V_g| \geq 10$ and 14 V for devices 7 and 8 respectively.

A negative bulk resistance was found for device 8. The reason is that this is a type I device, i.e., one for which the bulk conductance (R_b^{-1}) is negligible and what we actually

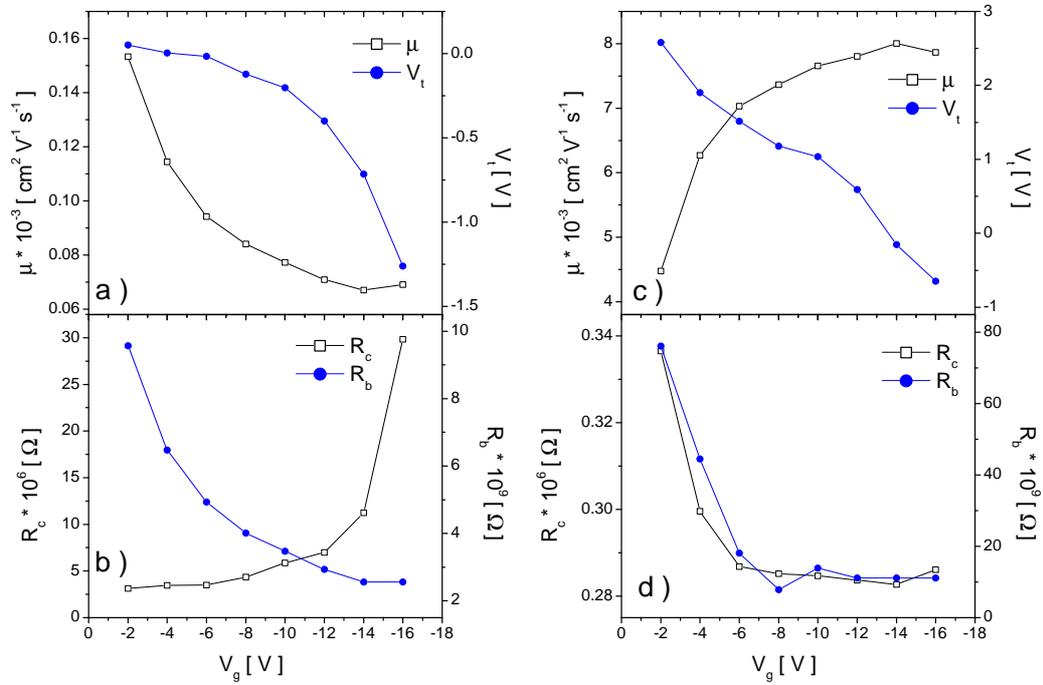


Figure 5.1: Gate-voltage dependent parameters for (a,b) the $L = 4 \mu\text{m}$ device prepared by spin coating, and (c,d) $L = 70 \mu\text{m}$ device prepared by drop-casting. a,c) Mobility and threshold voltage and b,d) contact and bulk resistances

N.	L [μm]	W [μm]	μ [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	V_t [V]	R_c [Ω]	R_b [Ω]	err. [%]	type
1	0.050	20	4.3×10^{-5}	0.6	-	-	0.1	s, II
2	0.145	156	3.8×10^{-5}	6.8	3.0×10^6	4.3×10^9	1.5	c, II
3	4	1260	9.5×10^{-5}	0.1	3.1×10^6	9.6×10^6	0.4	c, II
4	10	1260	1.1×10^{-3}	4.1	4.8×10^5	3.1×10^8	0.5	c, II
5	15	1260	4.4×10^{-4}	0.6	3.3×10^6	5.4×10^9	0.7	c, II
6	20	500	6.2×10^{-4}	0.8	5.8×10^6	4.2×10^{10}	1.2	c, II
7	30	500	7.7×10^{-3}	6.9	8.1×10^6	1.3×10^9	4.5	c, II*
8	39	980	1.4×10^{-3}	0.5	3.0×10^5	-5.6×10^{11}	1.2	s, I*
9	45	5000	4.7×10^{-3}	1.4	3.5×10^5	4.1×10^{10}	0.5	s, I
10	70	980	6.9×10^{-3}	2.6	3.4×10^5	7.6×10^{10}	0.5	s, I

Table 5.1: Channel dimensions of ten representative devices and fitting parameters of the respective $I_{ds} - V_{ds}$ curves using Equations 4.26 and 1.6. The average mobility for V_g between -2 and -16 V is given. The threshold voltage and the contact and bulk resistances are given at $V_g = -2$ V. The averaged relative fitting error and the device type are given. The first letter under the type column indicates drop casting (c) or spin coating (s) device while the second gives the type (I or II) of output characteristics. Devices marked with * showed non-Ohmic features at low V_{ds} and for $|V_g| \geq 10$ and 14 V for devices 7 and 8 respectively.

observe here is a slight decrease of mobility probably caused by gate-voltage stressing during measurement [53]. This gate-voltage stress refers to trapping of charges in less mobile states and has been discussed by Matters et al. in Ref. [53] as the cause for instability, such as threshold voltage shift, in OFETs. The fitting parameters were gate-voltage dependent as shown in Figure 5.1.

Several interpretations have been given to explain the mobility dependence on gate bias and more generally its dependence on electric field. For instance, according to these interpretations, gate bias dependant mobility appears as a result of charge transport limited by traps [42], variation in carrier concentration in the accumulation layer [43, 72] or by a variable range hopping mechanism [79]. The last seems to be the most adequate for solution processed organic semiconductors and predicts $\mu \propto V_g^{2T_0/(T-1)}$ [79] where T_0 is a parameter. Alternatively, it has been shown in the framework of the model for hopping in a Gaussian DOS [5] that a Poole-Frenkel or $\ln \mu \propto E^{1/2}$ behavior is found in a restricted range of applied fields and degrees of disorder. Nevertheless, for vanishing disorder and high electric fields decreasing mobility with increasing electric field was found. This behavior was ascribed to saturation of the drift velocity with field [5]. An increasing mobility with channel length was found for most of the devices as shown for device 10 with $L = 70 \mu\text{m}$ and prepared by spin coating (Figure 5.1c). The opposite behavior was found for device 3 with $L = 4 \mu\text{m}$ and prepared by drop-casting (Figure 5.1a). Not all devices show monotonically varying mobility with gate voltage probably due to instabilities such as stressing of the semiconductor layer.

The threshold voltage V_t was extracted independently from each $I_{ds} - V_{ds}$ curve because a fixed V_t for different V_g did not produce acceptable fitting results. In general,

we found decreasing V_t for increasing V_g as shown in Figure 5.1a and c. A threshold voltage shift has been reported for PTV FETs under negative gate bias [53]. This threshold voltage shift was attributed to trapping of carriers into less mobile states localized most probably in the semiconductor at the insulator interface induced by gate-voltage stress.

Our results suggest that the contact and bulk resistances are gate-voltage dependant (See Figures 5.1b and d). The variation of the contact resistance with V_g is a result of the modulation of the hole injection barrier from metal to semiconductor produced by the electric field created by V_g [76]. For all the analyzed devices, the bulk resistance decreases with increasing $|V_g|$. This seems surprising because it is a well-known fact that in standard MOSFETs the accumulation layer shields the bulk of the semiconductor from the gate field. This effect could be explained as an indirect enhancement of carrier density in the bulk due to diffusion of space charges from the accumulation layer to the bulk. These space charges appear due to the relative low mobility of DH4T and in this case do not limit but favor carrier transport between drain and source.

A typical transfer curve is shown in Figure 3.5b. After V_g reaches the switch-on voltage [57] the channel starts to build up as indicated by an increase of the absolute value of I_{ds} . At a certain point, the completion of the channel is reflected as a linear transfer curve. For higher absolute values of V_g a point is eventually reached where the slope of the transfer curve starts to decrease until $\partial I_{ds}/\partial V_g \approx 0$ which is most probably caused by the contact resistance.

The mobility calculated using the data of the transfer curve, measured at low V_{ds} , between $V_g = -4.2$ and 1.4 V, and Equation 4.23, was $3.6 \times 10^{-5} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. On the

other hand, the calculated value using the model presented here in the same V_g interval is $4.3 \times 10^{-5} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$.

No crossover from field-effect dominated (for $V_g < 0$) to bulk-dominated current (for $V_g > 0$) in the transfer characteristics was found for drop-cast DH4T FETs as it was the case of spin-coated PPV and P3HT FETs [55]. The reason is that for drop-cast DH4T FETs the conductance of the bulk is comparable to the one of the accumulation layer due to the low mobility of DH4T. Therefore, the effect of the bulk of the organic semiconductor is still observable for $V_g < 0$.

The time dependence of I_{ds} under ambient conditions for a drop-cast device with $L = 26 \text{ }\mu\text{m}$ and $W = 980 \text{ }\mu\text{m}$ is shown in Figure 3.6. The drain-source current increases first with time, reaches a maximum and then starts to decrease again. The initial current increase can be attributed to oxygen doping of the organic layer. The reduction in current of $\sim 35\%$ in 67 hours is a consequence of the organic material degradation under long exposure to ambient conditions.

5.3 Field-Effect Mobility

The maximum value of field-effect mobility obtained here for device 10 ($L = 70 \text{ }\mu\text{m}$, $W = 980 \text{ }\mu\text{m}$) at $V_g = -16$ is $8.0 \times 10^{-3} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. This value is two-thirds of the reported in the literature for the top contact electrode configuration [31]. The bottom contact configuration has the disadvantages of using poor charge-injecting materials close to the semiconductor-insulator interface and the tendency to form traps in the semiconductor close to the metal contacts. On the other hand, the advantages come

from the compatibility with processing conditions for organic materials and the availability of practical techniques for fabrication of bottom contacts with nanometer-scale separations.

The motivations to scale down the device dimensions are related to the possibility of large-scale integration and the enhancement of the device performance. One of the key parameters characterizing the device performance is the field-effect mobility that was expected to increase due to the better homogeneity and reduction of scattering at grain boundaries.

Preliminary experiments on spin coated DH4T FETs showed an increase of the apparent mobility for decreasing channel length from 40 μm to 0.8 μm . However, optical microscopy analysis revealed that this result was due to non-uniform coverage of the channel and the consequent overestimation of μ_{FE} in long channel devices. After optimization of the spin coating process the mobility increased in two orders of magnitude but it had a tendency to decrease with decreasing L . Similarly, for cast-DH4T FETs we have found decreasing μ_{FE} with decreasing L as indicated in Figure 5.2.

The metal-DH4T contact resistance limits the total device mobility at short channel lengths [56]. After compensating the effect of the contact resistance the μ_{FE} was still found to decrease with decreasing L . Lower field-effect mobilities for shorter channel lengths can be explained as a consequence of an incomplete channel filling due to the deposition and growth properties of DH4T from solution. First, DH4T forms relatively big-layered crystallites right after drop-cast deposition. It deposits as a mixture of terraces and overlapping crystallites. As seen in the AFM image of Figure 2.17, the DH4T layers overlap and are able to deform without breaking to adopt the form of

an irregular substrate (terraces steps) at least in the cases where the substrate does not have sharp and high edges as for high-aspect-ratio metal contacts. In this way the organic semiconductor layers can lay down on the substrate, filling the gap between source and drain and forming the channel. The results indicate that DH4T deposition from solution is more appropriate for devices with channel lengths of the order of 10 μm . The sharp bending of the crystallites and their reduced size necessary for filling short- L devices are not favorable conditions for DH4T deposited from solution casting. These problem are circumvented by the use of other deposition techniques such as thermal evaporation where small particles have the chance to fill the channel in its integrity.

In order to overcome the contact resistance limitation in short L devices, high work function metals such as Pt have been used for contacts [81] because of its good hole injection properties to pentacene as well as by burying the Ti adhesion layer using a CF_4 plasma. In that work pentacene FETs with $L = 30$ nm (single gap electrodes) were fabricated. The extracted mobility was of the same order of magnitude of the obtained for polycrystalline devices with $L = 20$ μm but still not similar to that of single crystals as expected from the implicit assumption of a channel-length independent field-effect mobility. They find no short channel effects as is the case for our $L < 200$ nm devices.

5.4 Channel Length Dependence of the Field-Effect Mobility

The motivations to scale down the device dimensions are related to the possibility of large-scale integration and the enhancement of the device performance. One of the key parameters characterizing the device performance is the field-effect mobility that was expected to increase due to the better homogeneity and reduction of scattering at grain boundaries. Concomitantly, increased transistor switching speeds proportional to μ/L^2 [7] are expected for an increase in mobility accompanied by channel length reduction.

Nevertheless, as shown by Meijer et al. [56], the reduction in channel length in disordered organic field-effect transistors does not produce an increase in mobility because, the parasitic series resistance limit the the device performance at short channel lengths. However, the results presented here show that this is not the only reason.

Furthermore, short channel effects such as absence of a saturation region or fast increase of the drain current have been reported for FETs with sub 100 nm channel length. Nevertheless, a recent report showed that with careful optimization of materials, and device geometry, these short channel effects do not play a role.

Results for the field effect mobility of DH4T OFETs with channel lengths ranging from $L = 70 \mu\text{m}$ down to 50 nm are presented next. The details of fabrication of nanoelectrodes were given in Section 2.2 and about DH4T deposition from solution in Section 2.6.3. Finally, the measured output characteristics were presented in Chapter 3.

The extracted field-effect mobility as a function of L is presented in Figure 5.2.

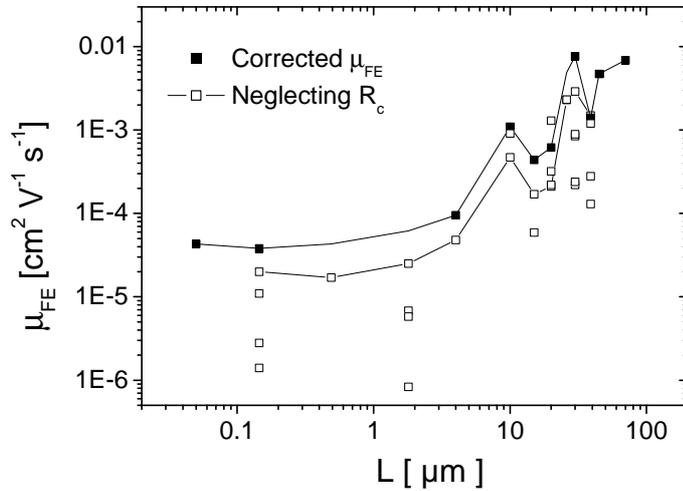


Figure 5.2: Field-effect mobility as a function of channel length for solution-processed DH4T FETs. The values were extracted after fitting the output characteristics to Equations 4.26 and 1.6 and therefore corrected for the contact resistance and bulk mobility (full squares). The plot also shows mobility values calculated when the contact resistance was neglected (empty squares). Additional results for devices not included in Table 5.1 are also given. The lines are guides to the eye.

The mobility values were extracted using the model given by Equations 4.26 and 1.6 for devices shown in Table 5.1. The plot also includes mobility values calculated when the contact resistance is neglected.

On average, the extracted field-effect mobility decreases with decreasing channel length. Despite the spread of the values, a clear trend can be observed showing that for channel lengths longer than approximately $4 \mu\text{m}$ mobilities are in the range of 10^{-4} to $10^{-3} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ while for shorter L , mobilities decrease down to approximately $4 \times 10^{-5} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ at 50 nm . This is not only a consequence of the contact resistance limitation at short L but also of the growth properties of solution-processed films, in particular channel coverage and coupling to the metal electrodes. Nevertheless,

sub-micrometer channel length organic devices with increased field-effect mobility are expected when deposition methods which allow short channels to be completely filled are employed and materials for electrodes with improved charge injecting properties are used.

5.5 Self-Assembled Layer Devices

The results of the electrical characterization of devices based on self-assembled DH4T layers are discussed in this section.

Few of the fabricated devices presented short circuits as a result of the presence of pinholes on the self-assembled layer. The I-V characteristics are asymmetric and some of them show nearly rectification properties (current flows only in one direction but it is not linear and it is noisy). In these devices, the equivalent of the anode is the electrode where molecules are self-assembled. For other devices, some peaks in the IV characteristics appear at certain values of V_{ds} . The gate voltage did modulate the value of the current nevertheless its effect was low compared to the current circulating at zero V_g . The modulated current depended on the absolute value of V_g .

Modulation of the device current is the results of changes on the electronic states of molecules close to the edges of the overlapping source and drain electrodes and gate electrodes (between points A and C in Figure 2.19). The low current modulation is then due to the low ratio between the length of the arc AC and the area of the surface sandwiched between source and drain. Improvement is expected from optimization of the device geometry, for example, using thin rectangular metal strips with increased

perimeter to area ratio. Additional improvement of the modulation is expected by using a thinner insulator.

The reason for the dependence on the absolute value of V_g and not on its sign is that this type of devices does not work by means of an accumulation layer but by modification of the molecular electronic levels under the application of an external field. The dips observed in some cases are probably related to electron reduction processes that take place when the external potential equals the molecular electron affinity [52].

Chapter 6

Conclusions and Perspectives

The purpose of this project was the fabrication and characterization of organic electronic devices with critical dimensions down to the nanometer scale. A minimum channel length of 50 nm was achieved by means of EBL and NIL with the standard organic FET architecture. However, in experiments towards molecular electronics, fabrication of electrodes separated by approximately 13 nm was accomplished as well as demonstration of devices where the electrode separation was given by the thickness of a self-assembled molecular layer (~ 3 nm).

Morphology, carrier injection and transport properties of solution-processed DH4T films used in the fabrication of OFETs have been found to be strongly dependent on surface treatment of the substrate and deposition method of the organic semiconductor. In particular, it was shown that HMDS-treated substrates exhibited improved performance over the untreated ones. Furthermore, drop-cast DH4T layers were thicker than those prepared by spin-coating that, in combination with the relatively low mobility of the semiconductor, resulted in an important contribution of the mobility of the bulk to the total device mobility. Nevertheless, the bulk current can be of importance for thin

spin-coated films when the channel length becomes comparable with the layer thickness. In summary, bulk conduction plays a significant role in devices with relatively low field-effect mobilities, thick organic layers and short channel lengths.

The observed non-saturating output characteristics were explained by a modified model for FETs in the gradual channel approximation in which the bulk contribution to the drain-source current was included. By fitting the experimental results to this model, which includes the accumulation layer and bulk conductances as well as the contact resistance, the mobility related only to field-effect in the accumulation layer was extracted. Considering the contribution of the bulk to the total mobility of the semiconductor layer allows the extraction of the mobility associated only to the field effect. The field-effect mobility is the one that gives rise to modulation of the device current and thus is the one useful in practical applications.

The maximum value of field-effect mobility obtained here for a device with $L = 70 \mu\text{m}$ and $W = 980 \mu\text{m}$ is $8.0 \times 10^{-3} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. This value is two-thirds of maximum reported in the literature for a spin-coated DH4T device with $L = 50 \mu\text{m}$ and $W = 5 \text{ mm}$ using the top contact electrode configuration [31]. This is a good result taking into account that the bottom contact configuration has the disadvantages of using poor charge-injecting materials close to the semiconductor-insulator interface and the tendency to form traps in the semiconductor close to the metal contacts. To the best of our knowledge, this is the first study on the channel length dependence of the mobility on solution processed DH4T OFETs.

On average, the extracted field-effect mobility decreases with decreasing channel length. Despite the spread of the values, a clear trend can be observed showing that for

channel lengths longer than approximately 4 μm mobilities are in the range of 10^{-4} to $10^{-3} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ while for shorter L , mobilities decrease down to approximately $4 \times 10^{-5} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at 50 nm. This is not only a consequence of the contact resistance limitation at short L but also of the growth properties of solution-processed films, in particular channel coverage and coupling to the metal electrodes. Therefore, sub-micrometer channel length organic devices with increased field-effect mobility are expected when deposition methods, which allow short channels to be completely filled, are employed and materials for electrodes with improved charge injecting properties are used.

In addition to OFETs, devices based on a self-assembled layer of DH4T sandwiched between two gold layers were demonstrated. Modulation in the device current by application of a voltage to the gate electrode was observed and ascribed to a modification of the molecular electronic levels under the application of an external field rather than to the formation of an accumulation layer.

The main directions in research towards the improvement of the performance of OFETs, with an emphasis on the nanometer channel length devices, are summarized next. The analysis will be split into fabrication techniques and materials for electrodes, gate insulator, deposition methods for organic semiconductors and ambipolar operation.

In the definition of nanoelectrodes, NIL has demonstrated its capability because of its high resolution and low cost characteristics. Nevertheless, the stamps for NIL still need to be fabricated by serial techniques such as EBL. New fabrication procedures using EBL, such as the multi-step exposure technique relying in the use of a nano-manipulated stage [81], need to be investigated in order to prepare stamps with shorter

channel lengths in a reproducible way. An additional factor is the material for the electrodes, in this case Pt and Pd has shown better results than gold due to a better coupling of the metal work function with the HOMO of most of the p-type organic semiconductors. An alternative is the use of organic materials for the electrodes, which may improve coupling to the organic semiconductor, but the feasibility for their use in nanometer channel length devices has not been investigated yet.

In the case of short channel lengths devices, the gate insulator thickness has to be reduced accordingly in order to get saturating output characteristics important for switching applications in logic circuits. The alternative in this case is the use of SAM of insulating molecules that, in addition to their nanometer-scale thickness, provide an organic interface for the semiconductor. Currently, the limitation of this approach is the presence of high leakage currents through the gate insulator.

An additional factor is the deposition of the organic semiconductor. In this case, the objective is to investigate low-cost processes leading to the deposition of layers with improved properties. An interesting example is the simple method of dip coating that has been used to deposit the active layer of OFETs. From the point of view of the applications, further research is necessary in the area of complementary circuits involving n and p-type organic semiconductors in a single layer as demonstrated in Ref. [54].

Research in miniaturization of electronic devices has already reached the molecular scale. Nevertheless, the physical mechanisms responsible for current modulation in this type of devices are fundamentally different to the ones on OFETs. More specifically, the modulation of the drain-source current by the gate voltage is not the result of a

change in the charge density of an accumulation layer but corresponds to a modification of the molecular electronic levels under the application of an external field. Further research in techniques capable to address single molecules is needed as well as novel device geometries using self-assembly techniques. In addition, development of new electronic circuit architectures adapted to the characteristics of molecular devices and making use of their advantages is required.

Publications

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