Silicon Integrated Radio Front-End Design for 100 Gbit/s and Beyond

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Declaration

I, Stefan Malz, herewith declare that I have produced this thesis without the prohibited assistance of third parties and without making use of aids other than those specified; notions taken over directly or indirectly from other sources have been identified as such. This work has not previously been presented in identical or similar form to any other German or foreign examination board.

The thesis work was conducted from 2012 to 2019 under the supervision of Prof. Dr. Pfeiffer at the University of Wuppertal. This work was partially funded by the German Research Foundation (DFG) as part of the priority programme 1655 'Drahtlose Ultrahochgeschwindigkeitskommunikation für den mobilen Internetzugriff'.

Wuppertal, April 2019

Abstract

Wireless communication is one of the fastest growing fields of technology, which constantly enables new innovations in all sectors of industrial, scientific, and consumer applications. To meet the ever-increasing demand for higher data-rates, parts of the electromagnetic spectrum that were previously unexploited are being acquired for wireless communication. Particularly large bandwidth for high-speed communication is available in the high millimeter-wave frequency range above 200 GHz. Due to the recent technological progress, these bands have become accessible using silicon technologies, which are attractive for their capability of co-integration of high-frequency radios and digital baseband processing, low quality variation within series production, and low cost of production at higher volumes. Silicon germanium (SiGe) heterojunction bipolar transistors (HBT) show a large f_T and f_{max} in combination with moderate breakdown voltages. This translates into a higher gain, higher output power and overall better performance at millimeter-wave frequencies.

This thesis investigates novel circuit concepts for silicon integrated radio front-ends with data-rates of 100 Gbit/s and beyond. These shall enable wireless communication on an entirely new scale. By combining high-performance circuit building blocks with a new system level concept for direct-conversion transmitter and receiver in the 200 GHz to 300 GHz frequency range, the measured data-rates surpass those achievable with previously reported highly directive wireless links.

Within the scope of this thesis, multiple circuit building blocks are designed and characterized in a 0.13 µm SiGe BiCMOS technology. An in-depth analysis of the system level requirements of an ultra-wideband radio front-end in the 200 GHz to 300 GHz frequency range is conducted. For the carrier generation pathway, two ×8 frequency multiplier chains in different technologies are presented, which are investigated for their output power, bandwidth, and spurious harmonic suppression. Balanced frequency doublers with reduced conduction angle use a novel harmonic tuning scheme for increased conversion gain within a bandwidth that is well defined by miniaturized passive baluns. A novel, very compact quadrature phase generation scheme increases the conversion gain and harmonic suppression of multiplier-based frequency doublers. For frequency translation, novel fundamentally-driven up- and down-conversion mixers overcome bandwidth limitations through the use of innovative circuit topologies and a co-design approach with an optimized package. Additionally, a methodology for the design of high gain, low noise cascode amplifiers operating above 1/3 of the maximum oscillation frequency of a given technology is presented and verified with two 212 GHz and 233 GHz amplifiers.

On a system level, front-end imperfections that lead to the degradation of wireless link performance through quadrature channel interference are overcome by adding a layer of channel orthogonality with a wideband, dual-polarized, lens-integrated antenna.

Finally, a highly directive, dual polarized 240 GHz quadrature transmitter and receiver chipset in 0.13 µm SiGe BiCMOS technology demonstrates an outstanding 140 Gbit/s data-rate over a distance of 60 cm. The system presented in this thesis reaches well beyond the state-of-the-art in purely electronic wireless links.

In conclusion, the design insights presented herein build the basis for future low-cost, compact, robust and fully electronic wireless links with data-rates exceeding 100 Gbit/s.

Zusammenfassung

Die drahtlose Kommunikation ist eines der am schnellsten wachsenden Technologiefelder, welches fortlaufend Innovationen in allen Bereichen der industriellen, wissenschaftlichen und Endverbraucheranwendungen ermöglicht. Zuvor un- oder anderweitig genutzte Teile des elektromagnetischen Spektrums werden für die drahtlose Hochgeschwindigkeitskommunikation reserviert, um dem konstant anwachsenden Bedarf nach immer höheren Datenraten gerecht zu werden. Besonders große Bandbreiten für die Hochgeschwindigkeitskommunikation stehen im Millimeterwellenbereich über 200 GHz zur Verfügung. Diese Frequenzbänder wurden durch den jüngsten technologischen Fortschritt auch mit Siliziumschaltkreisen nutzbar, welche durch die Möglichkeit der Co-Integration von Hochfrequenzradios und digitaler Basisbandsignalverarbeitung, kleiner Serienstreuung und niedrigen Produktionskosten in Serienfertigung attraktiv sind. Insbesondere Silizium-Germanium (SiGe) Bipolartransistoren mit Heteroübergang (HBT) stechen mit hohen f_T, f_{max} Werten und gemäßigten Durchbruchspannungen hervor, welche sich in Kombination in hoher Verstärkung, Ausgangsleistung und einer insgesamt höheren Leistungsfähigkeit im Millimeterwellenbereich ausdrückt.

Diese Dissertation behandelt die Erforschung von innovativen Schaltungskonzepten für hochintegrierte Radio-Frontends mit Datenraten über 100 Gbit/s in Siliziumtechnologie, die eine drahtlose Kommunikation in einer neuen Größenordnung ermöglichen sollen. Durch die Zusammenführung von hochperformanten Schaltungsblöcken mit einem neuartigen Systemkonzept für Direktmischsender und -empfänger im Bereich von 200 GHz bis 300 GHz werden die Datenratenbegrenzungen bisheriger Richtfunksysteme überschritten.

Nach einer eingehenden Analyse der Anforderungen an ein ultra-breitbandiges Radio Front-End im genannten Frequenzbereich auf dem Systemlevel, wurden im Rahmen dieser Forschungsarbeit verschiedenste Schaltungsblöcke entworfen und charakterisiert. Für die Erzeugung der Trägerfrequenz werden zwei ×8 Frequenzvervielfacherketten in unterschiedlichen SiGe-HBT-Technologien vorgestellt, deren maximale Ausgangsleistung, Bandbreite und Unterdrückung von störenden Oberwellen untersucht wurden. Eine neue Methode zur separaten Impedanztransformation der Fundamentalen und der zweiter Oberwelle steigert den Wandlungsgewinn von balancierten Frequenzverdopplern mit reduziertem Leitungswinkel, deren Bandbreite durch miniaturisierte Baluns klar definiert wird. Ein neues, sehr kompaktes Verfahren zur Erzeugung von Treibersignalen, welche die Ausgangsströme von multiplizierbasierten Frequenzvervielfachern in Quadratur bringt, erhöht deren Wandlungsgewinn und die Unterdrückung störender Oberwellen. Für die Frequenztranslation in Sender und Empfänger wurden neue Mischer entworfen, die Bandbreitenlimitierungen durch innovative Schaltungskonzepte und einem Co-Designansatz mit einem optimiertem Platinenaufbau. Zusätzlich wird eine Methodik vorgestellt, die eine Grundlage bildet für die Entwicklung von

Niederrauschverstärkern mit hoher Verstärkung oberhalb 1/3 f_{max} einer beliebigen Technologie. Die Methodik wird durch zwei Verstärker bei 212 GHz und 233 GHz verifiziert.

Auf der Systemebene werden Unvollkommenheiten des Front-Ends, welche dessen Leistungsfähigkeit durch Interferenz der Quadraturkanäle verringern, durch das Hinzufügen einer weiteren Orthogonalität kompensiert. Die Zuordnung der Quadraturkanäle zu einzelnen Polarisationen einer breitbandigen, dual-polarisierten Antenne mit angeschlossener Siliziumlinse erhöht die Kanalisolation signifikant.

Zum Abschluss wird unter der Benutzung der neu in einer 0.13 µm SiGe BiCMOS Technologie entwickelten Quadratursender und -empfänger eine Datenrate von 140 Gbit/s bei einer Trägerfrequenz von 240 GHz und über eine Distanz von 60 cm demonstriert. Das in dieser Dissertation vorgestellte System reicht weit über den aktuellen Stand der Technik in rein elektronischer, drahtloser Hochgeschwindigkeitskommunikation hinaus.

Zusammenfassend bilden die hier vorgestellten Erkenntnisse die Grundlage für eine preiswerte, kompakte, robuste und rein elektronische Lösung für die drahtlose Datenübertragung mit Datenraten über 100 Gbit/s.

Contributions

This thesis explores novel circuit and system level concepts in search for a silicon integrated radio front-end, that supports a data-rate in excess of 100 Gbit/s. A small part of the circuits were designed by my colleagues or in a team effort. All contributions are detailed below.

Chapter 1

I briefly introduced the sub-THz and THz frequency ranges and discuss how communication in these frequency bands is a logical consequence of the historical progression. I reviewed a key figure of merit for the valuation of wireless links and the suitability of currently available Silicon-Germanium heterojunction bipolar technology for such links.

Chapter 2

I reviewed the state-of-the-art in MMIC and silicon integrated wireless links in the sub-THz region published in the scientific community. The derivation of system level design goals draws heavily on the published characterization results of a first generation radio front-end performed by Janusz Grzyb and Pedro Rodríguez-Vázquez.

Chapter 3

I discuss the influence of multiplier chains for carrier generation on wireless link performance. Because the spurious harmonic content of multiplier chains in the sub-THz range is rarely discussed in published literature, a first generation $\times 16$ multiplier chain is presented for reference, which was designed by Neelanjan Sarmah and measured by me. I then introduce two novel $\times 8$ multiplier chains in two different technologies and supporting input and inter-stage passive baluns. The output balun in IHP technology was designed by Janusz Grzyb and ported to Infineon technology by Thomas Bücher.

Chapter 4

I present novel, wideband frequency translation circuits, that are integrated into a wireless transmitter and receiver chip-set. The quadrature hybrid in the carrier generation path was designed by Janusz Grzyb. The front-end power amplifier was a design by Neelanjan Sarmah and its S-parameter characterization was done by me. The packaging approach was initially conceived by Pedro Rodríguez-Vázquez, but realized by me, with help during the EM-simulation phase by Marcel Andree.

Chapter 5

The RF characterization of the wireless transmitter and receiver chip-set was done by me on a setup build by Pedro Rodríguez-Vázquez. The dual-polarised antenna was designed by Janusz Grzyb.

Chapter 6

The communication test of the radio front-end was done in cooperation with Pedro Rodríguez-Vázquez.

Chapter 7

Both low noise amplifiers and their design methodology were conceived by me. The balun and the tuned contact pad placed at both input and output were designed by Ullrich Pfeiffer. The gain chart analysis and the equations for relating the maximum transducer gain with the unilateral gain of a two port were found in the published literature, but the derivations of these equations has, to my best knowledge, never been published before and is included in the appendix.

Acknowledgement

Humans are pack animals. Which is why we achieve the most, when we support each other.

Therefore my gratitude first goes to professor Ullrich Pfeiffer, for giving me the opportunity to work in the ridiculous vast field that is RF circuit design. And thank you, Ullrich, for reviewing this thesis, by the way.

I am deeply indebted to my colleagues of the last 6 years. My first insights into RF electronics came from analysing the work of Neelanjan Sarmah. He also is a complete foodie and Japanese noodle soup tastes the best in his company.

My development as a circuit designer sky-rocketed, when Philipp Hillger and Ritesh Jain joined our team. It is quite astounding what you can achieve, if you are surrounded by people smarter than yourself every day of the week. And yes, that includes all those crazy tape-out weekends.

Everything I know about *practical* communication front-ends I learned from Janusz Grzyb and Pedro Rodríguez-Vázquez. Thank you for the late night discussions and sharing your knowledge with me.

Thank you to Thomas Bücher for discussing the wildest circuit design ideas with me, even in the most inconvenient of moments.

Thank you to Marcel Andree for sharing his chocolate with me.

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Shout out to Marc Papenheim. Our friendship started in the pre-study maths course and still lasts today.

The person that I am today, I am only because of that one time, when my parents Jürgen and Inge forced me to do my math homework. And because my brother Thorsten demonstrated to me, how much you can achieve, if you just sit down and do the work. Thank you for your unending love and support.

And finally, my deepest appreciation goes to my queen of hearts, Sarah. Thank you for hugging me, and then kicking me out of the living room to work on this thesis. This would not have been possible without you.

Thank you, all of you.

List of Abbreviations

4G	fourth generation
5G	fifth generation
ACPR	adjacent channel power ratio
AWG	arbitrary waveform generator
BB	baseband
BCM	Bose-Chaudhuri-Hocquenghem
BEC	base emitter collector
BEOL	back-end-of-line
BER	bit error rate
BiCMOS	bipolar complementary metal-oxide-semiconductor
BPSK	binary phase shift keying
BV	breakdown voltage
BW	bandwidth
CMOS	complementary metal-oxide-semiconductor
DPSA	double-polysilicon self-aligned
EM	electromagnetic
EVM	error vector magnitude
FEC	forward error correction
f_{max}	maximum oscillation frequency
FMCW	frequency modulated continuous wave
f_T	maximum transit frequency
FoM	figure of merit
GF	globalfoundries
GSG	ground-signal-ground
HBT	heterojunction bipolar transistor
IC	integrated circuit
IHCT	institute for high frequency & communication technology
IHP	innovations for high performance microelectronics
IF	intermediate frequency
imec	Interuniversity Microelectronics Centre
IR	infra-red
ITU-R	international telecommunication union, radiocommunication sector
IQ	in-phase and quadrature
LBE	local backside edging
LNA	low noise amplifier
LO	local oscillator
mHEMT	metamorphic high-electron-mobility transistor
MIM	metal-insulator-metal

MMIC	Monolithic Microwave Integrated Circuit
NF	noise figure
NXP	next experience semiconductors
PCB	printed circuit board
PHY	physical layer
RADAR	radio detection and ranging
RF	radio frequency
RPG	Radiometer Physics
RX	receiver
TowerJazz	Tower Semiconductor Ltd.
TP	transconductance pair
TX	transmitter
SMA	SubMiniature version A
SNR	signal-to-noise-ratio
SSB	single-sideband
ST	STMicroelectronics
SQ	switching quad
QAM	quadrature amplitude modulation
QPSK	quadrature phase-shift keying
VDI	Virginia Diodes
VGA	variable gain amplifier

1. Introduction

1.1. The Scope of this Thesis

With the advent of fifth generation mobile networks (5G) on the horizon, industry and research institutes alike search for new ways to meet the customers ever-increasing demand for higher data-rates, while improving spectral efficiency and decreasing latency. A promising approach is the move to millimeter-wave (mmWave) frequencies. While standardization is still underway, current industrial developments focus on the 28 GHz and the 38 GHz band with over 1 GHz spectral bandwidth. For data-rates in the order of 100 Gbps, communication in these spectrally limited bands requires complicated modulation schemes, that are noise and compression sensitive. Thanks to the recent progress in silicon technologies, a potentially low-cost alternative has emerged by moving to much higher frequencies in the 200 GHz to 300 GHz frequency range. This is in line with the recent IEEE Standard 802.15.3d-2017 [1] for high data-rate wireless multi-media networks. At these wavelength, the use of a small fractional bandwidth means the availability of a high absolute bandwidth for future high speed communication with simple and robust modulation schemes. Other possible applications also benefit from the high available bandwidth at mmWave frequencies, e. g. Frequency Modulated Constant Wave (FMCW) Radio Detection and Ranging (RADAR), imaging systems for material characterization or industrial automation.

The DFG priority program SPP 1655 - *Wireless Ultra High Data Rate Communication for Mobile Internet Access* funds fundamental research regarding wireless communication systems with data-rates exceeding 100 Gbps. The project Real100G.RF - *Fully integrated Radio-Front-End Module for wireless 100 Gbps Communication* - within this priority program aims to explore new architectures on all system levels for silicon integrated communication circuits above 200 GHz, including circuit building blocks, power generation, antennas and ultra-compact packaging.

This thesis documents the research into a novel highly directive, dual polarized 240 GHz quadrature transmitter and receiver chip-set in a 0.13 µm SiGe BiCMOS technology.

The thesis approaches the design of silicon integrated radio front-ends for data-rates in excess of 100 Gbit/s from two different angles. On the one hand, starting from a first-generation hardware, which was the result of design efforts during the EU funded DOTSEVEN project [2], the performance, limitations and impairments of all building blocks of said RF front-end are analyzed in detail. System level design goals are derived from this analysis in Chapter 2. Except for the RF power amplifier, the building blocks are then successively replaced. Novel multiplier chains for carrier generation are presented in Chapter 3.

Wideband up- and down-conversion mixers integrated into an optimized, PCB based package are described in Chapter 4, along with the used dual-polarized, lens-integrated on-chip antenna.

On the other hand, it is impairment mitigation by system design that enables data-rates beyond 100 Gbit/s in the transmit and receive chip-set presented in Chapter 4. By improving the channel isolation, front-end imperfections that influence the wireless link performance are compensated. RF characterization results are presented in Chapter 5 and the successful establishment of a wireless in Chapter 6. Additionally, an original design methodology for high gain, low noise amplifiers above 1/3 f_{max} of a given technology is discussed in Chapter 7. Finally, Chapter 8 provides a conclusion and an outlook on the further options for the development of high-speed communication systems.

1.2. The Terahertz Frequency Range

At the turn of the 20th century, Guglielmo Marconi and Reginald Fessenden ushered in the era of radio communication. While Marconi demonstrated the first transatlantic wireless communication using spark technology, Fessenden pioneered constant-wave based transmission and contributed the method of heterodyning, which is nothing less than the fundamental basis of modern radio communication [3].

Since then, humanity has been exploring increasingly higher carrier frequencies in a race for higher speed and channel capacity. A hundred years later, just at the turn of the 21st century, researchers push towards the last frontier of radio communication: the Terahertz (THz) frequency range. Eerily similar to Marconi and Fessenden, the first THz transmitter was impulse based [4], while constant-wave transmission followed shortly after [5].

The THz frequency range sits in between the millimeter-wave and the far-infrared region in the electromagnetic spectrum. There are various definitions on the specific range of the THz region found in the literature. While physics and optics communities consider all frequencies between 0.1-10 THz to belong to the THz region [6], microwave electronics communities equate the THz region with the sub-millimeter-wave region from 0.3-3 THz [7]. The frequency range from 100-300 GHz therefore is often termed "sub-THz" region.

Fig. 1.1 shows the atmospheric attenuation from 0 Hz to 1 THz according to the ITU-R model [8]. From this graph it becomes instantly clear, why both the sub-THz and the low THz region are attractive for the future of wireless communication: they offer huge bandwidth in distinct frequency segments with moderate absorption rates. Beyond 1 THz, many water and oxygen absorption lines limit the usefulness of THz frequencies for data transmission.

Instead, spectrometers and imaging systems use the THz range for niche and industrial applications: explosive and concealed weapon detection, pharmaceutical and non-destructive quality control and medical sensors by now stand next to the classical use of THz frequencies in radio astronomy [10]. Traditionally, these frequency bands were the domain of III-V semiconductors, due to their superior device characteristics. But the recent advances in SiGe HBT technology enables the development of RF integrated circuits operating at higher

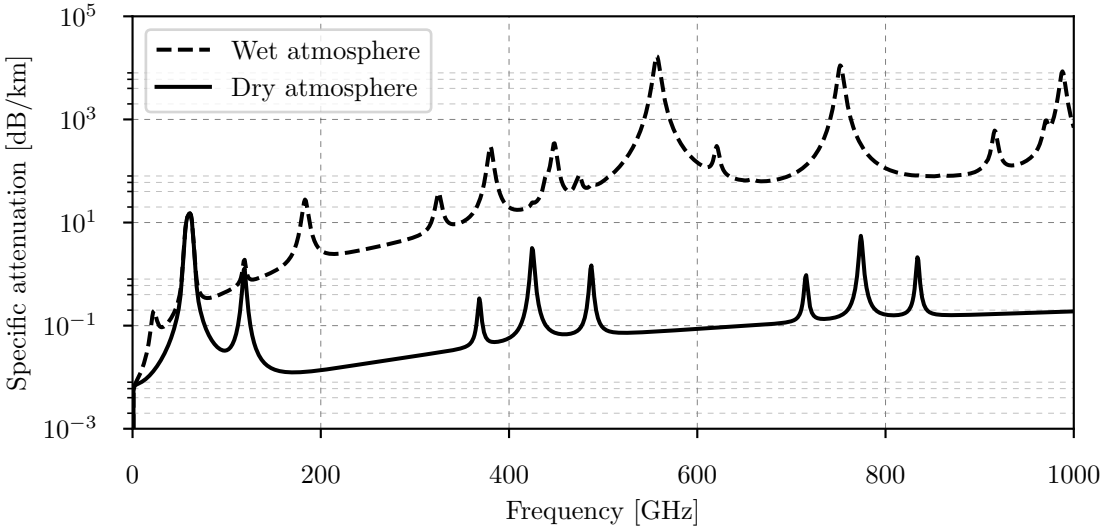


Figure 1.1.: Specific attenuation due to atmospheric gases [9].

frequencies than previously deemed feasible in silicon. The resulting lowered production costs at high volumes are one of the major requirements for further growth in emerging consumer markets.

1.3. Sub-THz and THz Communication

The foreseeable mass-employment of sub-THz and THz communication is easily derived from three "laws". First, Edholm's law of bandwidth states, that data-rates in telecommunication evolve predictably just like chip performance according to Moore's law: doubling every 18 month. It distinguishes three categories of communication, from fastest to slowest:

1. Wireline, where data transmission is bound to a specific location, like LAN.
2. Nomadic, where the user can move between a multitude of stationary radii, like Wi-Fi.
3. Wireless, where the user can move freely and data transmission is truly mobile.

These three communication categories increase their data-rate with similar exponential slopes, where wireless and nomadic trail wireline communication with a constant time step. As wireless and nomadic are both based on radio technology, Edholm's law predicts their convergence around the year 2030. Fig. 1.2 shows the original graph from the 2004 IEEE Spectrum article by S. Cherry [11], which led to the widespread recognition of Edholm's law.

Comparing wireless standards for mobile phones of the recent years, the trend seems unbroken: while the third generation (3G) High Speed Downlink Packet Access (HSDPA) category 8 enabled downstream data-rates of 7.2 Mbit/s in 2007, the since 2015 widely adopted 4G Long Term Evolution (LTE) standard has 100 Mbit/s downstream. The upcoming fifth

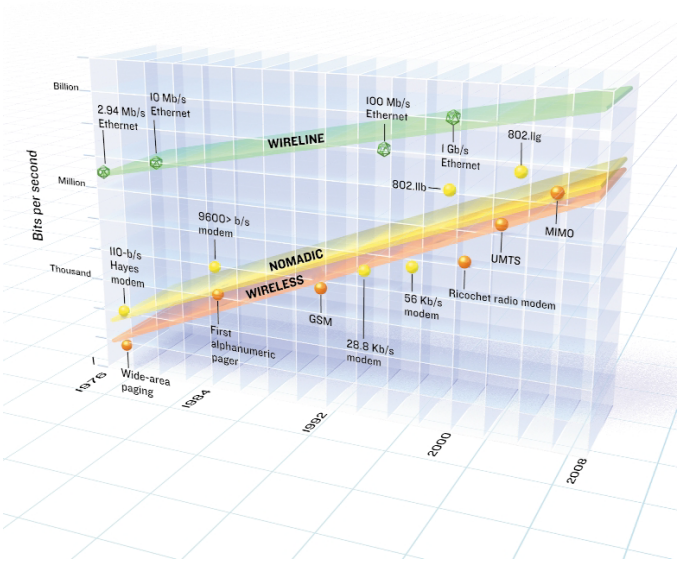


Figure 1.2.: Edholm's law: wireline, nomadic, and wireless data-rates improve reminiscent to Moore's Law [11] © 2004 IEEE.

generation (5G) mobile networks will enable data-rates in the order of 20 Gbit/s by the end of 2020.

To full-fill its data-rate promise, 5G includes new carrier frequencies in the mmWave range with a maximum channel bandwidth of 400 MHz. Therefore, the second "law" predicts the move to even higher frequencies: the Shannon-Hartley theorem states, that the maximum channel capacity C in bits/s with a defined signal-to-noise ratio SNR is directly proportional to the available bandwidth BW, with

$$\mathrm{C} = \mathrm{BW} \cdot \log_2(1 + \mathrm{SNR}). \tag{1.1}$$

Following this basic relation, 5G mobile devices have to use a multi-carrier approach to combine a multiple of their maximum 400 MHz into a 2 GHz total bandwidth to deliver the previously mentioned 20 Gbit/s with a SNR of 30 dB. Contrarily, the sub-THz and THz range offer bandwidth around high carrier frequencies in unallocated bands large enough to further increase channel capacity, without the need for multi-carrier capable baseband hardware.

Finally, Cooper's law of spectral efficiency is based on the obversation of name-giving radio scientist Martin Cooper, that the number of wireless signals that can simultaneously be transmitted without interfering with each other has been doubling approximately every 30 months since the early 1900s [12]. And while frequency, time and code division as well as advancing further into the usable radio spectrum all play a role in this staggering rate, the real contributor is spatial multiplexing. To allow for an increased number of simultaneous conversations, the area necessary for any individual conversion has to be confined to a minimum. As the following link budget calculation will show, wireless communication in

the sub-THz and THz frequency range intrinsically relies on highly directive, short range links.

The received power P_r can be calculated with Friis' transmission equation:

$$P_r = P_t + G_t + G_r + 20\log_{10}\left(\frac{c_0}{4\pi \cdot d \cdot f}\right), \tag{1.2}$$

where P_t is the transmitter output power, G_t and G_r are the antenna gains of the respective transmitter and receiver antenna, c_0 is the free space speed of light, d is the distance and f is the frequency. From there, the signal-to-noise ratio at the receiver output is:

$$\mathrm{SNR} = P_r - (N_0 + 10\log_{10}(BW) + NF + M), \tag{1.3}$$

where N_0 is the noise power spectral density, BW is the system noise bandwidth, NF is the total noise figure of the receiver and M is the link margin. Fig. 1.3a shows the achievable data-rates for different modulation schemes, dependent on the antenna gain G_t and G_r equally employed in both transmitter and receiver respectively. The remaining parameters are listed in Tab. 1.1. As the RF front-ends presented in this thesis use carrier frequencies in the higher sub-THz range, the carrier is chosen accordingly. Simple L-matching circuits yield fractional bandwidth around 10 %, which is used for the system bandwidth. With currently available SiGe transistor technology, 0 dBm of output power in this frequency range is realizable without the use of massive power combining. The receiver noise figure (NF) is set to 15 dB. The bit error rate (BER) sets the required signal-to-noise ratio for the different modulation schemes, as outlined in section 1.4. Additionally, a link margin of 10 dB is included.

P_t	d	f	BW	N_0	NF	M	BER
0 dBm	1 m	240 GHz	10 %	-178 dBm/Hz	15 dB	10 dB	$< 4.5{\cdot}10^{-3}$

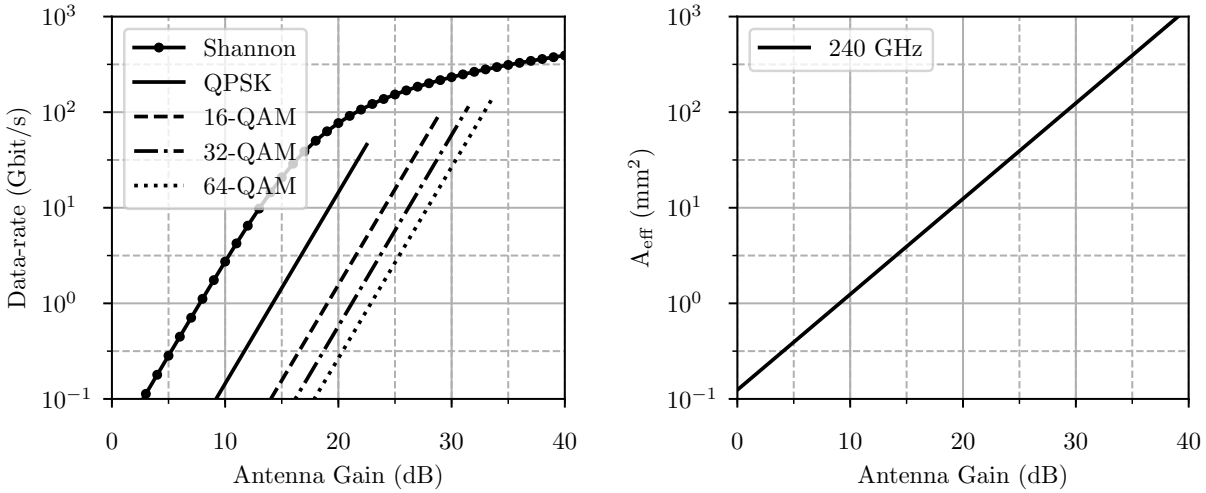
Table 1.1.: Parameters for calculation of maximum data-rate and effective antenna area.

With the fixed system bandwidth of 24 GHz, the maximum data-rate for each modulation scheme is calculated by multiplying with the respective spectral efficiency. For QPSK, the maximum data-rate is 48 Gbit/s. This requires an antenna gain of 22.6 dB, when transmitting over a 1 m distance. For the 96 Gbit/s maximum of 16-QAM or the 120 Gbit/s of 32-QAM, a 29 dB or 31.6 dB antenna gain would be needed in both the TX and the RX.

Fig. 1.3b shows the effective antenna area necessary to achieve the antenna gain used for the data-rate calculations from Fig. 1.3a. The effective antenna area is calculated in reference to an ideal isotropic radiator with

$$\mathrm{A_{eff}} = G \cdot \frac{1}{4\pi} \cdot \left(\frac{c_0}{f}\right)^2. \tag{1.4}$$

An antenna with 25 dB gain requires an effective area of 40 mm^2. The silicon integrated RF front-end circuitry presented in this thesis are only a fraction of this size. With dimensions



(a) (b)

Figure 1.3.: TX & RX antenna gain versus (a) maximum channel capacity according to Eq. 1.1 and data-rate with a BER $< 4.5{\cdot}10^{-3}$, a 240 GHz carrier and 10 % bandwidth; or (b) effective antenna area for the same carrier frequency.

this small, co-integration of a transmitter or receiver including an external antenna in a mobile device such as a phone or tablet computer is a definite possibility.

Nonetheless, the range of THz communication systems can be extended by dielectric focussing lenses or mirrors. The latter might also enable non-line-of-sight communication in office or other indoor environments [13] [14]. In [15], reflection and scattering are identified as the most important propagation phenomena apart from line-of-sight phenomena for wireless communication systems beyond 100 GHz. Considering the surface roughness of commonly used single-layer and multi-layer building materials in a closed room scenario, a ray-tracing simulation predicts a detrimental effect of scattering on data-rates available in the room center.

An all electronic monolithic microwave integrated circuit (MMIC) based link at 120 GHz was used in a trial of television broadcasting at the 2008 Beijing Olympic Games [16]. The first allocation of a sub-THz band for industrial application happened in Japan in 2014, with wireless broadcasting services allowed in a frequency range from 116 GHz to 134 GHz [17]. In 2017, the IEEE Standards Association released "Amendment 2: 100 Gb/s Wireless Switched Point-to-Point Physical Layer" [1] to their "IEEE Standard for High Data Rate Wireless Multi-Media Networks", which defines a physical layer (PHY) in a frequency range from 252 GHz to 325 GHz with different assigned bandwidths, the largest of which is 69.12 GHz centered around a 287.28 GHz carrier.

How THz communication fares against free-space infra-red (IR) communication is discussed in [6]. In comparison, THz waves are more robust against scintillation effects and certain atmospheric conditions like fog. Also, intensity modulation and detection with IR photodetectors is not as sensitive as THz heterodyne detection.

1.4. Error Vector Magnitude as Performance Measure

To evaluate the performance of a wireless link, the error vector magnitude (EVM) is the most commonly chosen performance measure. The following discussion uses the notation from [18]. Fig. 1.4 shows a graphical representation of the relevant variables in a 16-QAM constellation diagram.

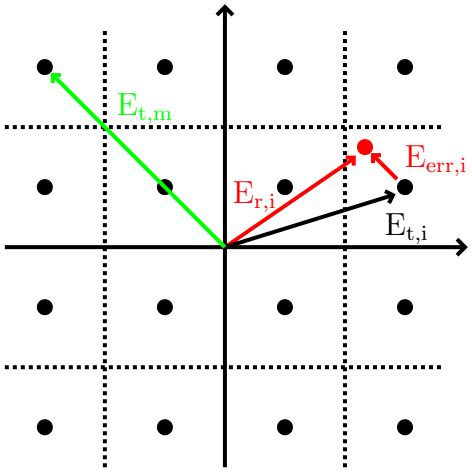


Figure 1.4.: Constellation diagram for 16-QAM. $E_{t,m}$ is the longest vector in the ideal constellation. $E_{t,i}$ is the vector of a single ideal point, $E_{r,i}$ is the vector to the actually received symbol and $E_{err,i}$ is their difference.

To arrive at the EVM, the root-mean-square deviation σ_{err} of a number I of actually received signal vectors E_r from the ideal transmitted vector E_t is calculated. Its error vector E_{err} includes all linear, non-linear and noise induced impairments.

$$\sigma_{err} = \frac{1}{I}\sum_{i=1}^{I} |E_{err,i}|^2 \text{ with } E_{err,i} = E_{r,i} - E_{t,i} \tag{1.5}$$

Two slightly differing EVM definitions can be found in the literature [19]. $\mathrm{EVM_m}$ uses the power of the longest ideal constellation vector $|E_{t,m}|^2$ for normalization.

$$\mathrm{EVM_m} = \frac{\sigma_{err}}{|E_{t,m}|} \tag{1.6}$$

$\mathrm{EVM_a}$ on the other hand refers to the average power $|E_{t,a}|^2$ of all symbol vectors M within a constellation.

$$\mathrm{EVM_a} = \frac{\sigma_{err}}{|E_{t,a}|} \text{ with } |E_{t,a}|^2 = \frac{1}{M}\sum_{i=1}^{M} |E_{t,i}|^2 \tag{1.7}$$

Both definition are related by a factor k, which depends on the modulation scheme.

$$\mathrm{EVM_a} = k \cdot \mathrm{EVM_m} \text{ with } k^2 = \frac{|E_{t,m}|^2}{|E_{t,a}|^2} \tag{1.8}$$

To trace back the influence of various system imperfections on the EVM, the author of [19] constructed a model of a single carrier quadrature transmit and receive system. By working on linear, memoryless modulated signals with zero-mean un-correlated in-phase and quadrature components, formulations for the influence of modulator and demodulator imbalances, their phase difference and channel white noise on the EVM are found.

In the absence of modulator and demodulator imperfections, EVM is solely dependent on the signal-to-noise-ratio:

$$EVM = \sqrt{\frac{1}{SNR}} \tag{1.9}$$

With a SNR of 8.4 dB, EVM is 38 % and therefore sufficient for a practically error-free transmission with QPSK modulation. To reach the same condition with 16-QAM, a SNR of 15 dB would be necessary.

Equations 1.10 and 1.11 allow a more intricate analysis of the degradation of $\mathrm{EVM_a}$ by separately including different imperfections. Both were derived in [19].

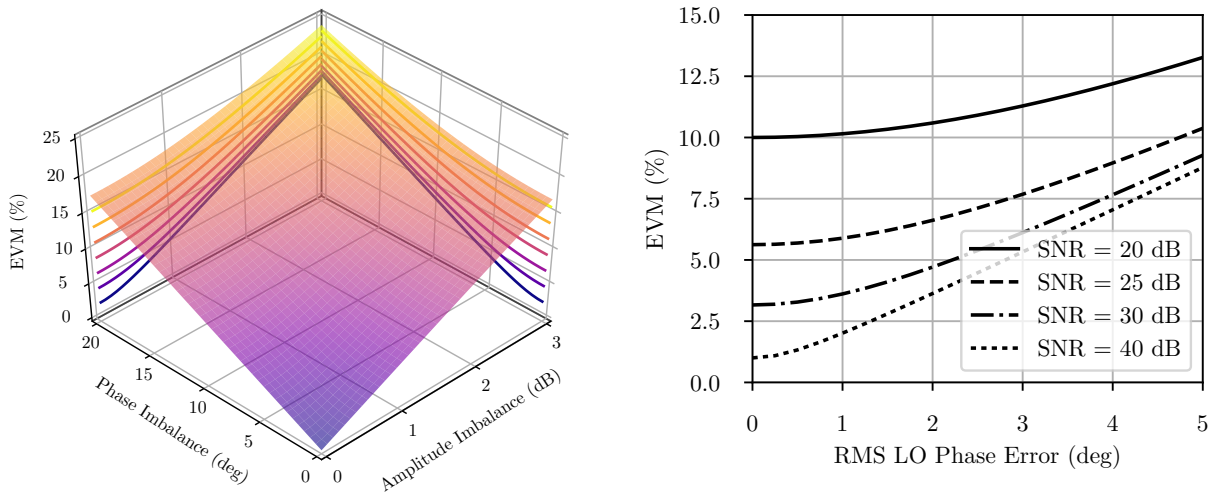
Fig. 1.5a was generated using Eq. 1.10. It depicts the variance of $\mathrm{EVM_a}$ with quadrature gain imbalance g_{Imb} and phase imbalance ϕ_{Imb} in the transmitter under the assumption of infinite SNR. A 1 dB amplitude imbalance or a 5° phase imbalance causes an $\mathrm{EVM_a}$ of 5.74 % or 4.36 % respectively. The combination of both leads to an $\mathrm{EVM_a}$ of 7.21 %. With a typical SNR of 25 dB, $\mathrm{EVM_a}$ is at 9.14 % under the same conditions.

$$EVM = \sqrt{\frac{1}{SNR} + 2 - \sqrt{1 + \frac{2g_{Imb}}{1+g_{Imb}^2} + \cos(\phi_{Imb}) + \frac{2g_{Imb}}{1+g_{Imb}^2} \cdot \cos(\phi_{Imb})}} \tag{1.10}$$

On the other hand, Eq. 1.11 describes how zero-mean Gaussian phase noise with variance σ_{LO} degrades $\mathrm{EVM_a}$, bringing transmitter and receiver out of phase alignment. Fig. 1.5b shows the calculation results for a variety of SNR values. With a typical SNR of 25 dB, an LO rms phase error of 1° increases the baseline $\mathrm{EVM_a}$ of 5.62 % by 0.16 %, a 5° error by 4.75 %.

$$EVM = \sqrt{\frac{1}{SNR} + 2 - 2\exp\left(-\frac{\sigma_{LO}^2}{2}\right)} \tag{1.11}$$

The work in [20] relies on a similar model as [19], but provides detailed example graphs to identify the source of the imperfections by analysing recorded constellation diagrams. A closed form expression for the EVM combining all above described imbalances was found in [21].



(a) (b)

Figure 1.5.: EVM_a variance with (a) transmitter gain and phase imbalance for infinite SNR or (b) rms LO phase error σ_{LO} between transmitter and receiver [19].

The BER for quadratic M-QAM signal constellations can be estimated from measured EVM under the assumption, that errors are dominated by electrical white Gaussian and other electronic noise. Eq. 1.12 as presented in [22] allows direct calculation of the BER using the modulation format-dependent factors from Tab. 1.2, where L is the number of identical signal levels in one dimension of the quadratic constellation, M is length of the word represented by each QAM symbol and k^2 is the re-normalization factor when inserting either EVM_m or EVM_a into the equation.

$$BER \approx \frac{1 - L^{-1}}{\log_2(L)} \cdot \operatorname{erfc}\left(\sqrt{\frac{3 \cdot \log_2(L)}{L^2 - 1} \cdot \frac{1}{(k \cdot EVM_m)^2 \cdot \log_2(M)}}\right) \tag{1.12}$$

	QPSK	16-QAM	32-QAM	64-QAM
L	2	4	6	8
M	4	16	32	64
k^2	1	9/5	17/10	7/3

Table 1.2.: Modulation format-dependent factors for calculating the expected BER from EVM.

Fig. 1.6 shows the interdependency of BER and EVM for common quadrature modulation schemes. According to [23], hard-decision forward error correction (FEC) using a Bose-Chaudhuri-Hocquenghem (BCH) cyclic error-correcting code achieves a net coding gain (NCG) of 9.35 dB within a 7 % overhead rate. This leads to a nearly optimal, error free transmission with a BER $< 10^{-15}$, if the channel input error rate does not surpass the threshold of $< 4.5 \cdot 10^{-3}$. For QPSK modulation, this threshold is reached at an EVM_a of 38.3 %, for 16-QAM at 17.8 %, for 32-QAM at 12.1 % and for 64-QAM at 9 %.

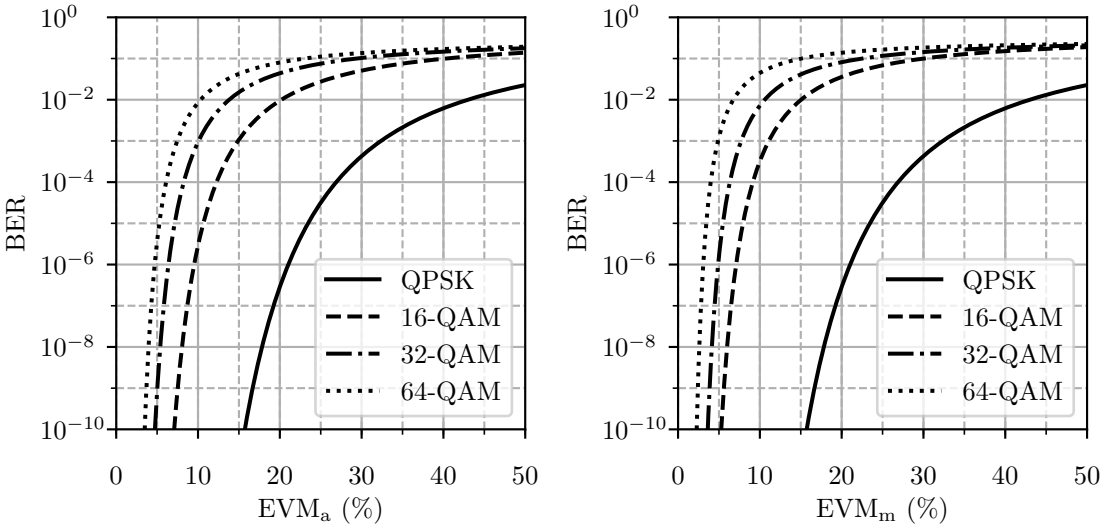


Figure 1.6.: Interdependency of bit error rate and error vector magnitude. EVM_a refers to the average power of all symbol vectors within a constellation for normalization, EVM_m refers to the power of the longest vector respectively [18].

1.5. Silicon-Germanium Technology

Silicon based heterojunction bipolar transistors (HBTs) are the prime choice for the future broad-scale adaptation of high-performance and low-cost sub-THz and THz applications. Chevalier *et al* describe the current status of SiGe HBTs in [24], [25]. Bipolar transistors feature larger transconductance, larger breakdown voltages and lower 1/f noise compared to MOS transistors. But the most commonly used figures of merit (FoM) to evaluate the high frequency performance of a transistor are:

- f_T, the maximum transit frequency, or unity current gain frequency, where the current gain drops to one.
- f_{max}, the maximum oscillation frequency, until which a device is considered active and provides power gain.

It is customary to de-embed parasitics of the connecting metallization layers, then extract the small-signal current gain h_{21} and the unilateral gain U of the device at lower mmWave frequencies up to 40 GHz and extrapolate f_T and f_{max} by assuming a 20 dB decline per frequency decade. Caution is called for when comparing f_T/f_{max} values of bipolar and CMOS technologies: while de-embedding has no relevant effect on the translation from measured to real world bipolar performance, additional parasitic capacitance stemming from wiring degrades the f_T of the devices in advanced CMOS nodes. Also, CMOS relies on channel length reduction for increased speed, which leads to shrinking operating voltages. Chevalier *et al* conclude, that the utilizable RF performance of MOS technologies reached its peak at the 40 nm/20 nm nodes. The recent appearance of dedicated RF technologies at these technology nodes [26] reinforces this point of view.

The European Union funded the development of today's fastest silicon germanium bipolar transistors in two successive projects under the "Seventh Framework Programme for Research and Technological Development" to establish a leadership position for the European semiconductor industry for mmWave applications: the goal of DOTFIVE (grant agreement number 216110) were HBTs with a maximum oscillation frequency of 500 GHz; in DOTSEVEN (grant agreement number 316755) research focused on process technology for an f_{max} of 700 GHz, with a balanced increase of f_T. The success of this endeavour is shown in Fig. 1.7. Published at the 2018 IEEE BCICTS, it lists the f_T/f_{max} values of various bipolar technologies as recently reported.

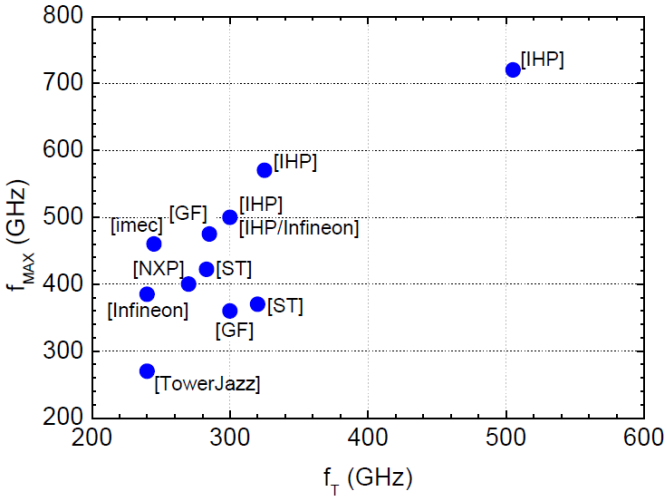


Figure 1.7.: Overview of f_T and f_{max} of current bipolar technologies. References are available in [24]. [25] © 2018 IEEE.

At the time of this writing, the transistors developed during the DOTFIVE project are the fastest that are commercially available. Integrated circuits in IHP's SG13G2 technology can be ordered by way of a multi-project-wafer (MPW) through Europractice [27]. Their even farther advanced transistors [28] [29] in development during the DOTSEVEN project were available to the project partners. These resulted in communication experiments with outstanding results, which were reported on in [30] and [31]. Similarly, Infineon granted access to its B11HFC technology to their project partners as part of DOTSEVEN.

1.5.1. IHP's 130 nm Hetero Bipolar Transistor

Most circuits presented in this thesis were designed in IHP's SG13G2 technology, which Europractice made available to research institutes after the end of the DOTFIVE project.

Fig. 1.8 shows the influence of the collector current density on the measured transit and maximum oscillation frequency of different HBT devices during the technological progression of the DOTFIVE project, originally published by B. Heinemann *et al* at the 2010 IEEE IEDM [32]. The D53 devices then became the standard HBTs in IHP's SG13G2 technology. Their effective emitter width is 120 nm. The peak f_T/f_{max} is 300/450 GHz.

The authors of [32] attribute the increased transistor performance compared to prior generations only to a minor part to device scaling, but predominantly to a changed selectively-implanted collector (SIC), which led to a later onset of the Kirk effect and reduced specific resistances.

The technology design kit offers a unit cell HBT with fixed emitter area A_E of (0.12× 0.96) µm^2, from which larger transistors are derived by placing unit cells in parallel. Therefore all appurtenant circuit schematics in this thesis show integer multiples of this smallest size. The unit cell transistor has a BEC configuration. In addition to its 0.13 µm CMOS baseline process, the technology is equipped with five fine and two thick top patterned aluminum metal layers (2 µm and 3 µm) for RF applications, silicided and unsilicided polysilicon resistors and MIM capacitors (1.5 fF/µm^2).

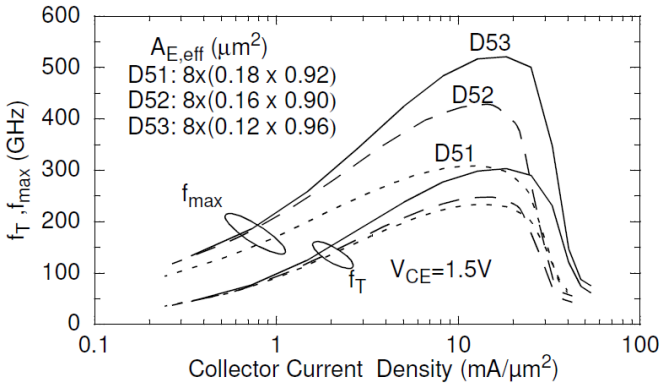


Figure 1.8.: Measured f_T and f_{max} as a function of the collector current density for different HBT devices during the technological progression of the DOTFIVE project. The D53 devices with effective emitter area of 0.12×0.96 µm^2 are the HBTs available in IHP's SG13G2 technology [32] © 2010 IEEE.

1.5.2. Infineon's 130 nm Hetero Bipolar Transistor

During the predecessor to the DOTSEVEN project, Infineon upgraded their double-polysilicon self-aligned (DPSA) HBT technology B7HF200 towards better RF performance. Consequentially, their goal during the DOTSEVEN project was the co-integration of these advanced HBT devices with their existing 130 nm CMOS platform named C11. The resulting BiCMOS technology is called B11HFC. Fig. 1.9 shows the progression of the measured transit and maximum oscillation frequency with collector current for a model device, originally published by J. Böck *et al.* at the 2015 IEEE BCTM [28]. The peak f_T/f_{max} values are 250 GHz/370 GHz. The back-end-of-line of this technology includes four narrow and two thick copper layers for RF design purposes. Additionally, there are MIM capacitors (1.54 fF/µm^2) and both TaN- and polysilicon resistors, to cover the whole range of typically needed resistance values.

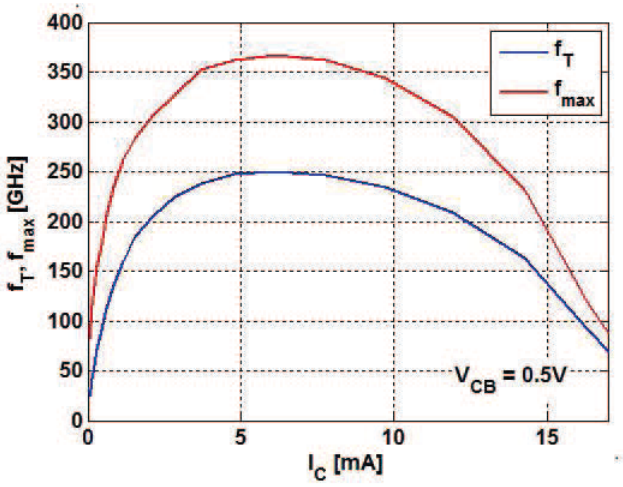


Figure 1.9.: Measured f_T and f_{max} as a function of the collector current I_c for a HBT with effective emitter area of 0.13×2.73 µm^2 in Infineon's B11HFC technology [28] © 2015 IEEE.

1.5.3. Future Technological Progress

The current state-of-the-art in SiGe HBT technology was published in [29]. HBTs with f_T/f_{max} of 505 GHz/720 GHz ring oscillator gate delay of 1.34 ps were presented. This large increase of device speed was accomplished with a multitude of methods like using a SiGe base profile with higher Ge content, while simultaneously reducing the thickness of lower doped parts of the base-collector and emitter-base transition. But most notably the emitter-base spacer, the emitter width, the emitter-poly width and the collector window were reduced. The consequence of these scaling efforts were weaker breakdown properties, particularly the base-emitter reverse breakdown voltage BV_{EBo} was reduced from 1.4 V in SG13G2 to 0.75 V and the collector-emitter breakdown voltage with shorted base BV_{CEs} from 4.4 V to 3.2 V.

M. Schröter *et al* proposed a TCAD-based roadmap for the future technological progression of SiGe HBTs in [33]. According to the 15 year time frame of this roadmap, the performance limit of SiGE HBTs lies around an f_T/f_{max} of 1.1 THz/2.5 THz with BV_{ECo} approaching 1 V. These new high-speed devices will enable fundamentally operated transceiver implementations deep in the THz frequency range.

Until now, BiCMOS technologies are built on CMOS nodes trailing behind the current state-of-the-art. Future co-integration with the latest CMOS nodes is going to combine high digital density with superior RF performance. SiGe HBTs will offer the power, bandwidth, low noise and reliability for sub-THz and THz high-data-rate communication, while dense CMOS digital circuitry is needed for high resolution analog/digital conversion, high-speed memory and computing power.

2. Wireless Links in the 200 GHz - 300 GHz Band

2.1. Introduction to the Chapter

This chapter first reviews the state-of-the-art MMIC or silicon integrated high data-rate wireless links published in recent literature. Afterwards, the impairments of a first generation direct conversion wireless link are analysed. From this, system level design goals are derived for a second generation front-end chip-set, which shall exceed the previously published data-rates despite the use of a slower, but commercially available SiGe HBT technology.

2.2. State-of-the-Art in Wireless Links

A small variety of approaches to high data-rate wireless communication at high mmWave frequencies can be found in the literature. In [34], 35 nm InP-HEMT based split block modules use a direct conversion architecture to transmit 96 Gbps at 240 GHz using an 8-PSK modulation scheme. A super-heterodyne chip-set in 80 nm InP-HEMT presented in [35] transmits 100 Gbps in 16-QAM. A data-rate of 32 Gbps is achieved in [36] with a 40 nm CMOS super-heterodyne receiver. A $\times 6$ multiplier chain generates the 270 GHz carrier in the receiver, while the transmitter from [37] supplies the 16-QAM modulated signal with its doubler based square mixers. Two independent 16-QAM, 60 Gbps streams are transmitted with a super-heterodyne transceiver chip in [38]. The data streams are split into two 17.5 GHz bands. The first is modulated with a 70 GHz carrier generated by a doubler, using low side injection. For the second band, a tripler provides a 105 GHz signal to a mixer using high side injection. Together, both bands fill 35 GHz in the W-band.

Other work in 0.13 µm SiGe can be found in [39], where a direct conversion transceiver chip-set uses BPSK modulation to transmit 50 Gbps. The chips are placed opposite to each other on a probe station, such that probes connected to an extender module can feed the 190 GHz carrier. Both chips use 5 dBi wire bond monopole antennas. In [40], an on-chip $\times 8$ multiplier chain generates a 240 GHz carrier for a SiGe transmit and receive chip-set. With BPSK modulation, 25 Gbps were demonstrated. High directivity is achieved in this work with on-chip antennas utilizing local backside edging (LBE) radiating into polyethylene lenses.

In [30] and [31] a quadrature direct conversion transceiver chip-set in an advanced SiGe technology with f_T/f_{max} of 350/550 GHz was presented. With RF amplifiers in both transmitter

and receiver, 90 Gbps were demonstrated in both 16-QAM and 32-QAM. The 230 GHz carrier for this TX and RX was generated by a ×16 multiplier chain. The front-end amplifier of the receiver was omitted in [41] to arrive at a mixer-first architecture. The topology of the used mixer had a particularly broadband RF input, such that the receiver bandwidth was limited by the baseband amplifier. Consequently a data-rate of 100 Gbps in 16-QAM was demonstrated.

The above mentioned work in III/V or CMOS technologies all use highly directive horn antennas. In the work done in SiGe, meaningful transmission distances were achieved with high directivity lens-integrated on-chip antennas. The used antennas are all single polarised. The quadrature architectures from [30], [31] and [41] solely rely on orthogonality by phase for channel isolation.

A comparison of all publications discussed above can be found in Tab. 6.1 in Chapter 6, including the measured communication test results of the wireless link presented within this thesis.

2.3. A Review of Direct-Conversion Wireless Link Impairments

To analyse the impairments of a direct conversion wireless link on a system level, this section reviews the limitations of the first generation hardware developed at the IHCT. It uses an experimental 0.13 µm SiGe HBT technology with an f_T/f_{max} of 350/550 GHz [2]. First communication results with this hardware were published in [42]; an update with modified, wideband baseband inputs was published in [43]. A variant with a wideband mixer-first architecture was introduced in [44]. Data-rates of 65 Gbit/s using QPSK were reported in [45], 81 Gbit/s using 64-QAM in [46], 90 Gbit/s using 32-QAM in [31] and finally 100 Gbit/s with an EVM of 17 % using 16-QAM in [41].

The first generation transmitter and receiver chip-set generates the respective carrier signals from an external local oscillator. An active balun converts this single-ended signal into a differential one for a ×16 multiplier chain. A circuit description and on-wafer measurement results of the ×16 multiplier chain can be found in Ch. 3.5. The output power of a three stage power amplifier following the multiplier chain is split in an integrated 90° coupled line hybrid. The Gilbert cell based up-conversion mixers in the TX use current combining on the collector level of their switching quads to feed both the in-phase and quadrature channel into a shared four stage RF power amplifier. A broadband, single-polarized on-chip ring antenna radiates through the ICs substrate into the 5.9 mm extension of a 25 dBi hyper-hemispherical lens antenna with a diameter of 9 mm and made out of high-resistivity silicon. A block level diagram of the TX is shown in Fig. 2.1a. The receiver uses the same lens-antenna, followed either by a front-end amplifier and a Gilbert cell based IQ down-conversion mixer, as shown in Fig. 2.1b, or an IQ mixer-first architecture, which omits the front-end amplifier and feeds the signal coming from the antenna directly into a switching-quad based mixer.

The mixers in both TX and RX use a differential baseband signal feed per channel. Together with the local oscillator signal, there are 5 high-frequency signal lines per front-end.

The chip-on-lens assembly of TX or RX is glued to the backside of a 338 µm thick Rogers 4350B printed circuit board, such that the IC is accommodated in a recess in the PCB. The height difference between the chip surface to the top of the signal layer on the PCB front-side is 213 µm. 17.5 μm^2 diameter gold wire-bonds connect all DC and baseband signal pads on the IC to the gold-plated copper lines on the PCB. The wire-bond inductance of each high-frequency pathway is absorbed into an eight-section stepped-impedance low-pass filter entirely implemented on the PCB. Microstrip transmission lines route the high-frequency baseband and local oscillator signals to soldered SMA connectors at the PCB edge.

In [41], the key figures of the first generation front-end chip-set for a 230 GHz carrier frequency are recapitulated: The TX has a maximum output power of 5.5 dBm with a 3-dB RF bandwidth of 28 GHz and an IQ imbalance below 0.7 dB. From the two reported receiver architectures, the one with front-end amplifier has a 23 dB conversion gain with a 23 GHz bandwidth and a single-side-band noise figure of 10 dB. The other RX uses a mixer-first architecture for a 3-dB bandwidth of 26 GHz, a conversion gain of 8 dB and an estimated SSB NF of 14 dB. The IQ imbalance is below 1 dB at the 230 GHz carrier frequency.

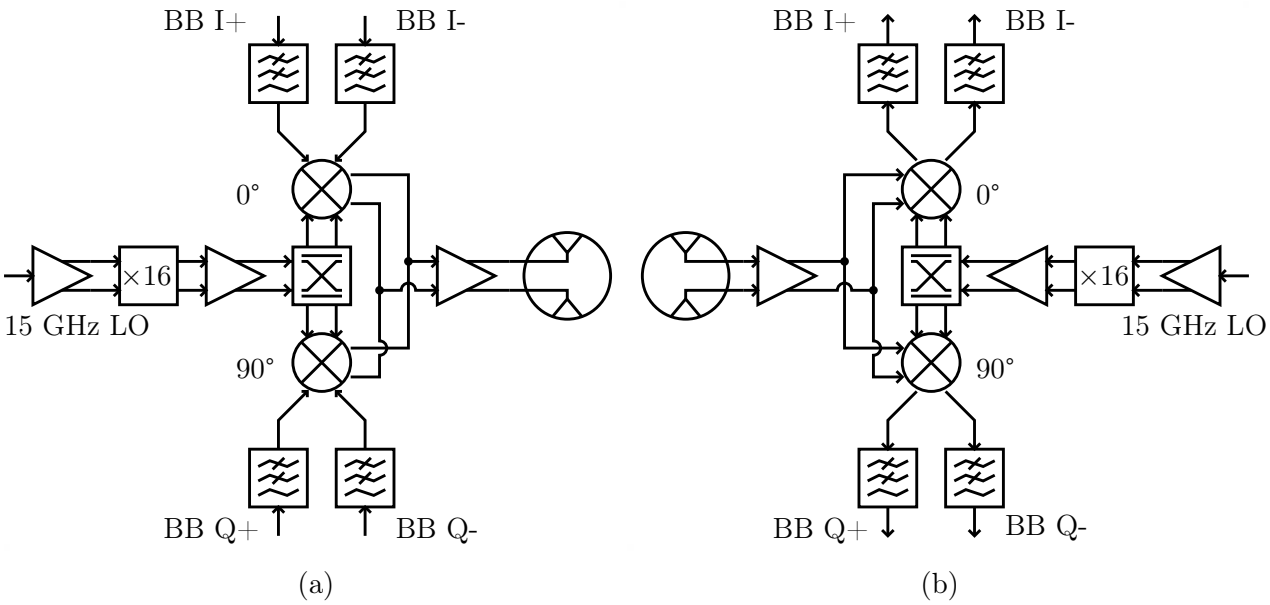


Figure 2.1.: 1st generation direct conversion (a) transmitter and (b) receiver block diagram.

2.3.1. Isolation Between Local Oscillator Feed and Baseband Ports

Fig. 2.2a shows a schematic illustration of the packaging approach of the first generation hardware. Even though the baseband and local oscillator signals are routed orthogonal to each other, [41] reports an isolation of 50 dBc between them. Possible sites for the generation of this spurious EM-coupling are discontinuities like the transition from the SMA connectors to the microstrip transmission lines, the wire-bonds to the IC or a coupling through the ground plane of the IC.

This coupling is critical in the receiver case. With a free space path loss of 80 dB over 1 m distance, using the output power of the first generation TX with 6-dB back-off, the power

at the receiver output does not exceed -21.5 dBm. The multiplier chain drive power at the SMA connector level can be an order of magnitude greater than the 0 dBm required for optimum harmonic rejection in the first generation multiplier chain as discussed in Ch. 3.5.2, to compensate for ohmic losses of the signal routing and reflection losses due to discontinuities. In [41], the LO to BB leakage exceeds -30 dBm and thus is of similar signal strength as the baseband signal itself.

This sets a hard limit on the usable baseband bandwidth of the first generation receiver. Fig. 2.2b visualizes the issue. With a 15 GHz local oscillator signal for a 240 GHz carrier after multiplication, the usable bandwidth is limited to a value lower than that.

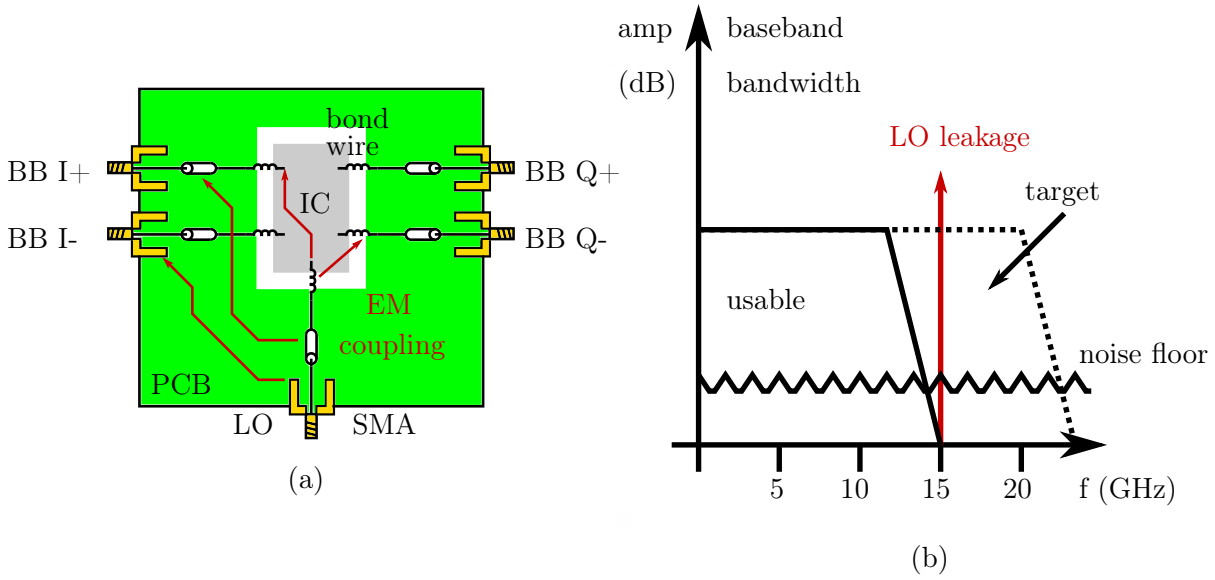


Figure 2.2.: Electromagnetic coupling of the strong LO signal into the baseband. (a) Various pathways on the PCB assembly level. (b) Reduction of usable bandwidth due to LO leakage.

2.3.2. Transmitter Output Power

The transmitter output power is limited by the front-end power amplifier. As discussed in 1.5, the breakdown voltage of modern high-speed SiGe HBTs limits the usable voltage swing. To compensate with a larger current swing and with a fixed current density for peak f_{max} biasing to achieve any gain in the 200 GHz to 300 GHz range, the emitter length can be scaled. But with a high capacitive part of the output impedance of large devices over 200 GHz, the transmission line length used for output tuning becomes impractically small. Considering additionally the fact, that load-line matching is not possible due to the low output impedance of the devices at frequencies near $1/2\ f_{max}$ [47] and the low quality factor of on-chip transmission lines for impedance tuning, power generation is severely limited.

An alternative is the use of power combining from a multitude of PAs with transistor cores employing small device sizes. Options include in-phase combining [48], balancing [49] or

in-antenna power combining [50]. The latter was explored in a proof-of-concept transmitter in [51] using the first generation ×16 multiplier chain for 240 GHz carrier generation. The published data-rate of 30 Gbit/s using 8-PSK was the highest in a SiGe chip-set at the time.

2.3.3. Receiver Noise Figure

The receiver noise figure in the first generation hardware varies dependent on whether a front-end amplifier or a mixer-first architecture is used. The exceptional 10 dB NF achieved with the front-end amplifier is owed to the experimental technology used for the implementation. Typical noise figures of state-of-the-art low noise amplifiers in commercially available SiGe HBT technology can be found in Tab. 7.1 in Chapter 7. The noise figure of the mixer-first receiver is set by the switching quad based mixer with its conversion loss and the NF of the baseband buffer. It adds sufficient gain to suppress the noise contribution of any following components, like external broadband amplifiers or the high-speed oscilloscope for communication tests.

2.3.4. Phase Noise

The phase noise scaling in the 1st generation ×16 multiplier chain was analysed in [52]. For this purpose, the single-side-band phase-noise spectral power density of an Agilent E8257D signal generator at 15 GHz was measured with an Agilent E4440A spectrum analyzer before and after multiplication with the ×16 multiplier chain. A nearly ideal phase noise scaling of $20{\cdot}\log_{10}(16) = 24.1$ dB was observed, indicating that additional phase noise from carrier generation does not limit link performance beyond expectation.

Nonetheless, [52] concludes that uncompensated phase noise from the carrier generation path is one of the key limiting factors for wideband wireless links in the 200 GHz to 300 GHz band. This is a fundamental issue, as the integrated phase noise floor linearly scales with the modulation bandwidth and therefore quickly exceeds the contribution of the integrated close-carrier phase noise to the overall rms phase error σ.

The individual contributions are highlighted during the following integration over the measured close-carrier phase noise $L_{cc}(f)$ of the E8257D synthesizer and over its 150 dBc/Hz noise floor up to a baseband bandwidth limit of 15 GHz, including ×16 multiplication:

$$\begin{aligned}\sigma &= \sqrt{2 \cdot \left(\int_{100\ \mathrm{Hz}}^{1\ \mathrm{MHz}} L_{cc}(f) df + \int_{1\ \mathrm{MHz}}^{15\ \mathrm{GHz}} \frac{10^{-15}}{\mathrm{Hz}} \right) \cdot 16^2} \\ &= \sqrt{2 \cdot (2.977 \cdot 10^{-7} + 1.5 \cdot 10^{-5}) \cdot 16^2} \\ &= 0.0885 \\ &= 5.07^\circ \end{aligned} \tag{2.1}$$

2.3.5. Spurious Harmonic Tones

In [41], the detrimental effect of spurious harmonic tones stemming from the carrier generation path is discussed. The ×16 multiplier chain of the first generation hardware produces the 14th, 15th, 17th and 18th spurious tones besides its' desired 16th harmonic tone. These spurious tones mix with the baseband signal in the up-conversion mixers in the TX, generating modulated copies of the baseband in the RF spectrum. In the receiver, these copies mix with the strong carrier frequency and appear centered around a frequency offset in the baseband. With a 15 GHz local oscillator drive signal, the false baseband copies start overlapping the desired baseband, if the baseband bandwidth exceeds 7.5 GHz.

Further discussion and a graphical illustration of this issue may be found in Chapter 3. The harmonic content of the ×16 multiplier chain is strongly dependent on the input drive power level; measurement results are given for reference in Ch. 3.5. An illustrative analysis on the basis of two different frequency doubler topologies shows their sensitivity to drive signal imperfections and the consequent generation of spurious harmonic tones.

2.3.6. Bandwidth Limitations

The overall system bandwidth is of utmost importance for achieving multiple 10s of Gbit/s of data-rate with modulation schemes with low spectral efficiency like QPSK. Fig. 2.3 highlights a variety of possibly problematic building blocks in a generic wireless link restricting the overall system bandwidth. Every building block has to support the target bandwidth. If for example, as shown in (d), the bandwidth of the TX baseband electronics is sufficiently large (green), but the BW of the front-end PA is not (red), the bandwidth of all following components is restricted to the PA bandwidth (orange).

In the transmitter of the 1st generation wireless front-end, the mayor source of RF bandwidth limitation is the four stage power amplifier, whose measurement results are recapitulated in Ch. 4.4. But the baseband bandwidth in both TX and RX is set to 14 GHz by the eight-section stepped-impedance low-pass filter realized on the PCB to compensate the wire-bond inductance. Additionally, as discussed in Ch. 2.3.1, the leakage of the carrier generation drive signal to the baseband connections limits the receiver bandwidth.

2.3.7. IQ mismatch

There are two sources of IQ mismatch in a quadrature transceiver. The detrimental effect of IQ mismatch stemming from the quadrature carrier generation path is well understood and thoroughly discussed in textbooks like [53]. In conclusion, if the carrier signal driving either the in-phase or quadrature up or down-conversion mixer has larger or smaller amplitude or a phase offset in relation to the respective other up or down-conversion mixer, the constellation diagram experiences distortion. In the case of an amplitude mismatch, the constellation is stretched along either the I or Q-axis. In the case of a phase mismatch, the constellation is compressed along one diagonal and extended along the other. Additionally, the baseband output of each channel is superimposed with a fraction of the data symbols

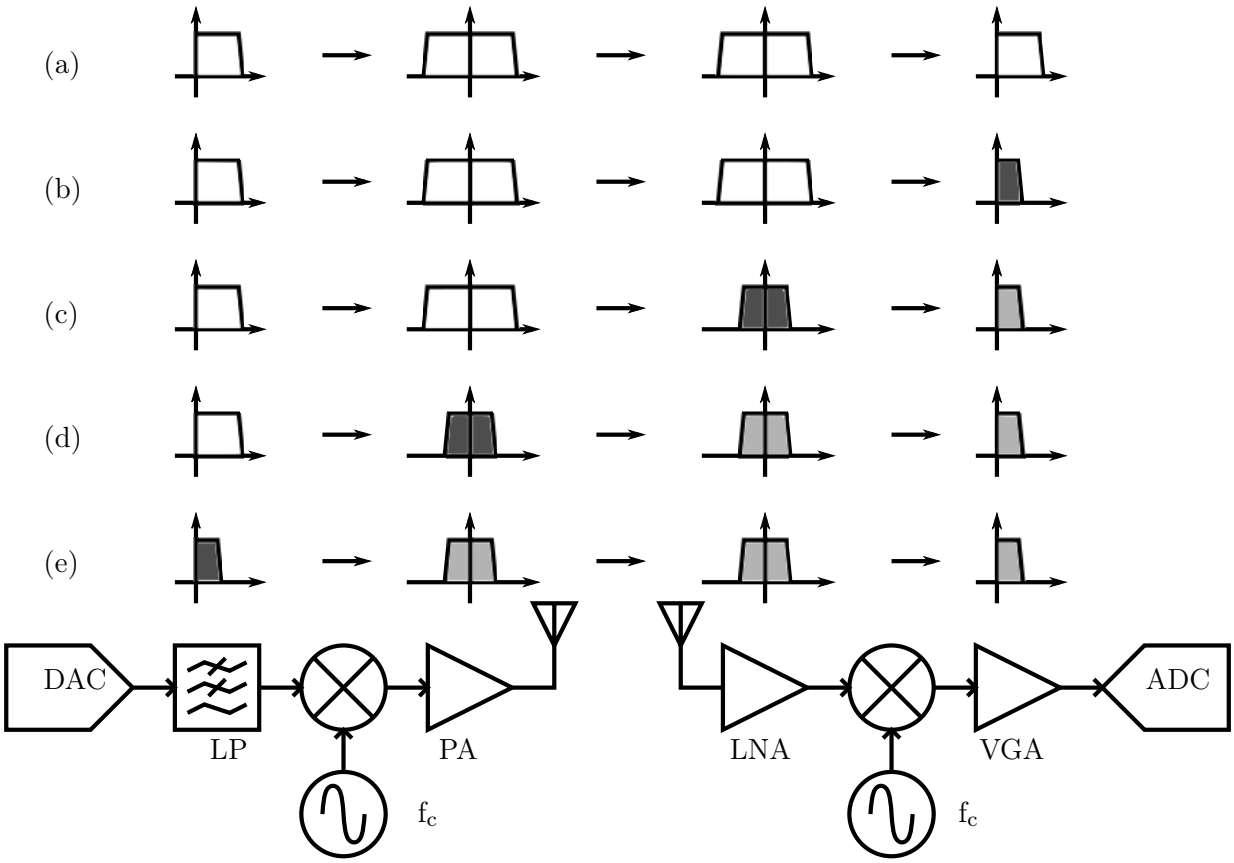


Figure 2.3.: Bandwidth limitation options in a generic wireless link. (a) No BW limitation. (b) The receiver output VGA limits the BW. (c) The RX front-end limits the BW. (d) The TX front-end PA limits the BW. (e) The TX IF bandwidth constricts the overall system BW.

from the respective other channel. The influence of this form of IQ imbalance on the wireless link performance is included in the equations from Ch. 1.4. Referring to the TX/RX chipset of the first generation hardware in [52], the simulated amplitude and phase imbalance at the output of the quadrature carrier generation path is reported to be below 0.5 dB and 2° respectively over the whole 200 GHz to 300 GHz range.

A second source of IQ mismatch, which is largely unique to wideband systems, is side-band asymmetry. If, for example, the bandwidth of the front-end power amplifier in the TX is not symmetric around its center frequency, an amplitude mismatch during the quadrature down-conversion process leads to frequency dependent leakage from one channel into the other.

Fig. 2.4 illustrates the issue in the spectral domain for the case of an amplitude mismatch between side-bands around a carrier frequency f_c. But a phase mismatch between upper and lower side-band components leads to the same issue. This could be caused by a distortion of the group delay vs. frequency during up or down-conversion or amplification at any point along the signal path in the RF front-end.

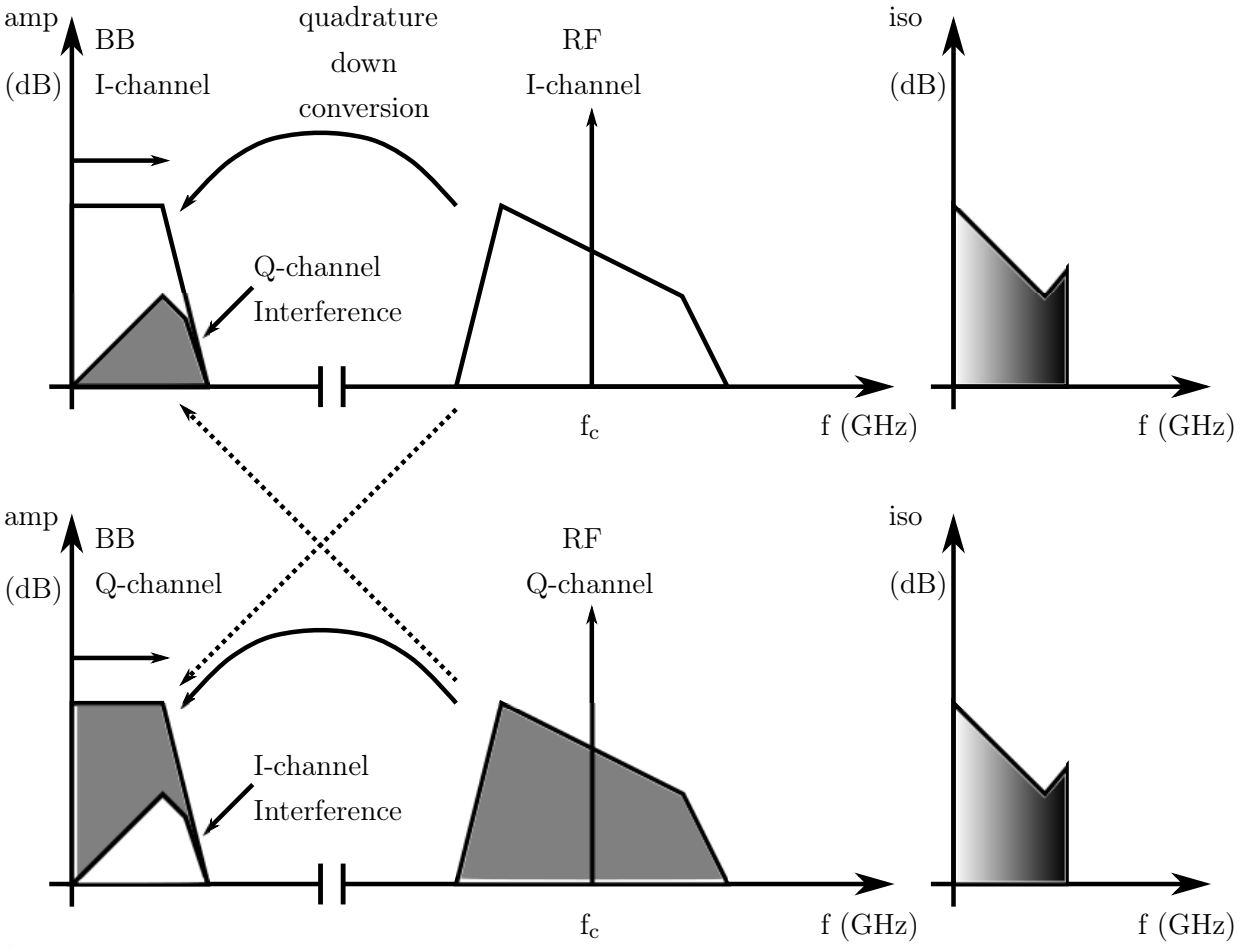


Figure 2.4.: IQ spectral leakage caused by side-band imbalance when performing quadrature down-conversion and corresponding channel isolation.

A *double side-band* quadrature direct-conversion wireless link therefore relies on side-band symmetry for good isolation between its two channels. In narrowband mmWave wireless links with bandwidth smaller than 1 GHz, which for example are part of the upcoming 5th generation wireless communication standard, this issue rarely occurs, as the absolute difference in side-band power and phase is negligible. But for a wireless link in the 200 GHz to 300 GHz band with an RF bandwidth of 20 GHz or more, side-band symmetry is highly relevant. The RF PA of the first generation hardware is also used in the chip-set presented in this thesis and is discussed further in Ch. 4.4. It has a peak gain of 13.4 dB at 226.5 GHz with a 3-dB bandwidth of 20 GHz. But a closer examination reveals, that this 3-dB bandwidth does not span symmetrically around the peak gain frequency. The gain at the frequency points with 10 GHz offset are 9.6 dB at 216.5 GHz and 11.5 dB at 236.5 GHz.

2.4. Chapter Conclusion: System Level Design Goals for a Wireless Link with Data-Rates in Excess of 100 Gbit/s

In conclusion, the analysis of the impairments of the 1st generation wireless front-end reveals a number of system level design goals for a 2nd generation wireless link to surpass this initial performance. A limiting factor is the used technology: In contrast to the experimental SiGe HBT technology used in the 1st generation hardware, the 2nd generation shall only use a commercially available technology. The choice fell on IHP's 0.13 µm SiGe HBT technology SG13G2, which is described in Ch. 1.5.1, with its 50 GHz lower f_T and 100 GHz lower f_{max} compared to the experimental technology.

These system level design goals are, in the order of the above sections:

1. **Increase the local oscillator frequency feeding the carrier generation path, such that LO leakage on the PCB level does not intersect the baseband bandwidth.** This is realized with the 30 GHz input to the 2nd generation ×8 multiplier chain in Chapter 3.

2. **Increase the transmitter output power.** This is hindered by the used technology, which effectively limits the PA output power. Instead, separating I- and Q-channel and feeding them to individual PAs for reasons discussed further below, could be considered as a form of power-combining.

3. **Reduce the receiver noise figure.** Again the used technology is a limiting factor. The 2nd generation receiver does not employ a low noise amplifier because of the following consideration: The noise figure of state-of-the-art LNAs does not justify a potential bandwidth reduction. Instead, a switching-quad based down-conversion mixer offers a superior bandwidth with a reasonable NF, if a following low noise baseband amplifier adds sufficient gain. The resulting down-conversion mixer and baseband VGA are presented in Ch. 4.3.2. Nonetheless, a design methodology for high-gain LNAs is discussed in Chapter 7.

4. **Reduce phase noise in the carrier generation path.** The close-carrier phase noise of an Agilent E8257D signal generator is higher at 30 GHz than at 15 GHz, but at least according to its data-sheet, the phase noise floor is the same. However, even in combination with the lower multiplication factor of the carrier generation path in the 2nd generation chip-set, phase noise remains one of the limiting factors in the presented wireless link. An illustrative calculation shows the lower boundary of the achievable EVM: with a multiplication factor of 8, integrating the phase noise from Ch. 2.3.4 over a bandwidth of 2.5 GHz for a 10 Gbit/s data rate using 16 QAM and inserting the result into Eq. 1.11 from Ch. 1.4, EVM can not be better than 1.9 % even with infinite SNR.

5. **Reduce the power of spurious harmonic tones stemming from carrier generation.** The new ×8 multiplier chain presented in Ch. 3.6 removes the former 15th and 17th spurious harmonic tones due to its higher input frequency. The two new tones

closest to the carrier are the 7th and the 9th harmonic. In Ch. 3.3, a sensitivity analysis of the multiplier topologies used in the $\times 8$ multiplier chain with the goal to reduce the generation of spurious harmonic tones reveals further design goals for inter-stage baluns, whose design is discussed in Ch. 3.6.1.

6. **Increase the usable bandwidth.** As the system bandwidth is mainly limited by the wire-bonds connecting the integrated circuits baseband in and outputs, a mitigation strategy is implemented in Ch. 4.5. Additionally the up-conversion mixer is replaced by a single-ended input micromixer, described in Ch. 4.3.1. A wideband variable gain amplifier at the output of the down-conversion mixer extents the receiver baseband bandwidth. All front-end components in the path of the baseband signal must have minimum amplitude and group delay variation with frequency to prevent symbol distortion.

7. **Reduce IQ mismatch.** Without exchanging the front-end PA in the transmitter, reducing IQ mismatch to increase IQ channel isolation is futile. The 2nd generation wireless front-ends use an entirely different approach instead. An individual micromixer and front-end PA per channel feeds a single polarization of a dual-polarized antenna. The antenna polarizations are orthogonal to each other; therefore their isolation increases the IQ channel isolation as a consequence. The use of both, channel isolation by phase in a quadrature scheme, and channel isolation by antenna polarization, is a form of stacking of orthogonalities.

The addition of channel isolation by polarization also enables an entirely different mode of operation in the presented 2nd generation wireless front-ends: By placing the carrier frequency not at the center of the RF bandwidth, but at its edges, the direct conversion wireless link moves from a *double-sideband* to a *single-sideband* mode. The isolation due to the polarization diversity of the antenna is sufficient to separate the former I and Q channels by 16 dB over the 6-dB baseband bandwidth, which is discussed in Ch. 5.3. This allows the data transmission with a data-rate in far excess of the 100 Gbit/s previously published in recent literature. A data-rate of 140 Gbit/s using 16-QAM and 32-QAM is demonstrated in Ch. 6.3.

3. Carrier Generation in the 200 GHz - 300 GHz Band

3.1. Introduction to the Chapter

Generating the typically needed 0 dBm power to feed a fundamental mixer in the 200 GHz to 300 GHz band with high efficiency and low phase noise remains a difficult challenge. The calculations in Chapter 1 show, how crucial the minimization of phase noise for a low error vector magnitude of a communication link is.

There is a variety of approaches to carrier generation for fundamental mixing, each with their own advantages and potential drawbacks. Using purely electronic methods, either high frequency voltage controlled oscillators (VCOs) or a low frequency local oscillator (LO) with a subsequent frequency multiplier chain can be used to generate a carrier signal above 200 GHz.

Leeson's model [54] is often used to characterize the power spectral density of oscillator phase noise $L(f_m)$ at carrier offset frequency f_m in dBc/Hz with

$$L(f_m) = 10log_{10}\left(\frac{FkT}{2P_{avs}}\left(1+\left(\frac{f_0}{2f_mQ_L}\right)^2\right)\left(1+\frac{f_c}{f_m}\right)\right) \tag{3.1}$$

where F is a measurement derived empirical fitting parameter to account for the increased noise in the $1/f_m^2$ region [55], f_c is the flicker corner frequency of the device, k is the Boltzmann constant and T is the temperature in Kelvin. Most relevant for this discussion are the carrier frequency f_0, the average power through the resonator P_{avs} in Watt and the loaded Q-factor Q_L. Increasing phase noise due to higher oscillation frequency can only be countered either by generating more P_{avs} or by using a resonant tank with higher Q-factor. The necessary condition for oscillation is met easier with faster transistors, but these typically exhibit lower breakdown voltages, as discussed in Ch. 1.5. This limits the achievable P_{avs}. Q_L is limited by the varactor Q-factor and the lossy BEOL, in which transmission lines for resonance tuning are implemented. Until high-Q resonators like dielectric pucks can be co-integrated with silicon based circuits [54], oscillator phase-noise performance in the 200 GHz to 300 GHz range are inherently limited [56].

In his book "Nonlinear Microwave Circuits" [57], S. Maas elucidates, that a frequency multiplier in fact is a phase multiplier. Therefore even an ideal, noiseless frequency multiplier increases the phase noise of an input signal by $20\log_{10}(N)$, where N is the multiplication factor. Accordingly a doubler adds at least 6 dB of phase noise; a tripler adds 9.54 dB;

a quadrupler adds 12 dB. Especially in low-noise receivers at mmWave frequencies, a balanced mixer architecture should be used in conjunction with a multiplier chain, to reduce the impact of carrier AM noise on the receiver noise figure.

A wideband multiplier chain allows exploring a larger amount of different carrier frequencies. The multiplier chains presented in this chapter have a 3-dB bandwidth far in excess of 10 % of their output center frequency. In contrast, the 234 GHz VCO presented in [56] has a tuning range of merely 5 %.

Additionally, using a frequency multiplier chain for carrier generation also has a very practical advantage in a laboratory setting: to characterize the maximum data-rate of an RF front-end chipset, transmitter and receiver have to be phase-locked. Carrier recovery circuitry for data-rates in excess of 100 Gbit/s are the subject of contemporary research [58] and not readily available from a commercial vendor. Instead, a single synthesizer can be connected to both TX and RX at the same time, and the phase can be adjusted through external phase shifters.

This chapter discusses the intricacies of frequency multiplier chain design in the 200 GHz to 300 GHz band under the constraints of the current technological state-of-the-art. Ch. 3.2 introduces all major active multiplier topologies used at mmWaves and found in the recent literature. Ch. 3.3 investigates the effect of spurious harmonic tones also generated in a multiplier chain on communication systems with tenth of GHz RF bandwidth and identifies the mechanisms of their generation with a sensitivity analysis performed on two doubler topologies.

Ch. 3.4 introduces the measurement setup used for characterizing their output power and harmonic rejection.

In Ch. 3.5 the first generation multiplier chain, which was used in the pioneering work on SiGe based communication front-ends at 240 GHz [42], and its shortcomings are recapitulated. Fig. 3.11 shows a block diagram of this $\times 16$ multiplier chain, with its four Gilbert cell mixer based multiplier, whose central transconductance pair and switching quad are driven in-phase.

A 2nd generation $\times 8$ multiplier chain with greatly improved output power and harmonic rejection is then introduced in Ch. 3.6. This multiplier chain uses a novel harmonic tuning scheme in the input of its first two frequency multipliers, which enables separate impedance transformations at the fundamental and at the second harmonic. This tuning scheme is custom fitted to miniaturized baluns used to drive balanced common-base doublers, which were chosen for their wide input matching bandwidth. The design procedure and simulation results of the three baluns used to convert the single-ended signals to differential ones within the multiplier chain is discussed in Ch. 3.6.1.

The output power and harmonic generation behaviour of the first two doublers are characterized in a $\times 4$ multiplier chain breakout measurement. The circuit schematic and measurement results of a 120 GHz pre-amplifier before the third doubler are presented. For the last multiplication step into the 200 GHz to 300 GHz frequency range, the classic Gilbert frequency doubler topology is revised for optimum conversion gain and output power using a new, very compact quadrature phase generation scheme. The complete $\times 8$ multiplier chain is part of

the radio front-end presented in Ch. 4. Its block diagram can be found in Fig. 3.15. This multiplier chain was used in the chip-set discussed in the remainder of this thesis.

Lastly, a second ×8 multiplier chain in B11HFC technology is presented in Ch. 3.7. It consists entirely of Gilbert frequency doublers, whose topology is a variation of the new phase optimized Gilbert doubler from the SG13G2 ×8 multiplier chain. Within its bandwidth lie the carrier frequencies of 41 of the total 69 designated channels included in the recent IEEE THz physical layer standard [1] for wideband communication. A block diagram of this multiplier chain is shown in Fig. 3.27. This multiplier chain was accepted for publication in [59] ; parts of the presented graphics are re-used here and marked with

3.2. An Overview of Frequency Multiplier Topologies

The simplest form of an active frequency multiplier requires only one transistor. By setting the appropriate conduction angle to class-B operation and below, the harmonic content at the output can be optimized for a single harmonic [60]. The earliest application of this principle to a SiGe HBT was published in [61]. A device with a f_{max} of 67 GHz was used as a frequency doubler with 55 GHz output frequency and 12 dB conversion loss. A 60 GHz frequency quadrupler in a 0.25 µm SiGe technology with 18 dB conversion loss was presented in [62].

With a different topology, a larger part of the input wave can be used for frequency multiplication to generate more output power. In [63] the most often used frequency multiplier topologies are recapitulated.

Balanced frequency multipliers make use of both input sine half-waves, but require a balun if driven from a single ended source. (a), (b) and (c) as shown in Fig. 3.1 are the transistor cores of balanced frequency doublers. They utilize a reduced conduction angle, such that only one transistor conducts current during a half-wave. The output current waveform equals a squared form of the input voltage. Due to the AC short, no fundamental component is present at the output. Of the three variants shown in Fig. 3.1, (a) has the largest conversion gain, (b) and (c) have the broadest input and output bandwidth respectively. A completely single-ended form of a balanced frequency doubler is presented in [64], where a four finger InGaAs HEMT transistor is split into parallel common-source and common-gate devices to arrive at a balanced topology.

Balanced frequency triplers are Class-A amplifiers driven into hard saturation. Their output waveform clips into a rectangular shape, which contains a strong third harmonic component. In contrast to the balanced doubler, here the fundamental is present at the output and has to be filtered, if it shall not spuriously drive a following stage. This makes triplers less suited for compact, integrated multiplier chains without high-Q filters. In terms of circuit properties, (d), (e), (f) follow the same pattern as their respective doubler counterparts. When in idle state, the discussed Class-A biased frequency triplers consume significantly more power than Class-B doublers.

The Gilbert cell is a versatile frequency multiplier. By feeding the same input signal to both its transconductance pair (TP) and switching quad (SQ) as shown in Fig. 3.1 (g), a current domain multiplication is performed. The Gilbert cell can be used either as doubler or quadrupler [65], depending on the input power split ratio between its TP and SQ. A new, optimum design procedure for the use of the Gilbert cell as a compact frequency doubler is discussed in Ch. 3.6.4. But from an intuitive standpoint, if the input signal is split evenly between the TP and the SQ and does not drive either into compression, the input signal is multiplied with itself, leading to a squaring action and a doubling of the fundamental frequency. In contrast, if the input signal compresses either the TP or the SQ, a rectangular waveform with a strong third harmonic component is present during multiplication. Therefore the fourth harmonic is produced. Because of the stacking of transistors, Gilbert cell frequency doublers require more voltage headroom than their Class-B counterparts.

Frequency quadrupling in an environment where less headroom is available can be done by driving four Class-C biased transistors with four copies of the fundamental input signal with 0°, 90°, 180° and 270° phase offset. Their combined output current has a strong fourth harmonic component [66] [67].

Another approach to frequency quadrupler design was introduced in [68]. Here, a pseudo-differential Class-C biased common-emitter pair feeds its output current to common-base cascode transistors, that have Class-AB bias and are driven with the opposite phase. By combining the resulting currents of two such transistor cores driven in quadrature, the fourth harmonic is produced.

The major drawback to both quadrupler topologies is the necessity of generating the aforementioned four phase-offset copies of the fundamental input signal. This can either be realized with a lossy polyphase network, often requiring additional pre-amplification before frequency multiplication, or by employing quadrature hybrids, whose size is proportional to the wavelength of the fundamental and therefore area-consuming.

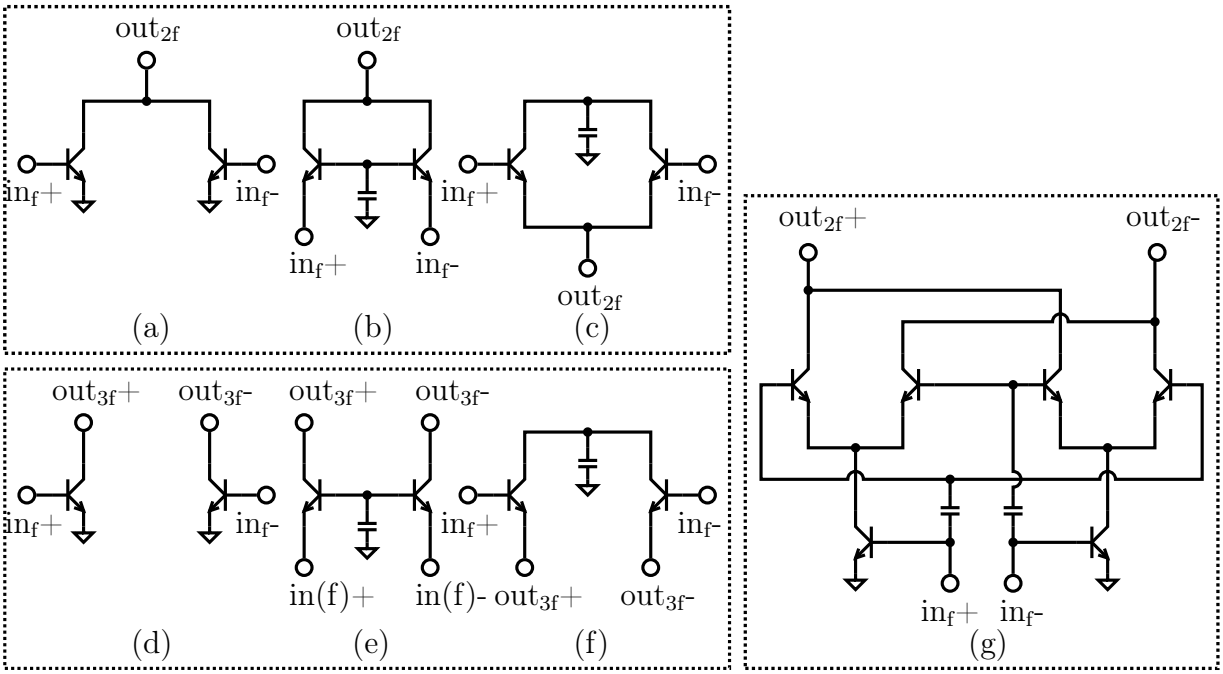


Figure 3.1.: Most commonly used frequency multiplier topologies. (a), (b), (c) are balanced frequency doublers using a reduced conduction angle. (d), (e), (f) are balanced frequency triplers when driven into hard saturation. (g) is a Gilbert cell, where the incoming signal mixes with itself to produce a second harmonic.

3.3. Spurious Harmonic Rejection

Not many of the publications on frequency multiplier chains in the 200 GHz to 300 GHz band report on the spurious harmonic rejection of their frequency multipliers. From the work of other groups in Tab. 3.2, only [69] shows measured results; in [70] at least simulated values are reported. But poor harmonic suppression can significantly diminish circuit performance in wideband communication or RADAR applications. In the latter, spurious tones generated in a hypothetical multiplier chain may not only be received after they were reflected by the targeted object. They may also mix with each other in the receiver, as it is typically driven from the same multiplier chain. This leads to the generation of multiple false targets in the low frequency output spectrum and thus impede target acquisition.

In short range, wideband communication based on a direct conversion transceiver system, harmonic spurs leaking from the carrier generation path into up- and down-conversion mixers cause two separate issues: First, the up-conversion mixer produces false copies of the baseband bandwidth centered around the most adjacent spurious tones. Very similar to the non-linear effects of compressed RF PAs, which are typically characterized with the adjacent channel power ratio (ACPR), these false copies lie outside the main channel and leak into the adjacent ones.

Second, if these false baseband copies in the RF spectrum are picked up by the receiver, they produce two different mixing products: When mixing with the same spurious harmonic

as they were produced with, they land directly at baseband. But instead of contributing to the overall signal strength, their different phase delay in relation to the main carrier makes them appear as noise, effectively reducing the signal-to-noise ratio. If the harmonic rejection of the multiplier chain driving either up- or down-conversion mixer is sufficiently high, these direct spurious-with-spurious harmonic mixing products are of little practical concern due to their small total power.

But when a false baseband copy is mixed with the strong carrier, it arrives at an intermediate frequency at considerable strength. This is why the absolute fundamental local oscillator frequency is important: Fig. 3.2a shows the RF and BB spectrum in a direct conversion transceiver, if a 240 GHz carrier is derived from a 15 GHz LO. The false copy than lies directly inside an imaginary baseband bandwidth of 20 GHz, raising the noise floor considerably. If the 240 GHz carrier instead is derived from a 30 GHz local oscillator as in Fig. 3.2b, the false copy starts moving out of the BB bandwidth, potentially only masking the higher frequency components of the original baseband.

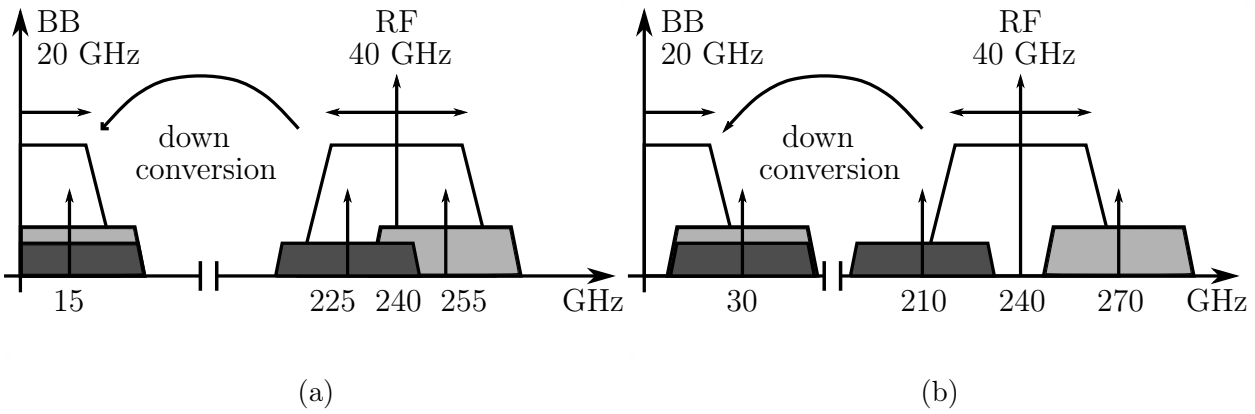


Figure 3.2.: Spurious harmonics in the TX generate false baseband copies at RF. With an imagined baseband bandwidth of 20 GHz, their down-conversion products with the strong carrier (a) lie completely in-band if the carrier is derived from a 15 GHz LO or (b) move out of band, if the carrier is derived from a 30 GHz LO.

The harmonic rejection of SiGe multiplier chains reported in the literature shall serve as a general reference for the following discussion. In [62], a 60 GHz single-transistor quadrupler has a 2nd harmonic rejection of 30 dBc, but only of 20 dBc regarding the 3rd harmonic. The 15 GHz to 120 GHz octupler from [71] suppresses the 7th and 9th spurious harmonics with 25 dBc. The 245 GHz doubler from [70] also produces a 4th harmonic, with is at simulated 30 dBc. The 240 GHz sixtupler in [69] has a 5th and 7th harmonic rejection of 25 dBc and 30 dBc respectively. And the 120 GHz quadrupler presented in [65] suppresses the higher 5th, 6th and 7th spurious tones by 30 dBc; the 2nd harmonic rejection was not reported, even though only a single Gilbert cell is used for generation.

The main sources of spurious harmonics in balanced frequency multiplier circuits can be identified in no particular order as

- imbalanced excitation, caused for example by unsymmetrical input balun layout

- compression of the active devices by an excessively large drive signal
- imbalances in differential pairs, either due to device mismatch itself or due to DC biasing offsets

A sensitivity analysis of the two frequency multiplier topologies used in the ×8 multiplier chain in SG13G2 technology reveals the precision necessary in feed network design for good harmonic suppression in a balanced circuit.

For the class-B doubler, the analysis is carried out at 30 GHz, using the common-base circuit from Fig. 3.1b with 8×0.12×0.96 µm^2 large transistors. $\lambda/4$ transmission lines at in_f+ and in_f- act as AC blocks at the fundamental, but short circuit the second harmonic. A simple LC circuit with a shunt inductor to DC supply and a series capacitor for AC decoupling matches the output to 50 Ω at 60 GHz. The supply voltage is 1.2 V and the current density of a single HBT is set to 0.33 mA/µm^2, which is the beginning of the forward-active region and results in peak conversion gain at 0 dBm input power.

The compression behaviour for an assumed 5° phase imbalance of the input signal can be found in Fig. 3.3. The spurious 4th harmonic rises rapidly as typical for a doubler entering compression. A back-off of 5 dB from peak conversion gain at 0 dBm input power is necessary to get a 30 dB suppression of the 4th harmonic.

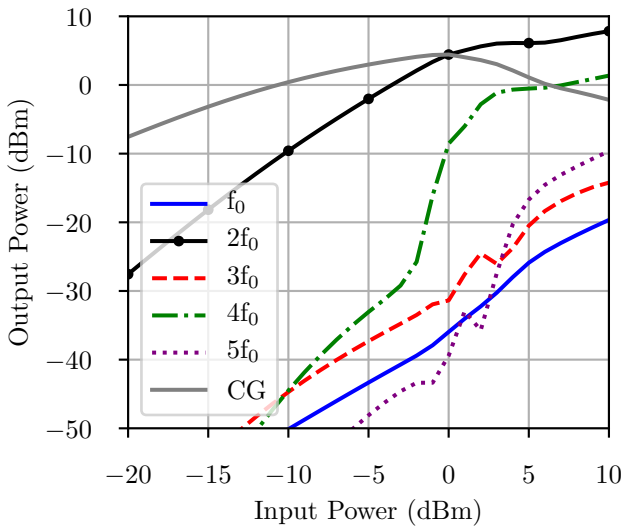
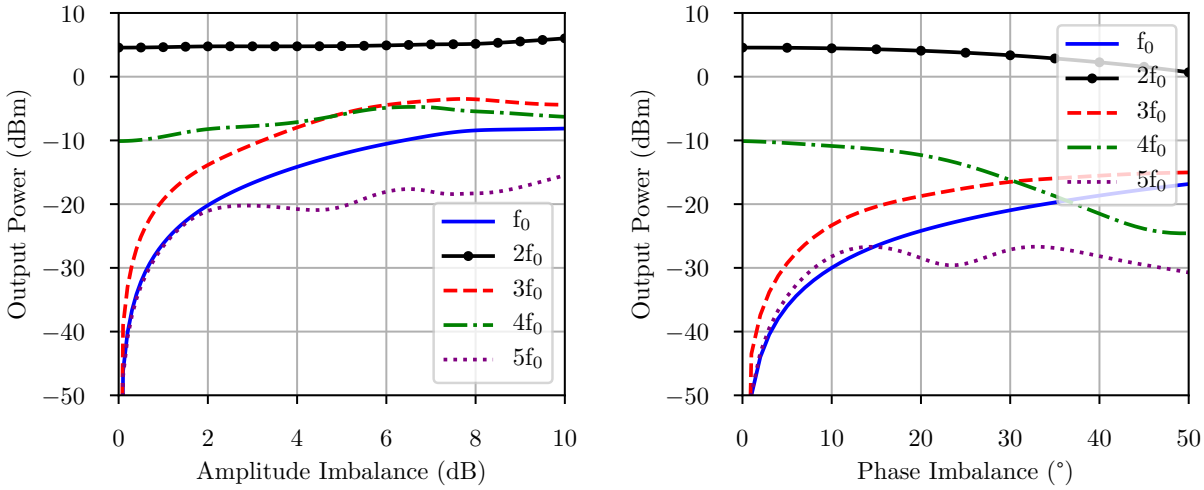


Figure 3.3.: Simulated harmonic generation in a generic 30 GHz pseudo-differential common-base Class-B frequency doubler with increasing input power for an assumed 5° phase imbalance of the input signal.

Fig. 3.4a shows the influence of an amplitude imbalance between the input port in_f+ and in_f- at peak conversion gain. The 4th harmonic is only 14.5 dB below the 2nd. But additionally, a 0.3 dB amplitude imbalance is sufficient to raise the output power of the 3rd harmonic to -30 dBm. 0.7 dB imbalance push the fundamental and the 5th to the same level.

Subjected to a phase imbalance, the class-B doubler behaves similar. According to Fig. 3.4b, the 3rd harmonic rises above -30 dBm at 5 ° phase imbalance between in_f+ and in_f-. The fundamental and the 5th harmonic surpass that level at 9 °.



(a) (b)

Figure 3.4.: Simulated harmonic generation in a generic 30 GHz pseudo-differential common-base Class-B frequency doubler caused by (a) amplitude imbalance or (b) input phase imbalance of the input signal.

The last frequency multiplier in the ×8 multiplier chain is a 120 GHz to 240 GHz Gilbert cell based doubler, for which the same sensitivity analysis can be conducted. Fig. 3.1g shows the general topology. For this analysis, the transistors in the transconductance pair and the switching quad are of 3 and 2 unit cell size, respectively. Shunt inductors resonate the input capacitance of the TP and the SQ. The output, similar to the class-B doubler, is matched to a differential 100 Ω using a simple LC circuit.

For the Gilbert doubler topology, there are two additional degrees of freedom: The relative phase of the signal feeding the TP to the signal driving the SQ, and the power difference between those two. For the subsequent analysis, the coupling capacitors from the circuit in Fig. 3.1g are removed and the differential terminals of the switching quad are driven separately from the transconductance pair.

By adjusting the relative phase between the SQ and the TP, the respective conduction angle can be aligned such that the an maximum amount of second harmonic current is generated for a given input power in the differential mode, but the second harmonic current in the differential mode is minimized. Fig. 3.5a shows the collector currents of the switching quad transistors, if the TP and the SQ are coupled in-phase, showing a clear imbalance of output current amplitudes and a non-90° phase shift between them. In contrast, Fig. 3.5b shows the collector currents with an optimized feeding phase angle, which results in a quadrature phase between the single collector currents. Fig. 3.5c and Fig. 3.5d depict, that optimizing the phase between the TP and the SQ presents a slight trade-off, as the maximum differential mode power does not coincide with minimized common mode output power. Also, the

optimal phase is not constant with input power, with -10 dBm input power in Fig. 3.5c and 0 dBm in Fig. 3.5d.

When setting the optimum phase angle, the input power is best split equally between the TP and the SQ, to achieve maximum output power. Fig. 3.6 depicts, that this split ratio is largely independent of the absolute input power level.

To highlight the advantage of choosing the correct phase angle between the TP and the SQ, the further analysis regarding spurious harmonic generation is conducted for two cases: First, for in-phase coupling, such that the TP and the SQ are fed with the same phase angle. And second, for a 30° phase offset between the two.

Fig. 3.7a and Fig. 3.7b show, that with increasing input power, a Gilbert cell utilizing an optimized phase angle produces around 1.5 dB higher differential mode conversion gain in the critical range before compression. In compression however, the output power of the fundamental, the 3rd and the 5th harmonic are greatly decreased. Only the 4th harmonic, while initially having a lower power level, rises above the in-phase fed one, once the Gilbert doubler goes into hard saturation.

To evaluate the influence of amplitude and phase imbalances on the harmonic generation in a $\times 2$ Gilbert frequency multiplier, a 6 port simulation is conducted. While recording the differential mode and common mode output power, the transconductance pair and switching quad are driven either in-phase or at optimized phase angle. Additionally, an amplitude or phase imbalance between the respective differential ports can be introduced.

Inspecting Fig. 3.8a and Fig. 3.8b elucidates, that an amplitude imbalance of more than 0.5 dB is equally detrimental to the differential mode harmonic rejection of the Gilbert multiplier, whether it is driven in-phase or not. But Fig. 3.8d shows that adhering to the optimized phase angle feeding method, the Gilbert doubler is more resilient against phase imbalance compared to in-phase coupling in Fig. 3.8c. The effect is especially pronounced with regards to the spurious 3rd harmonic, which reaches a level of -30 dBm only at a 30° phase imbalance, instead of 9°.

Fig. 3.9 presents the simulated common-mode output power of the generic 240 GHz pseudo-differential Gilbert frequency doubler when driven with a 0 dBm input signal. An amplitude imbalance of more than 0.5 dB leads to a pronounced spurious harmonic generation. Choosing an optimized phase angle between the TP and the SQ suppresses the second harmonic common mode by 8 dB, while the fourth harmonic power is practically unchanged. For a phase imbalance of the input driving signal, the behaviour is similar. The odd harmonics pass -30 dBm at 20° phase imbalance.

A number of design guidelines for balanced frequency multiplier and their feeding networks can be derived from this sensitivity analysis. Again in no particular order:

- For both doubler topologies, operating in a considerable back-off from their saturated output power decreases the generation of the spurious 4th harmonic.
- The amplitude imbalance generated for example in a non-ideal balun shall not exceed 0.3 dB, when it feeds a balanced doubler.

- The drive signal phase imbalance should stay below 5° for a class-B doubler.
- An optimized phase relation between the TP and the SQ can desensitize a Gilbert doubler against phase imbalance of its drive signal.
- The same phase relation increases the conversion gain of a Gilbert doubler before it reaches saturation. This improves conversion efficiency when operating in back-off.
- A 1:1 input power split ratio between the transconductance pair and the switching quad in a Gilbert cell doubler is optimal for power generation.

A final note from a systems perspective: long range communication transceivers suffer less from spurious harmonic tones stemming from multiplier chain based carrier generation. The free space path loss affects the aforementioned false baseband copies in the RF spectrum in the same way as the wanted channel contents. Due to the high noise in circuits using the current state-of-the-art SiGe technology and operating in the 200 GHz to 300 GHz band, the mixing products from the false baseband copies submerge in the noise floor in wireless links over more than five meter distance. But as transistor technology progresses, leading to increased output power and reduced noise, the limited harmonic rejection has to be addressed. Otherwise the problem is going to re-appear.

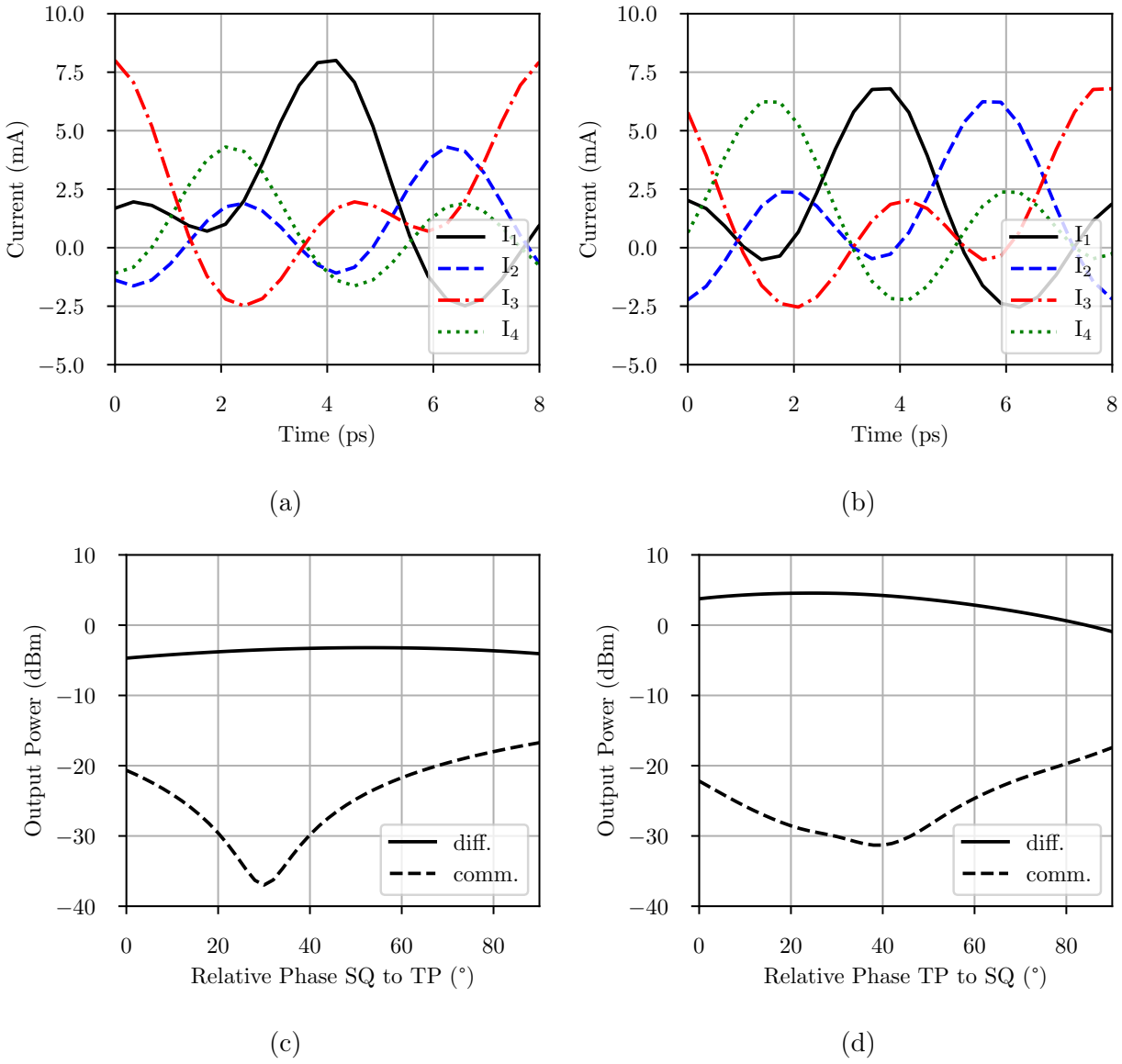


Figure 3.5.: Simulated switching quad collector currents of a generic 240 GHz pseudo-differential Gilbert frequency doubler with the drive power (a) in-phase or (b) with optimized phase to the TP and the SQ. The optimized phase leads to higher power in the differential mode and better suppression of the common mode, but it is not independent from drive power, with -10 dBm in (c) and 0 dBm in (d).

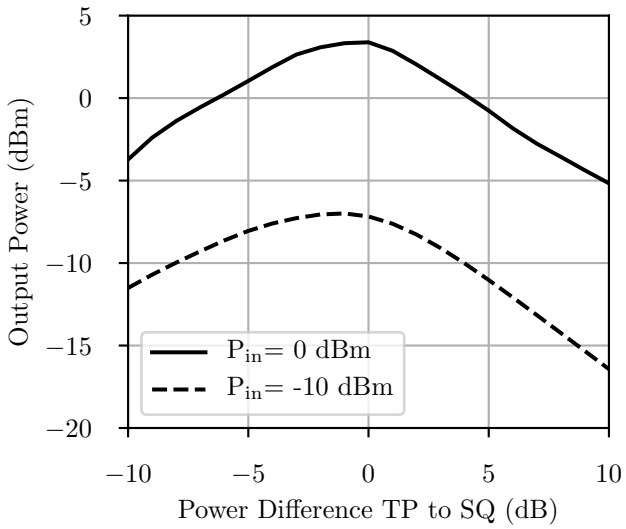
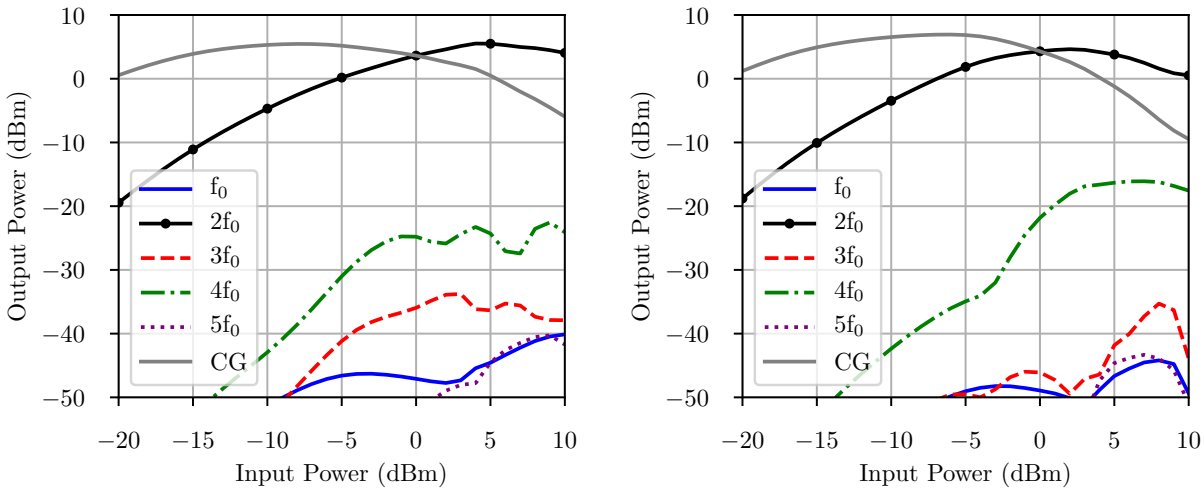


Figure 3.6.: Simulated differential mode output power of a generic 240 GHz pseudo-differential Gilbert frequency doubler dependent on the division of the input power between the TP and the SQ, when the SQ has a 30° phase advance in relation to the TP.



(a) (b)

Figure 3.7.: Simulated differential mode harmonic generation in a generic 240 GHz pseudo-differential Gilbert frequency doubler with increasing input power for an assumed 5° phase imbalance of the input signal and when the transconductance pair and the switching quad are fed (a) in-phase or (b) at optimum phase offset.

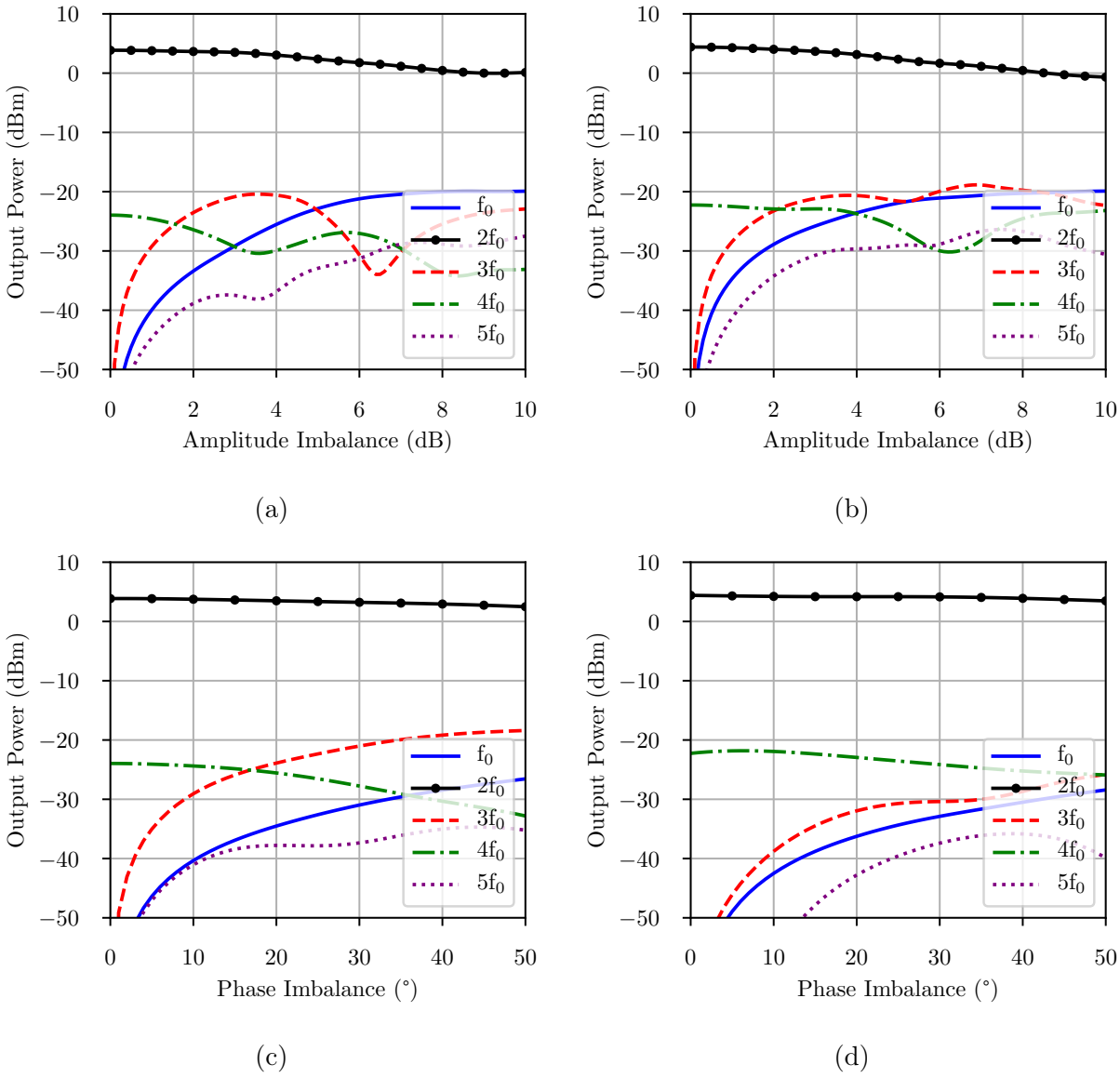


Figure 3.8.: Simulated differential mode harmonic generation with 0 dBm input power in a generic 240 GHz pseudo-differential Gilbert frequency doubler caused by amplitude or phase imbalance of the input signal when the transconductance pair and the switching quad are fed (a) (c) in-phase or (b) (d) at 30° phase offset for common mode suppression.

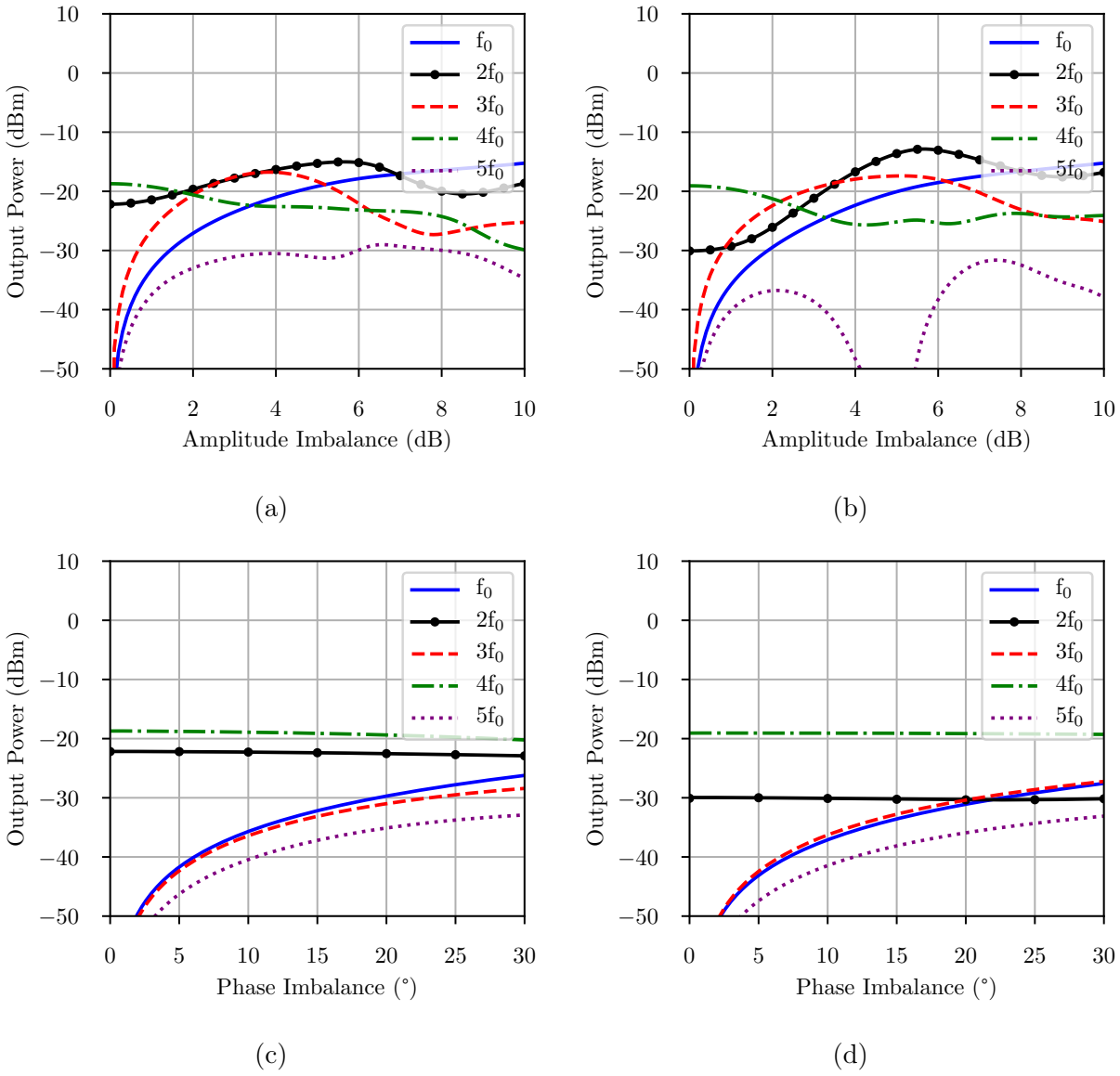


Figure 3.9.: Simulated common mode harmonic generation with 0 dBm input power in a generic 240 GHz pseudo-differential Gilbert frequency doubler caused by amplitude or phase imbalance of the input signal when the transconductance pair and the switching quad are fed (a) (c) in-phase or (b) (d) at 30° phase offset for common mode suppression.

3.4. Multiplier Chain Measurement Setup

The measurement setup for the ×4, ×8 and ×16 multiplier chains is shown in Fig. 3.10. A Keysight E8257D generates the drive signal with frequencies up to 40 GHz, which was applied to the multiplier chain through a 1.5 m coax cable and a GGB ground-signal-ground (GSG) probe. The probe and cable losses were calibrated out using a Short-Open-Load (SOL) method. Frequency extender modules from RPG and OML are used for down-conversion of all harmonic tones. In W-band, a RPG extender mmWave extender module connects to a 1 mm coax cable and associated GSG probe. In D-band a 110 GHz to 170 GHz OML mmWave extender module, WR06 waveguide and GSG probe are used, as are in J-band with a 220 GHz to 325 GHz module, appropriate WR03 waveguide and GSG probe. The resulting low frequency tone was fed into an Agilent E4440A spectrum analyzer. The down-conversion gain of these extender modules was previously calibrated with a counterpart module, whose respective output power was determined with a VDI PM4 total power calorimeter. With this data, the waveguide and probe losses were recorded with a second set in a back-to-back fashion by probing a short transmission line piece on a calibration substrate.

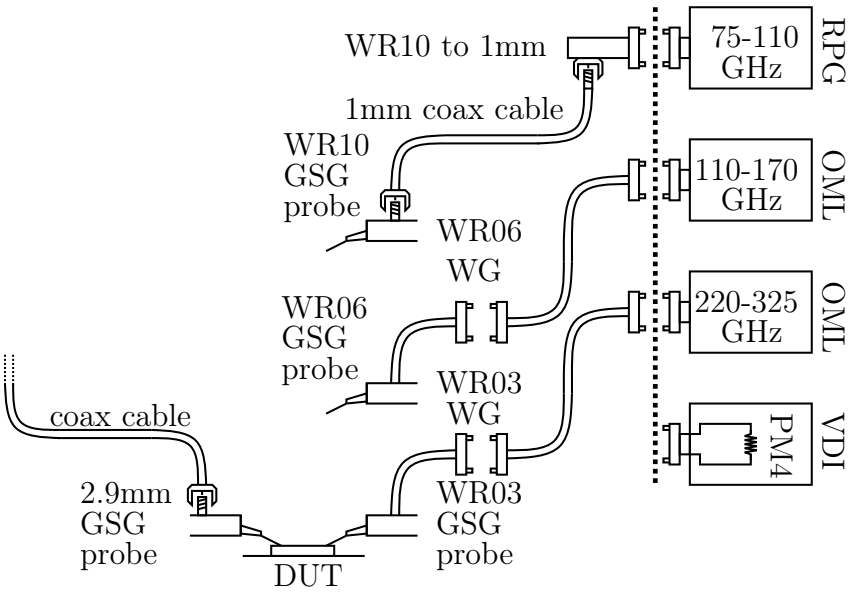


Figure 3.10.: Measurement setup for the ×4, ×8 and ×16 multiplier chains. Frequency extender modules from RPG and OML are used for down-converting all harmonic tones.

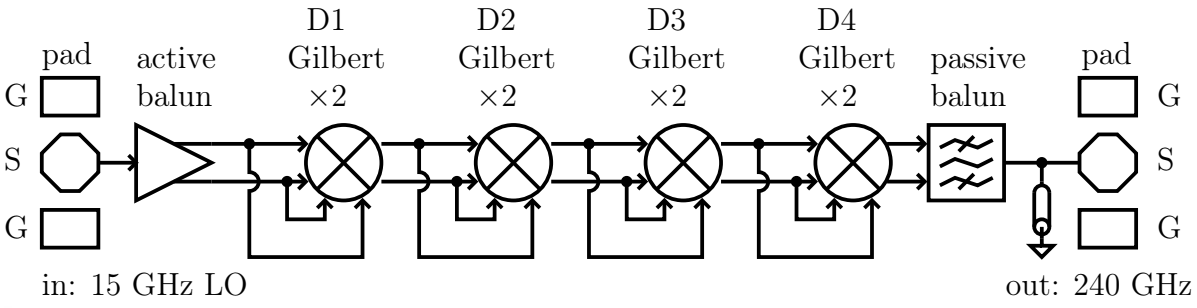


Figure 3.11.: Block-level overview of the 1st gen. ×16 multiplier chain from [72]

3.5. 1st Generation ×16 Multiplier Chain in SG13G2 Technology

3.5.1. Circuit Description

The ×16 multiplier chain used in this section has first been reported in [72]; further design details are presented in [42]. A block diagram of this ×16 multiplier chain is shown in Fig. 3.11. This multiplier chain employs a Gilbert cell mixer based architecture. Fig. 3.12 shows the schematic of a single frequency doubler stage; Table 3.1 lists the component values of all stages D1-D4 as assigned in Fig. 3.1. Since according to

$$\sin(2\pi ft) \cdot \sin(2\pi ft) = \frac{1}{2} \cdot (1 - \cos(2 \cdot 2\pi ft)) \tag{3.2}$$

an input sine wave with frequency f multiplied with itself generates a second harmonic at frequency $2f$, an in-phase coupling mechanism through capacitor C3 is implemented here. In contrast to driving the transconductance pair and the switching quad in quadrature [73], this significantly reduces the area consumption by omitting any quadrature hybrids. The drawback is a slightly reduced conversion gain and a generation of dc-offsets, which are easily blocked by interstage capacitors.

Four cascaded ×2 stages are staggered tuned in frequency to enhance the bandwidth and smooth the roll-off beyond the 3-dB bandwidth in the LO chain. The output impedances of the doubler D1 and D3 are tuned high in respect to their center frequency, D2 and D4 are tuned low, resulting in an overall flat response. An active balun for single-ended to differential conversion of the external low-frequency signal ($<$ 20 GHz) drives the succeeding ×16 multiplier chain.

3.5.2. Measurement Results

The ×16 multiplier chain breakout was measured using the setup described in Fig. 3.10. The output power levels at the 14th, 15th, 16th, 17th and 18th harmonic were measured single-ended through an on-chip balun. Its loss is estimated to be 2.5 dB from a back-to-back

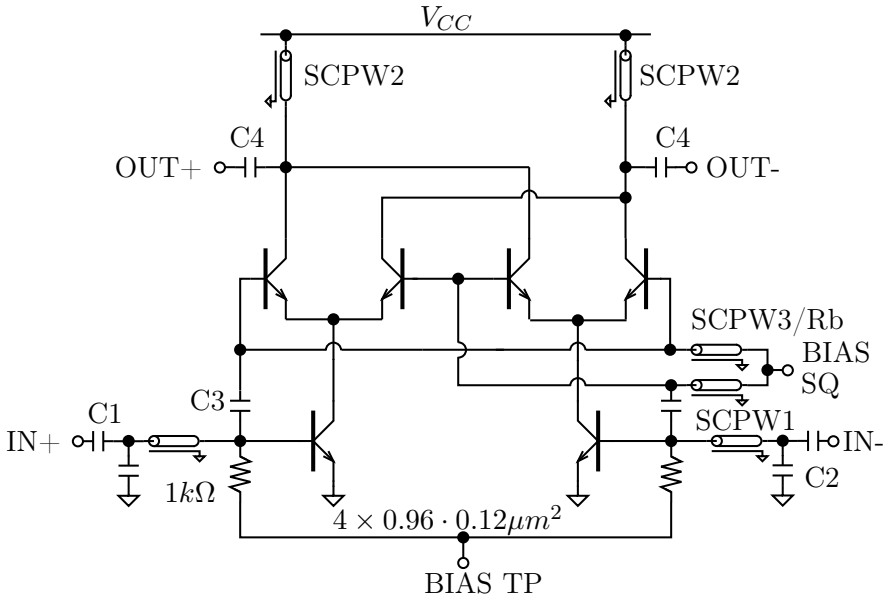


Figure 3.12.: The frequency doublers D1-D4 used in the ×16 multiplier chain are Gilbert cell based. The transconductance pair is biased through a current mirror, the switching quad through a resistive voltage divider. To reduce area at lower frequencies, the resistive voltage divider connects to resistances Rb, at higher frequencies to shielded coplanar waveguides SCPW3. Table 3.1 shows all component values.

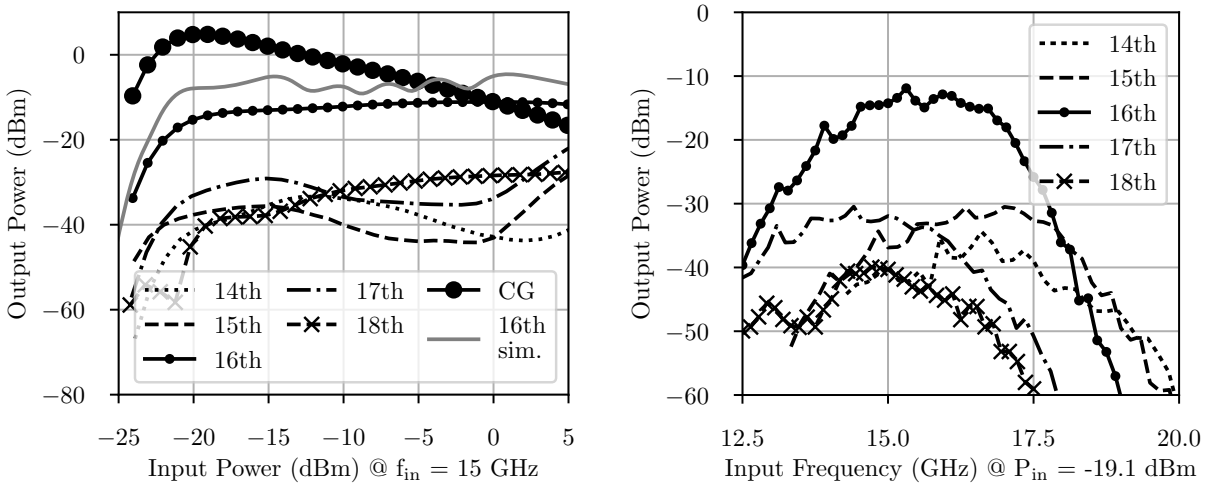
breakout, that was manufactured alongside the multiplier chain, but it was not de-embedded from any measured result.

Fig. 3.13a shows the output power of the ×16 multiplier chain in relation to the input power, when driven with a 15 GHz input signal. A peak conversion gain of 4.8 dB is reached at -19.1 dBm input power, with an output power of -14.3 dBm. The closest spurious harmonic in terms of power is the 17th at -32 dBm; the next tone in the output signal is the 15th, which then is at -36.9 dBm. The 14th is at -39.8 dBm and the 18th at -40.3 dBm. By driving the multiplier chain deeper into compression, the harmonic content of the output signal changes. At 0 dBm input power, the output power of the 16th harmonic is -11 dBm. The suppression of the 14th harmonic rises to 32.9 dB, the 15th to 32 dB and the 17th to 23 dB. Only the 18th harmonic rejection degrades to 17.4 dB.

Fig. 3.13b shows the output spectrum over frequency of the ×16 multiplier chain at the -19.1 dBm input power belonging to the peak CG point. A peak output power of -11.9 dBm was measured at 245 GHz. The 3-dB bandwidth spans a total of 29 GHz from 232 GHz to 261 GHz. When driven into compression as shown in Fig. 3.14, the 3-dB bandwidth widens to 41 GHz, from 232 GHz to 273 GHz and a peak output power of -8.65 dBm at 245 GHz. When driven into compression, the multiplier chain consumes 0.3 W.

	D1	**D2**	**D3**	**D4**
C1	–	–	–	40 fF
C2	–	–	–	20 fF
C3	200 fF	200 fF	75 fF	80 fF
C4	105 fF	33 fF	20 fF	20 fF
SCPW 1	105 µm 55 Ω	105 µm 55 Ω	105 µm 55 Ω	105 µm 55 Ω
SCPW 2	535 µm 70 Ω	285 µm 70 Ω	90 µm 55 Ω	30 µm 55 Ω
SCPW3	–	–	265 µm 55 Ω	90 m 55 Ω
Rb	1 kΩ	1 kΩ	–	–

Table 3.1.: Frequency doubler component values as marked in Fig. 3.12



(a) (b)

Figure 3.13.: Measured results of the ×16 multiplier chain breakout. (a) Output power versus input power with a 15 GHz input signal. (b) Output power versus input frequency when driven with a -19.1 dBm input signal for optimum conversion gain at 15 GHz.

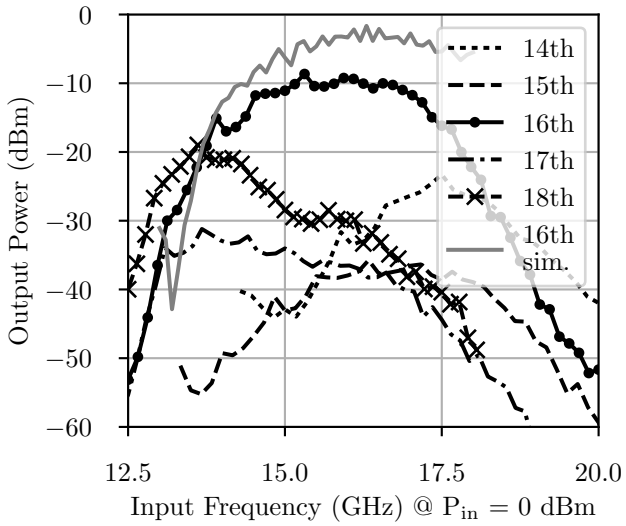


Figure 3.14.: Measured output power of the ×16 multiplier chain breakout versus input frequency when driven into compression with a 0 dBm input signal.

3.6. 2nd Generation ×8 Multiplier Chain in SG13G2 Technology

3.6.1. Lumped-Distributed Balun Design

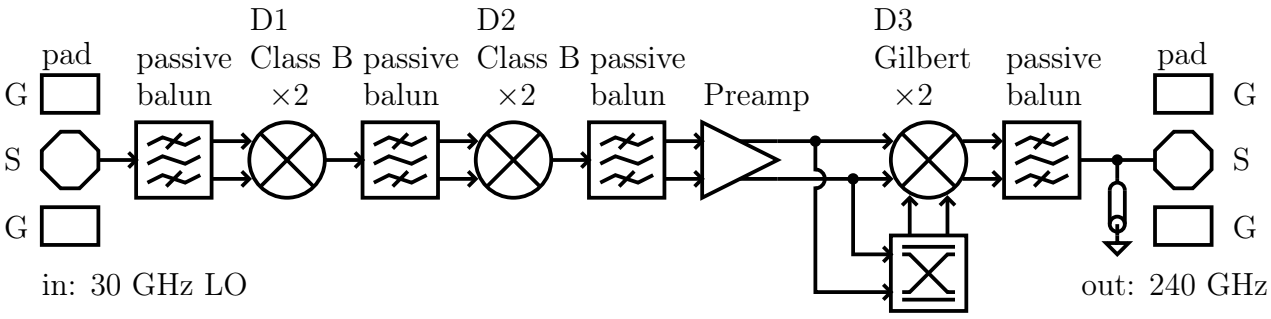


Figure 3.15.: Block-level overview of the 2nd gen. ×8 multiplier chain in SG13G2

When utilizing a balanced driving scheme for all three frequency doublers, two of which are realized in a class B topology, in a × 8 multiplier chain as shown in the block diagram in Fig. 3.15, three single-ended to differential baluns are required. If active baluns are not an option because of power consumption, passive distributed baluns are a viable alternative. Classical Marchand type baluns employ two quarter wavelength coupled line sections for wideband impedance matching. Due to their wavelength dependence, the baluns also act as band pass filters for spurious harmonic suppression. A lossless $\lambda/4$ Marchand balun with a coupled line common mode impedance Z_{oe} of 97 Ω and an odd mode impedance Z_{oo} of 26 Ω provides 116 % bandwidth [74]. But it also consumes a large amount of area, even at mmWave frequencies.

A methodology was introduced in [75], which trades of the bandwidth of the balun for its size by adding odd mode lumped capacitors to shrink down the coupled line length. Fig. 3.16a shows a general circuit schematic of such a miniaturized balun. Two coupled line sections with Z_{oe}, Z_{oo} and electrical length Θ transform a single-ended real input impedance Z_{in} into a real output impedance Z_{out}. The second coupled line section can either be terminated in a short circuit or an open. In the confines of this thesis, a balun whose second coupled line section is terminated in a short circuit shall be termed *transformer* balun; when terminated in an open, the balun shall be called *Marchand* balun.

Capacitors C_1 or C_2 at either input or output introduce additional degrees of freedom for choosing the electrical length of the coupled line sections. [75] then derived equations for calculating the necessary Z_{oe}, Z_{oo} for transforming an arbitrary Z_{in} to an arbitrary Z_{out}, in dependence of their length and the reactance from the capacitors. Fig. 3.16b depicts potential combinations of Z_{oe}, Z_{oo} and coupled line length for a 50 Ω Z_{in} and a 30 Ω Z_{out}, if the reactance presented by C_1 is 0.025 and C_2 is set to 0. The chosen Z_{in} and Z_{out} are used in the input balun of the first Class-B frequency doubler used in the ×8 multiplier chain in SG13G2 technology.

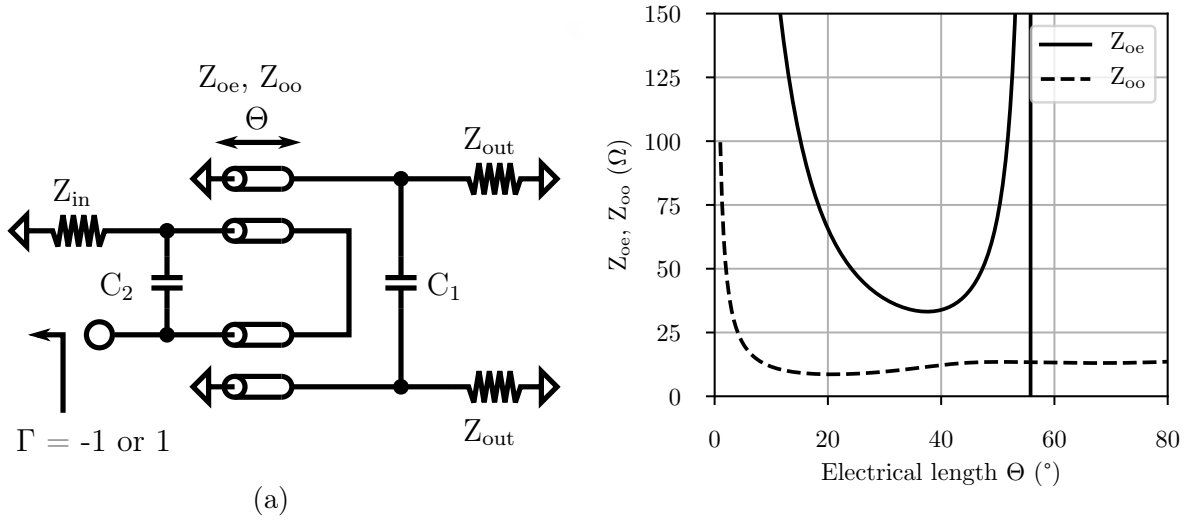


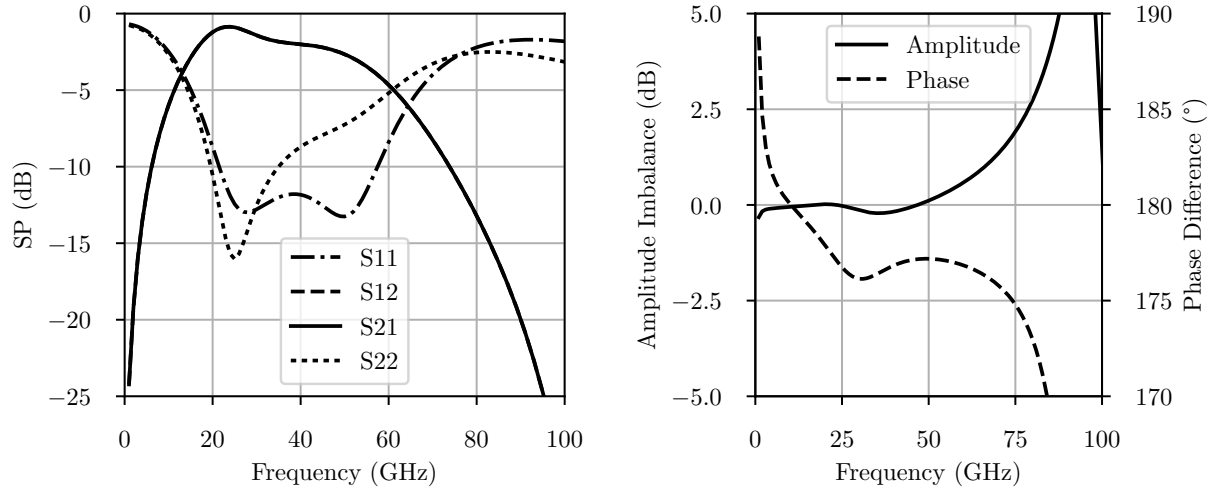
Figure 3.16.: (a) General lumped distributed balun schematic. (b) Even and odd mode coupled line impedance for Z_{in} = 50 Ω, Z_{out} = 30 Ω and wC_1 = 0.025.

Some of the assumption made in the methodology from [75] do not hold when designing mmWave silicon integrated circuits. Primary concerns are the rather limited choice of realizable coupled line impedances in the BEOL, their loss and their disparate even and odd mode phase delay. Thus all baluns used in the presented multiplier chains underwent thorough EM-simulation using Ansoft HFSS. The circuit schematics for a 30 GHz transformer balun and a 60 GHz Marchand balun can be found in Fig. 3.20 alongside the respective common-base frequency doublers, for whose input they generate the differential excitation. Furthermore a 120 GHz Marchand balun is included in the schematic of the pre-amplifier presented in Fig. 3.23a.

The first, lumped distributed transformer balun converts the 60 Ω differential input impedance of the 30 GHz to 60 GHz Class-B frequency doubler into a 50 Ω impedance for on-wafer probing and as termination for the PCB-IC distributed filter of the communication front-end from Chapter 4. The balun consists of two 375 µm long coupled line sections. The input line is shorted at its very end. Two series capacitors of 133 fF each are placed in shunt between the two differential ports at the output of the balun. This introduces an even mode node, which is used in a novel harmonic tuning scheme in Ch. 3.6.2.

Fig. 3.17a presents the simulated differential mode scattering parameter of the 30 GHz transformer balun, including the second harmonic tuning elements further discussed in Ch. 3.6.2. The balun has a minimum loss of -0.86 dB at 24 GHz, with its 3-dB bandwidth spanning from 13 GHz to 57 GHz. The amplitude imbalance between the transformer baluns output ports at 24 GHz stays below 0.5 dB until 59 GHz, and the phase imbalance stays below 5° between 10 GHz and 75 GHz, as shown in Fig. 3.17b.

The second, lumped distributed Marchand balun uses equal sized 70 fF capacitors at the input port and the input line termination. Furthermore, two of these 70 fF capacitors are



(a) (b)

Figure 3.17.: Simulation results of the first, lumped distributed transformer balun. (a) shows the differential mode scattering parameters and (b) shows the amplitude imbalance and the phase difference at the two output ports versus frequency.

connected in series between the differential output nodes to form a 35 fF capacitor in the differential mode. The coupled transmission line sections are of 227 µm length.

Fig. 3.18a and 3.18b summarise the same parameters for this 60 GHz Marchand balun feeding the second Class-B frequency doubler in the ×8 multiplier chain in SG13G2 technology. The doubler has a 100 Ω differential input impedance. At 64 GHz center frequency, the minimum loss is 2.85 dB with a 3-dB bandwidth from 49 GHz to 86 GHz. The amplitude and phase imbalance at center frequency is 0.12 dB and 2.7° respectively.

The 120 GHz balun uses the same topology for the same impedance transformation ratio as the previously described 60 GHz Marchand balun, but scales the capacitors to 32 fF and the coupled line sections to 145 µm.

At 120 GHz center frequency, Fig. 3.19a shows the scattering parameter for the third, lumped distributed Marchand balun. The simulated minimum loss is 2.15 dB at 120 GHz with a 65 GHz 3-dB bandwidth. Fig. 3.19b shows a 0.01 dB amplitude imbalance and a phase imbalance below 1° at that frequency.

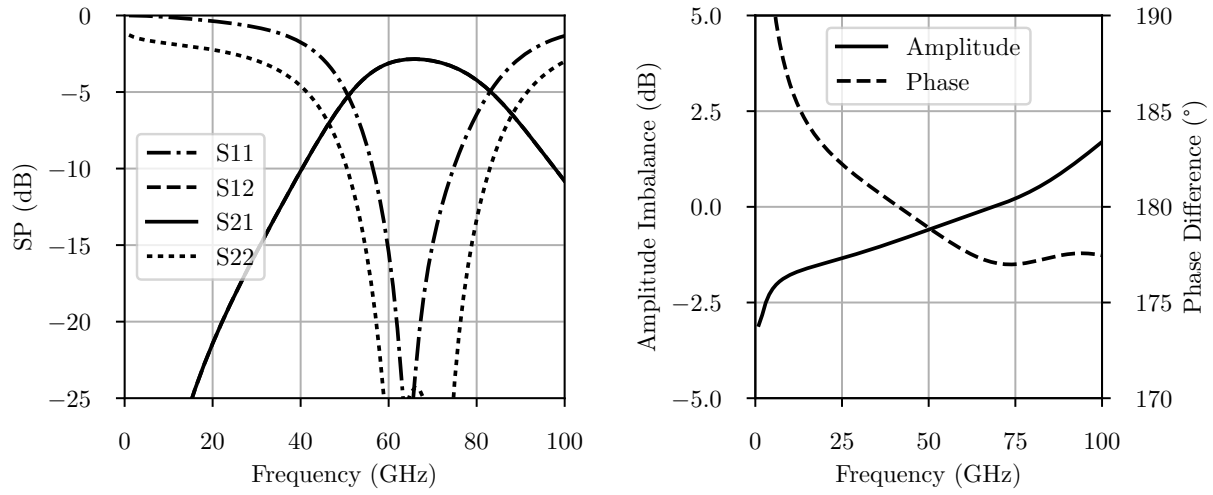


Figure 3.18.: Simulation results of the second, lumped distributed Marchand balun. (a) shows the differential mode scattering parameters and (b) show the amplitude imbalance and the phase difference at the two output ports versus frequency.

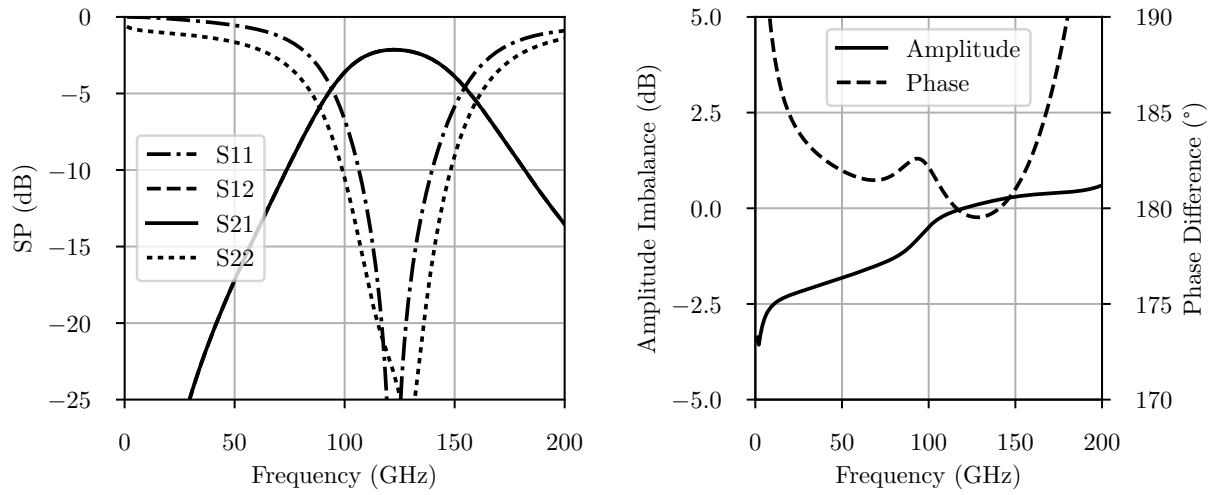


Figure 3.19.: Simulation results of the third, lumped distributed Marchand balun. In relation to the frequency (a) shows the differential mode scattering parameter and (b) amplitude imbalance and phase difference at the two output ports.

3.6.2. Class B Doubler

Circuit Description

The first two frequency multipliers in the ×8 multiplier chain both use a differentially driven class-B topology as shown in Fig. 3.20. They are deliberately designed for just enough bandwidth to allow free choice of carrier placement within the bounds of the fixed RF bandwidth of the TX front-end amplifiers. But as a secondary feature, the employed doubler design also diminishes the propagation of spurious harmonic tones. Common-base transistors are at the doubler cores. With the real part of its input impedance approximately equal to $1/g_m$ for all frequencies, the input matching bandwidth is defined by their respective input balun and its ability to present a short circuited second harmonic at the transistors emitters.

One approach then is to extend the methodology for the design of miniaturized lumped-distributed baluns introduced in [75] and discussed in Ch. 3.6.1 by a harmonic tuning technique.

The first doubler uses transistors with a size of $8\times0.12\times0.96$ µm^2. The miniaturized input balun transforms the 50 Ω single-ended input impedance to the doublers 60 Ω differential impedance seen at the emitter nodes.

A capacitor at the balun output common mode node, in combination with 30 Ω series transmission lines, tunes the second harmonic impedance in the common mode, without affecting the fundamental impedance in the differential mode. Using this novel harmonic tuning scheme, a second harmonic short circuit is presented to the doublers input. Fig. 3.21a shows the simulated common-mode output reflection coefficient of the transformer balun. The second harmonic at 60 GHz is highlighted with a red circle. Simulation predicts, that this enhances the doublers peak conversion gain by 5 dB at 30 GHz input frequency.

At the output, an L-match with two small on-chip inductors transforms the doublers output impedance to 50 Ω.

The second doubler uses smaller $4\times0.12\times0.96$ µm^2 transistor sizes. The differential input impedance with 100 Ω is therefore higher than in the first doubler. This enables the use of a miniaturized Marchand balun with lower impedance transformation ratio, therefore higher bandwidth and without DC short circuit at its input. Thus no lumped capacitor is needed between first and second multiplier stage, which also would limit the low frequency bandwidth.

Similar to the first stage, a common mode tuning at the second harmonic was realized by tapping the baluns common mode node with a transmission line stub with adjacent capacitor and series transmission lines with 50 Ω characteristic impedance, which do not affect the differential mode at the fundamental frequency. Fig. 3.21b shows the simulated output reflection coefficient of the miniaturized Marchand balun. The second harmonic at 120 GHz is highlighted with a red circle.

Large capacitors present a common mode AC ground at the transistors base nodes. A series-shunt transmission line circuit matches the output to 50 Ω.

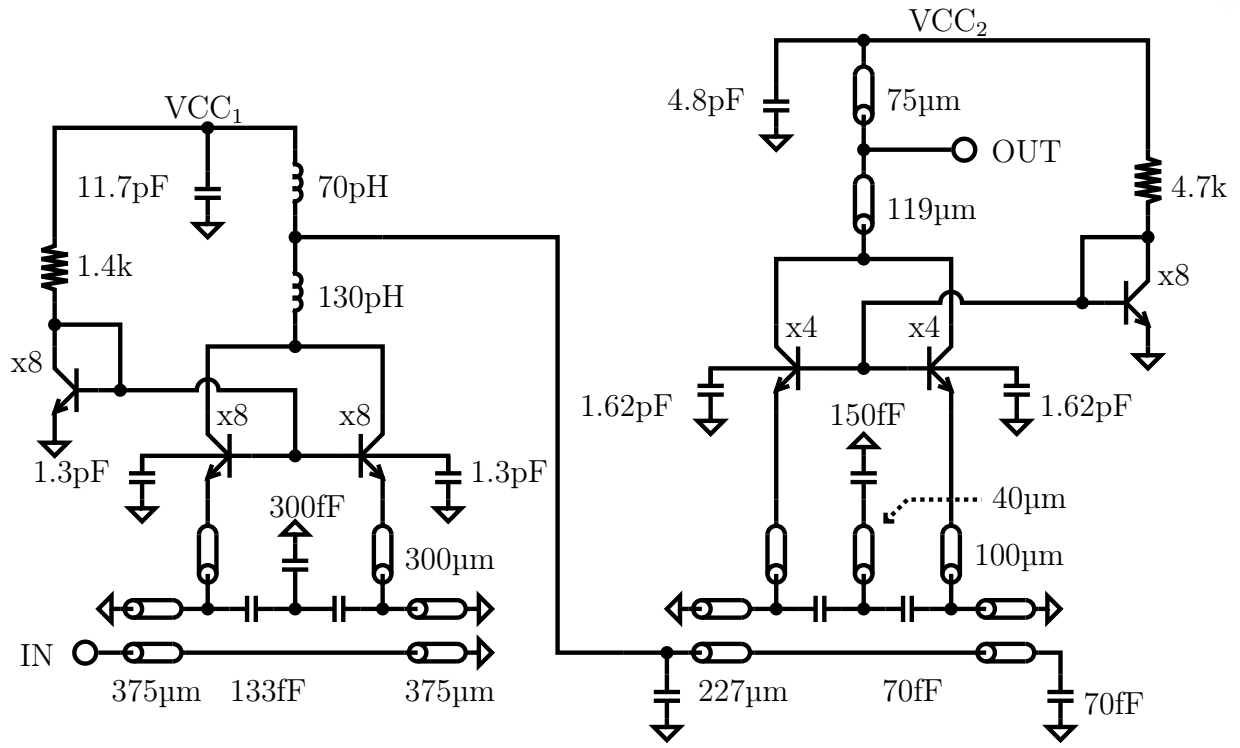
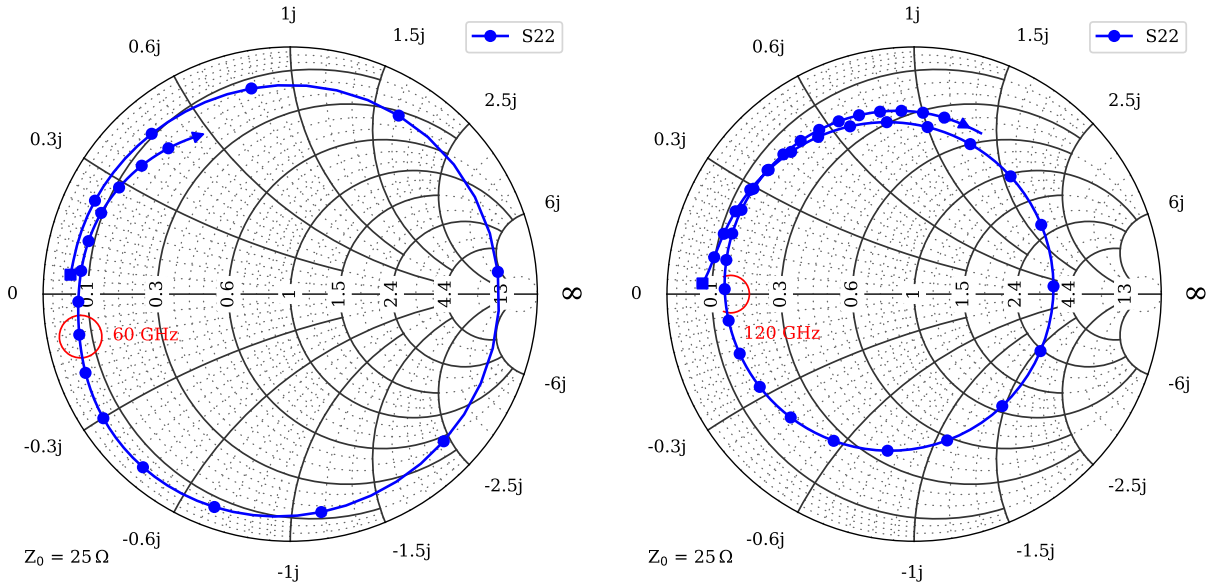


Figure 3.20.: First frequency doubler stage from 30 GHz to 60 GHz. A miniaturized transformer balun generates a balanced input signal from a single ended feed. This differential signal drives a class B doubler in common base topology, which presents a flat input impedance.

Breakout Measurement Results

A breakout for on wafer measurements of the first two frequency doublers connected in series into a ×4 multiplier chain was manufactured alongside the complete ×8 multiplier chain. The breakout has a size of 925×410 µm^2. Fig. 3.22a shows output power and conversion gain with respect to input power at 27.5 GHz. When driven with 4 dBm input power at this frequency, the ×4 multiplier chains conversion gain peaks at -10.2 dB. Fig. 3.22b presents the respective output power and spurious harmonics at this operating point. The output powers 3-dB bandwidth ranges from 93 GHz to 123 GHz. The 3rd, 6th and 8th harmonic are 34.2 dB, 37 dB and 17 dB below the 4th harmonic respectively. At 27.5 GHz input frequency, the ×4 multiplier chain delivers -6 dBm of saturated output power, at 30 GHz it is -7.7 dBm.

When the ×4 multiplier chain reaches its peak conversion gain, the first doubler draws 16 mA from a 1 V supply; the second doubler takes 4 mA from a 0.9 V supply.



(a) (b)

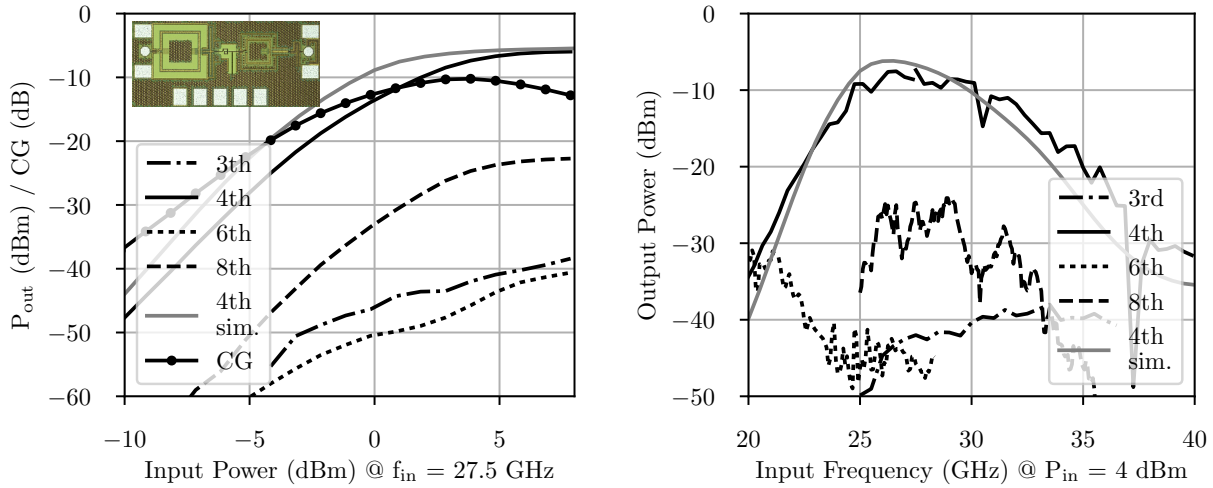
Figure 3.21.: Common mode output reflection coefficient of (a) the first, lumped-distributed transformer balun and (b) the second, lumped-distributed Marchand balun of the SG13G2 ×8 multiplier chain. At the second harmonic, either balun presents a short circuit to the tailing Class-B doubler.

3.6.3. 120 GHz Power Amplifier

Circuit Description

A power amplifier directly in front of the last frequency multiplier stage in a multiplier chain can serve multiple purposes. It relaxes the output power requirements of the preceding multiplier. Thus smaller devices can be used in the common-base doubler, raising its input impedance and equalizing the impedance transformation ratio of the input balun matching circuit. This in turn leads to coupled line impedances easier realizable in the IC's BEOL. With sufficiently narrowband tuning, the power amplifier also acts as an active filter, suppressing spurious harmonic tones from the previous multiplier stages.

In the presented ×8 multiplier chain in SG13G2 technology, a two stage power amplifier is employed after the second class B frequency doubler. Fig. 3.23a shows one amplifier stage plus the miniaturized Marchand balun used for converting the previous frequency doublers single-ended signal into a differential one. At the amplifiers core is a pseudo-differential cascode with (8×0.12×0.96) µm^2 devices. A fourth order matching network transforms the input impedance to differential 100 Ω. At the output, two capacitors in series decrease only the differential mode impedance. This reduces the necessary shunt transmission line length, which in turn reduces the common mode load impedance, the amplifiers common mode gain and therefore helps with common mode stability. A series capacitor completes the conjugate matching circuit at the output.



(a) (b)

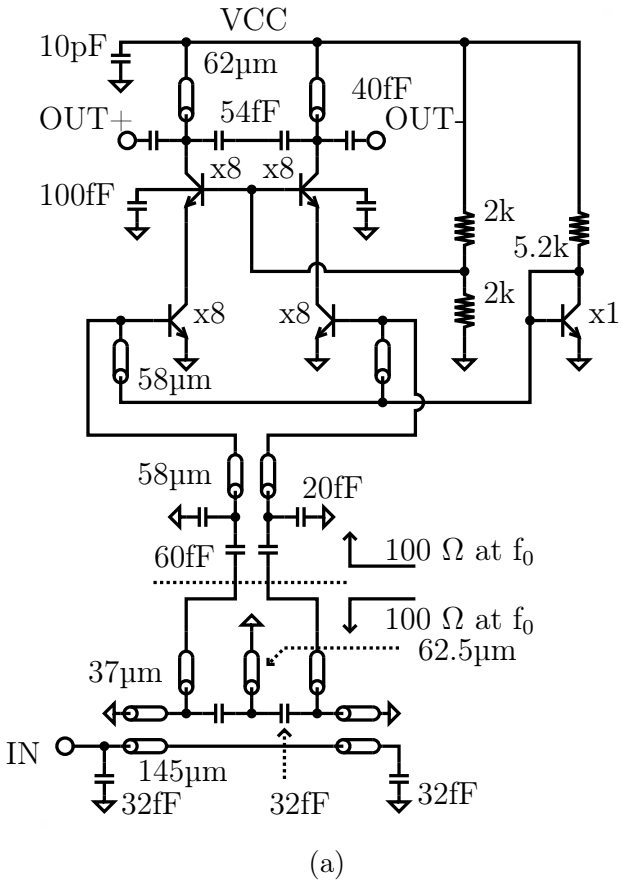
Figure 3.22.: ×4 multiplier chain breakout measurement results. (a) Output power versus input power with 27.5 GHz input frequency. The inset shows the breakout used for the presented measurements. (b) Output power in relation to input frequency at 27.5 GHz peak conversion gain. Except for the 8th harmonic, all spurious tones are at least 30 dB below the 4th harmonic.

Breakout Measurement Results

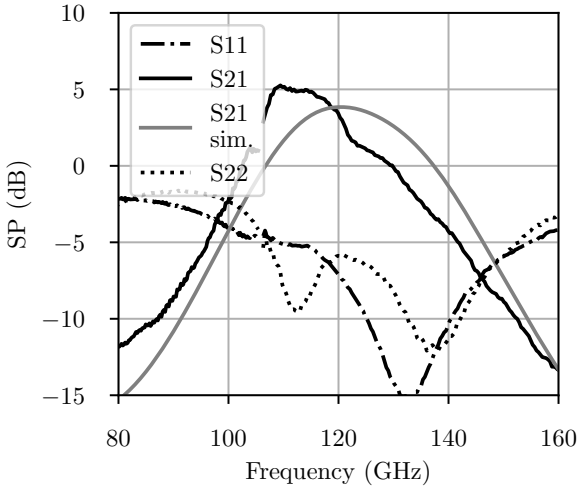
A circuit breakout of the 120 GHz power amplifier was manufactured alongside the ×8 multiplier chain. It encompasses a single stage with the previously mentioned miniaturized Marchand balun at both input and output.

The breakout was characterized in the small signal domain using an Agilent E8361A PNA, frequency extender modules from RPG for W-band measurements, connected to 1 mm coax cables and GGB GSG probes for on-wafer probing. In D-band, extender modules from OML, WR06 S-bend waveguides and corresponding GGB GSG probes were used. For large signal characterization, the output power of the RPG extender modules was calibrated with a VDI PM4 total power calorimeter and afterwards the modules were connected back-to-back to measure their down-conversion loss. The losses of the GGB probes and coax cables were recorded in the same way by probing a short piece of transmission line on a calibration substrate.

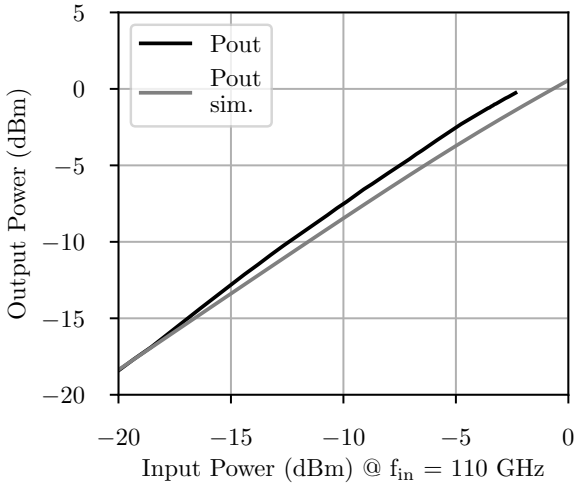
Fig. 3.23b shows the small signal measurement results of this single stage PA breakout. At 4.6 V supply voltage, it draws 17 mA current and has a peak small signal gain of 4.9 dB at 113 GHz. The 3-dB bandwidth is 16 GHz. Reverse isolation S_{12} is below -30 dB until 140 GHz and stays below -20 dB afterwards. As visible in Fig. 3.23c, it was not possible to compress the single stage amplifier with the power available from the mmWave extender modules used for the measurement. Simulation predicts a P_{sat} of 7 dBm at 110 GHz.



(a)



(b)



(c)

Figure 3.23.: (a) Pseudo differential power amplifier at 120 GHz with a preceding miniaturized Marchand balun. Input and output of the power amplifier are matched to differential 100 Ω. (b) Single stage 120 GHz power amplifier breakout measured scattering parameter. S12 (not shown) stays below -20 dB over the whole measurement range. (c) Measured output power versus input power at 110 GHz.

3.6.4. ×2 120 GHz to 240 GHz Gilbert Cell Doubler

Circuit Description

The main advantage of Gilbert cell frequency doublers over their class B counterparts as found in the literature [76] is their better ratio of conversion gain per power consumption. A multitude of variants have been reported, often in multiplier chains [72] [77] [78]. In this specific application, their basic operating principle has a rarely discussed drawback: spurious harmonic tones from previous frequency multiplier stages are not only doubled in frequency themselves, but also mixed with all other present tones. This is particularly critical in a wideband heterodyne communication setting, where after up- and down-conversion spurious out-of-phase copies of the data stream interfere with the wanted baseband signal. Therefore the input to any Gilbert doubler requires either strong filtering or the output spectrum of prior multiplier stages needs to be sufficiently pure.

Gilbert doublers exhibit their best conversion gain, if the transconductance pair and the switching quad are driven with an optimized relative phase producing quadrature currents at the collectors of the switching quad [79], which in contrast to Eq. 3.2 also eliminates the DC part generated by multiplying two in-phase sinusoidal signals, following

$$\sin(2\pi ft) \cdot \cos(2\pi ft) = \frac{1}{2} \cdot \sin(2 \cdot 2\pi ft) \tag{3.3}$$

The argument for in-phase instead of quadrature coupling between the TP and the SQ for high frequency Gilbert doublers in [72] was that passive hybrids are lossy, consume a large chip area and increase layout complexity. Indeed, even state-of-the-art implementations which omit a passive hybrid, still use large $\lambda/4$ series transmission lines in the input tuning circuit [73] or $\lambda/6$ series transmission lines in between the TP and the SQ if bootstrapping is employed [71].

The third and last frequency doubler stage of the presented ×8 multiplier chain uses a novel, compact implementation of a quadrature coupled Gilbert cell topology. First, similar to the standard upconversion mixer design methodology [54] the current densities of the TP and the SQ are set to J_{pfT} and $J_{pfT}/1.5$ respectively, which is equivalent to using SQ transistors of 2/3 the size of the TP ones.

Using this device size ratio, simulation as previously shown in Ch. 3.3 predicts an optimum conversion gain, if the input power is split equally between the TP and the SQ and if they are driven at an optimum phase offset. To fulfil the power split constraint, matching networks for the TP and the SQ have to be chosen, which transform both input impedances to the same purely real impedance. When choosing a transconductance pair devices of $3\times0.12\times0.96$ µm^2 size, which fixes the switching quad device size to $2\times0.12\times0.96$ µm^2, the additional condition of optimum phase offset is met simultaneously with simple single shunt stubs and a small capacitor between the TP and the SQ. These shunt stub impedance tuning networks can be laid out extremely compact in a differential circuit by routing microstrip lines in symmetric loops, introducing AC grounds at their point of contact.

At 120 GHz, the input impedance of the parallel connected TP and SQ is 85 Ω. Thus a short series coupled line section and a series capacitor match the input to 100 Ω differential impedance. At the output, an L-matching network serves the same purpose.

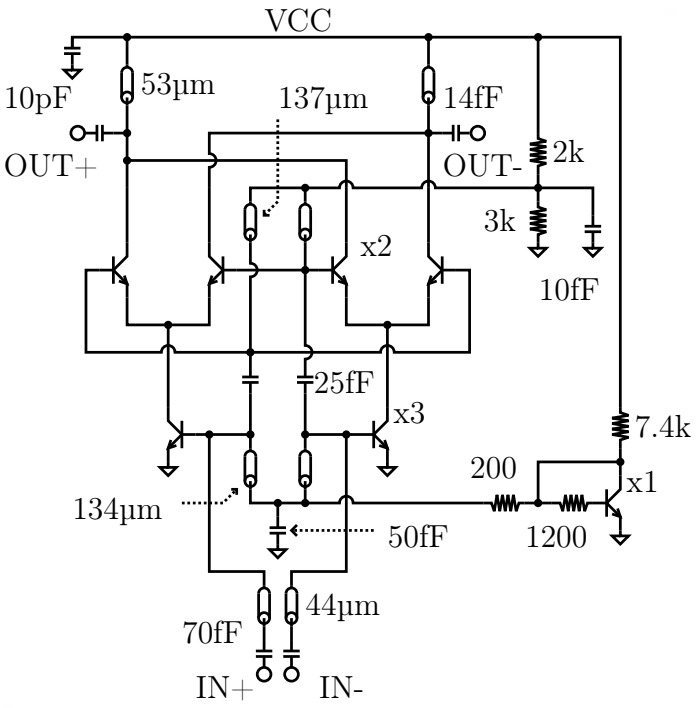


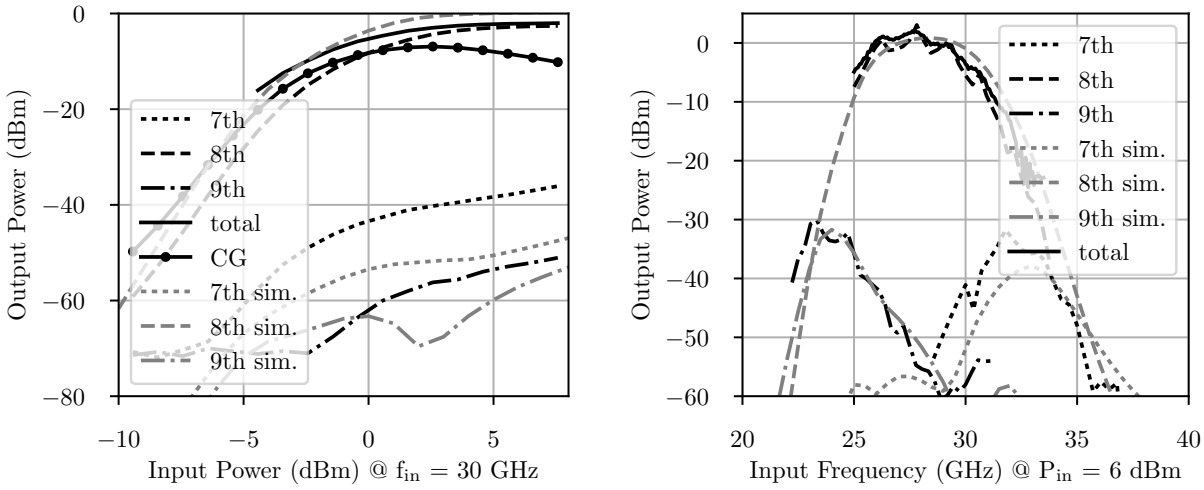
Figure 3.24.: Last frequency doubler stage from 120 GHz to 240 GHz. For optimum conversion gain, a Gilbert cell based frequency doubler requires a 90° phase shift between the signals feeding the transconductance pair and the switching quad. Instead of using an area consuming 90° hybrid implementation, here transistor parasitics are scaled by choosing the appropriate device size to provide this phase shift in conjunction with single stub matching circuits.

3.6.5. ×8 Multiplier Chain Breakout Measured Results

The ×8 multiplier chain breakout was measured using the setup described in Fig. 3.10. The output power at the 7th, 8th and 9th harmonic were measured single-ended through an on-chip balun. Its loss is estimated to be 1 dB from simulation, but it was not de-embedded from any measurement result. The balun has a high common mode rejection over its entire bandwidth, therefore measuring the power of any common-mode harmonics is not possible. Also, the total output power of the multiplier chain was recorded with a PM4 total power calorimeter to verify the measured results.

When driven into saturation with 4-5 dBm drive power, the ×8 multiplier chain has a peak saturated output power of 2.3 dBm at 221 GHz, with a 36 GHz 3-dB bandwidth. The peak conversion gain of -0.33 dB is reached at 1.57 dBm of input power; the 3-dB bandwidth is then reduced to 29 GHz, as presented in Fig. 3.25b. At this drive power, the differential mode spurious 7th and 9th harmonic are 54 dB below the desired 8th harmonic.

Fig. 3.25a shows the output power of the multiplier chain with a 30 GHz drive signal. At 2.6 dBm input power, the ×8 multiplier chain has a peak conversion gain of -6.9 dB. At this point, the differential mode spurious 7th and 9th harmonics are 36 dB and 51.9 dB below the 8th, respectively. P_{sat} is -2.6 dBm at 6.6 dBm input power.



(a) (b)

Figure 3.25.: ×8 multiplier chain breakout measured results. (a) Output power versus input power with a 30 GHz drive signal. (b) Output power versus input frequency when driven with a 2 dBm input signal for optimum conversion gain at 30 GHz. Peak output power then is 2.0 dBm at 221 GHz.

When driven into compression, the multiplier chain consumes 210 mW. The breakout of the ×8 multiplier chain in SG13G2 technology is (1545×480)µm² large. A micrograph is shown in Fig. 3.26.

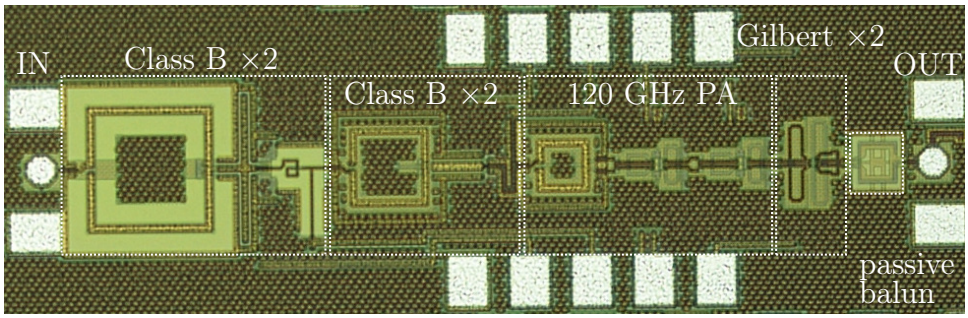


Figure 3.26.: ×8 multiplier chain breakout micrograph.

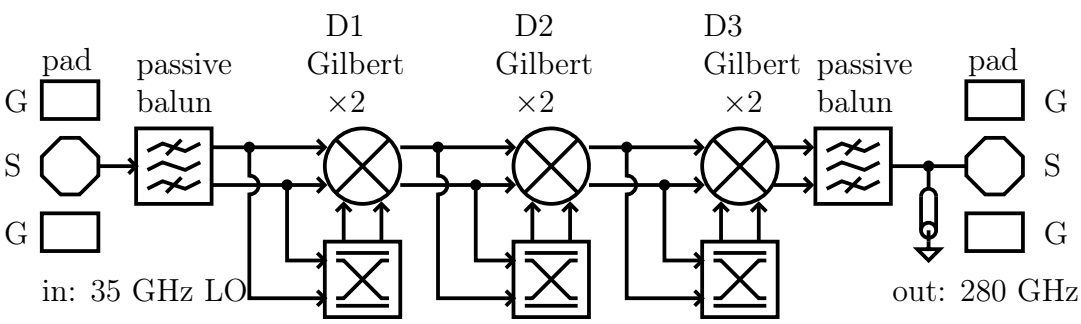


Figure 3.27.: Block-level overview of the wideband ×8 multiplier chain in B11HFC.

3.7. ×8 Multiplier Chain in B11HFC Technology

3.7.1. Circuit Description

The ×8 multiplier chain in B11HFC technology is specifically designed to generate the 287.28 GHz carrier frequency of the channel with the largest, 69.12 GHz wide bandwidth of the recent IEEE THz physical layer standard [1]. But due to its wideband design, the 3-dB bandwidth of this ×8 multiplier chain also nearly covers the entire 200 GHz to 300 GHz frequency band.

Fig. 3.27 shows a block diagram of this ×8 multiplier chain. All frequency doubler stages use a Gilbert topology with their superior conversion gain compared to Class-B based doublers. The transconductance pair, switching quad and also the current mirror transistors all feature equal sizes. The DC base voltage for the transconductance pair is generated in said current mirror. A resistive voltage divider supplies the base voltage of the switching quad.

The multiplier chain is fed from a miniaturized marchand balun as discussed in Ch. 3.6.1. It transforms a 100 Ω differential impedance at the input of the first multiplier into 50 Ω single-ended impedance at the ground-signal-ground pad for probing. Two coupled line sections with 545 µm length each are arranged into a square. MIM shunt capacitors with 110 fF capacitance are placed at the coupled line end points.

The first Gilbert doubler, as presented in Fig. 3.28, has (0.13×10) µm^2 transistors in both its transconductance pair and switching quad. A degeneration inductor flattens the input impedance seen at the base terminal of the transconductance pair. Together with the L-type matching networks used to tune the transconductance pair and switching quad input impedance to equal 200 Ω real impedances, it also introduces the necessary phase shift for maximum conversion gain at 35 GHz. An output transformer with center tap for DC current supply and 1:1 winding ratio relies on a differential shunt capacitance to transform the complex impedance of the switching quad into a 100 Ω differential output impedance.

The second and third Gilbert frequency doublers use smaller (0.13×6) µm^2 HBTs. Similar to the bootstrapping frequency doublers presented in [71], a series transmission line in between the transconductance pair and the switching quad is employed. But, contrarily to the

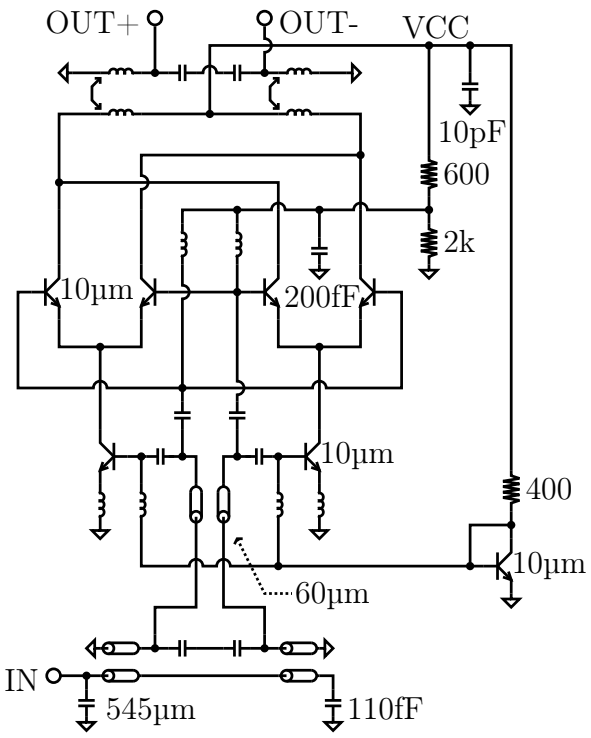


Figure 3.28.: Circuit schematic of the first frequency doubler and miniaturized input Marchand balun in the B11HFC ×8 multiplier chain.

bootstrapping method, it is not 90° at the doublers design frequency. Instead, it is considerably shorter, as the remaining phase shift for optimum conversion gain is generated in the L-type matching networks used for tuning the transconductance pair and the switching quad input impedance to equal real impedances. As the resulting input impedance is smaller than 100 Ω in both doublers, a series transmission line and a shunt capacitor transform it to that value.

In the second frequency doubler, shown in Fig. 3.29a, a T-type matching network generates the 100 Ω impedance at the output. The switching quad of the last frequency doubler has an output impedance considerably smaller. A 36 µm shunt transmission line compensates the capacitive part of said impedance. A 80 µm series transmission line and a 40 fF series capacitor then transform the resulting impedance to the 100 Ω required by the tailing wideband Marchand output balun. A GSG pad, whose shunt capacitance is compensated with a short-circuit shunt stub, enables on-wafer probing.

When driven into compression, the first doubler takes 42 mA from a 2 V supply, the second 30 mA from 2.6 V supply and the third 25 mA from a 3 V supply. In total, the multiplier chain consumes 237 mW.

The breakout of the ×8 multiplier chain in B11HFC technology is (1430×600) µm^2 large. A micrograph is shown in Fig. 3.30.

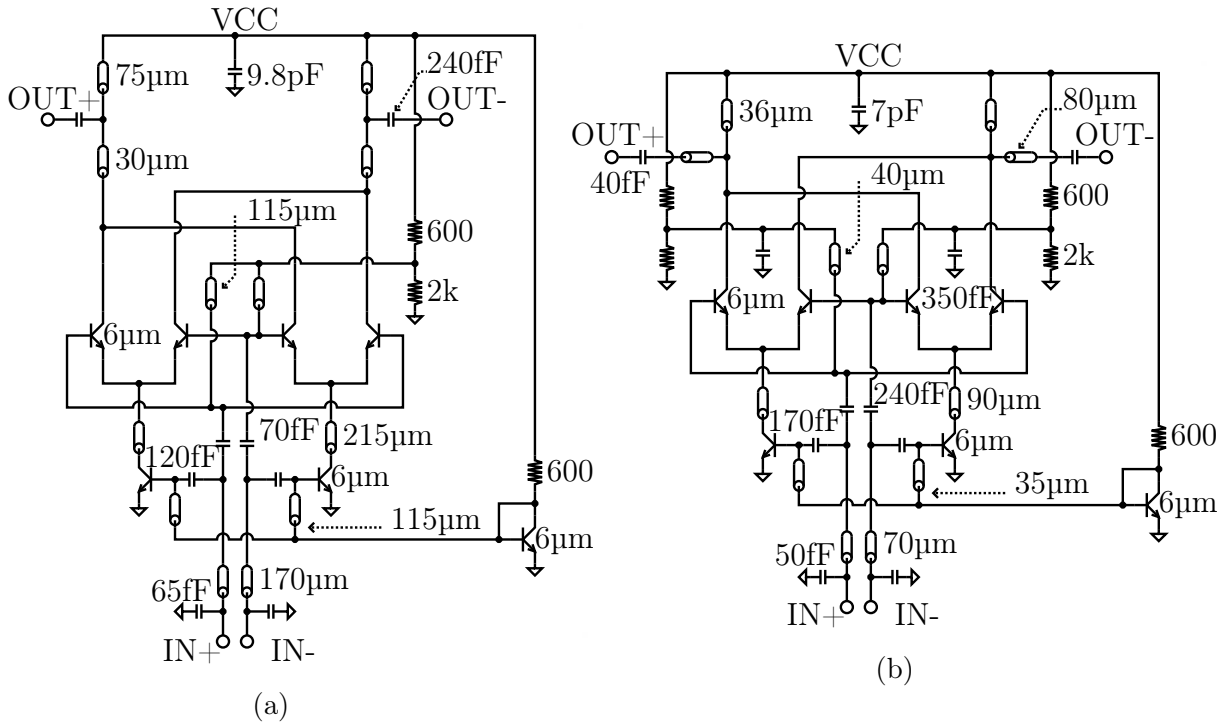


Figure 3.29.: Circuit schematic of (a) the second and (b) the third Gilbert doubler of the ×8 multiplier chain in B11HFC technology.

3.7.2. Measured Results

Fig. 3.31a shows the output power of the ×8 multiplier chain versus input power with a 30 GHz input signal. A peak conversion gain of -8 dB is reached, when an input power of -3.4 dBm is applied. The output power then is -11.4 dBm. Again, like in the ×8 multiplier chain, the output balun prevents measuring common mode harmonics. The differential mode spurious 7th and 9th harmonics produced in the multiplier chain for this input power and frequency are at -31.4 dBm and -31.7 dBm respectively.

Fig. 3.31b shows the corresponding frequency behaviour for this input power point. A red

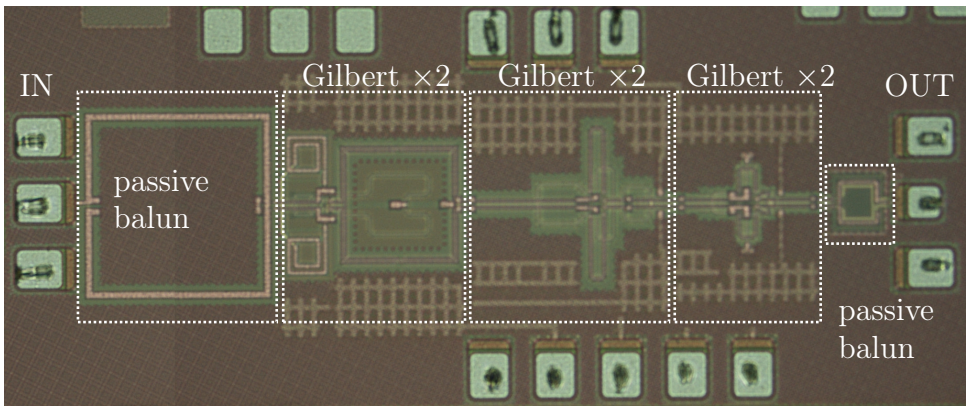
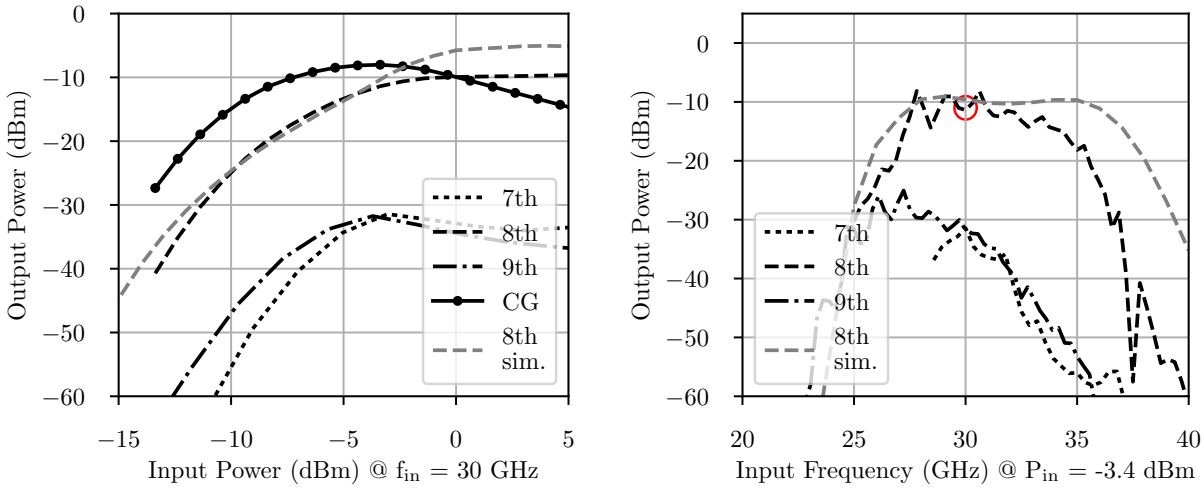


Figure 3.30.: ×8 multiplier chain breakout micrograph. [59] © 2020 IEEE.



(a) (b)

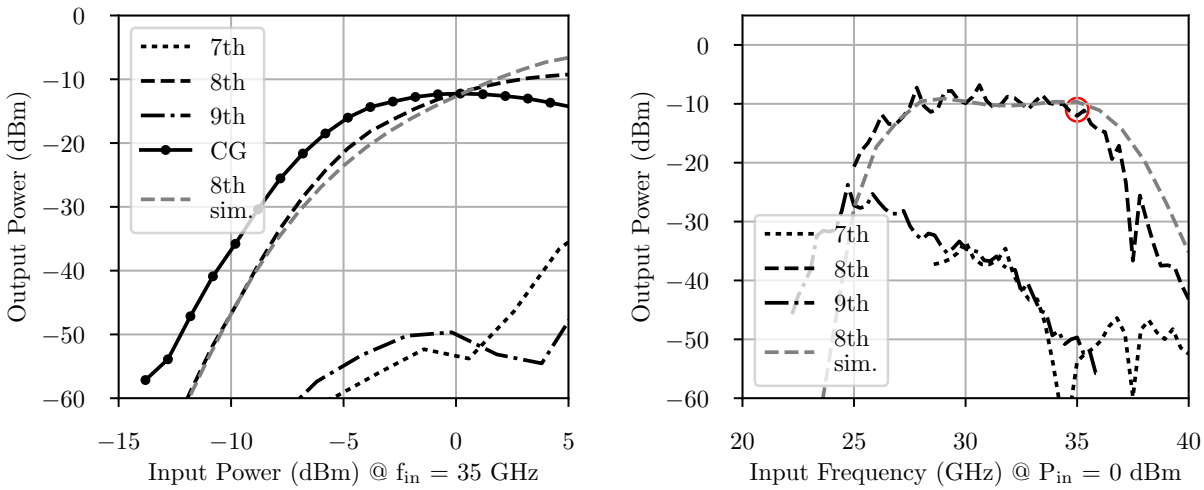
Figure 3.31.: ×8 multiplier chain breakout measured results. (a) Output power versus input power with a 30 GHz input signal. (b) Output power versus input frequency when driven with a -4 dBm input signal for optimum conversion gain at 30 GHz. [59] © 2020 IEEE.

circle marks the frequency point, at which the respective peak CG is achieved. The output power 3-dB bandwidth spans from 220 GHz to 257 GHz for a total of 37 GHz. The graph indicates a 10 dB better harmonic rejection for a 35 GHz drive signal.

Therefore, to compare, Fig. 3.32a presents the input to output power behaviour of the ×8 multiplier chain, when driven with a 35 GHz input signal. A peak conversion gain of -12.2 dB is reached at 0 dBm input power. The power of the differential mode 7th spurious harmonic is 41.6 dB smaller than of the desired 8th harmonic; the power of the 9th harmonic is 37.6 dB smaller. Fig. 3.32b shows the corresponding frequency behaviour. Again, a red circle marks the frequency point, to which peak conversion gain the graph refers. The increased input power boosts the 3-dB bandwidth to a total of 66 GHz, spanning from 218 GHz to 284 GHz.

The 3-dB bandwidth extents to 81 GHz, when the ×8 multiplier chain is driven into saturation. With an input power of 6 dBm, the peak output power is -7.7 dBm at 244.5 GHz. Fig. 3.33 shows, that the saturated bandwidth spans from 210 GHz to 291 GHz. Especially the harmonic rejection of the 7th spurious tone degrades, when driving the multiplier chain into compression.

With a 30 GHz drive signal, the saturated output power is -9.6 dBm, while the differential mode 7th and 9th spurious tones are at -33.5 dBm and -37.2 dBm respectively. When a 35 GHz input signal is applied, P_{sat} is -9 dBm. The 7th and 9th harmonic suppression then is -25.8 dB and -27.6 respectively.



(a) (b)

Figure 3.32.: ×8 multiplier chain breakout measured results. (a) Output power versus input power with a 35 GHz input signal. (b) Output power versus input frequency when driven with a 0 dBm input signal for optimum conversion gain at 35 GHz. [59] © 2020 IEEE.

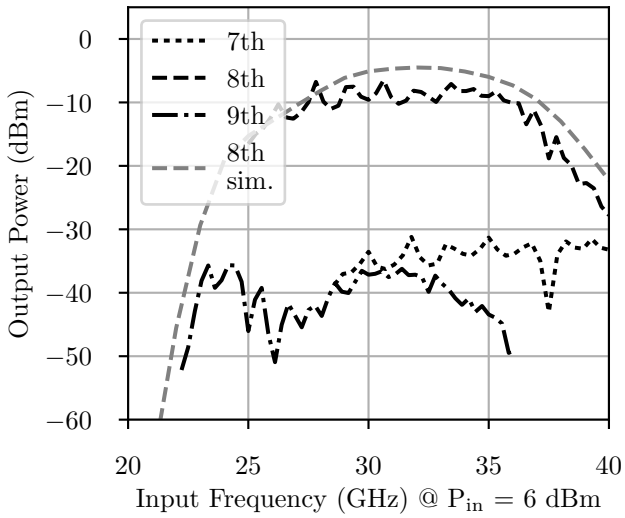


Figure 3.33.: ×8 multiplier chain breakout measurement results. Output power versus input frequency when driven into compression with a 6 dBm input signal. [59] © 2020 IEEE

3.8. Chapter Conclusion

This chapter discussed the design of two ×8 multiplier chains in different SiGe technologies and design goals. Tab. 3.2 summarizes the current state-of-the-art of SiGe frequency multiplier and multiplier chains in the 200 GHz to 300 GHz band in chronological order. The 1st generation ×16 and both new ×8 multiplier chains are highlighted by a bold typeface.

The ×8 multiplier chain in SG13G2 technology has an output power level, which otherwise is only approached by state-of-the-art ×2 multipliers, but its corresponding DC power consumption is two times smaller.

With 81 GHz, the ×8 multiplier chain in B11HFC technology has the highest 3-dB bandwidth ever published in the 200 GHz to 300 GHz range. It reaches 60 % of the assigned carrier frequencies of the IEEE 802.15.3d-2017 standard for high data rate wireless multi-media networks, which start at 253.8 GHz.

The ×8 multiplier chains presented in this chapter show excellent differential mode spurious harmonic suppression at the peak CG point of their respective target frequencies. General design guidelines for multiplier chains with distinctly good harmonic rejection were derived from a sensitivity analysis on class-B and Gilbert cell based doublers. According to the resulting critical boundaries on amplitude and phase imbalance, three miniaturized passive baluns were designed. A novel harmonic tuning scheme was introduced, which is integrated in the same baluns and boost the conversion gain of the presented class-B common-base doublers. Two methods of achieving an optimum phase offset between the transconductance pair and the switching quad of a Gilbert doubler have been explored for conversion gain optimization and desensitisation against phase imbalance of the input signal.

Ref.	Technology Node f_T/f_{max} (GHz)	Mult.	Topology	Freq. (GHz)	P_{out} (dBm)	3-dB BW (GHz)	P_{DC} (W)	Area (mm^2)
[80]	SiGe 0.13 µm 250/380	×2	PA + Class B ×2	220	-1	35	0.43	0.611
[73]	SiGe 0.13 µm 240/380	×2	VCO + Gilbert ×2 with λ/4 line	220	-6	48	0.58	0.75
[72]	SiGe 0.13 µm 300/450	×16	Gilbert ×2	245	-8.65	41	0.3	0.7
[81]	SiGe 0.12 µm 200/250	×4	Class B ×2 + PA + Class B ×2	240	-0.5	14	0.52	1.92
[70]	SiGe 90 nm 310/350	×2	PA + Class B ×2	245	1.8	28	0.41	0.54
[69]	SiGe 0.13 µm 300/500	×6	Gilbert ×2 + Cascode ×3	240	-4	15	0.9	0.75
[78]	SiGe 0.13 µm 300/500	×8	Gilbert ×4 + PA + Gilbert ×2	236	-8	32	0.15	1.2
[82]	SiGe 0.13 µm 250/300	×2	PA + Class B ×2	270	0	50	0.43	0.57
3.7	SiGe 0.13 µm 250/370	×8	Gilbert ×2 with 90° phase shift	244.5	-7.7	81	0.24	0.86
3.6	SiGe 0.13 µm 300/450	×8	Class B ×2 + Class B ×2 + PA + 90° Gilbert	221.5	2	36	0.21	0.74

Table 3.2.: Comparison of 200 GHz - 300 GHz frequency multiplier (chains)

4. Front-End Components and Packaging

4.1. Introduction to the Chapter

This chapter presents a block level overview, component descriptions and measurement results and the packaging approach of a novel quadrature transmitter and receiver chip-set. TX and RX are fabricated in IHP's 0.13 µm SiGe BiCMOS technology SG13G2 as described in Ch. 1.5.1.

A block level overview of the transmitter and the receiver is presented in Ch. 4.2. All used circuit building blocks are described in detail. The 2nd generation ×8 multiplier chain with high spurious harmonic suppression presented in Ch. 3.6 generates a 215 GHz to 240 GHz carrier from an external reference source. Novel wideband up- and down-conversion mixers in Ch. 4.3.1 and Ch. 4.3.2 connect to baseband filters distributed among IC and PCB for bandwidth enhancements in Ch. 4.5.

To increase channel isolation in line with the design goals discussed in Ch. 2.4, a two-track approach is used. Besides the commonly used practice to orthogonalize the individual channels by phase, making them IQ channels in the mixing process by employing a 90°hybrid at the output of the carrier generation circuitry, an additional orthogonality by polarization is introduced. Thus, I and Q-channel are fed separately to orthogonal polarizations of a lens-integrated dual polarized antenna. The design details and antenna patterns of the dual-polarized antenna are described in Ch. 4.6. The tunability of the multiplier chain then allows for experiments with the individual contributions to the overall channel isolation, which is further discussed in Chapter 5.

This additional orthogonality by polarization also enables a direct conversion, single-side-band mode of operation. In contrast to a double-side-band mode, the baseband bandwidth then is not symmetrically mirrored around the carrier frequency, but the entire TX RF bandwidth is used for a single modulated copy of the baseband. This concept is schematically depicted in Fig. 5.11.

4.2. TX and RX Block Level Overview

Fig. 4.1 and Fig. 4.2 present block level diagrams of the transmitter and receiver ICs respectively. Both use the ×8 multiplier chain from Ch. 3.6 for converting an external 26.875 GHz to 30 GHz reference local oscillator (LO) signal into a 215 GHz to 240 GHz carrier frequency.

After the last doubler of the multiplier chain follows a four stage power amplifier. Its output power is split in a 90° coupled line hybrid, which splits the carrier power to drive two separate up- or down-conversion mixers. The aforementioned PA ensures appropriate power levels to drive the respective mixers despite the hybrid and transmission line losses.

In the TX, after direct up-conversion from baseband, both in-phase and quadrature channel are individually amplified by a power amplifier and separately transmitted via a single polarisation of the dual polarised on-chip antenna.

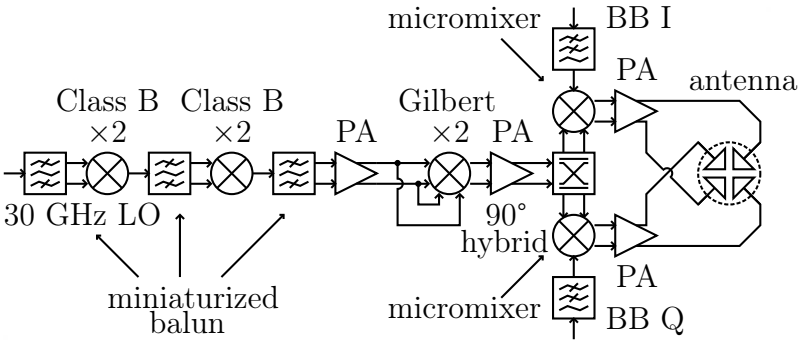


Figure 4.1.: Transmitter block diagram. From left to right: ×8 multiplier chain, 90° hybrid, one micromixer and RF PA per channel, dual polarised antenna.

In the receiver, both in-phase and quadrature channel are received via a respective single polarisation of the dual polarised on-chip antenna. A mixer first architecture provides large RF bandwidth. After direct down-conversion to baseband, both I and Q channel are individually amplified by differential variable gain transimpedance amplifiers.

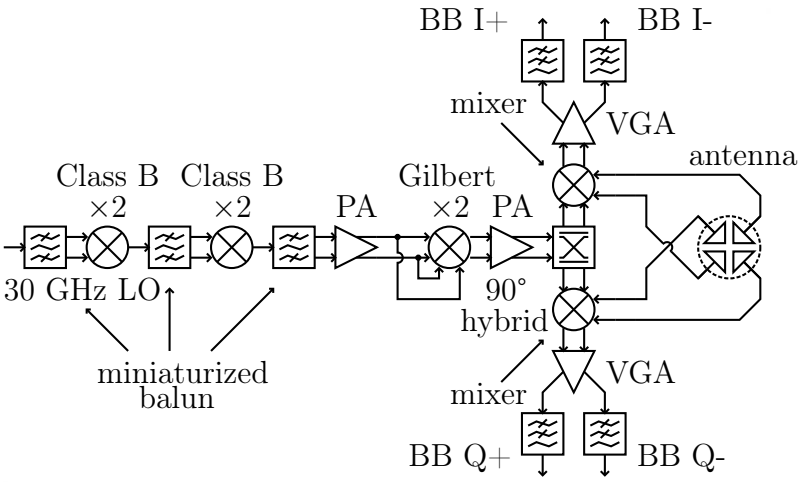


Figure 4.2.: Receiver block diagram. From left to right: ×8 multiplier chain, 90° hybrid, one downconversion mixer and VGA per channel, dual polarised antenna.

Circuit micrographs and the physical dimensions of both TX and RX ICs can be found in Fig. 4.3.

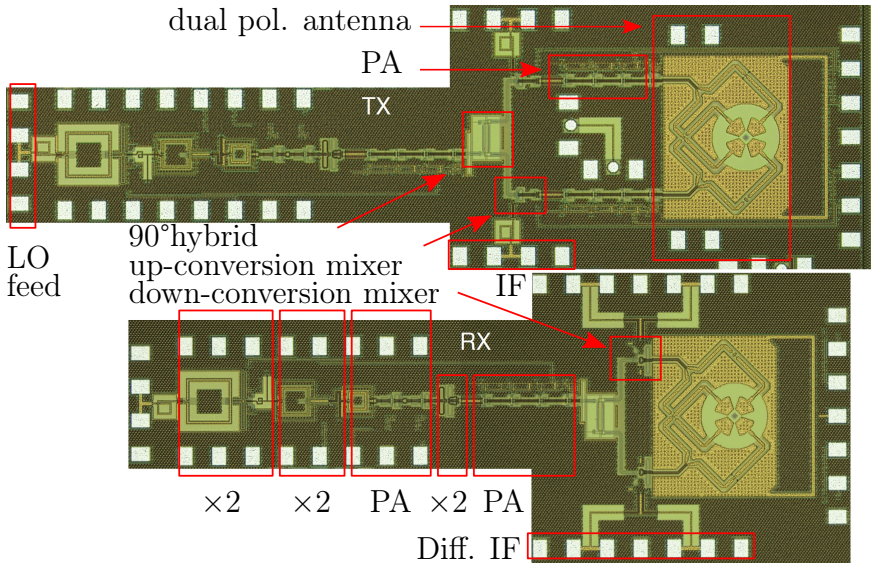


Figure 4.3.: Transmitter and receiver circuit micrographs. The transmitter is displayed at the top; its dimensions are 3.745 mm × 1.13 mm. The receiver is 3.205 mm × 1.27 mm large.

4.3. Frequency Translation

4.3.1. Up-Conversion Mixer

Circuit Description

One not instantly obvious shortcoming of using differential up-conversion mixers driven by arbitrary waveform generators is, that the AWGs differential drive is not perfect, therefore increasing EVM. Thus a single ended option would be preferable. A topology with wide input matching bandwidth, single ended input but differential output and high linearity was introduced as the MICROmixer in [83] as a down-conversion mixer with a slight noise penalty. In contrast, as noise is not of the essence in a transmitter, here the micromixers qualities are used for up-conversion.

Just like in the classic Gilbert cell, a switching quad driven by an LO signal is responsible for frequency translation. But instead of a differential pair at the input, a bisymmetric class AB input stage provides a single ended input to the micromixer. With its input resistance equal to $1/g_m$, a common base transistor defines the micromixers input impedance, while its DC current is mirrored through a diode connected BJT to a parallel common emitter transistor. In relation to the input voltage, the common base transistor delivers its current in-phase to the first mixer pair, while the common emitter transistor delivers its current out-of-phase to the second mixer pair.

The presented micromixer has a topology described as "T-padded form" in [83]. For transistor sizing and biasing two considerations are in the foreground: First, maximum switching speed in the mixing quad is necessary to minimize conversion loss. This is accomplished

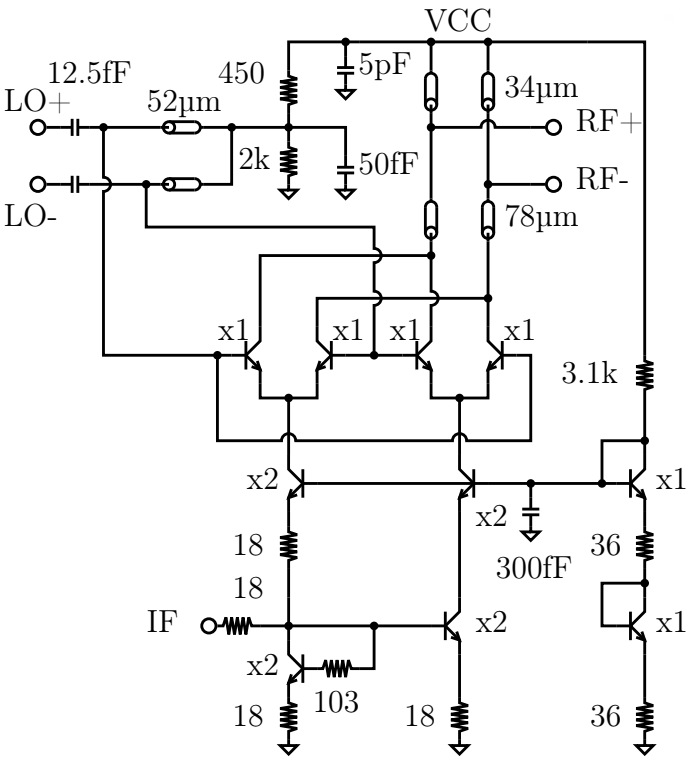


Figure 4.4.: Upconversion mixer. A micromixer provides large baseband input matching bandwidth to 50 Ω through its common base transistor, resistive degeneration and a small series resistor.

by biasing the switching quad transistors at $J_{PfT}/1.5$, as described in [54]. Second, the baseband input impedance needs to be matched wideband to 50 Ω, to not limit the overall system bandwidth. With the bias current set by the device sizes of the switching quad, the transistor sizes in the input stage can be chosen in conjunction with appropriate emitter degeneration and series resistance.

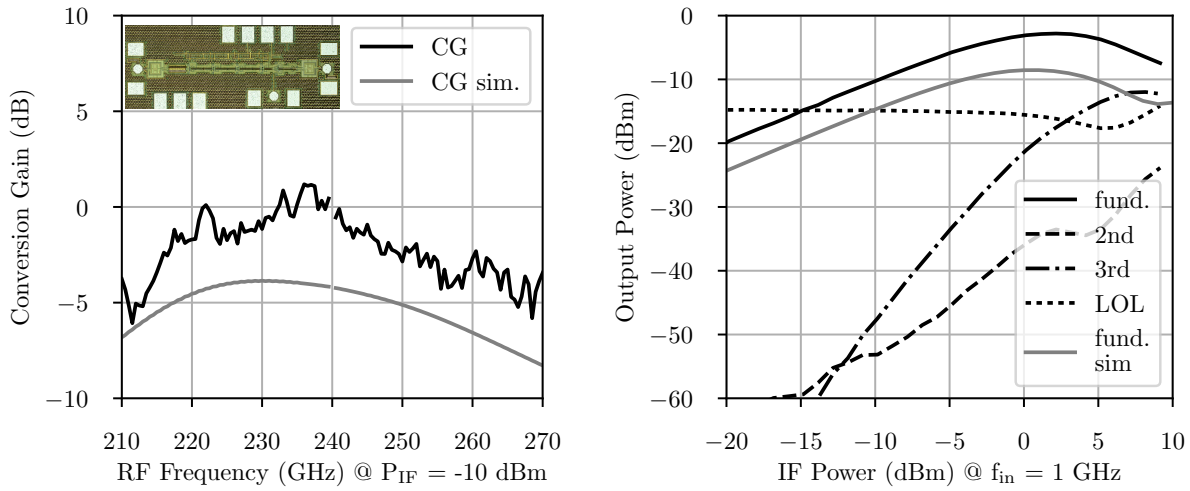
The cascode transistor serves three functions: It eliminates the common emitter transistors Miller capacitance, while presenting a load impedance to the switching quad more similar to the common base transistor in the other mixer branch. Furthermore, it equalizes the collector-emitter voltages of the common emitter and the diode connected transistor, which helps with current balance in both mixer branches. The 103 Ω resistor also aids this purpose, but additionally raises the input impedance of the mirror section at high frequencies.

A series capacitor and shunt transmission line stubs are responsible for LO matching to 100 Ω differential impedance. A resistive voltage divider sets the bias voltage for the switching quad through a center tap at the transmission line stubs. On the RF side, series transmission lines and shunt stubs match to 100 Ω.

Breakout Measured Results

The up-conversion micromixer was characterized separately on wafer. The breakout consists of the micromixer itself, driven by an on-chip PA as described in 4.4. The differential output is measured single-ended through an on-chip balun. The breakout has a size of 1080×415 µm^2. The inset in Fig. 4.5a shows a micrograph of the breakout.

At -10 dBm IF power, the up-conversion micromixer has 0 dB conversion gain with a 3 dB bandwidth of 38.5 GHz, see Fig. 4.5a. The input referred 1 dB compression point IP_{1dB} is at -3.8 dBm. At this point, the measured second and third harmonic are 38 dB and 25 dB below the fundamental respectively. The micromixer delivers a saturated output power P_{sat} of -2.9 dBm. The power of the LO leaking into RF is never lower than -17.6 dBm.



(a) (b)

Figure 4.5.: Up-conversion micromixer breakout measurement results at a 240 GHz carrier frequency. (a) Conversion gain versus output frequency. The inset shows a micrograph of the breakout. (b) Output power versus input power at an input frequency of 1 GHz.

4.3.2. Down-Conversion Mixer

Circuit Description

A design insight was presented in [44], stating that due to the high baseline noise figure of SiGe low noise amplifiers above 200 GHz, a rather narrowband receiver front-end amplifier can be omitted for a wideband mixer-first topology without a severe noise penalty. A high gain, low noise baseband amplifier directly following the mixer then is mandatory to suppress the noise contribution of subsequent components in the signal path.

Therefore, each respective channel in this receiver uses a switching quad as shown in Fig. 4.6 for frequency translation, followed by a low noise Cherry-Hooper transimpedance amplifier

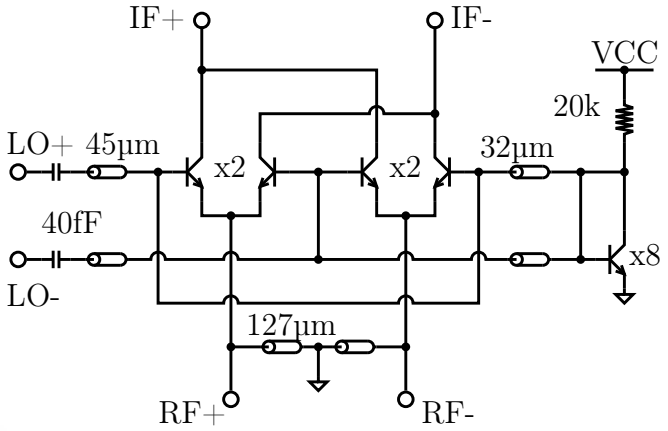


Figure 4.6.: Down-conversion mixer. Omitting the input transconductance pair from the classic Gilbert cell mixer significantly increases input matching bandwidth, but comes with a noise penalty. A high gain baseband amplifier directly after the mixer is therefore mandatory.

for baseband gain, detailed in Fig. 4.7. The RF input is emitter coupled to the HBTs, whose sizes are scaled to provide 100 Ω input impedance under full LO drive. A pair of 127 µm shunt transmission lines tunes out their input capacitance. The LO is fed to the bases of the transistors through an L-type matching network consisting of short shunt and series transmission lines. Two 40 fF series capacitors are responsible for DC decoupling.

The currents generated from the switching quad are fed into the baseband Cherry-Hooper transimpedance amplifier. The first differential pair is biased for low noise operation through a current mirror, but also provides a high fixed gain with its 1.4 kΩ load resistors. Part of the output voltage is coupled back to the input through emitter followers, significantly increasing the bandwidth. The extent to which the bandwidth can be widened, however, is limited by a trade-off for group delay variation, which increases inversely to the gain-peaking effect of the feedback circuit. To prevent distortion of the received symbols, amplitude and phase variation with frequency are to be avoided.

Another differential pair with small size 2 transistors and 50 Ω wideband impedance matching load resistors follows. In its initial state, this differential pair provides further gain. But if a control current, denoted as Ictrl in Fig. 4.7, of up to 500 µA is applied, the g_m of the devices is reduced. Therefore the last stage provides gain variability. The current mirror configuration for this mechanism was first introduced in [84] as "linear-in-dB cell". The name refers to the relationship between the slope of the variable gain, which drops linearly when observed on a logarithmic axis, and the control current. In this particular variation, a 4:1 bipolar current mirror with β-helper is supplied by a reference current from a PMOS current source. The control current introduces an additional voltage drop over the current mirrors resistors, lowering the transistors respective base-emitter voltage and therefore lowers the tail current of the differential pair.

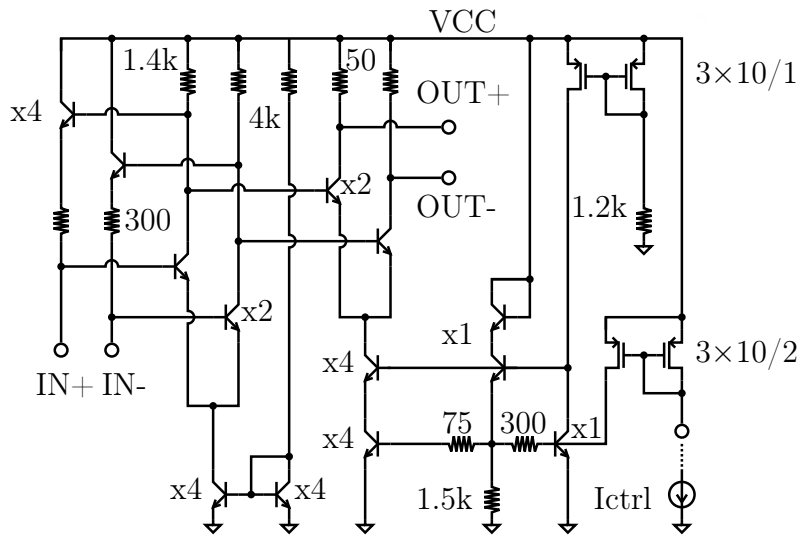
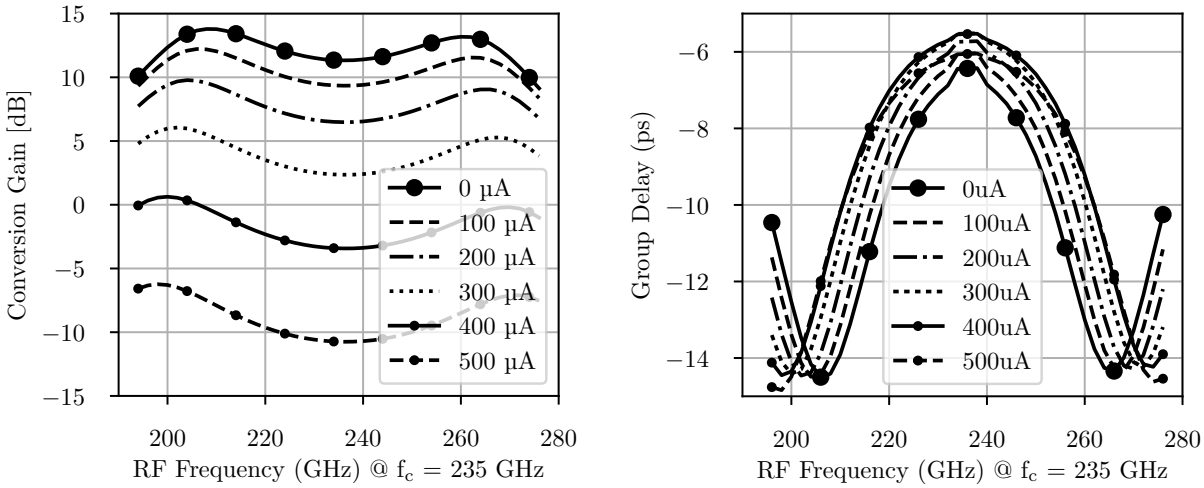


Figure 4.7.: Variable gain transimpedance amplifier. A Cherry-Hooper amplifier with emitter follower feedback converts the output baseband current from the down-conversion switching quad mixer to a voltage. A current controlled linear-in-dB gain cell as introduced in [84] modifies the transconductance of the output common emitter amplifier for gain variability. PMOS dimensions are in µm.

Simulation Results

The simulated conversion gain of the down-conversion mixer including the baseband transimpedance VGA is shown in Fig. 4.8a. With a maximum CG of 11.3 dB at center frequency, a slight gain-peaking behaviour due to feedback in the VGA extents the 3-dB bandwidth to 78 GHz. The peak CG is reached at 208 GHz and is 2.4 dB higher than the CG at the center frequency. The CG can be lowered by applying a control current of maximally 500 µA to the VGA to -10.7 dB at center frequency. The conversion gain is continuously variable within these boundaries and the bandwidth does not reduce in the lowered gain settings. The simulated noise figure of this mixer/VGA combination is depicted in Fig. 5.5 in comparison with the measured NF of the overall receiver. The simulated NF is lower than 13 dB over the whole mixer bandwidth.

Fig. 4.8b shows the simulated group delay variation of the down-conversion mixer and VGA in relation to RF frequency and chosen control current. The maximum group delay variation with frequency in full-gain setting is 8 ps. At minimum conversion gain with 500 µA control current, the frequency distance between minimum and maximum group delay increases by 5 GHz, but the absolute variation grows by only 1 ps.



(a) (b)

Figure 4.8.: Down-conversion mixer simulation results at a 235 GHz carrier frequency. (a) Conversion gain and (b) group delay in relation to input frequency. Increasing the VGA control current from 0 µA up to 500 µA lowers the conversion gain.

4.4. RF Power Amplifier

4.4.1. Circuit Description

A power amplifier is used both after the ×8 multiplier chain for generating drive power for the mixers and as an RF front-end amplifier. First presented in [72], it utilizes four stages of a pseudo-differential cascode topology. By tuning all stages to the same center frequency, the gain compresses evenly around the peak frequency with increasing input power. This also minimizes the group delay dispersion with frequency. As a counterexample, if staggered tuning of the individual power amplifier stages had been used to extent the small signal bandwidth, the last stage would compress first under large signal drive. This would contort the transfer function of the power amplifier such that the gain and phase balance around the center frequency of the PA would not have been preserved when entering compression. A single stage circuit schematic is shown in Fig. 4.9.

4.4.2. Measurement Setup

A breakout of the RF power amplifier was manufactured. It includes the four stage power amplifier, on-chip Marchand baluns and tuned pads at input and output. The front-end PA was characterized on-wafer using a measurement setup consisting of GSG waveguide probes for the 220-325 GHz band by GGB, OML mmWave VNA extender modules, and an Agilent E8361A network analyzer. Fig. 4.10 shows a schematical representation of the setup.

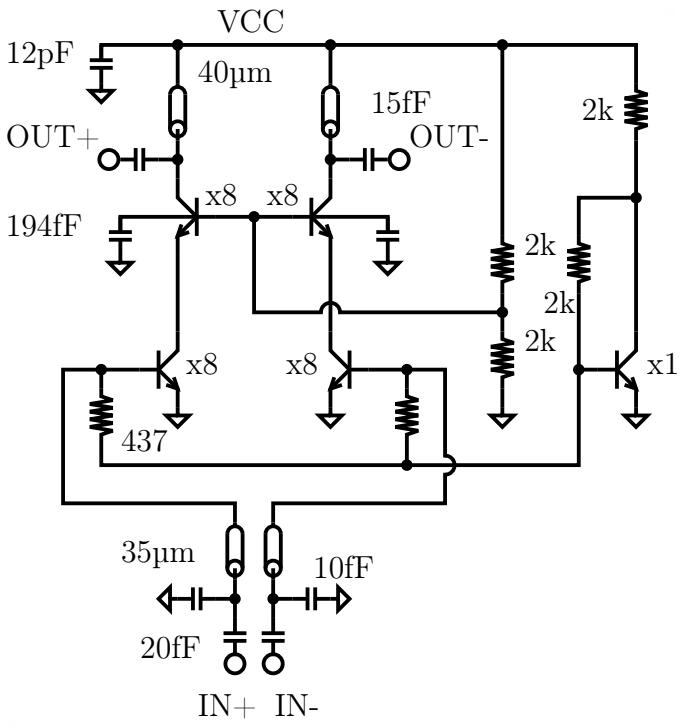


Figure 4.9.: Amplifier single stage circuit schematic. All stages are tuned to the same center frequency. Further details are available in [72].

4.4.3. Breakout Measured Results

The average loss of the pads and baluns is around 2.5 dB per side, measured in a separate back-to-back breakout. Fig. 4.11 shows the measured scattering parameters of the RF power amplifier. Including balun losses, the peak small signal gain is 13.4 dB at 226.5 GHz with a 3-dB bandwidth of 20 GHz. At the center frequency, the simulated input referred P_{1dB} is -9 dBm. The simulated P_{sat} is 5.3 dBm including balun losses of estimated 2.5 dB. The power amplifier draws 98 mA from a 4 V supply.

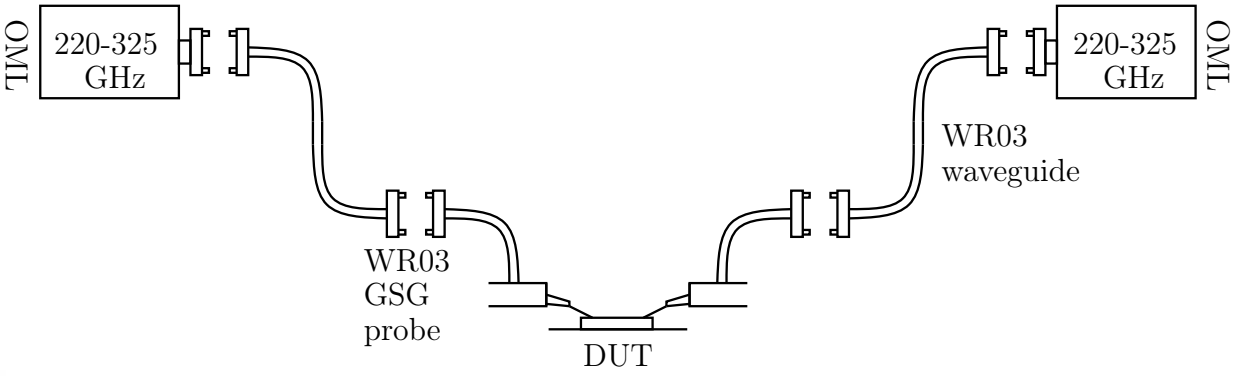


Figure 4.10.: Amplifier S-parameter measurement setup. A VNA with OML mmWave extender modules, WR03 S-bend waveguides and GSG probes are used for characterizing J-band amplifiers.

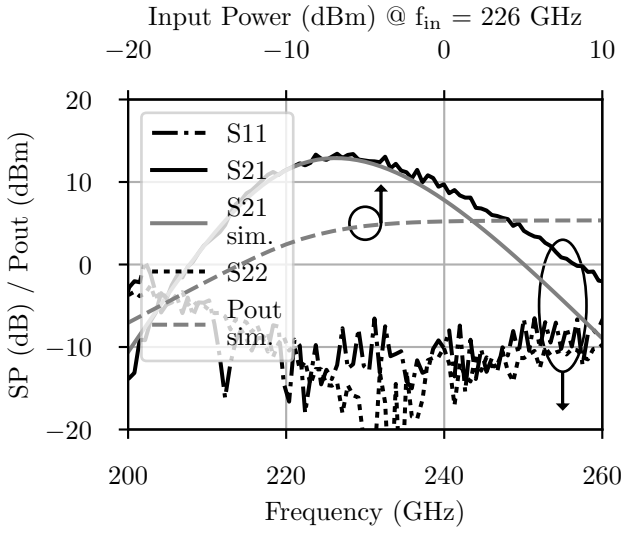


Figure 4.11.: Four stage RF power amplifier breakout measurement results. S12 stays below -30 dB over the whole measurement range. The simulated P_{sat} at 226 GHz after the output balun is 5.3 dBm.

4.5. Packaging

4.5.1. Board Assembly

The transmitter and receiver chips are each glued to the backside of a hyper-hemispheric high resistivity silicon lens. This chip-on-lens assembly is then mounted and wire-bonded on the backside of a 0.254 mm thick laminated Rogers 4350B PCB with a recess to accommodate the chip. With a silicon substrate height of 150 µm plus a back-end-of-line (BEOL) height of 12 µm, bond-wire length is kept short. Screwable, solderless K-connectors launch the baseband and LO waves into 50-Ω shielded coplanar wave transmission lines. DC supply voltages are applied from external voltage sources through soldered SMA connectors. Fig. 4.12 shows photographs of the TX and RX board assemblies. On the opposite of the PCBs, a circular copper heat sink encircles the silicon lens and is connected to it with thermally conductive glue, similar to the procedure from [85]. The heat sink is embedded in an aluminium plate, which is fixed to the thin Rogers PCB through six screws to prevent mechanical stress on supply and signal lines induced from a rigid cable assembly.

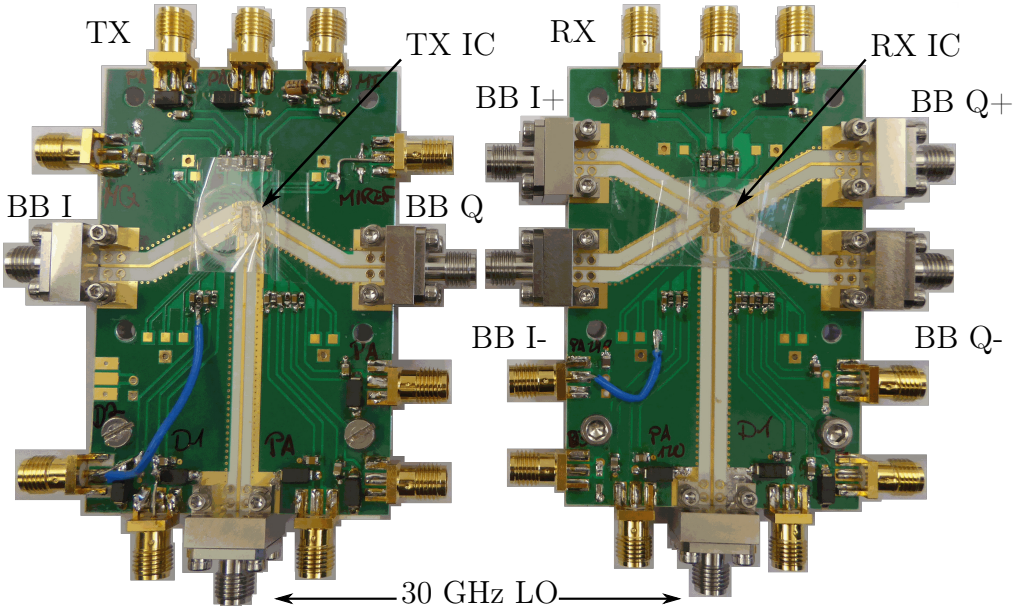


Figure 4.12.: PCB backside. Threadable K-connectors launch baseband and LO waves into 50-Ω shielded coplanar wave transmission lines on 0.254 mm Rogers 4350B. The IC is counterbored into the PCB. With a silicon substrate height of 150 µm, bondwire length is kept short. In the TX on the left side, I and Q signals are single ended; in the RX they are differential.

4.5.2. Matching Filter Design

To facilitate the transmission of the wideband baseband signals and the high frequency LO feed, a 6-section step-impedance low pass filter with minimum group delay dispersion compensates the inductance of the wire-bonds. The design of such a filter starts with generating

element values from a prototype [86]. A single 1 mm long wire-bond has an estimated inductance of 1 nH. This does not allow for the implementation of a low pass filter with an envisioned 30-GHz bandwidth, if the filter is solely PCB based and the wire-bond is its last element. Thus in [43] the bandwidth was limited to 13 GHz. Contrarily, in this work a 220 pH inductor was placed on chip. This moves the prototype element value equivalent to the wire-bond further into the overall filter. Placing two wire-bonds in parallel further reduces the total wire-bond inductance. A complete schematic of the 6th order filter is shown in Fig. 4.13.

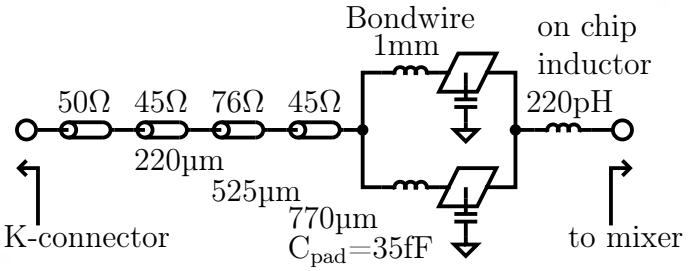


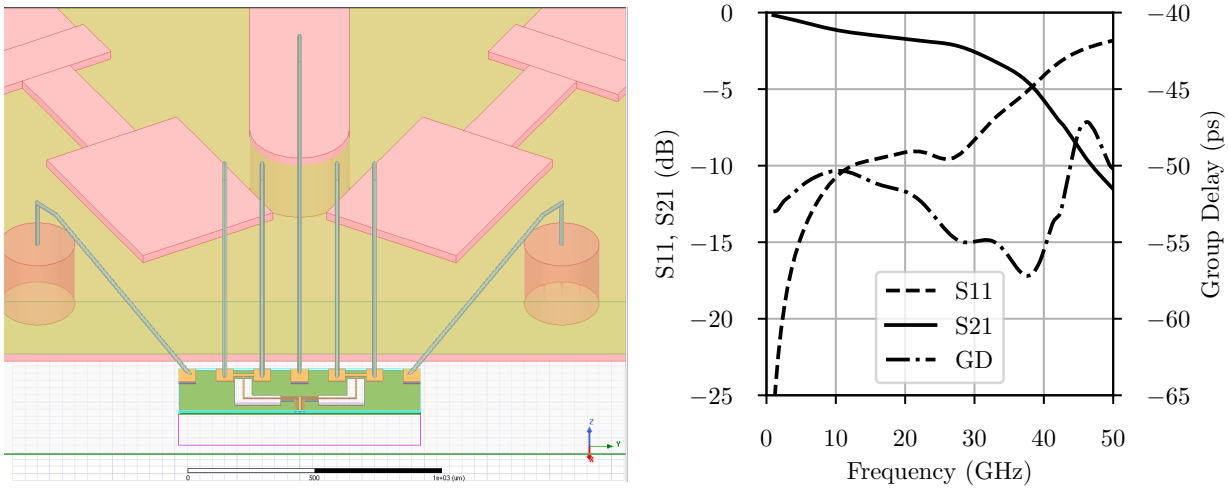
Figure 4.13.: IF/LO low pass filter schematic. The bond-wires and on-chip pad capacitances are absorbed into a 6th order filter with maximally flat transfer function for minimum group delay dispersion. One inductor is placed on chip to move the bond-wire inductance to a place in the filter, whose prototype value resembles the bond-wire inductance.

The filter was simulated using a full wave EM solver. Fig. 4.14a shows a screenshot of the filters for the differential baseband output of the receiver in the user interface of the EM solver. One on-chip inductor per side is connected to two parallel signal pads, onto which bond-wires are placed. The other ends of the bond-wires are attached to the stepped impedance microstrip filter on the PCB. Three ground vias coming from the PCB backside are wire-bonded to ground pads on the IC.

The 3-dB bandwidth of a single matching filter is 32.1 GHz according to simulation. The group delay varies by 5 ps over this bandwidth. The simulation results up to 50 GHz are shown in Fig. 4.14b.

The matching filter properties were characterized with a one port scattering parameter measurement, performed with an Agilent PNA and 85052D 3.5 mm mechanical calibration kit. Fig. 4.15 shows the connector level return loss, measured single ended at the TX and RX quadrature and the LO K-connectors. In the case of the TX and the RX baseband ports, measurement and simulation results agree reasonably well, although standing wave effects are recognizable in the measured results. For the TX, a return loss of -10 dB until 9.3 GHz and for the RX until 13.2 GHz is observed, respectively. For both the TX and the RX BB ports, the return loss stays below -6 dB over the whole calibrated measurement range.

With this new matching filter, the TX bandwidth is only limited by the front-end power amplifier, as will be seen in Ch. 5.2. The baseband bandwidth of the RX extents beyond 25 GHz, as measured in Ch. 5.3.



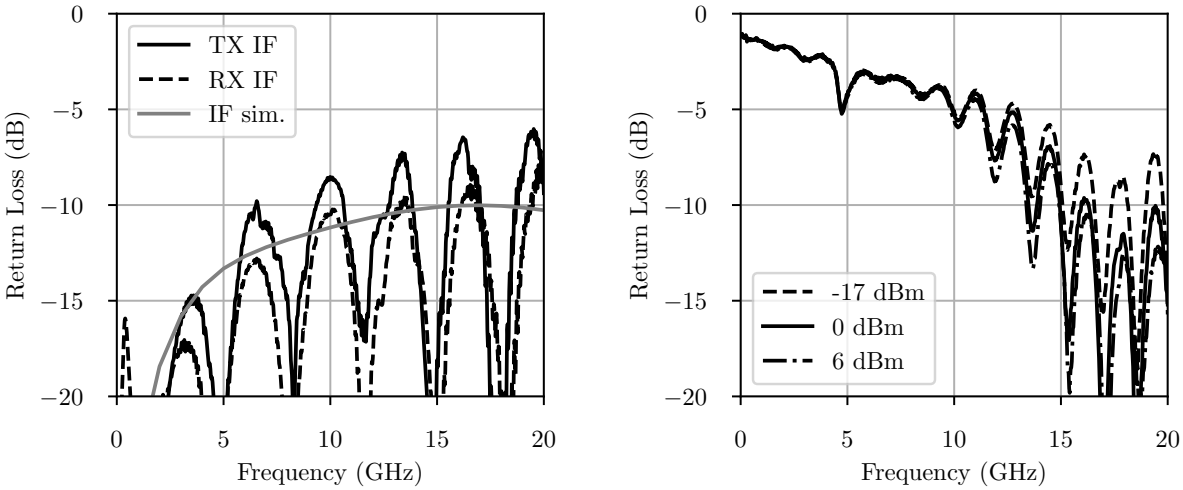
(a) (b)

Figure 4.14.: (a) A screenshot from the EM solver simulating the receiver baseband matching filter and (b) simulated reflection coefficient, insertion loss and group delay of single-ended filter.

In the case of the LO, the same matching filter is followed by a passive 30 GHz on-chip balun, which in turn feeds a class-B doubler. Therefore, the return loss only reaches levels below -10 dB at frequencies beyond 15 GHz and improves with increasing drive power.

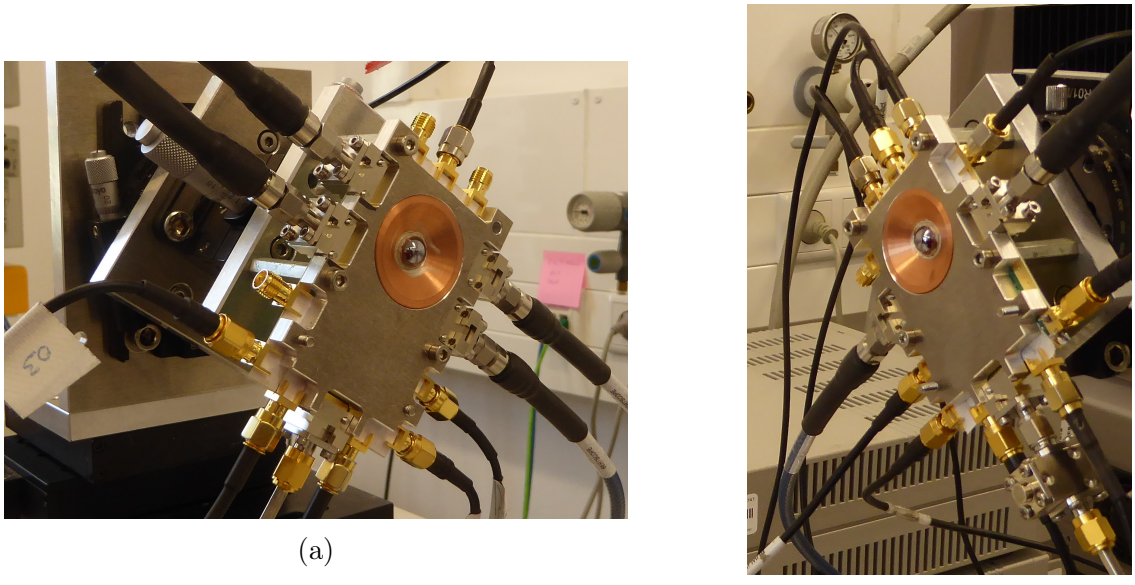
4.5.3. Complete TX and RX modules

A photo of the completely packaged transmitter and receiver modules can be found in Fig. 4.16. Clearly visible are the 9 mm silicon lenses. Thermally conductive glue connects the very edge of the lens with a copper cooler. The conical inlet of the cylindrical cooler is covered with absorber during all RF measurements to avoid reflections. The copper cooler is surrounded by an aluminium plate, which is fixed to the Rogers PCB below and to the holder in the measurement setup by a total of six screws. SMA connectors are distributed around the PCB. They serve as DC supply connections. The high-frequency local oscillator signal is launched onto the microstrip line on the back of the PCB through a solderless K-connector at the bottom. In the receiver in Fig. 4.16a, four of such connectors feed the differential I- and Q-channel baseband signals over phase-matched cables to a spectrum analyzer or high-speed oscilloscope, depending on the the type of measurement performed. In the TX in Fig. 4.16b, only two K-connectors are necessary due to the single-ended input of the up-conversion micromixers.



(a) (b)

Figure 4.15.: Matching filter return loss measured single ended at the connector level. (a) TX and RX baseband inputs show broadband low pass behaviour. (b) The LO input is power sensitive due to the class-B doubler and shows a bandpass characteristic due to the passive on-chip balun.



(a) (b)

Figure 4.16.: Photographs of the fully packaged (a) receiver and (b) transmitter module placed on rotational stages for RF characterization.

4.6. Polarisation Diversity Antenna

A micrograph of the lens-integrated polarisation diversity antenna used in both TX and RX can be found in Fig. 4.3. This antenna has first been published in [87]. It utilizes the multi-layer metal stack in the 12 µm thick SiO_2 BEOL. A circular slot aperture is excited by two orthogonal differentially driven pairs of sectorial probe elements. The antenna illuminates a 9 mm hyper-hemispherical silicon lens through the combined length of a 5.9 mm lens extension and the IC's 150 µm lossy silicon substrate.

The antenna patterns of the TX and the RX were measured in the respective setups of Fig. 5.1 and Fig. 5.4. A precision two axis rotational stage moves the respective fully-packaged module through a $\pm 30° \times \pm 30°$ sector of a hemisphere. The distance to the reference OML mmWave extender module is 30 cm, which is sufficient to ensure a far-field measurement. For both TX and RX, both polarizations have been characterized. Fig. 4.17a presents the transmitter antenna pattern at the RF PA center frequency of 225 GHz, when it is excited at the quadrature port. The directivity was calculated by integrating over the acquired power density values, while neglecting back radiation. The measured directivity at 225 GHz is 25.1 dBi. For measuring the cross-polar radiation patterns, the TX was rotated by 90°. At the center of the main beam, the normalized crosspolar directivity in the E- and H-plane is -31.9 dBi.

In the receiver, the measured coplanar directivity is also 25.1 dBi. The normalized power at the cross-plane are -25 dB below at the main beam center. Fig. 4.17b shows the measured antenna patterns. As attested by the considerable difference of radiated/received power between co- and cross-plane, the presented polarisation diversity antenna is well suited to enhance IQ channel isolation.

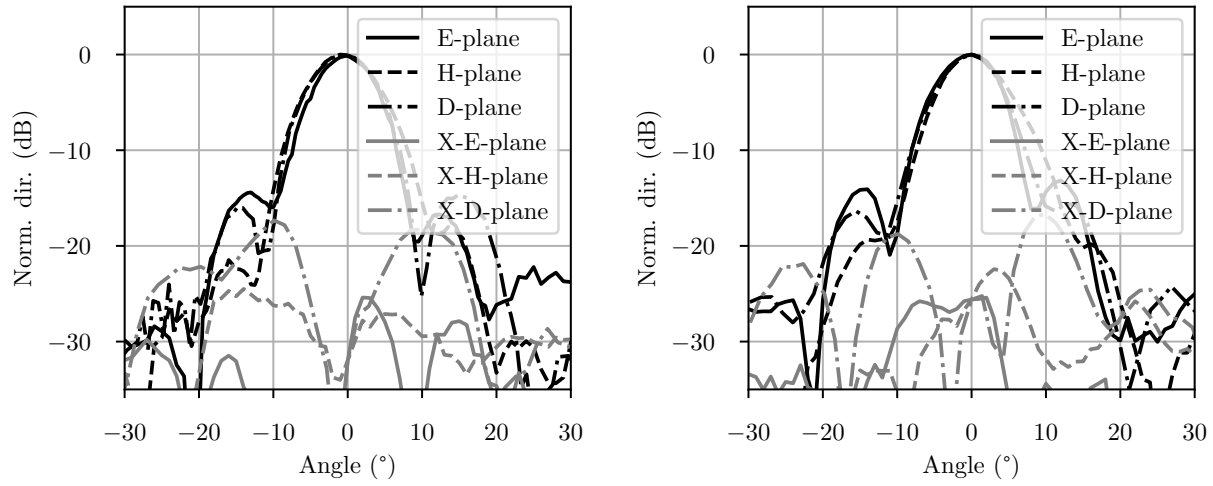


Figure 4.17.: Q-channel (a) transmitter and (b) receiver antenna patterns at 225 GHz carrier frequency. The directivity of 25.1 dBi is equal in both. The crossplanar radiation patterns are shown in grey.

4.7. Chapter Conclusion

This chapter presented block level diagrams and front-end components of a novel silicon integrated direct-conversion transmitter and receiver chip-set. To meet the design goals specified in Ch. 2.4, new frequency translation circuits were presented. A fundamental up-conversion micromixer has a 3-dB RF bandwidth of 38.5 GHz with 0 dB conversion loss when driven with a 240 GHz carrier. Due to its high linearity, the output power at the input referred 1-dB compression point of the mixer exceeds the IP_{1dB} of the following building block in a novel direct-conversion transmitter, which is the front-end power amplifier. The saturated output power of the PA is 5.4 dBm; its measured peak small signal gain is 13.4 dB at 226.5 GHz with a 20 GHz 3-dB bandwidth. This sets the RF bandwidth limitation of the overall transmitter.

In the receiver, a wideband switching quad based down-conversion mixer is followed by a novel variable gain amplifier. The simulated 3-dB RF bandwidth of the receiver front-end is 78 GHz. The VGA has a simulated tuning range of 22 dB, without negatively effecting the bandwidth of the conversion gain of the receiver. An improved packaging scheme increases the baseband bandwidth of the novel TX/RX chip-set in comparison with the 1st generation hardware discussed in Ch. 2.3. A reduced PCB height shortens the bond-wire length to the respective IC and the remaining wire-bond inductance is absorbed in a 6th order minimum group delay filter, part of which is realized on-chip and part on the PCB. This effort, in combination with the large RF bandwidth, ensures the overall link bandwidth will not be limited by the receiver. The low noise amplifier simulation results later in Ch. 7 make clear, that the omission of a front-end LNA did not worsen the overall receiver noise figure.

The I- and Q-channel signals are fed to individual polarizations of a dual polarized on-chip antenna, which radiates through the silicon substrate into a 9 mm silicon lens. The directivity of this lens-integrated antenna is 25.1 dBi in both transmitter and receiver. The isolation between polarizations at the main beam center are 25 dB in the RX and 31.9 dB in the TX. The effect of this polarization orthogonality should improve the overall IQ channel isolation in a link between TX and RX, which is investigated in the next chapter.

5. Front-End RF Characterization

5.1. Introduction to the Chapter

This chapter presents the measurement setups used to characterize the RF behaviour of both transmitter and receiver. The measurement results of the complete, packaged TX and RX can be found in Ch. 5.2 and Ch. 5.3 respectively. The wireless link RF performance is investigated in Ch. 5.3.

5.2. Transmitter Characterization

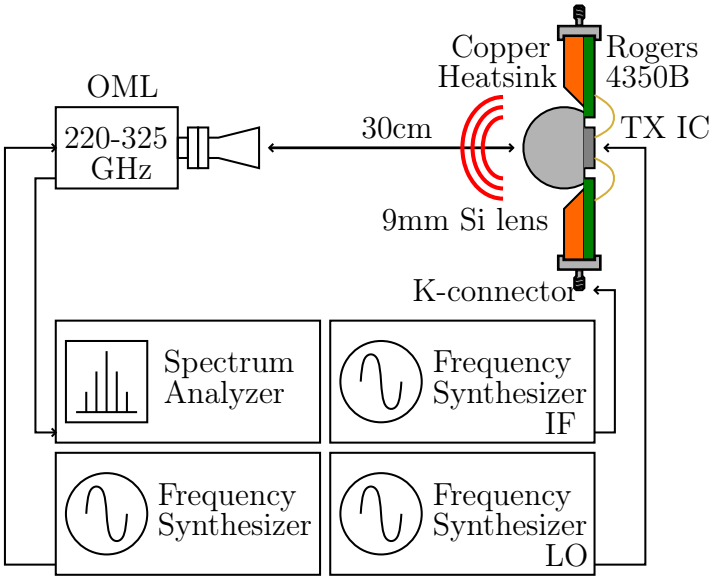


Figure 5.1.: Transmitter RF measurement setup. An OML mmWave extender module is used in receive mode to down-convert the transmitted signal. Agilent/Keysight E8257D PSGs generate LO/IF signals.

The transmitter was characterized using the measurement setup depicted in Fig. 5.1. A Keysight E8257D signal generator with up to 40 GHz output frequency generates the reference LO. An Agilent E8257D signal generator with up to 20 GHz output frequency is connected to a K-connector corresponding to either I- or Q-channel. Through a rotational stage, the transmitter is polarisation aligned to the 19 dBi horn antenna of a 220 GHz to 325 GHz OML mmWave extender module in downconversion configuration, whose reference

LO is stepped simultaneously to the IF of the TX. The resulting offset frequency of 33 MHz is recorded with an Agilent E4440A spectrum analyzer.

Fig. 5.2 and Fig. 5.3 show the characterization results of the transmitter with a 225 GHz and a 240 GHz carrier frequency respectively. In both, the I- and Q-channel conversion gains are equal with regards to the measurement tolerance.

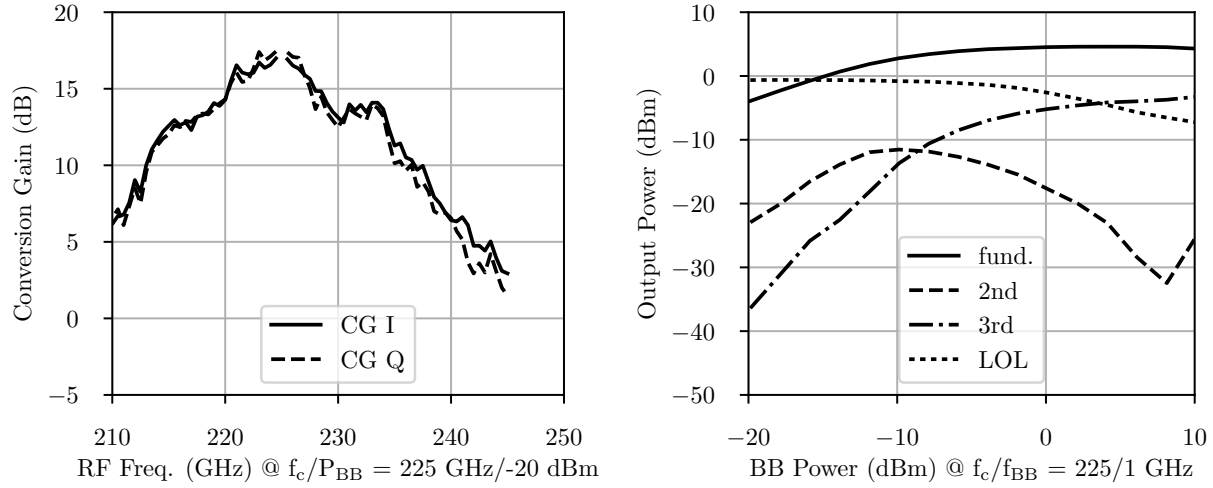
The conversion gain with respect to output frequency at -20 dBm of baseband input power is shown in Fig. 5.2a. Here, the RF PA maximum gain frequency and the carrier frequency of the transmitter are the same, which leads to a maximum gain of 17 dB at that point. The 3-dB bandwidth extents 5 GHz into the lower and 4 GHz into the upper sideband.

At a carrier frequency of 225 GHz and a baseband frequency of 1 GHz, the transmitter has a linear gain of 12.3 dB in the lower side band of the I-channel. The input referred P_{1dB} is reached at -17.8 dBm. At this point the second and third harmonic have a power of -20 dBm and -31.1 dBm respectively. The carrier leakage has -0.6 dBm of power, but decreases to a minimum of -7.2 dBm when the input micromixer goes into compression. The saturated output power of the TX then is 4.6 dBm, as shown in Fig. 5.2b

Fig. 5.3a shows the transmitter conversion gain when driven with a 240 GHz carrier, which is 12.2 dB at the RF PA center frequency of 225 GHz with a 3 dB bandwidth of 22 GHz.

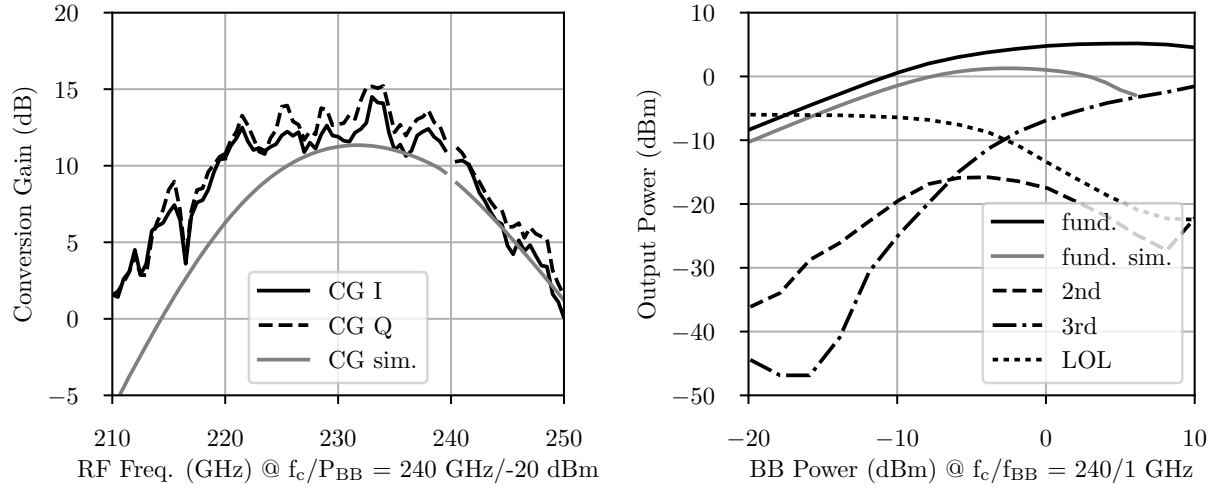
At a 240 GHz carrier and a 1 GHz BB frequency, the transmitter has a linear gain of 12.3 dB in the lower side band of the I-channel. The IP_{1dB} is reached at -12.1 dBm. Here the second and third harmonic have a power of -21.1 dBm and -27.4 dBm respectively. The carrier leakage has -6.0 dBm of power, but decreases to -10.3 dBm when the input micromixer goes into compression. The saturated output power of the TX then is 3.9 dBm, as shown in Fig. 5.3b.

In total, the transmitter consumes 1771.2 mW of DC power.



(a) (b)

Figure 5.2.: Transmitter RF characterization results with a 225 GHz carrier frequency. (a) Conversion gain when driven with -20 dBm of baseband input power. (b) I-channel LSB output power, 2nd and 3rd harmonic power and carrier leakage when IF is 1 GHz.



(a) (b)

Figure 5.3.: Transmitter RF characterization results with a 240 GHz carrier frequency. (a) Conversion gain when driven with -20 dBm of baseband input power. (b) I-channel LSB output power, 2nd and 3rd harmonic power and carrier leakage when IF is 1 GHz.

5.3. Receiver Characterization

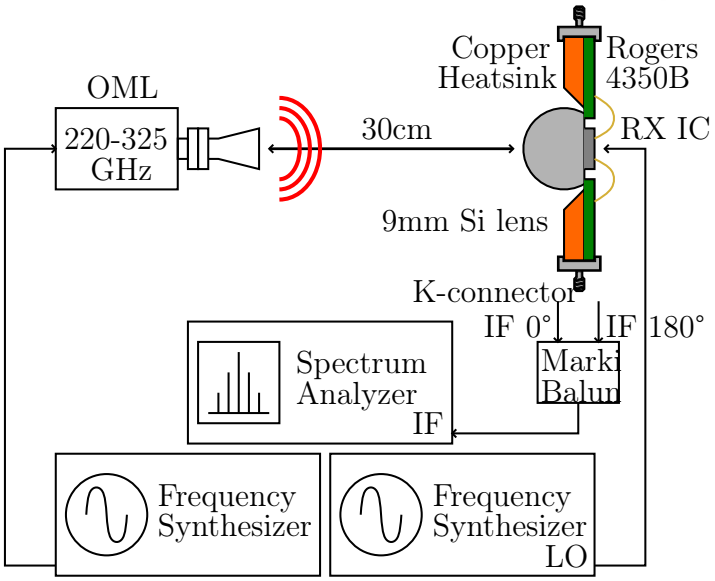


Figure 5.4.: Receiver RF measurement setup. A reference signal from an OML mmWave extender module in transmit mode is down-converted at the receiver and evaluated on an Agilent E4440A spectrum analyzer.

The receiver was characterized using the measurement setup depicted in Fig. 5.4. An OML mmWave extender in transmit mode is placed in a 30 cm distance to the fully packaged receive module, which is mounted on a rotational stage for polarization alignment. Similar to the transmitter measurement setup, a Keysight PSG supplies the LO. Phased matched cables feed the differential baseband output of the receiver into an external Marki broadband balun, which in turn is connected to an Agilent E4440A spectrum analyzer. The frequency response up to 26.5 GHz is directly recorded; for baseband frequencies up to 40 GHz, a Keysight 11970A harmonic mixer extends the bandwidth of the spectrum analyzer.

When driven with a 225 GHz carrier as shown in Fig. 5.5a, the measured conversion gain of the receiver is 10.6 dB at 0.5 GHz baseband frequency. The 3-dB bandwidth spans 25.5 GHz into the upper and 17 GHz into the lower sideband for a total of 42.5 GHz. Because no noise sources were available, the noise figure is calculated using the direct method [88] under the assumption that the input noise floor equals the thermal noise at room temperature with -174 dBm/Hz. The single-sideband noise figure is 14.7 dB.

With a 240 GHz carrier in Fig. 5.5b, the CG of the receiver is 10.6 dB at the center of its 51.5 GHz 3-dB bandwidth. At 0.5 GHz baseband frequency, the SSB NF then is 14.5 dB.

When driven with a 240 GHz carrier, the CG of the receiver can be reduced by up to 24.3 dB in the lower and by 27.3 dB in the upper sideband, if a maximum control current of 500 µA is applied to its linear-in-dB cell. Fig. 5.6 shows the progression of the CG with respect to the control current Ictrl.

In full gain setting, the receiver consumes 832.9 mW of DC power.

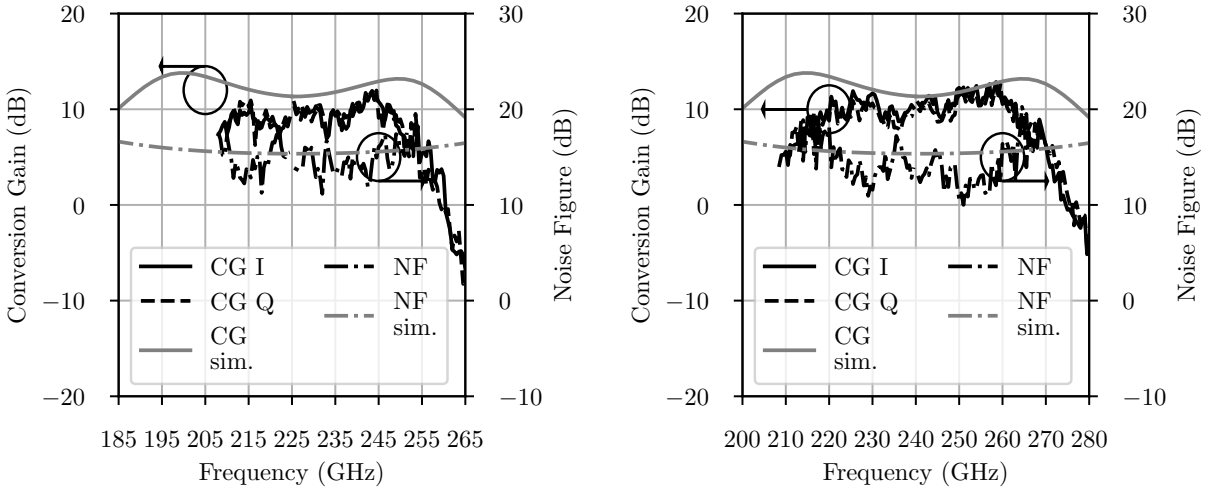


Figure 5.5.: Receiver conversion gain and noise figure at a carrier frequency of (a) 225 GHz and (b) 240 GHz.

Link Characterization

The RF performance of the link was characterized in free space by placing the TX and the RX in a 1 m line-of-sight distance. The rotational stages, on which the TX and RX were mounted, allowed to investigate the influence of the polarization diversity antenna on the link performance. For measuring the link conversion gain, the TX and the RX were polarization aligned; for measuring the channel isolation, the RX was rotated from co-polar to cross-polar excitation by the TX.

The LO path of the TX and the RX were fed from the same synthesizer. External phase shifters were used to move TX and RX from phase alignment for measuring the conversion gain of each channel, to opposing phases for channel isolation measurements.

The link conversion gain in the linear range of the TX is shown in Fig. 5.9a. It presents the link conversion gain for two different carrier frequencies: at 225 GHz, which is the center of the RF PAs bandwidth. And at 240 GHz, which lies on the higher edge of said bandwidth. At -20 dBm input power and a carrier frequency of 225 GHz, the Q-channel link CG is 25.9 dB with a 3-dB and 6-dB bandwidth of 8 GHz and 11.5 GHz respectively. If the carrier frequency is shifted to 240 GHz, the maximum link CG drops to 20.5 dB, but its 3-dB/6-dB bandwidth increases to 12 GHz/19 GHz.

The compression behaviour of the TX dominates also the wireless link. In Fig. 5.9b, the higher conversion gain of the TX at a 225 GHz carrier frequency and a baseband frequency of 0.5 GHz leads to an earlier onset of compression than with a 240 GHz carrier.

The Q-to-I channel isolation was characterized using the external phase shifters. The link conversion gain was measured in a single channel, once for exact phase alignment and once for opposing phase relations. The difference is the channel isolation by quadrature. The result

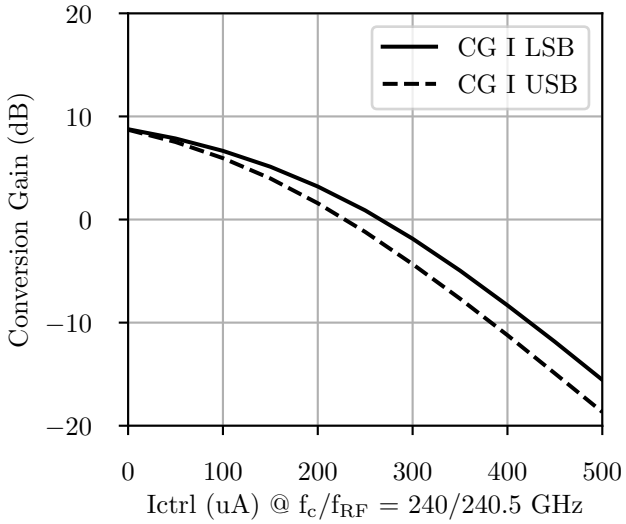


Figure 5.6.: Receiver conversion gain of the I-channel in relation to the VGA control current.

is depicted in Fig. 5.10. Again, the above described two carrier frequencies are differentiated. At an 225 GHz carrier, both channels are isolated by 20 dB through quadrature operation, courtesy to the good amplitude balance of lower and upper sideband. When the 6 dB bandwidth point is exceeded, the isolation deteriorates, with only 10 dB at 13.5 GHz.

At a 240 GHz carrier, upper and lower sideband have quickly declining amplitude balance, therefore the Q-to-I channel isolation by quadrature drops below 10 dB already at a baseband frequency of 4.5 GHz and decreases steadily over the measurement range. This would prohibit the use of quadrature modulations schemes, if not for an additional orthogonality introduced by the polarisation diversity antenna.

With a 225 GHz carrier, the combination of both quadrature and polarization orthogonality provides a channel isolation of more than 29 dB inside the 6 dB bandwidth of the link conversion gain. For a 240 GHz carrier, this stacking of orthogonalities guarantees an isolation of more than 15 dB over the whole measurement range. As will be seen in 6.3, this is even sufficient to use TX and RX in a form of single side-band operation to maximize the available RF bandwidth for data transmission.

Figure 5.7.: Photograph of the wireless link characterization setup. The receiver is placed on the left hand side, the transmitter on the right. Both are covered in absorbers to reduce reflections.

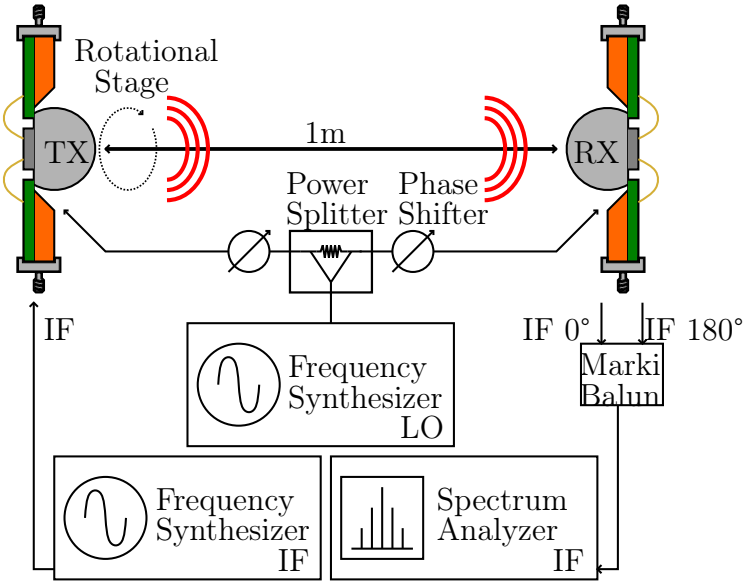
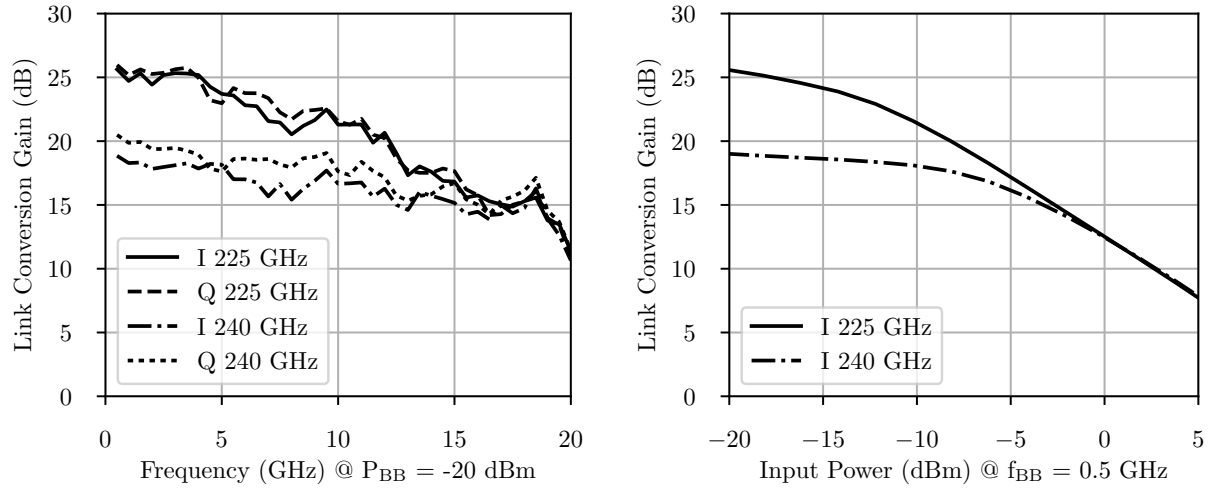
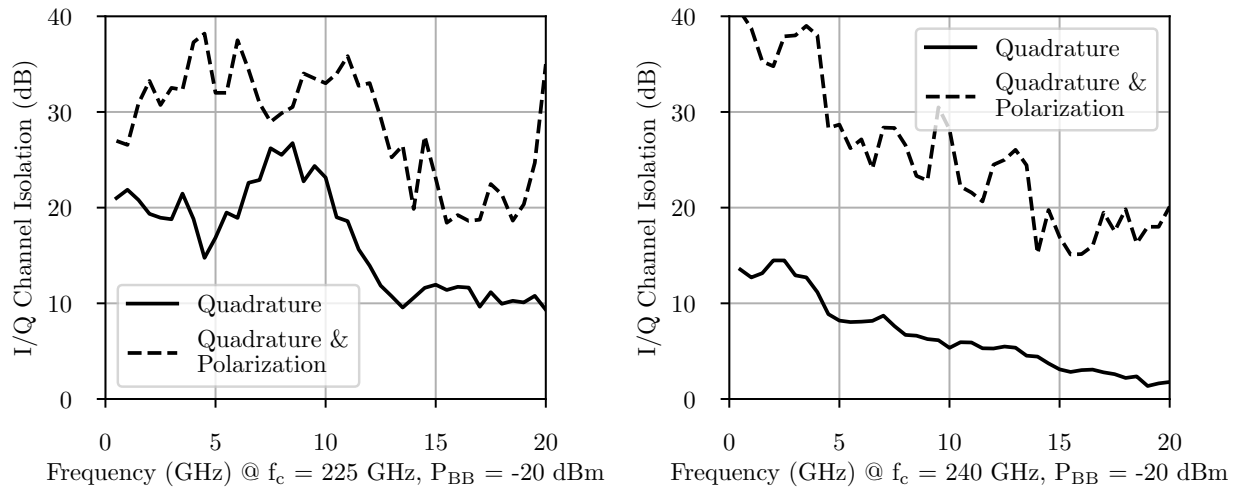


Figure 5.8.: Link RF characterization setup. Supplied from the same LO, TX and RX can be shifted in and out of phase alignment. A rotational stage is used for investigating the influence of the polarisation diversity antenna on link performance.



(a) (b)

Figure 5.9.: Link conversion gain over (a) BB input frequency and (b) BB power to the transmitter. TX and RX are placed in a distance of 1 m and are polarization and phase aligned. If the carrier is placed at the edge of the PAs bandwidth instead of at its center, the link conversion gain 3 dB bandwidth increases from 8 GHz to 12 GHz.



(a) (b)

Figure 5.10.: Channel isolation for a carrier frequency of (a) 225 GHz and (b) 240 GHz. The Q-channel of the TX is fed with a reference signal, the RX is rotated from co-polar to cross-polar excitation and its I- and Q-channel outputs are measured consecutively.

5.4. Chapter Conclusion

This chapter presented RF characterization results of the proposed novel transmitter and receiver chip-set packaged as described in Ch. 4.5.

The RF 3-dB bandwidth and saturated output power of the transmitter is dependent on the chosen carrier frequency. At 225 GHz, a 9 GHz BW and P_{sat} of 4.6 dBm per quadrature channel is achieved. By placing the carrier at the edge of the bandwidth of the transmitter at 240 GHz, the 3-dB bandwidth extents to 22 GHz and P_{sat} is 3.9 dBm.

The receiver has a 10.6 dB conversion gain and 14.5 dB noise figure at 0.5 GHz baseband frequency. Due to its wideband input match and baseband variable gain amplifier, the 3-dB bandwidth is 42.5 GHz with a 225 GHz carrier and 51.5 GHz with a 240 GHz carrier.

By placing the carrier frequency at 240 GHz, the wireless link emulates a single-sideband mode of operation. This increases the available bandwidth for modulation provided by the TX. Subsequently, the 6-dB link bandwidth extents by 7.5 GHz in comparison to the 11.5 GHz of the double-sideband mode of operation with a 225 GHz carrier. The polarization diversity antennas provide the necessary channel isolation, if the link is used in single-sideband mode. The switch from double-sideband to single-sideband operation in a direct conversion chip-set and its impact on channel isolation is conceptionally visualized in Fig. 5.11.

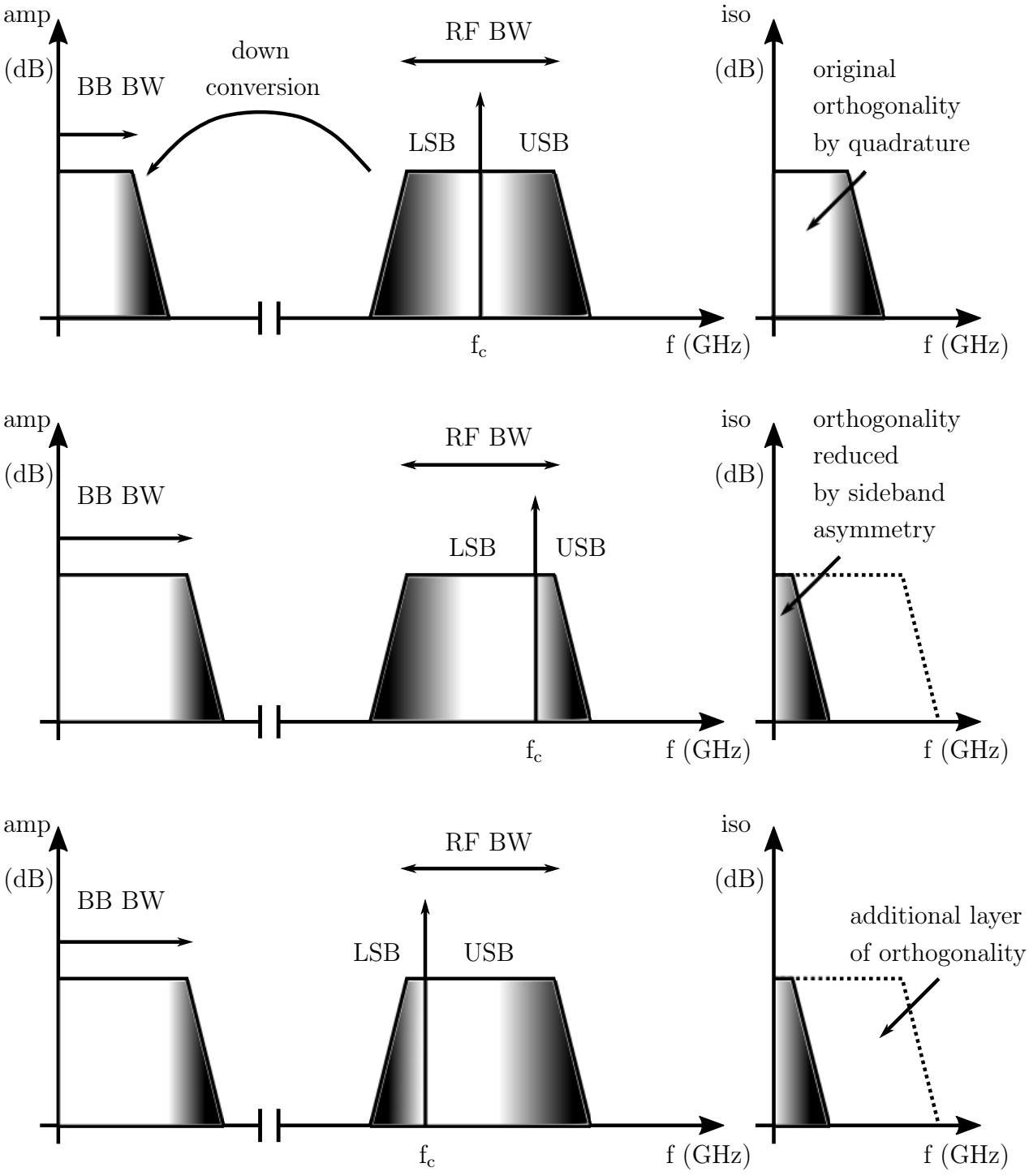


Figure 5.11.: I/Q channel isolation depending on carrier placement assuming a fixed available RF bandwidth. Isolation degrades rapidly, if upper and lower sideband in relation to the carrier are unbalanced in amplitude and/or phase. An additional layer of channel orthogonality has to be employed to benefit from the additional baseband bandwidth made available by high or low side carrier injection.

6. Wireless Link Communication Demonstration

6.1. Introduction to the Chapter

This chapter presents the measurement setup and results for a communication test of the presented radio front-end. While sweeping simultaneously over the carrier frequency in the transmitter and the receiver, a variety of quadrature modulation schemes and speeds are tested for their error vector magnitude. The measurement setup is introduced in Ch. 6.2 and data-rates with their corresponding EVM are recorded in Ch. 6.3.

6.2. Communication Measurement Setup

The setup used for measuring data-rates is shown in Fig 6.1. A pair of Tektronix AWG70001A with a sampling rate of 50 GS/s feed quadrature data streams to the TX. A pseudo-random bit sequence of order 9 resulting in a stream length of 2^9-1 was digitally modulated with a variety of standard modulation schemes. A root raised cosine filter with an α between 0.1 and 0.7 was applied to the data stream for pulse shaping to reduce the effective bandwidth of the baseband signal. 5 dB SMA-type attenuators reduce the AWG output power to avoid compression in the TX.

The RX was placed in a 60 cm line-of-sight distance. Its differential output signals first run through a set of PSPL5882 broadband amplifiers, then they are captured by two Tektronix DPO77002SX high speed oscilloscopes with 100 GS/s. This signal was post-processed using the SignalVu vector signal analysis software. It analyzes the EVM, constellation and eye diagram in real time and facilitates clock recovery, I/Q imbalance correction and has an adaptive decision-directed FIR feed-forward equalizer. An equalizer with 51 taps was applied to the received signal.

All baseband signals are routed via phase matched cables. The setup was covered with absorbers to avoid multipath effects caused by reflections. A Keysight E8257D signal generator supplies the LO drive for both TX and RX, which are phase aligned through external phase shifters and polarization aligned with a rotational stage.

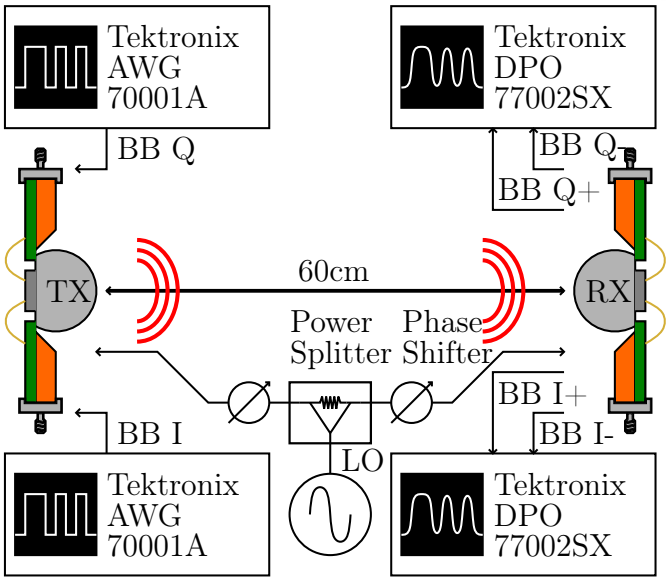


Figure 6.1.: Communication measurement setup. TX and RX are placed in a 60 cm distance. They are fed from the same LO and phase aligned through external phase shifters.

6.3. Communication Measurement Results

To evaluate the performance of the presented wireless link, the error vector magnitude (EVM) was recorded using the communication measurement setup from Ch. 6.2. All shown EVM values refer to the average power of all symbol vectors within the used constellation for normalization, as discussed in Ch. 1.4. All EVM values are read directly from the SignalVu oscilloscope software as previously described. No further post processing has been done.

The achievable data-rates depend on the selected carrier frequency f_c. The $\times 8$ multiplier chain is sufficiently tunable to place f_c either at the center of the RF bandwidth for double side-band mode or at its edges, effectively running the link in a single side-band mode with low side or high side injection.

Fig. 6.2 shows the measured error vector magnitude for different data-rates at a variety of carrier frequencies. The constellation diagram insets in all figures are unaltered screen shots directly from the oscilloscope software.

The highest data-rate of 140 Gbit/s was measured using high side injection by placing the carrier at 240 GHz. As Fig. 6.2f shows, an EVM of 11.5 % was measured using a 32-QAM scheme. Assuming only additive white Gaussian noise to the received signal, this EVM translates to a bit error rate of $3.1 \cdot 10^{-3}$ calculated from Eq. 1.12 in Ch. 1.4.

140 Gbit/s were also reached using 16-QAM with the same carrier, but with an EVM of 19 %, which is not sufficient for a BER $< 4.5 \cdot 10^{-3}$. As shown in Fig. 6.2e, when switching to a 235 GHz carrier, the EVM drops to 16.4 %. This equals a BER of $2.4 \cdot 10^{-3}$. When switching to low side injection by choosing a carrier frequency of 215 GHz, 120 Gbit/s were obtained in 16-QAM and 32-QAM with an EVM of 12.8 % and 10.9 % respectively.

Other modulation schemes were also explored. With a QPSK modulation scheme, a maximum of 85 Gbit/s were transmitted with a minimum EVM of 30.3 % on a 220 GHz carrier. Also for all other tested carrier frequencies, EVM does not rise above 31 % for this modulation order and speed. The TX linearity and bandwidth suffice for 90 Gbit/s in 64-QAM with an EVM of 6.8 % with a 240 GHz carrier, which is depicted in Fig. 6.2f.

When placing the carrier at the 225 GHz center of the RF bandwidth, the TX output power increases. But due to the consequent reduced link bandwidth, the EVM for 85 Gbit/s in QPSK modulation still is 31 %. The highest achieved data-rate with a 225 GHz carrier was 100 Gbit/s using 16-QAM with an EVM of 11.3 %.

Theoretically it should be possible to translate the increased TX output power into a greater back-off capability for even higher order modulation schemes. This however could not be confirmed in practice. For this experiment, the 5 dB attenuators in the input to the TX were replaced with 15 dB ones. The phase error from the used synthesizer multiplied by the $\times 8$ multiplier chain sets a hard limit to the achievable EVM, with 4 % at 10 Gbit/s using 16-QAM. This prevents locking for higher modulation orders.

Including the carrier generation circuitry and when operated with a 240 GHz carrier, the transmitter and receiver front-ends consume a total of 2.6 W of DC power. With a data-rate of 140 Gbit/s, the link has an energy efficiency of 18.6 pJ/bit.

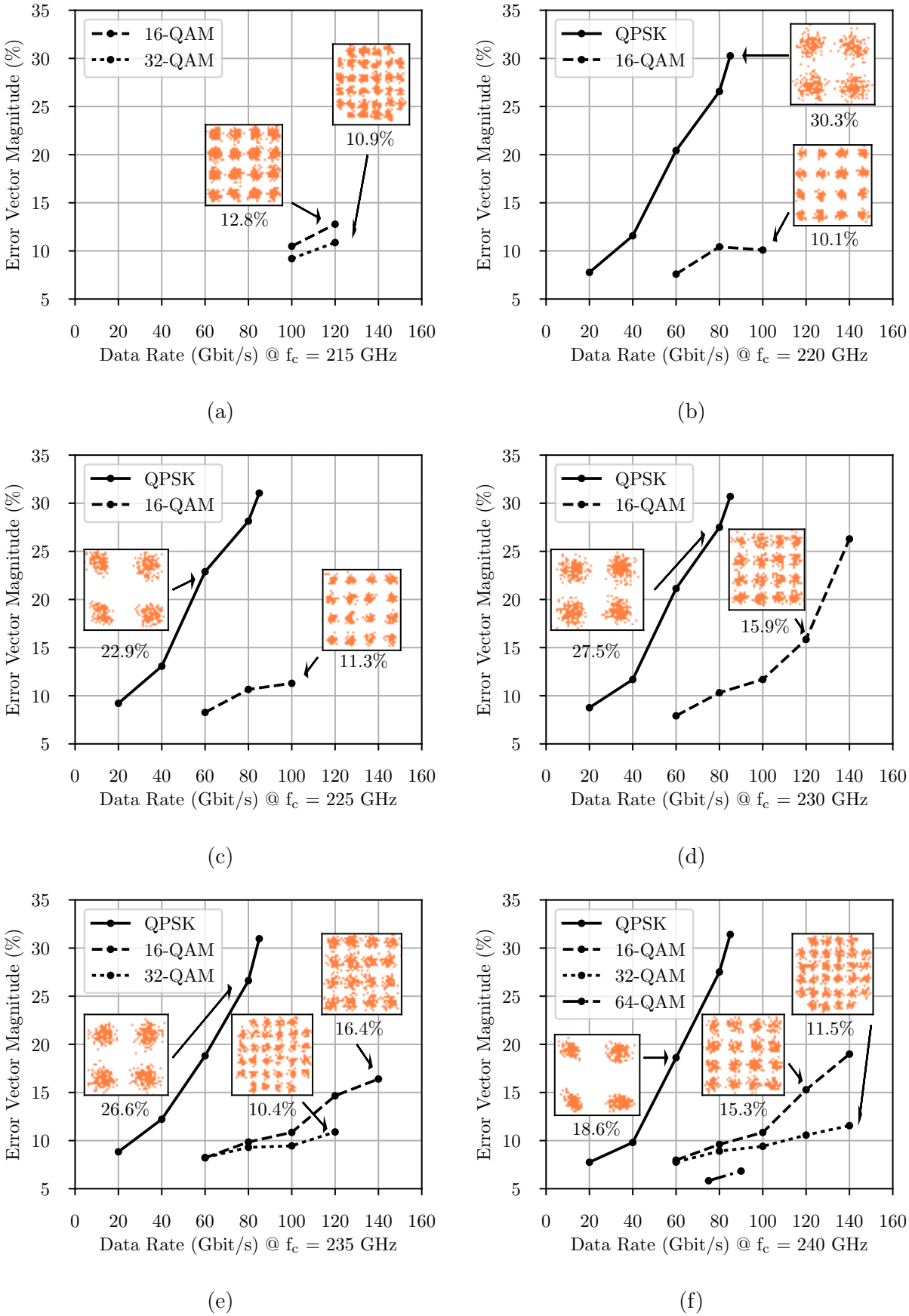


Figure 6.2.: EVM for different data-rates with a carrier frequency of (a) 215 GHz (b) 220 GHz (c) 225 GHz (d) 230 GHz (e) 235 GHz (f) 240 GHz. 140 Gbit/s were achieved using 16-QAM with an EVM of 16.4 % at a carrier frequency of 235 GHz and using 32-QAM with an EVM of 11.5 % at 240 GHz.

6.4. Chapter Conclusion

A wireless link was established over a 60 cm distance. The EVM limit for an error free transmission as discussed in Ch. 1.4 for the 16-QAM modulation scheme is 17.8 %. A data-rate of 100 Gbit/s within this limit is possible for all carrier frequencies between 215 GHz and 240 GHz.

A maximum data-rate of 140 Gbit/s was achieved with a 32-QAM modulation scheme at a 240 GHz carrier frequency. The corresponding EVM was 11.5 %, which translates to a BER of $3.1 \cdot 10^{-3}$. 140 Gbit/s were also achieved in 16-QAM at 235 GHz carrier frequency. Here, the measured EVM was 16.4 %, which translates to a BER of $2.4 \cdot 10^{-3}$.

The limits to the achievable data-rates are cumulative as discussed in Ch. 1. However, the main contributors differ with the used carrier frequency and modulation scheme.

Carrier frequencies outside of the multiplier chain bandwidth shown in Fig. 3.25b from Ch. 3.6.5 could not be tested, because of the missing drive power to the mixers.

As shown in Fig. 5.9, the link conversion gain and thus the TX output power are higher, if the carrier is placed at the 225 GHz center frequency of the front-end PAs. Despite this fact and because IQ imbalance is of no concern due to the system architecture, the data-rates achieved at this carrier frequency indicate a hard bandwidth constraint for 16-QAM. The measured results in Ch. 4.3.1, Ch. 4.3.2 and Ch. 4.4 allow the conclusion, that the up and down-conversion mixers do not limit the overall link bandwidth, but the front-end PAs do.

With the improved IQ channel isolation due to the use of the presented polarization orthogonality technique, placing the carrier frequency at the edges of the front-end PA bandwidth extents the usable bandwidth. The fixed RF bandwidth of the front-end PA then is used for a single side-band mode of operation. Depending on the carrier position, the RF bandwidth is nearly exclusively utilized for either the lower side-band or the upper side-band. This enables the higher data-rates of 120 Gbit/s or more visible in Fig. 6.2a, d, e, f, when compared to the maximum of 100 Gbit/s with a 220 GHz or a 225 GHz carrier.

For 16-QAM modulation, the maximum channel capacity is nearly reached with the achieved 140 Gbit/s. For 32-QAM modulation, the data-rate is limited by the achieved signal-to-noise ratio and high phase noise. In combination, they prevent the use of higher order modulation schemes to increase the data-rate.

The transmission range is limited by the SNR. With the current technology, an improvement of the noise figure is cumbersome. As shown by the simulated NF of the low-noise amplifiers in Ch. 7, receiver noise figure would not change for the better.

Therefore, to achieve even greater transmission speed or range without increasing antenna directivity, a more sophisticated power amplifier design is in order. An increased PA bandwidth in combination with power combining could provide higher data-rates or transmission ranges in a future transceiver implementation. Further system-level ideas and possible improvements of the achievable data-rates are discussed in Ch. 8.2.

A comparison with the current state-of-the-art work can be found in Tab. 6.1.

Ref.	Technology Node f_T/f_{max} (GHz)	Frequency (GHz)	Modulation	Data rate (Gbit/s)	P_{DC} (W)	Efficiency (pJ/b)	Antenna Type	Antenna Gain (dBi)	Distance (m)
[34]	InP HEMT 35 nm 515/–	240	8 PSK	96	—	—	horn	—	40
[35]	InP HEMT 80 nm 300/700	270	16-QAM	100	—	—	horn	2×50	2.22
[36] [37]	CMOS 40 nm –/–	300	16-QAM	32	2.05	65	horn	—	0.01
[38]	CMOS 65 nm –/–	70/105	16-QAM	2×60	0.28[1]	2.5	horn	2×23	0.2
[39]	SiGe 130 nm 300/450	190	BPSK	50	0.154[1]	3	bond wire monopole	2×5	0.006
[40]	SiGe 130 nm 300/500	240	BPSK	25	0.95	38	LBE[2] dipole + plastic lens	2×14	0.15
[30]	SiGe 130 nm 350/550	225-255	16-QAM	90	1.96	22	single pol. + Si lens	2×26	1
[31]	SiGe 130 nm 350/550	220-260	32-QAM	90	1.96	22	single pol. + Si lens	2×26	1
[41]	SiGe 130 nm 350/550	220-255	16-QAM	100	1.41	14	single pol. + Si lens	2×26	1
This work	SiGe 130 nm 300/450	240	16-QAM	**140**	2.6	18.6	**dual pol.** + Si lens	2×25.1	0.6
This work	SiGe 130 nm 300/450	235	32-QAM	**140**	2.6	18.6	**dual pol.** + Si lens	2×25.1	0.6

[1] Without carrier generation circuitry. [2] Local backside edging.

Table 6.1.: Comparison of state-of-the-art 200 GHz - 300 GHz wireless links

7. Amplifier Design in the 200 GHz - 300 GHz Band

7.1. Introduction to the Chapter

Despite the advances in SiGe technology, the amplifier gain in the higher realms of the sub-THz range is still limited. By embedding the transistor core of an amplifier in a passive feedback network, the gain at frequencies above 1/3 f_{max} of a chosen technology can be increased to a certain extend.

In 2015, the "International Journal of Microwave and Wireless Technologies" included the paper titled "J-band amplifier design using gain-enhanced cascodes in 0.13 µm SiGe" in its European Microwave Week 2014 special issue [89]. This paper described experiments with a particular gain enhancement method using series-series feedback applied to SiGe HBT cascodes. Starting from a simplified equivalent circuit model, a formula for the voltage transfer function based on standard two-port parameter calculations was derived. With this rather general knowledge in mind, a methodology for low noise amplifier (LNA) design relying on S-parameter analysis was presented. This methodology aimed to equip the reader with an algorithmic design procedure for stable, high-gain, low noise amplifiers above 1/3 f_{max} of a given technology. Two LNAs in IHP's SG13G2 and Infineon's B11HFC technology were then presented.

Since then, an approach to amplifier design was re-discovered and gained popularity in the recent literature, that originally was first presented in 1966. In [90], A. Singhakowinta from the Faculty of Medical Science at the University of Bangkok and A. R. Boothroyd from the Department of Electrical Engineering at the Queen's University of Belfast first derived an expression for the absolute maximum gain G_{max}, that a linear two-port amplifier can deliver. It is based on Mason's unilateral power gain U, which is invariant with respect to lossless, passive embedding for a given two-port [91] [92]. Shortly afterwards [93] they presented a graphical tool they named the "normalized gain chart", which correlates the maximum transducer power gain G_{ma} (the maximum gain of a two-port with simultaneous conjugate impedance match at input and output) to U and Rollet's stability factor k [94]. Singhakowinta and Boothroyd's original envisioned application for their theory was de-sensitizing transistor amplifiers to manufacturing spread. However, as a number of very recent publications [95] [96] [97] show, it is also suited to aid in transistor amplifier design above 1/3 f_{max}.

This chapter applies both the original design methodology presented in my 2015 paper [89] and Singhakowinta and Boothroyd's design approach to the aforementioned SiGe HBT cas-

codes. For this purpose, the original S-parameter based methodology has been revised into a clearer, even more detailed form. The analysis presented in this chapter is carried out based on the latest available simulation models supplied by the respective foundries. This leads to slightly different looking graphs, as the simulation data in the original paper [89] was generated with older models. This just reinforces the point of exercising caution, when designing gain-enhanced amplifiers using reactive feedback.

Singhakowinta and Boothroyd's gain chart consists of a set of constant-G_{ma} circles and constant-k contours. The equations for generating these were extended to incorporate low values of U as typical above $1/3$ f_{max} in [98], 50 years after the initial publication by Singhakowinta and Boothroyd. The derivation of the equations in the gain chart is presented in Appendix A. To my best knowledge, while the final equations were first presented in [98], their derivation has never been published before.

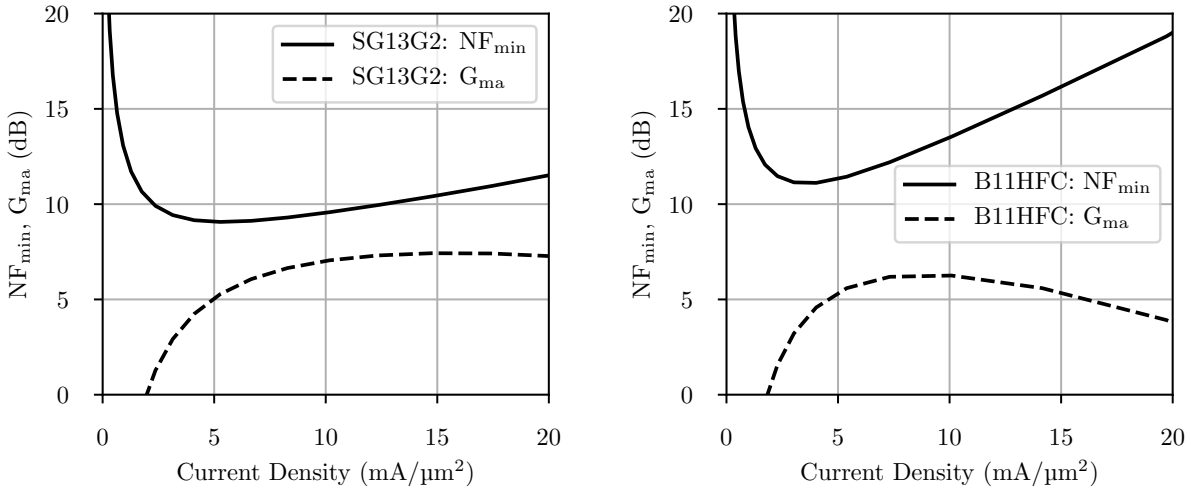
The chapter shows the limits of practical usability of the "gain chart" for the specific case of series-series feedback applied to the common-base transistor in a cascode, but also recognizes the additional information that it provides. It shows, how the original methodology and designing with the help of the gain chart converge for the extreme point of G_{max} because of a specific boundary condition.

Section 7.2 discusses the basic considerations and trade-offs of LNA design in SiGe HBT technology. Section 7.3 describes the original design methodology from [89], using series-series feedback to boost the gain of a cascode topology. Afterwards, Section 7.4 shows an new perspective on this methodology using an extended version of the theory introduced by Singhakowinta and Boothroyd. The circuit architectures and measured results of both LNAs are presented in section 7.5. Finally, Section 7.6 provides a conclusion.

7.2. Low Noise Amplifier Design Considerations

Whether in communication, radar or imaging applications, there is a need to minimize noise in a wireless receiver front-end. Referring to Friis' formula [99], typically, a low noise amplifier as a first active building block in such a system provides sufficient gain to reduce the noise impact of subsequent components. Bandwidth and power consumption are also of considerable importance for a LNA integrated into a wireless receiver front-end. For radar circuits, wider bandwidth improves the range resolution [100]. For passive imaging [101] RF bandwidth is of utmost importance, because it is part of the equation of the noise equivalent temperature difference (NETD), which is a measure for detector sensitivity. In this particular application, cost-effective solutions with silicon technology have the potential to revolutionize the field of security screening. At airports for example, large scale passive imaging arrays could replace the currently employed screening booth with active radiators. This could resolve traveller's doubts about the impact on health of the security screening. In extension of this idea, hidden screening could streamline the travelling experience by removing the screening process from the conscious perception of the travellers.

In bipolar transistors, the optimum collector current density J_{opt} for minimum noise figure NF_{min} in the 200 GHz to 300 GHz frequency band is a factor of two times smaller than the



(a) (b)

Figure 7.1.: Minimum noise figure and maximum transducer gain for a pseudo-differential cascode core in (a) IHP's SG13G2 technology at 240 GHz; or (b) Infineon's B11HFC technology at 220 GHz. In both, the current density for minimum noise is smaller by a factor of two than for peak f_{max} operation.

necessary current density to reach peak f_{max} [54]. Fig. 7.1 shows the simulated NF_{min} and G_{ma} for a pseudo-differential cascode in SG13G2 and B11HFC technology respectively. By biasing at J_{opt}, G_{ma} is reduced by around 2 dB.

An NF_{min} set by correct biasing translates only into a low realized NF, if the source impedance Z_s and the noise impedance of the LNA match. Simultaneously, the input impedance Z_{in} mismatch should be reduced to prevent reflection losses. Increasing the emitter length of a bipolar device reduces the optimum source impedance Z_{opt} for noise matching, which is described in [102]. An input matching network then has to tune out the remaining difference between both Z_s and Z_{opt}, as well as between Z_s and Z_{in}.

The matching procedure further described in [102], while being successfully employed in many low noise amplifier designs today, limits the achievable gain due to the use of inductive degeneration. This restricts its applicability to LNAs operating above 1/3 f_{max} of the chosen technology.

In summary, biasing the transistor for low-noise operation diminishes single stage gain. Different design approaches to increase single-stage gain have been proposed in the literature. If the resulting gain of a single stage is still too low for the envisioned application, multiple stages can be cascaded.

7.3. Original Design Methodology for Gain Enhanced Cascodes

This section recapitulates the S-parameter based methodology from [89], which was used during the design phase of the two presented amplifiers in that paper. It reliably and repetitively produces stable high gain amplifiers at frequencies above 1/3 f_{max} of the used technology.

According to the review paper from M. S. Gupta [92], Samuel J. Mason was searching for a figure of merit for the transistor, which has only been around for five years at the time of his work in 1953. He found the unilateral power gain U, which is an invariant for any linear two-port with respect to transformations as represented by any four-port, linear, lossless and reciprocal embedding network. U can be found from the two-port parameters [91]. As a function of Rollett's stability factor k:

$$U = \frac{|S_{21}/S_{12} - 1|^2}{2k|S_{21}/S_{12}| - 2 \cdot \mathrm{Real}(S_{21}/S_{12})} \tag{7.1}$$

Unilateralization then is the process of choosing an embedding network to a core two-port, such that the resulting overall network has no reverse transmission or, in S-parameter terms, perfect reverse isolation, with $S_{12} = 0$. If afterwards simultaneous conjugate matching is applied, the conceived transistor amplifier exhibits a power gain of exactly U.

A common approach to unilateralization is capacitive cross-coupling of a pseudo-differential transistor core, demonstrated in CMOS technology for common-source [103] or cascode [104] cores.

However, the unilateral power gain is not the absolute maximum achievable gain of a transistor. As shown in [90], the absolute maximum power gain G_{max} of a two-port is:

$$G_{max} = 2U - 1 + 2\sqrt{U(U-1)} \tag{7.2}$$

Or, if $U >> 1$:

$$G_{max} \approx 4U \tag{7.3}$$

Thus, by choosing an embedding network, which provides feedback with the correct amplitude and phase, the power gain of a transistor amplifier can be extended beyond U. As previously analysed for an equivalent CMOS topology [105], the introduction of inductor L_{fb} at the base terminal of the common-base transistor in a cascode is an option for introducing such a feedback mechanism, actually decreasing its inherently good reverse isolation. And while U is defined for $k < 1$, G_{max} is not, as simultaneous conjugated matching considering all possible passive source and load impedances requires unconditional stability. Simultaneously maintaining unconditional stability while increasing power gain thus becomes priority. Fig. 7.2a shows an illustrative AC circuit schematic of a pseudo-differential cascode amplifier

for analysing the influence of L_{fb}. RF choke (RFC) inductors and RF short (RFS) capacitors for biasing are also shown.

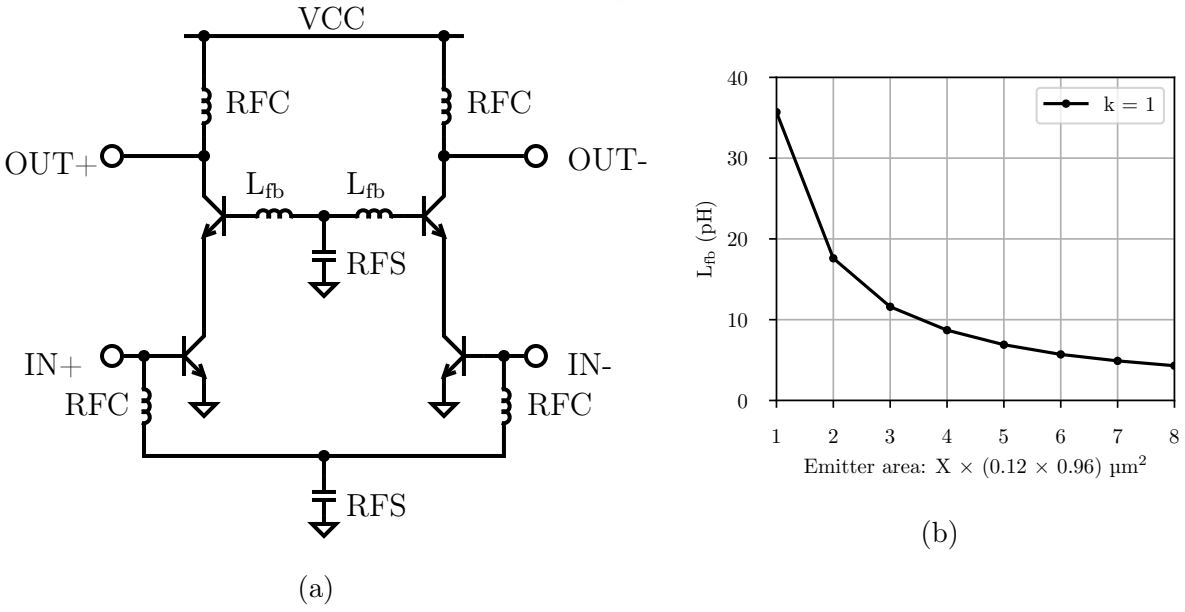


Figure 7.2.: (a) AC circuit schematic used for analysing the influence of feedback inductor L_{fb}. (b) Inductance of L_{fb}, for which SG13G2 cascodes of multiples of the HBT unit cell size exhibit k=1.

Fig. 7.3 breaks down a cascode consisting of common-emitter transistor, common-base transistor and series-series feedback inductor L_{fb} into their simplified high-frequency small signal equivalent circuits. Two-port representation is indicated by the dashed lines in the figure. Including the additional inductor, the cascode now consists of two cascaded single feedback loops. Formulas for the voltage transfer function in line with classical feedback theory based on two-port analysis as found in textbooks like [106] were derived in the original paper [89].

Fig. 7.2b shows for a cascode in SG13G2 technology and at a 240 GHz design frequency, for which combination of L_{fb} and HBT emitter area Rollett's stability factor reduces to the critical boundary one. This feedback inductance shall be called $L_{fb,max}$. The decrease of $L_{fb,max}$ with HBT size can be understood intuitively, by re-interpreting this gain-enhanced cascode topology as a Colpitts oscillator. From [54], the oscillation frequency f_{osc} can be approximated by:

$$\frac{1}{(2\pi f_{osc})^2} = L_{fb} \cdot \frac{C_1 C_2}{C_1 + C_2} \tag{7.4}$$

where C_1 is the base-emitter capacitance C_π of the common-base transistor and C_2 is $C_o||C_\mu$ of the common-emitter transistor under the assumption that its base-emitter terminal is AC short-circuited. Thus for larger junction capacitances of the HBTs, the necessary feedback inductance for potential oscillation reduces. The EM-simulated inductance of a typical via stack from lowest to highest metal layer in the BEOL of the SG13G2 technology is around 4 pH. It is apparent that, due to parasitics, the feedback inductor becomes harder to model

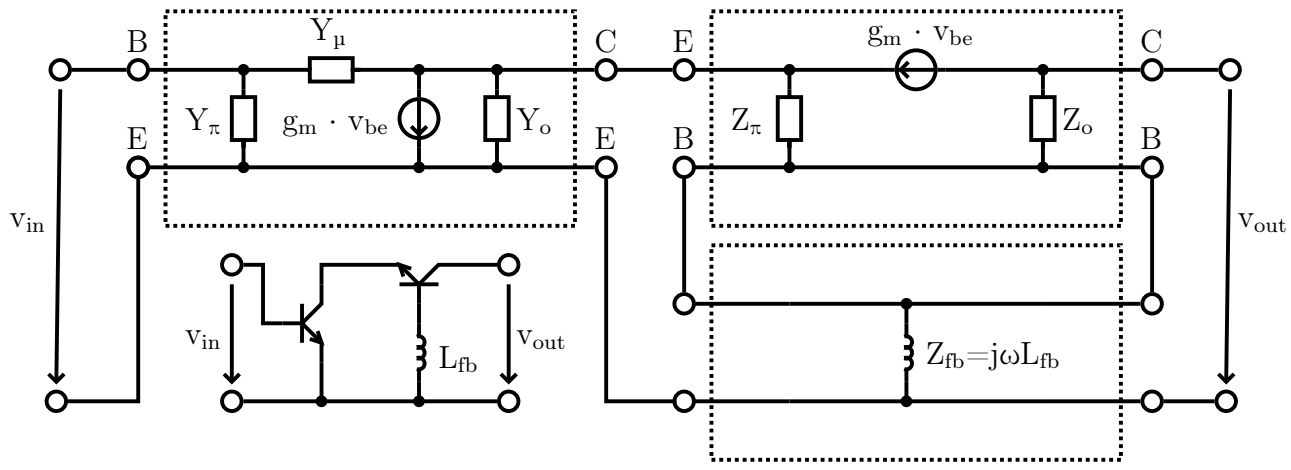


Figure 7.3.: Simplified equivalent half circuit of a gain-enhanced bipolar cascode with two-port boundaries marked with dashed lines.

correctly, the bigger the used transistors are. Thus, it is advised to choose the transistor size as small as still suitable for noise matching purposes.

Fig. 7.4 shows the simulated influence of feedback inductor L_{fb} on maximum available gain G_{ma}, maximum stable gain MSG, absolute maximum gain G_{max} and unilateral gain U for a pseudo-differential cascode transistor core. Fig. 7.4a refers to SG13G2 technology with an emitter size of 2× (0.12× 0.96) µm^2 at a design frequency of 240 GHz; Fig. 7.4a to B11HFC technology with an size of (0.13× 5) µm^2 at a design frequency of 220 GHz. These are the transistor sizes used in the LNAs presented in Section 7.5. Vertical demarcation lines are placed where Rollett's k factor indicates unconditional stability.

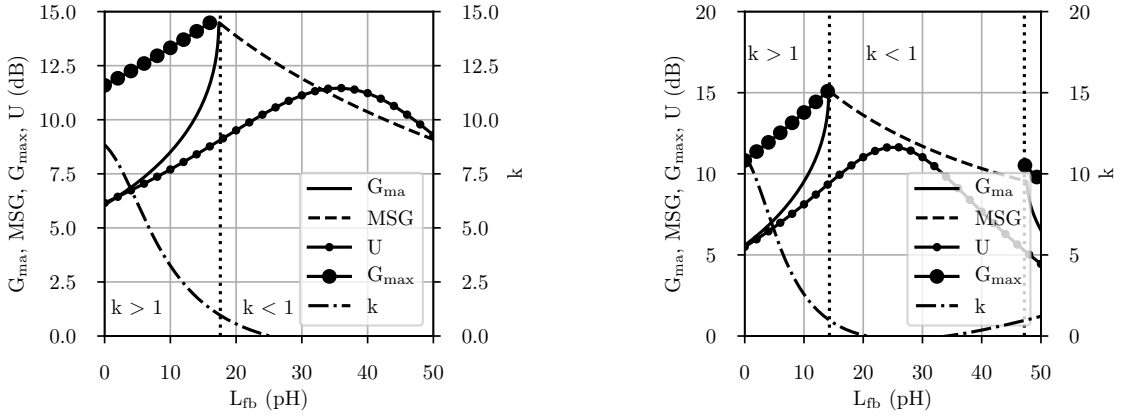
As L_{fb} is applied to the common-base transistor *within* the analysed two-port, U is not perceived as an invariant, but increases with larger L_{fb}. Therefore, G_{ma} becomes MSG and converges with G_{max} at k = 1. After this point, the cascode is no longer unconditionally stable, as the load stability circle moves into the Γ_L plane [107].

As is typical for series-series feedback, increasing L_{fb} reduces the output impedances of the cascode. This may be particularly critical for bandwidth considerations.

The choice of the absolute size of L_{fb} therefore depends on a multitude of factors. As is apparent in Fig. 7.4, the slope of G_{ma} is non-linear with L_{fb} and G_{ma} rises rapidly as it approaches G_{max}. At the same time, k drops. To preserve amplifier stability despite simulation model and manufacturing imperfections, in the presented LNAs L_{fb} was chosen conservatively to only compensate the around 2 dB lowered G_{ma} due to J_{opt} biasing. Rigorous EM-modeling of L_{fb} is mandatory. The influence of L_{fb} on NF_{min} and Z_{opt} is negligible.

The standard formulas for simultaneous conjugated matching as discussed in [86] provide values for input, output and interstage matching elements. The inherent loss at high frequencies of integrated matching elements like transmission lines reduces the achievable gain, but aids the preservation of circuit stability. Thus it is recommended not to compensate for the losses of matching elements by further increasing the feedback.

As a last step, every single amplifier stage on its own and all amplifier stages together are simulated not only in the desired frequency-band of operation, but over the whole frequency range, to ensure stability.



(a) (b)

Figure 7.4.: Simulated influence of L_{fb} on G_{ma}, MSG, G_{max} and U for a pseudo-differential cascode transistor core in (a) SG13G2 with two unit cell sizes at 240 GHz and (b) B11HFC technology with 5 µm emitter length at 220 GHz. Vertical demarcation lines are placed, where k = 1.

At this point, an algorithmic design methodology for SiGe based LNAs in the 200 GHz to 300 GHz frequency range can be formulated. The design steps are:

1. Bias the cascode at $J_{opt} \approx$ 4-6 mA/µm^2.
2. Scale the emitter length of the cascode transistors, such that
   - 1/2 Real(Z_S) < Real(Z_{opt}) < 2 Real(Z_S)
   - 1/2 Real(Z_S) < Real(Z_{in}) < 2 Real(Z_S)
3. Design an input matching network without using reactive degeneration, such that
   - $Z_S^* \approx Z_{opt}$
   - $Z_S^* = Z_{in}$

   Use noise circles in the Smith Chart, to judge the impact of deviations from Z_{opt}. Reiterate step 2, if necessary.
4. Apply L_{fb} at the common-base transistor. Due to EM and HBT modelling uncertainties, stay below 1/2 $L_{fb,max}$ of the chosen HBT size.
5. Use the standard formulas for simultaneous conjugated matching of a non-unilateral two-port to determine matching impedances.
6. Design an output matching network, such that $Z_L^* = Z_{out}$. Fit the input matching network to the updated matching impedance.

7. Check single stage stability from DC to f_{max} of the chosen technology.
8. If single stage gain is still insufficient, concatenate multiple stages. Be aware of linearity boundary conditions.

7.4. Gain Charts for S-Parameter Based Feedback Analysis

The gain chart plots the maximum available gain G_{ma} of a two-port against its transfer-parameter, or *measure of non-reciprocity* A and its inverse λ.

$$A = \frac{1}{\lambda} = \frac{S_{21}}{S_{12}} = \frac{Y_{21}}{Y_{12}} = \frac{Z_{21}}{Z_{12}}$$

Inserting A into Eq. 7.1,

$$U = \frac{|A-1|^2}{2k|A| - 2A_{\mathfrak{R}}} \tag{7.5}$$

where $\mathfrak{R}$ denotes the real part.

The relationship between the available gain G_{ma} of a two-port and its unilateral gain U and λ was derived in the aforementioned classic paper [90]. A particularly important boundary condition is $k \geq 1$, because only then the two-port is unconditionally stable and can be conjugately matched simultaneously at input and output.

$$\frac{G_{ma}}{U} = \left|\frac{A - G_{ma}}{A-1}\right|^2 = \left|\frac{1 - G_{ma}\lambda}{1-\lambda}\right|^2$$

In the follow-up paper [93], a normalized gain chart was introduced. It operates in the complex plane of λ under the approximation, that

$$|A| >> 1 \text{ or } |\lambda| << 1$$

For transistors used above 1/3 f_{max} of their respective technology this approximation is no longer applicable. In 2014, [98] first presented an exact formula which does not rely on this approximation. Its derivation can be found in Appendix A.1. Circles of constant G_{ma} in relation to U are found with

$$\left(\lambda_{\mathfrak{R}} - \frac{U-1}{UG_{ma}-1}\right)^2 + \lambda_{\mathfrak{J}}^2 = \frac{U}{G_{ma}} \cdot \frac{(G_{ma}-1)^2}{(UG_{ma}-1)^2}$$

The regions of unconditional stability indicated by Rollett's stability factor k are found from

$$K = \frac{(\lambda_{\Re}^2 + \lambda_{\Im}^2) + (2(U-1)\lambda_{\Re}) + 1}{2U\sqrt{\lambda_{\Re}^2 + \lambda_{\Im}^2}}$$

which is derived from 7.5 in Appendix A.2.

Fig. 7.5 shows a gain chart for an exemplary two-port with an unilateral gain U of two. The region, where k first takes on a value larger than one has a tear-drop shape. Increasing values of k are marked in darkening shades of blue, with a k of 2 returning to white colour around the origin of the graph. k approaches infinity at the origin of the graph, where the analysed two-port has a G_{ma} of exactly U. When any specific constant-G_{ma} circle intersects the real axis on the left hand side of the graph, it reaches its highest value of k. Thus, any two-port is maximally stable for a conceived value of G_{ma}, if its measure of non-reciprocity A or its inverse λ has no imaginary part and a negative real part.

Constant G_{ma} circles are drawn in green for $G_{ma} = U$, in red for $G_{ma} = 1.25U$ and purple for $G_{ma} = 2U$. An important detail is required for the correct understanding of this gain chart: The constant G_{ma} circles tangentially intersect the k = 1 boundary. From these points onwards, the next constant G_{ma} circle representing *lower* G_{ma} takes precedence.

The absolute maximum power gain G_{max} is found on the left-most point of the real-axis for k = 1. It is marked in all further presented graphs as a black dot.

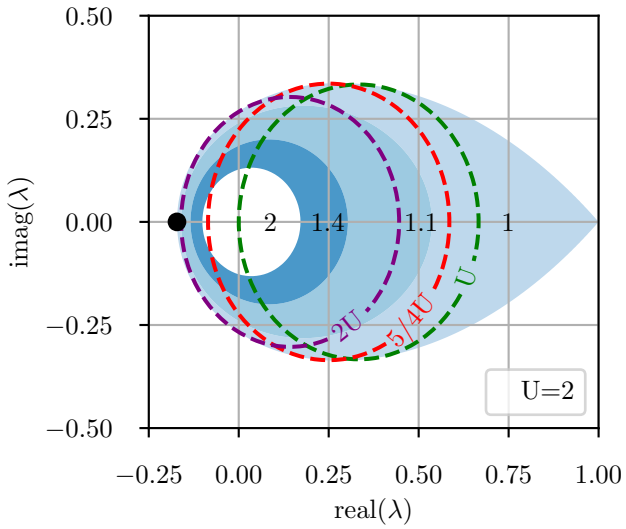


Figure 7.5.: Gain chart for an unilateral gain U of 2. The blue filled contours show for which λ the stability factor k has a constant value of 1, 1.1, 1.4, 2 or above. The coloured circles show a constant G_{ma}. Mason's unilateral gain U lies at the origin. The black dot at the leftmost point of the k = 1 contour marks the location of the absolute maximum gain G_{max}.

Fig. 7.6 shows gain charts for pseudo-differential cascodes in SG13G2 at 240 GHz and B11HFC at 220 GHz with the same transistor sizes as used in the original methodology.

The reader may note the scaled axis in comparison to Fig.7.5. The red dot marks the current value of G_{ma} in the λ-plane. The top graphs show, that the cascodes in the respective technologies are nearly unilateral, if no feedback inductor is employed, marked by the red dot near the origin of the graph. As expected from Fig. 7.4, G_{ma} progressively approaches the black dot of G_{max} with increasing value of L_{fb}. But, due to U of the examined two-ports increasing with L_{fb}, the area encompassed by the constant-k stability boundaries shrinks. This indicates reduced robustness against changes of λ caused for example by manufacturing spread.

At the same time, this shows why there is no "normalized gain chart", as envisioned by Singhakowinta and Boothroyd, for transistors used above 1/3 of their f_{max}: With $U < 10$, the gain chart changes its shape depending on U of the examined two-port.

In the middle graph of Fig. 7.6b, a L_{fb} of 8.3 pH applied to the 5 µm B11HFC cascode achieves a near maximum k for $G_{ma} = 1.25U$, with the red dot intersecting the real axis and on the red circle.

With $G_{ma} = 2U$ in the bottom graphs, three other points become clear: First, [98] rightfully states, that since G_{max} is achieved only on the edge of unconditional stability, it can hardly be a practical design target. Second, observing the progression of G_{ma} (marked with the red dot) through the λ-plane, series-series feedback at the common-base transistor of a cascode is not the optimal way to achieve G_{max}. It approaches G_{max} not by staying on the real axis, but λ has an imaginary part, therefore G_{ma} lies closer to the edge of the k = 1 contour and the slightest deviation of λ might lead to instability. And third, when L_{fb} pushes G_{ma} to G_{max} at the k = 1 boundary, no additional outside embedding of the cascode two-port can increase G_{max} further. Thus, the original methodology from [89] and the even older, but only recently popular theory of lossless reciprocal embedding of two-ports converge for the extreme point of G_{max}.

At first glance it might seem that using series-series feedback at the common-base transistor of the cascode produces superior G_{max} than just embedding the basic cascode in a lossless, reciprocal four-port network. But this is only the case because the embedding in the original methodology happens *within* the analysed two-port. Indeed both design approaches rely on trading off stability for gain. The gain chart allows a more intricate analysis of this trade-off.

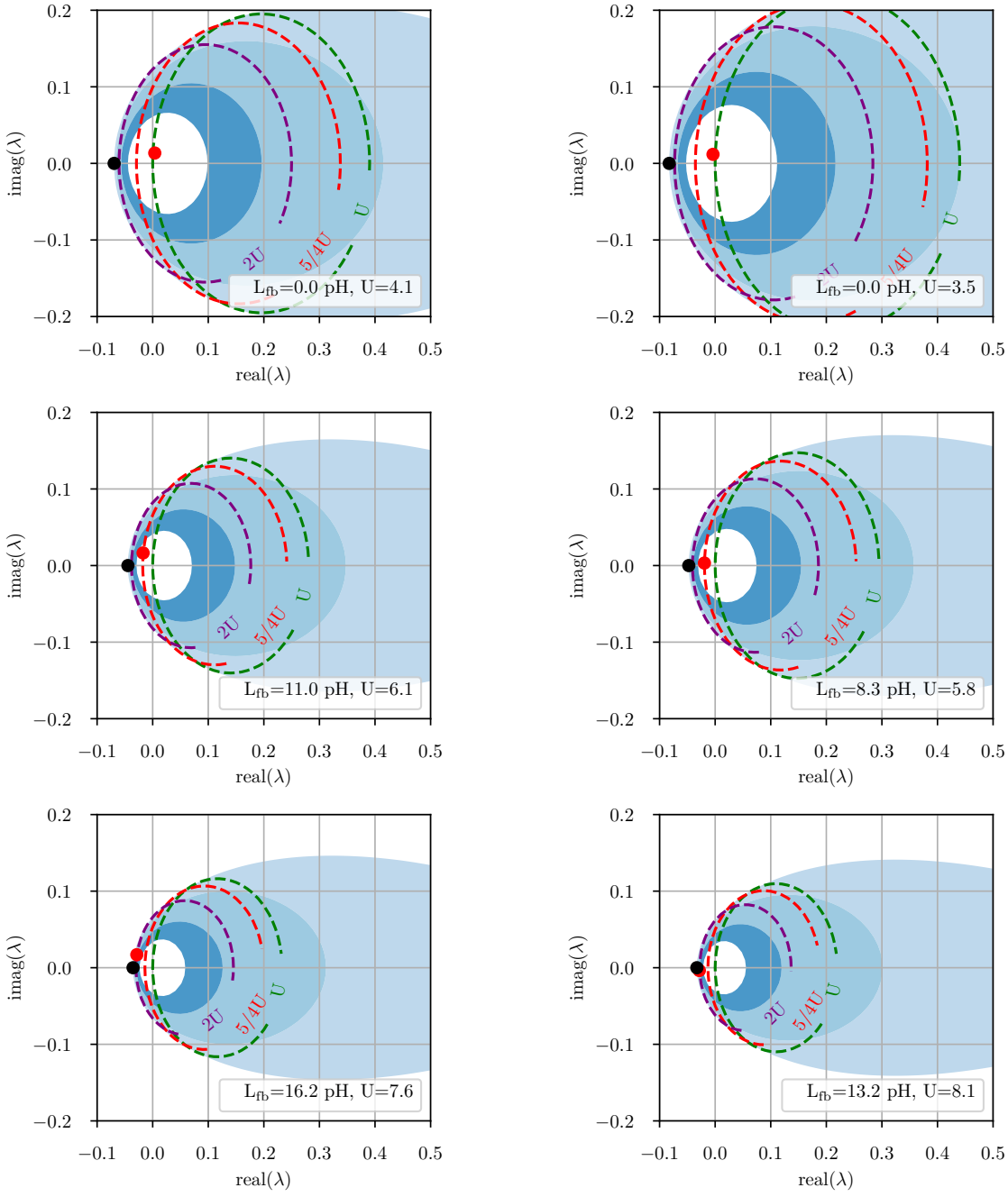


Figure 7.6.: Gain charts for different values of L_{fb} for pseudo-differential cascodes in (a) SG13G2 at 240 GHz (b) B11HFC at 220 GHz. The red dot marks the design point. Top: The cascodes are nearly unilateral, if no feedback inductor is applied. Middle: $G_{ma} = 1.25U$. Bottom: $G_{ma} = 2U$.

7.5. Circuit Architecture and Measured Results

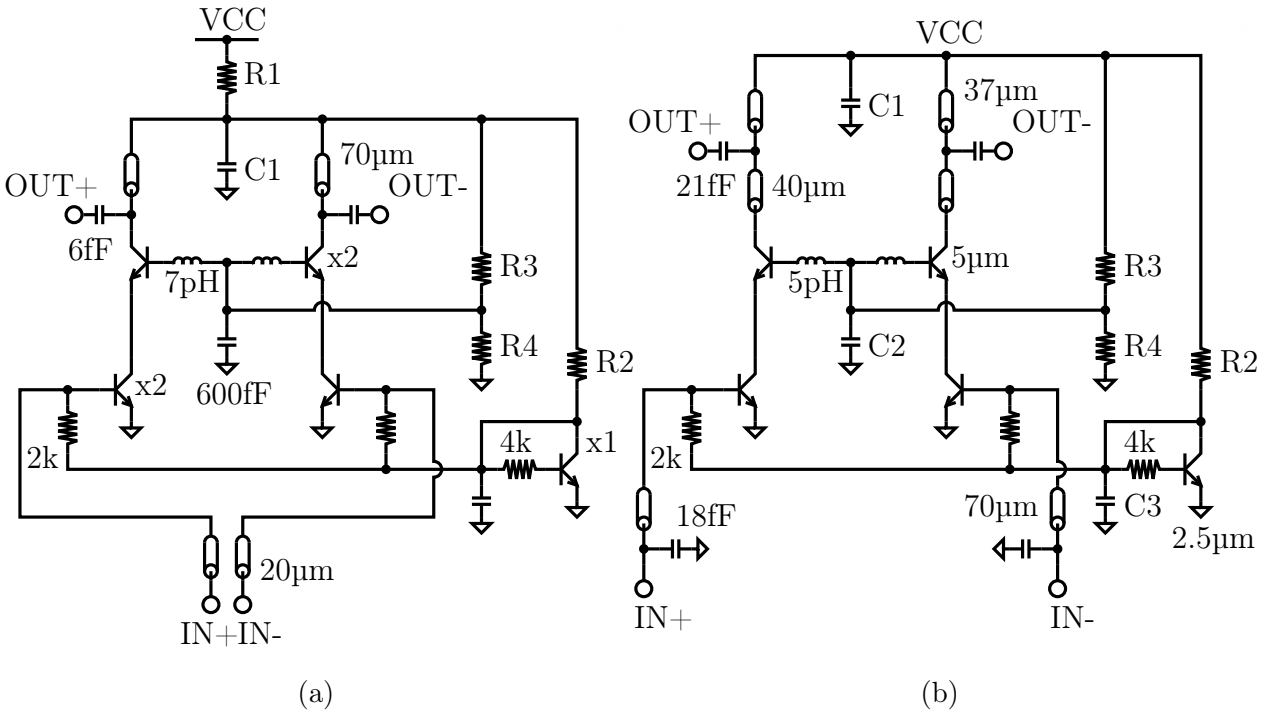


Figure 7.7.: Single stage circuit schematic of the LNA designed in (a) IHP's SG13G2 and (b) Infineon's B11HFC technology. In both, an inductor at the base of the common-base transistor is used for gain-enhancement.

To demonstrate the potential power and reliability of the presented design methodology, two amplifiers in technologies from different foundries have been designed. This section presents their circuit architecture and measurement results. A block-level representation of both amplifiers is shown in Fig. 7.8a, including the Marchand baluns and the tuned pads for on-wafer probing. Fig. 7.8b presents their micrographs.

Full-wave electromagnetic simulation results from HFSS of the transmission lines and interconnects were included as S-parameter blocks in the simulation during the design phase. In the single amplifier stages, the layout of all elements relevant at higher frequencies is completely symmetrical. This also includes all parasitics, which are due to inter-transistor connections or vias to the transmission lines and capacitors. These parasitics are incorporated into the simulation post-layout as S-parameter blocks to analyse their influence on circuit performance.

Both amplifiers consist of four concatenated pseudo-differential cascode stages. Standard resistive biasing is utilized for the cascodes in both cases. The bias network of the common-emitter transistor consists of a current mirror with a resistive connection to the base of the transistor. The resistor has a value of 2 kΩ, which is high enough for the current mirror to not compromise the noise figure of the amplifier. The transistor employed in the current mirror is of half the size of one cascode transistor. Thus the 4 kΩ resistance at the base of the current mirror transistor compensates for the smaller base current. The common-base

transistors in the cascodes are supplied through simple voltage divider with a high frequency short circuit to ground provided by MIM capacitors with a cumulative value of 600 fF.

To avoid the influence of via parasitics, a thin strip of metal on the lowest layer of both processes forms the small feedback inductor L_{fb}. During the design period, this metal-strip has been modelled as a shielded transmission line. Its impedance and length have been adjusted to provide high gain while maintaining circuit stability within the available transistor parameters. Simulation predicts unconditional stability for both amplifiers over the entire frequency range from 1 GHz to 300 GHz.

To use single-ended 50 Ω probe contacts for on-wafer measurements, Marchand baluns were added to both input and output. They transform the probe contact impedance to differential 100 Ω. In both technologies, these baluns are implemented with a coupled transmission line structure in the uppermost thick metallization layer with a 2.4 µm conductor width and a spacing of 2.4 µm, arranged in a rectangular loop of 360 µm length. A single balun has an EM-simulated loss of 1.5 dB. Ground-signal-ground (GSG) pads were added to the single-ended output of the baluns. A short grounded transmission-line stub compensates the capacitance of the contact pad at 240 GHz. To determine the characteristics of the amplifiers for differential in-system usage, it is necessary to de-embed the balun-plus-pad combinations on both sides of an amplifier. For that purpose, a breakout structure of two balun-plus-pad combinations were placed back-to-back in both technology runs.

Both amplifiers were characterized using GSG waveguide probes for the 220-325 GHz band by GGB, OML millimeter-wave VNA extender modules and an Agilent E8361A network analyzer. A schematical representation measurement setup was previously shown in Fig. 4.10. As extracted from the back-to-back breakout structures the measured average loss of the pads and baluns is around 2.5 dB per side from 200-280 GHz in both technologies.

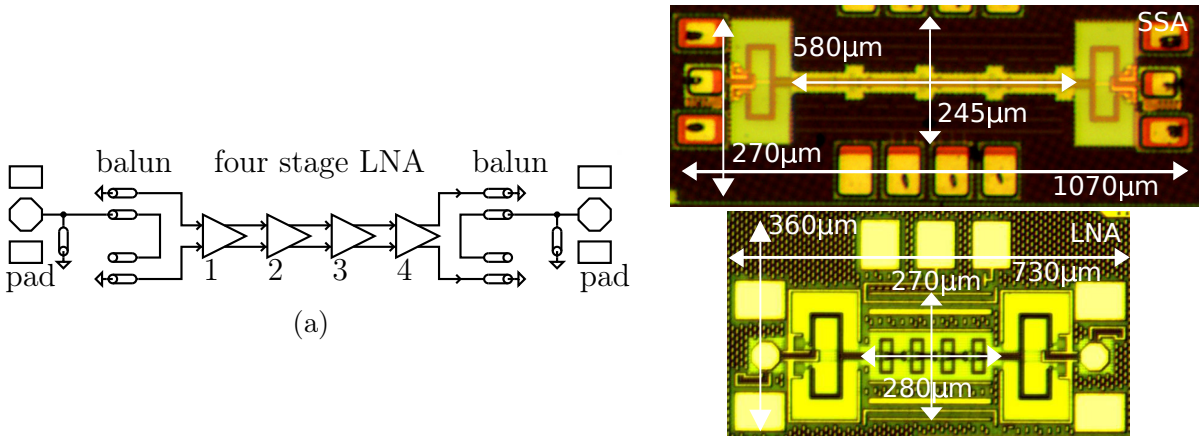


Figure 7.8.: (a) A block-level representation of both amplifier architectures. Each amplifier consists of four equal, pseudo-differential stages connected in series, with Marchand baluns and tuned pads on both ends. (b) Top chip micrograph: LNA breakout in B11HFC technology with (1070 × 270) µm^2 area. Bottom chip micrograph: LNA breakout in SG13G2 technology with (730 × 360) µm^2 area.

7.5.1. LNA in SG13G2

The low noise amplifier is fabricated in IHP's 0.13 µm SiGe BiCMOS technology SG13G2, which is described in 1.5.1.

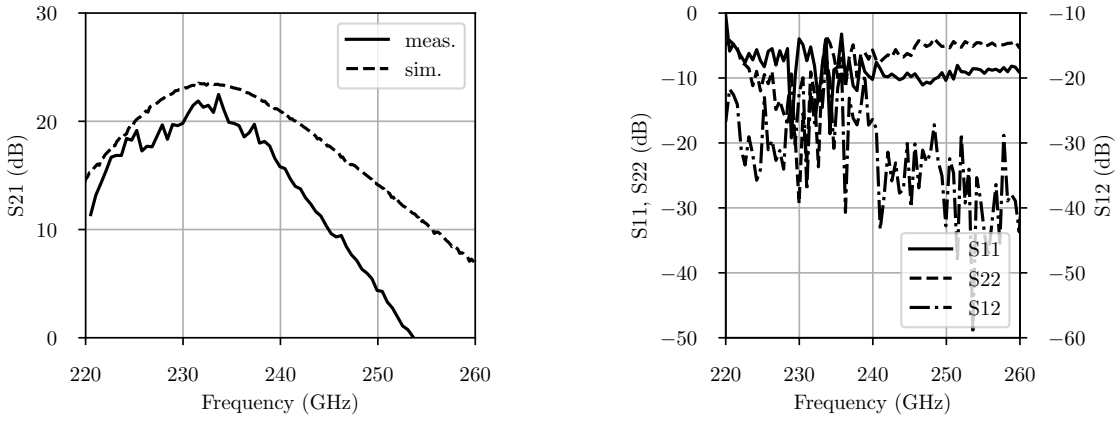
Fig. 7.7a shows one of the four identical concatenated pseudo-differential cascode stages used in this amplifier. To obtain an optimum noise match to a differential 100 Ω source impedance, the emitter-length of bipolar transistors is scaled by connecting two unit cell devices in parallel, resulting in a total emitter area per transistor of $A_E = 2\times$ (0.12× 0.96) µm^2. Their current density is set for minimum noise.

For this technology, bias point and transistor size, the effective inductance of the feedback inductor L_{fb} is chosen as determined in the design methodology section to be 7 pH. Post-layout EM-simulation shows a quality factor of 4 for this inductor.

A 70 µm long microstrip transmission line in the uppermost metal layer supplies each side of the differential cascode structure. DC-blocking MIM capacitors with a value of 6 fF each complete the output match to differential 100 Ω. Input matching is done with a 20 µm coupled transmission line.

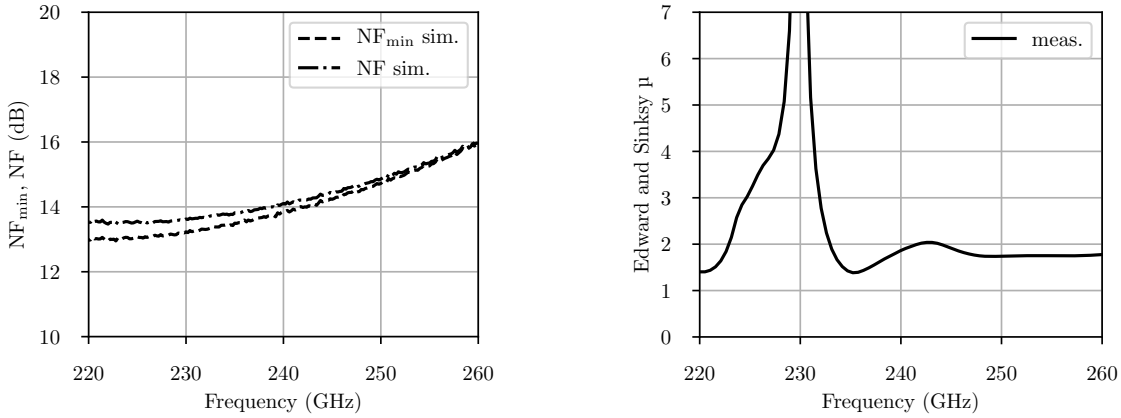
A filter network composed of R1 and C1 minimizes potential common mode instability due to coupling between the stages through the shared power supply connection [108].

All four stages of the low noise amplifier draw a total of 17 mA current from a 4 V supply. The output referred 1 dB compression point of this four stage amplifier was simulated to be -10.9 dBm. The circuit itself is 270 µm × 280 µm in size; each balun adds another 130× 240 µm^2 and the pads increase the break-out length by 95 µm. A circuit micrograph can be found at the bottom of Fig. 7.8b.



(a) (b)

Figure 7.9.: (a) Measured and simulated small signal gain of the low noise amplifier in IHP technology. The measured data includes the baluns and tuned RF pads at the input and output, the simulated data includes balun losses only. (b) Measured reverse isolation and reflection coefficients of the four-stage LNA including baluns and pads.



(a) (b)

Figure 7.10.: (a) Simulated NF_{min} and NF of the LNA in SG13G2. (b) Measured stability factor μ for the four-stage IHP amplifier breakout, indicating unconditional stability.

Fig. 7.9a presents the measured and simulated small signal gain S_{21} for the SG13G2 LNA. The four-stage amplifier has 22.5 dB maximum gain at 233 GHz. The 3-dB bandwidth is 10 GHz. Correcting for pad and balun losses, the LNA has a net gain of 27.5 dB for differential in-system usage, e.g. to drive a mixer directly from an on-chip differential antenna. The input and output return losses S_{11} and S_{22} are plotted in Fig. 7.9b, together with the reverse isolation S_{12}. The Edwards & Sinsky stability factor shown in Fig. 7.10b, which is calculated from the measured S-parameters, indicates unconditional stability over the whole measured frequency range.

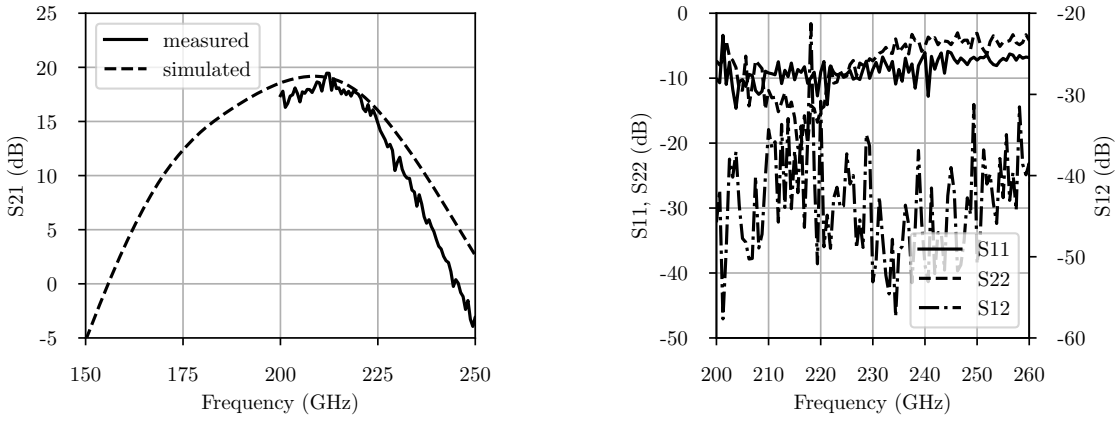
Because of limitations in measurement equipment, specifically the unavailability of a high frequency noise source and a fundamental J-band mixer, the actual noise figure has not been measured. Instead Fig. 7.10a presents the simulated NF_{min} and NF. The noise figure at the peak gain frequency is 13.7 dB. The difference between NF and NF_{min} is below 1 dB over the simulation range.

7.5.2. LNA in B11HFC

Infineon's 0.13 µm SiGe BiCMOS technology B11HFC as described in 1.5.2 is the basis for the second presented LNA.

Each of the four concatenated stages of the LNA consists of a pseudo-differential cascode as presented in Fig. 7.7b. In this technology, the emitter length of the device is freely adjustable. The transistors use an emitter length of 5 µm. The transistors are biased for optimum noise current density. The ensuing lowered gain is then mitigated through the use of the described series-series feedback method. The applied feedback inductor L_{fb} has 5 pH of effective inductance, while featuring a post-layout EM-simulated quality factor of 9.

Input impedance matching to a differential 100 Ω reference is done by an L-match consisting of a 18 fF MIM capacitor and a 70 µm transmission line. The output match is provided by a T-match with a 40 µm transmission line at the collector of each common-base transistor, a 37 µm transmission line as a short circuit stub to the supply and a 21 fF DC blocking MIM capacitor. The amplifier uses an area of 580 µm × 245 µm; baluns and pads add to that resulting in an overall area consumption of 1070 µm × 270 µm.



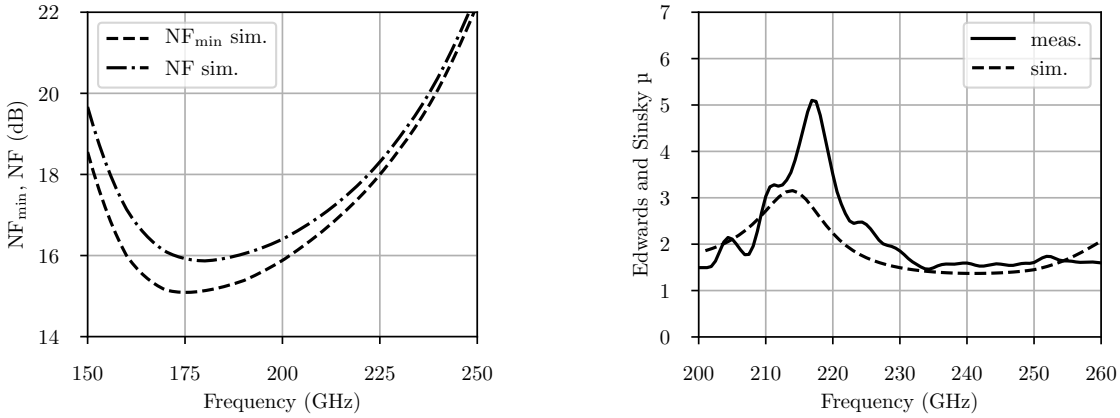
(a) (b)

Figure 7.11.: (a) Measured and simulated small signal gain of the amplifier in Infineon technology in comparison. The measured and simulated data both include the baluns and tuned RF pads at the input and output. (b) Measured reverse isolation and reflection coefficients of the four-stage Infineon LNA including baluns and pads.

The small signal amplifier in Infineon's B11HFC technology has 19.5 dB of gain at 212 GHz with a measured 3-dB bandwidth of 21 GHz, see Fig. 7.11a. If the pad and balun losses are deembedded, the gain is 5 dB higher and comes out at 24.5 dB. Measurement equipment limits the accurate determination of the bandwidth on the lower side, as the probes and OML modules are only specified between 220-320 GHz. The amplifier draws a total of 65 mA from a 3.3 V supply. A saturated output power of 0 dBm was measured using a VDI AMC378 high-power source and an Ericksson PM4 calorimeter.

The simulated noise figure at the peak gain frequency is 17.1 dB, which is 0.4 dB higher than NF_{min} at this point.

Unconditional stability is attested through the Edwards & Sinsky stability factor µ, which is above unity in the whole measured frequency range, as can be found in Fig. 7.12b. The reverse isolation is around -30 dB in the frequency band of interest, as shown in Fig. 7.11b.



(a) (b)

Figure 7.12.: (a) Simulated NF_{min} and NF of the LNA in B11HFC. (b) Measured stability factor μ for the four-stage Infineon amplifier breakout, indicating unconditional stability.

7.6. Chapter Conclusion

This chapter used two approaches to analyse the deliberate use of feedback for gain-enhancement to achieve high gain above 200 GHz. A "gain chart" allows further insights into the original design methodology for low noise amplifier design first published in [89], but has its own limits, which were also discussed. Two low noise amplifiers in the B11HFC technology from Infineon and the SG13G2 technology from IHP employing feedback were presented in [89]. Table 7.1 lists, to my best knowledge, all LNAs in SiGe technology in the 200 GHz to 300 GHz frequency range published at the time of this writing. The B11HFC LNA has the highest gain per stage and total gain ever published in its technology. The SG13G2 LNA has the second highest gain per stage compared to other work in the same technology, but also the largest total gain, even 5 years after its initial publication.

Ref.	Technology Node f_T/f_{max} (GHz)	Freq. (GHz)	Topology	Gain (dB)	3-dB BW (GHz)	NF (dB)	P_{DC} (mW)	Area (μm^2)
[109]	SiGe 0.13 µm 280/425	245	4 stage sing. CB	12 (p)	26	11.3 (s)	28	420 × 460
[88]	SiGe 0.13 µm 280/435	210	3 stage diff. casc.	14 (p)	28	13 (s)	151	385 × 155
[110]	SiGe 0.13 µm 280/435	245	5 stage diff. casc.	18 (p)	8	11	82	360 × 430
[111]	SiGe 0.13 µm 300/450	200	2 stage sing. casc.	16.9 (p)	44	9.4 (s)	18	240000
[89]	SiGe 0.13 µm 280/370	212	4 stage diff. casc.	19.5 (p) 24.5 (d)	21	17.1 (s)	214.5	580 × 245
[89]	SiGe 0.13 µm 300/450	233	4 stage diff. casc.	22.5 (p) 27.5 (d)	10	13.7 (s)	68	280 × 270
[112]	SiGe 0.13 µm 300/500	220	4 stage diff. casc.	21 (p)	6	13 (s)	234	940 × 730
[49]	SiGe 0.13 µm 300/450	210	4 stage sing. CB	10 (p)	55	10.5 (s)	16.8	800000
[113]	SiGe 0.13 µm 300/500	190	5 stage sing. CE + CB	24.7 (p)	16	9.2 (s)	37.2	800 × 600
[114]	SiGe 0.13 µm 350/500	260	3 stage diff. casc.	15 (p)	16.5	13 (s)	112	300 × 160

p: probing, d: baluns and pads deembedded, s: simulated

Table 7.1.: Comparison of mm-wave LNAs

8. Conclusion: A 140 Gbit/s Radio Front-End

8.1. Contributions to the State-of-the-Art

This thesis presented a 240 GHz silicon integrated radio-front end that is capable of a data-rate of 140 Gbit/s in a commercially available 0.13 µm SiGe BiCMOS technology. At the time of this writing, this is the highest data-rate ever published on a purely electronic wireless link, regardless of the used technology. Key system and circuit level challenges were identified in Chapter 2 and addressed throughout the component and packaging design process, to achieve this exceptional performance.

The design of a new ×8 frequency multiplier chain for a carrier generation at 240 GHz was presented in Chapter 3. In the first two frequency doubler stages, a balanced input common-base transistor core is biased in class-B. To supply the differential drive signal, miniaturized passive baluns were designed. The differential output ports of these baluns share a common-mode node, which enables a novel harmonic tuning technique. By short circuiting the 2nd harmonic in the common mode, without affecting the fundamental propagating in differential mode, this technique is uniquely useful in increasing the conversion gain of a balanced class-B frequency doubler.

The last frequency doubler is based on the Gilbert cell. By generating the correct phase offset between the transconductance pair and the switching quad, the conversion gain of this type of frequency doubler is increased for low input power levels. Additionally, this phase offset optimizes the spurious harmonic suppression of the Gilbert frequency doubler, both in the common and differential mode.

The overall ×8 multiplier chain was characterized on-wafer and delivers state-of-the-art 2 dBm saturated output power at 221.5 GHz with a 36 GHz 3-dB bandwidth. The spurious harmonic content was measured in the differential mode through an on-chip balun. The spectrally closest spurious harmonics are the 7th and the 9th, whose power is 54 dB below that of the wanted 8th harmonic.

Additionally, with its 30 GHz input, the new multiplier chain places the local oscillator frequency outside of the baseband bandwidth. This solves the issue of the LO leaking into the baseband outputs at the receiver, which had set an upper limit to the usable baseband bandwidth in the previously reported first generation chip-set.

To further explore the capabilities of the Gilbert cell frequency doubler topology with optimized phase alignment between transconductance pair and switching quad, a second ×8

multiplier chain was designed in a slower 0.13 µm SiGe HBT technology. The three stages of the multiplier chain solely employ the described Gilbert doublers and achieve a peak saturated output power of -7.7 dBm at 244.5 GHz with a 3-dB bandwidth of 81 GHz. This is the highest bandwidth of a multiplier chain ever reported within the 200 GHz to 300 GHz range and covers 60 % of the assigned carrier frequencies of the IEEE 802.15.3d-2017 standard for high data rate wireless multi-media networks.

To increase the bandwidth of the transmitter, a novel, single-ended input up-conversion micromixer was presented in Chapter 4. Its input stage provides wideband baseband matching, high linearity and a 3-dB RF bandwidth of 38.5 GHz. In the receiver, the baseband output current of a novel switching quad based down-conversion mixer with a RF 3-dB bandwidth of up to 78 GHz is fed into a differential transimpedance variable gain amplifier with 27.3 dB gain tuning range. The packaging approach of the TX and RX ICs retains this bandwidth, by reducing the bond-wire length with a thin PCB substrate height, two parallel bond-wires per signal. A maximally flat sixth order low pass filter compensates for the remaining bond-wire inductance by partly integrating the filter sections on chip.

The transmitter 3-dB bandwidth then is limited by the front-end power amplifier. A maximum of 22 GHz is achieved with a 240 GHz carrier. The saturated output power of the TX is 3.9 dBm.

Frequency dependent quadrature channel interference stemming from amplitude and phase imbalances in the up-conversion mixer and front-end power amplifier of the transmitter was counteracted by feeding both channels to separate polarization of a dual polarized antenna, improving their isolation by effectively adding a layer of orthogonality between the channels.

The additional channel isolation is sufficient to distinguish the separate data streams in the channels even when the isolation by quadrature is abandoned. The consequence of placing the carrier frequency at the edge of the RF bandwidth of the direct-conversion transmitter is a sideband imbalance, which heavily degrades the channel isolation by quadrature, and in the presented wireless link, reduces the link conversion gain by 5.4 dB. However, the remaining single sideband offers a larger bandwidth for modulation than by placing the carrier at the center of the RF bandwidth in a double-sideband mode would. Placing the carrier at the 225 GHz center frequency of the TX bandwidth leads to 6-dB link bandwidth of 11.5 GHz. With a 240 GHz carrier at the upper edge of the TX bandwidth, the link conversion gain bandwidth is 7.5 GHz larger.

Modulation dependent limits on the error vector magnitude for an error free transmission were discussed in Sec. 1.4. A communication test of the presented silicon integrated front-end over a 60 cm distance shows that a data-rate of 100 Gbit/s within these EVM limits is possible for all carrier frequencies between 215 GHz and 240 GHz. A maximum data-rate of 140 Gbit/s was demonstrated at a 235 GHz carrier using 32-QAM and at a 240 GHz carrier using 16-QAM. With this maximum data-rate, the wireless link has an energy efficiency of 18.6 pJ/bit.

Furthermore, the design of amplifiers in the 200 GHz to 300 GHz band was discussed. An original design methodology for gain-enhanced cascode amplifiers was derived from S-parameter analysis. For further design insights, a gain chart analysis for feedback in active

two-ports was applied to the gain-enhanced cascode amplifier, which showed the advantages and shortcomings of the original design methodology. Two low noise amplifiers in different 0.13 µm SiGe HBT technologies were then presented to validate the original design methodology.

8.2. Remaining Challenges, Predictions, and Further Ideas

For the successful widespread adoption of sub-THz and THz communication, that goes beyond fixed links in first or last mile applications, beam steering is mandatory. At this point in time, the only pure electronic THz beam steering solutions are injection-locked oscillator based and do not support complex modulation schemes: in [115], a 4-by-4 array of CMOS push-push oscillators radiate at 280 GHz and in [116] standing wave oscillators emit the fourth harmonic at 340 GHz in a SiGe 2-by-2 array.

Power generation at frequencies close to the technology cut-off comes with a greatly reduced efficiency. The high ohmic losses in all tuning elements can only be compensated for with multi-stage amplifiers. Therefore, vector-modulation based phase-shifters are best realized at lower frequencies, possibly before the last LO multiplier stage. Barrie Gilbert's linear-in-dB variable gain cell, which was adapted to the baseband VGA of the switching quad based down-conversion mixer presented in this thesis, can be used without much change in high frequency VGAs.

On the same note, output power and conversion gain of the presented up-conversion micromixer are sufficiently large to consider omitting all but maybe one follow-up power amplifier stage. The resulting extreme compactness and reduction in power consumption could greatly benefit a phased-array implementation.

When considering RF front-ends for frequencies deeper in the THz band, sub-harmonic mixers have proven effective for modulation purposes. There is no reason why square or cubic mixers based on advanced SiGe HBTs should not outperform their CMOS counterparts [37].

How can even higher data-rates than the 140 Gbit/s demonstrated in this thesis be transmitted? Higher order modulation schemes can only be an option if the phase noise floor of the local oscillator can be lowered, as it has the highest contribution to the rms phase error in the carrier generation path. Instead, channel isolation by polarization has proven to be an effective way of circumventing possible front-end impairments. The resulting direct-conversion, single-sideband operation mode uses the available RF bandwidth most efficiently. An improvement could be that instead of using direct-conversion, to implement a single-sideband, two step super-heterodyne up-conversion scheme. The quadrature LO drive of the intermediate frequency could be derived from the carrier frequency generation path to the second mixing stage using area efficient current mode logic.

If the amplitude balance of the front-end components can be improved, the need for an additional layer of orthogonality between quadrature channels disappears. Thus, two completely

separate quadrature data-streams could be transmitted on the orthogonal polarizations of the dual polarized antenna used in the presented chip-set in this thesis. By employing a quadrature hybrid in front of the dual polarized antenna, circular polarization could be implemented and would ease the alignment of the TX and the RX, while retaining polarization diversity.

With the above described system level improvements, data-rates approaching a quarter of a Terabit should be feasible.

The true strength of SiGe HBTs is their co-integration with standard CMOS. This enables the placement of the wireless front-end on the same chip as the baseband processing hardware. This could either be digital or even analog based, which could be vastly more efficient with respect to the high data-rates available from the RF front-end. A definite necessity is the implementation of fast digital-to-analog converters in the TX and analog-to-digital converters in the RX to reduce the bandwidth requirements of the packaging. Recently published DACs already support the required data-rates; currently, the fastest off-the-shelf ADCs support 256 GS/s.

A final observation: specialisation remains crucial. Only co-integration with faster SiGe HBTs or III/V transistors will give low-power CMOS the ability to bring THz communication to every household in the world. Which will happen eventually, as extrapolatable from the historical progression described in Chapter 1.

Appendices

A. Gain Chart Derivation

A.1. Constant-G_{ma}/U Circles

This section derives the formula for generating constant-$\frac{G_{ma}}{U}$ circles in the inverse gain space chart. The end result was presented in [98], but to the authors best knowledge, its derivation has not been published so far.

The gain chart plots the maximum available gain G_{ma} of a two port against its transfer-parameter, or *measure of non-reciprocity* A and its inverse λ.

$$A = \frac{1}{\lambda} = \frac{S_{21}}{S_{12}} = \frac{Y_{21}}{Y_{12}} = \frac{Z_{21}}{Z_{12}}$$

Starting from the relationship between the available gain G_{ma} of a two-port and its unilateral power gain U and λ as derived in the classic paper [90] from Singhakowinta and Boothroyd:

$$\frac{G_{ma}}{U} = \left| \frac{1 - G_{ma}\lambda}{1 - \lambda} \right|^2 \tag{A.1}$$

$$\frac{G_{ma}}{U} \cdot |1 - \lambda|^2 = |1 - G_{ma}\lambda|^2 \tag{A.2}$$

Decomposing the absolute square of λ into its real part $\lambda_{\Re}$ and its imaginary part $\lambda_{\Im}$:

$$\frac{G_{ma}}{U} \cdot (1 - 2\lambda_{\Re} + \lambda_{\Re}^2 + \lambda_{\Im}^2) = 1 - 2G_{ma}\lambda_{\Re} + G_{ma}^2\lambda_{\Re}^2 + G_{ma}^2\lambda_{\Im}^2 \tag{A.3}$$

$$\frac{U}{G_{ma}} - 1 = 2(U - 1)\lambda_{\Re} - (UG_{ma} - 1)\lambda_{\Re}^2 - (UG_{ma} - 1)\lambda_{\Im}^2 \tag{A.4}$$

Dividing with $UG_{ma} - 1$, extending with an extra $1 = \frac{UG_{ma}-1}{UG_{ma}-1}$ and $0 = 2UG_{ma} - 2UG_{ma}$:

$$\begin{aligned}
\lambda_{\Re}^2 - 2\frac{U-1}{UG_{ma}-1}\lambda_{\Re} + \lambda_{\Im}^2 &= \left(1 - \frac{U}{G_{ma}}\right) \cdot \left(\frac{1}{UG_{ma}-1}\right) \cdot \left(\frac{UG_{ma}-1}{UG_{ma}-1}\right) \\
&= \left(UG_{ma} - 1 - U^2 + \frac{U}{G_{ma}}\right) \cdot \frac{1}{(UG_{ma}-1)^2} \\
&= \left(\frac{UG_{ma}^2 - G_{ma} - U^2G_{ma} + U + 2UG_{ma} - 2UG_{ma}}{G_{ma}}\right) \cdot \frac{1}{(UG_{ma}-1)^2} \\
&= \left(\frac{U}{G_{ma}}(G_{ma}^2 - 2G_{ma} + 1) - (U^2 - 2U + 1)\right) \cdot \frac{1}{(UG_{ma}-1)^2} \\
&= \frac{U}{G_{ma}} \cdot \frac{(G_{ma}-1)^2}{(UG_{ma}-1)^2} - \frac{(U-1)^2}{(UG_{ma}-1)^2}
\end{aligned} \tag{A.5}$$

$$\lambda_{\Re}^2 - 2\frac{U-1}{UG_{ma}-1}\lambda_{\Re} + \frac{(U-1)^2}{(UG_{ma}-1)^2} + \lambda_{\Im}^2 = \frac{U}{G_{ma}} \cdot \frac{(G_{ma}-1)^2}{(UG_{ma}-1)^2} \tag{A.6}$$

$$\left(\lambda_{\Re} - \frac{U-1}{UG_{ma}-1}\right)^2 + \lambda_{\Im}^2 = \frac{U}{G_{ma}} \cdot \frac{(G_{ma}-1)^2}{(UG_{ma}-1)^2} \tag{A.7}$$

Eq. A.7 describes the constant-$\frac{G_{ma}}{U}$ circles with their offset on the real axis and their radius.

A.2. Constant-K contours

This section derives the equation for generating constant-K contours in the gain chart. The end result, although with a minor typesetting error, was first presented in [98].

Starting from Eq. 7.5 and inserting A = $1/\lambda$:

$$U = \frac{|A-1|^2}{2K|A| - 2A_{\Re}} = \frac{\left|\frac{1}{\lambda} - 1\right|^2}{2K\left|\frac{1}{\lambda}\right| - 2 \cdot \text{Real}\left(\frac{1}{\lambda}\right)} \tag{A.8}$$

Rearranging the nominator, while multiplying the equation with the denominator:

$$U \cdot \left(2K\left|\frac{1}{\lambda}\right| - 2 \cdot \text{Real}\left(\frac{1}{\lambda}\right)\right) = \frac{|1-\lambda|^2}{|\lambda|^2} \tag{A.9}$$

With $|1-\lambda|^2 = 1 - 2\lambda_{\Re} + |\lambda|^2$ and $\text{Real}(1/\lambda) = \lambda_{\Re}/|\lambda|^2$:

$$2KU|\lambda| - 2U\lambda_{\Re} = 1 - 2\lambda_{\Re} + |\lambda|^2 \tag{A.10}$$

Finally:

$$K = \frac{|\lambda|^2 + 2(U-1)\lambda_{\mathfrak{R}} + 1}{2U|\lambda|} \tag{A.11}$$

Or in the notation from [98]:

$$K = \frac{(\lambda_{\mathfrak{R}}^2 + \lambda_{\mathfrak{I}}^2) + 2(U-1)\lambda_{\mathfrak{R}} + 1}{2U\sqrt{\lambda_{\mathfrak{R}}^2 + \lambda_{\mathfrak{I}}^2}} \tag{A.12}$$

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