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Development and characterization of the Monitoring of Pixel System (MOPS) chip to monitor the ATLAS ITk Pixel Detector

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Abstract

A High Luminosity(HL) upgrade is planned for the Large Hadron Collider (LHC) at CERN, which will increase the originally designed luminosity by a factor of ten. The ATLAS experiment will get a completely new all-silicon Inner Tracking Detector (ITk) by 2026 to work with the new HL-LHC. The ITk consists of a Pixel Detector as the inner and a strip detector as the outer part. The ITk Pixel Detector design comprises five layers and over 10000 readout modules. The new Pixel Detector will use serial powering chains with a maximum of 16 readout modules in a single chain to reduce services inside the detector. A new Detector Control System (DCS) is required to monitor the temperature and voltages across the detector modules for reliable operation and data taking.

Due to the limited space, very stringent radiation requirements, and to reduce the material inside the detector volume, also in the DCS, a newly designed chip is required that can collect the monitoring data locally and send it over a long communication channel to a central station outside the detector volume. This dramatically reduces the number of service lines. The chip must be radiation hard to an ionizing dose of up to 500 Mrad, tolerant to Single-Event Effects (SEE), and requires a wide operational temperature range of -40 °C to +60 °C.

The Monitoring of Pixel System (MOPS) chip is an Application Specific Integrated Circuit (ASIC) that has been developed using the TSMC 65 nm CMOS process to provide the temperature and the voltage monitoring data of detector modules to the DCS. The chip offers 32 ADC channels using the Successive Approximation Register (SAR) based 12-bit ADC. The chip implements Controller Area Network (CAN) and CANopen protocols in a hardwired logic, uses a non-standard low voltage physical layer, and provides additional features like remote reset without a power cycle and automated on-chip frequency trimming using CAN messages. Irradiation studies have been performed to prove Total Ionizing Dose (TID) tolerance of up to 500 MGy and tolerance to Single Event Effect(SEE). The chip has proven to work reliably under irradiation at high operating temperatures of up to 40 °C as well as for an operational temperature range of -40 °C to 60 °C.

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Chapter 1

CERN and the Large Hadron Collider

1.1 Research at CERN and the LHC

Conseil Européen pour la Recherche Nucléaire (CERN) is an international research institute founded in 1954 by 12 member countries. Currently, the CERN provides one of a kind infrastructure to conduct research in high-energy physics. The institute hosts the world's largest high-energy particle collider. Over time, many experiment facilities were built, contributing a tremendous amount of scientific knowledge for humanity. The puzzle of the standard model of elementary particles was partially solved by the discovery of the W boson, Z boson, and Higgs boson. In addition to that, the institute provides the infrastructure to research in extra dimensions and antimatter, etc. Beyond the research in fundamental particle physics, CERN contributes towards the development of future technologies and provides scientists with tools to research; e.g., the World Wide Web is one of the key achievements at CERN, which has revolutionized information exchange. Technologies developed at CERN are used in the medical field to provide diagnoses and therapies and in the space industry to build radiation-hard electronics and tools. Figure 1.1 shows an overview of the complete CERN accelerator complex with all the installed experiment facilities.

The Large Hadron Collider The LHC is one of the largest and most complex machines ever built by mankind. The machine is 100 m under the ground in a circular tunnel with a circumference of approximately 27 km and a diameter of 3.8 m. Protons are acquired by removing electrons from the hydrogen atoms. Shown in Figure 1.1, the protons are then fed into the Booster and subsequently into the Proton Synchrotron(PS) and Super Proton Synchrotron (SPS), where they get accelerated before finally transferring to the LHC. Two proton beams accelerated up to 7 TeV in a counter direction collide at specific points around which the detectors are built to track the trajectories of the particles after a collision. In total, 9600 magnets are used in the LHC to steer and optimize the trajectories of the particles [2]. LHC is designed for a maximum collision energy of 14 TeV, equivalent to 22.4×10^{-7}J. However, it can also be operated using a Lead-nuclei beam, generating even higher collision energy of up to 1150 TeV. Although circular, the LHC is not symmetrical. The whole structure is divided into eight arcs and also eight insertion points. The dipole bending magnets are used in the arcs to guide the beam. Part of the machine lying inside an insertion point is entirely straight and goes through different experiments. It is used

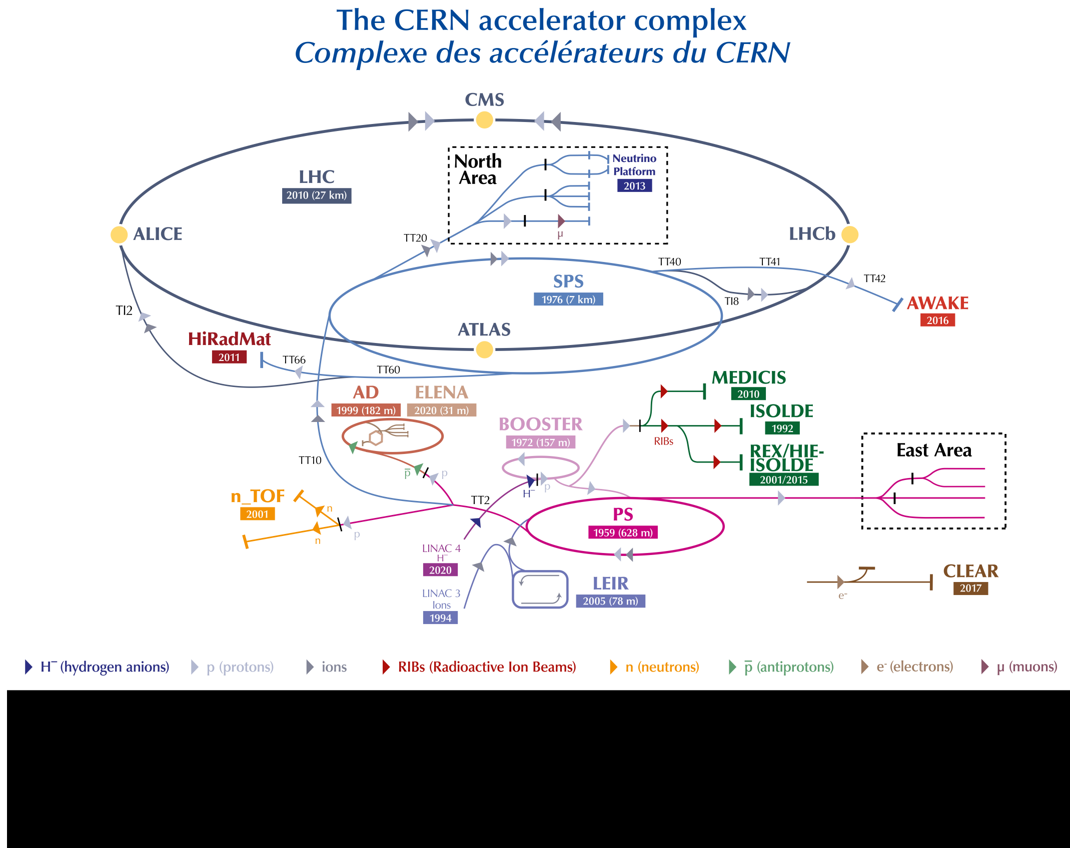


Figure 1.1: The CERN accelerator complex [1]

for dumping, cleaning, and injection of the beam. Combined, this incredible piece of engineering delivers a Luminosity of $1 \times 10^{34}\text{cm}^{-2}\,\text{s}^{-1}$ and up to 1 billion collisions per second [2].

1.2 Experiments running at the LHC

Figure 1.1 shows locations around the ring where the four big experiments and related facilities are installed at the LHC. These are the Compact Muon Solenoid (CMS), Large Hadron Collider Beauty (LHCb), A Toroidal LHC ApparatuS (ATLAS), and A Large Ion Collider Experiment (ALICE). The ALICE experiment is a dedicated machine of 10000 tonnes, 26 m long and 16 m high/wide, to study strongly interacting matters. It uses the lead-nuclei beam at the LHC to study conditions just after the Big Bang. The LHCb is dedicated to researching a particular type of particle called beauty quark to find differences between matter and antimatter. Instead of a single detector centered around a collision point, the LHCb is composed of a series of small detectors placed in a single direction over up to 20 m. The other two large detectors, ATLAS

and CMS, are general-purpose detectors that provide data to study the interaction of the particles. Although doing the same thing, ATLAS and CMS are built differently by two independent collaborations. This allows cross-confirmation of the scientific achievements made by the two experiments. The data from the CMS and the ATLAS is used to study the standard model, dark matter, and extra dimensions [3]. Section 2.1 describes the ATLAS experiment in detail.

1.3 LHC high luminosity upgrade

A high luminosity upgrade is planned for the LHC, which will increase the originally designed luminosity by a factor of 10. The new collider will start its operation in 2029 per the current plan. After several years of operation at 13 TeV, the machine was able to produce $160\,\mathrm{fb}^{-1}$ of data, while after the upgrade, the HL-LHC will produce $250\,\mathrm{fb}^{-1}$ of data per year and $4000\,\mathrm{fb}^{-1}$ of data over its lifetime of 12 years. The upgrade will allow producing a massive amount of collision data compared to the current system, e.g., 15 million Higgs bosons per year can be generated compared to a maximum of 3 million in 2017. To achieve the upgrade capabilities, 24 superconducting magnets made of niobium-titanium will be used with an intensity of 12 T compared to the current 8 T. In addition to that, the fundamental structure of the machine also needs an upgrade, e.g., Crab cavities to tilt the beam, reinforced machine protection to defend against a stray beam, and crystal collimators for better cleaning [4].

Chapter 2

The ATLAS experiment

ATLAS is a general purpose and the largest detector at CERN. Parallel to the CMS experiment, it also studies dark matter, Higgs boson, and extra dimensions. The whole machine is composed of several sub-detectors and built around a center point of collision. The whole detector is symmetric around the interaction/collision point. It is 46 m long, 25 m high, 25 m wide and weighs around 7000 t.

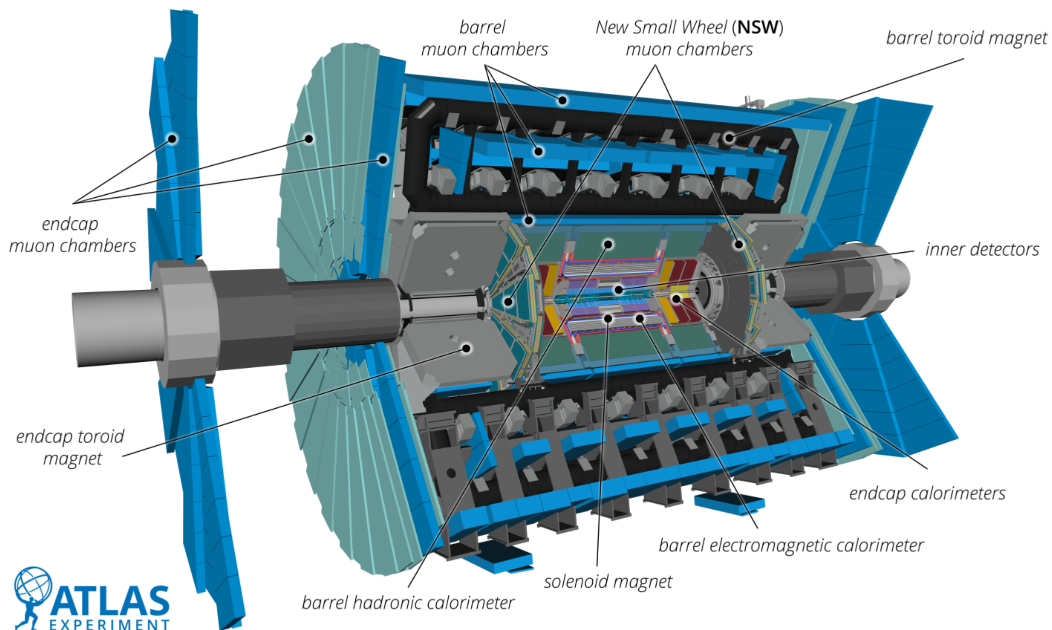


Figure 2.1: The ATLAS experiment [5]

2.1 Overview and sub-detectors of the ATLAS experiment

Figure 2.1 shows the computer-aided design of the ATLAS experiment and its sub-detectors. As shown in Figure 2.2, the center point of collision/interaction is defined as the origin of the coordinate system where the z-axis is used to define the beam direction, the positive x-axis is defined from the interaction point to the center of the LHC, while the positive y-axis is going in the upward direction. The pseudorapidity is defined as $\eta = -\ln\tan(\theta/2)$, where θ is the polar angle from the beam axis [6]. A larger pseudorapidity means closer to the beam pipe, as seen in Figure 2.4. Figure 2.3 shows a visualization of different particles detected inside the sub-detectors of the ATLAS experiment. The whole detector can be categorized into four sub-systems. Starting from the center point and going outward, the first is called the Inner Detector(ID). The second one is the Calorimeter, while the outermost and the third one is called the Muon Spectrometer. The fourth part is the magnetic system, which lies between the detectors to provide bending power. Brief details about each part are mentioned in the following paragraphs.

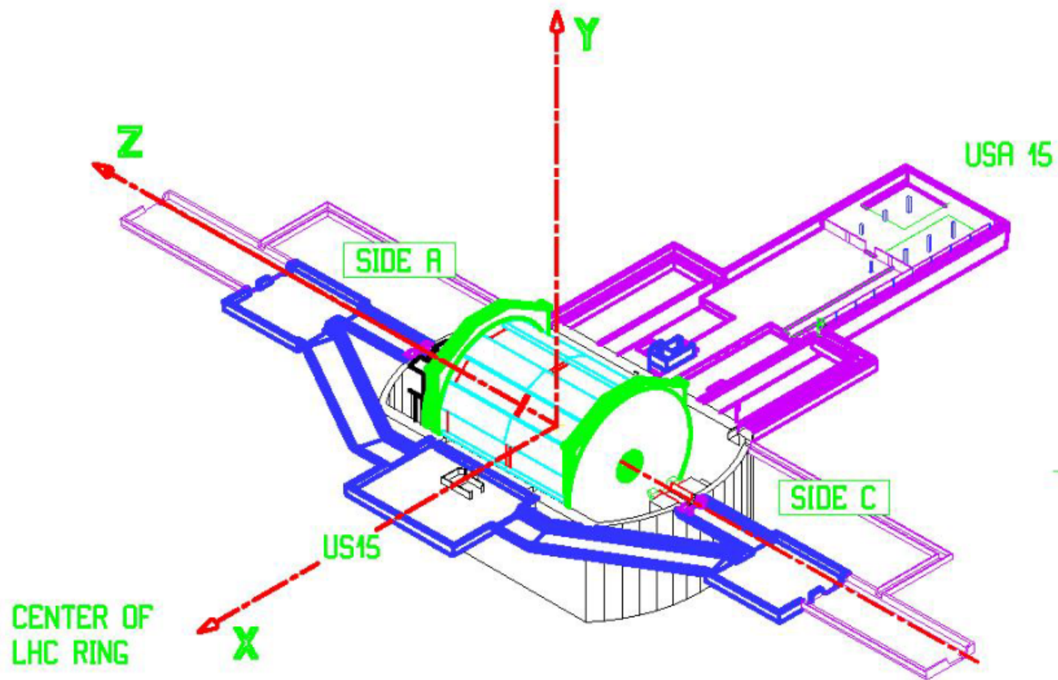


Figure 2.2: ATLAS experiment coordinates [7]

Inner Detector The inner detector(ID) is further divided into three parts: the Pixel detector, the Semiconductor Tracker(SCT), and the Transition Radiation Tracker (TRT). The complete ID is immersed in a magnetic field of 2 T provided by the central solenoid, briefly explained in paragraph 2.1, and can be seen in Figure 2.1.

The ID provides pattern recognition, momentum, and precise vertex measurements for the particles produced by a collision every 25 ns with a pseudorapidity of $|\eta| < 2.5$. This thesis will focus on the monitoring chip for the future Pixel detector. Therefore, the Pixel detector is explained in more detail in section 2.2 [6].

Calorimeter The Calorimeter is made up of two sub-detectors: the liquid argon, an electromagnetic calorimeter, and the hadronic Calorimeter. The Electromagnetic Calorimeter is used to find the energy and trajectory of electrons and photons. It provides a pseudorapidity of $|\eta| < 3.2$. The Hadronic Calorimeter is subdivided into a barrel section and an endcap section. It gives a pseudorapidity range of $|\eta| < 1.7$ and is used for hadron measurements like proton and neutron. Cumulative, the complete Calorimeter provides high granularity and a range of pseudorapidity of $|\eta| < 4.9$ [6].

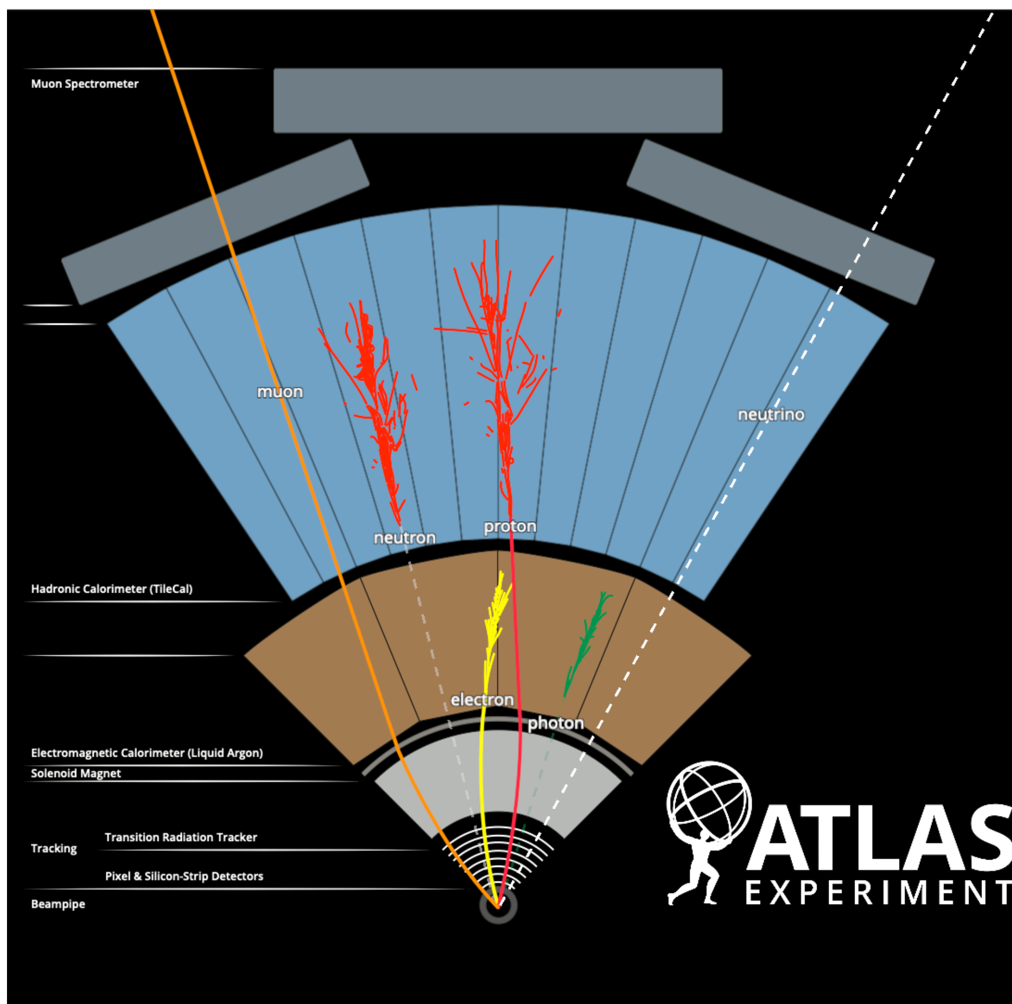


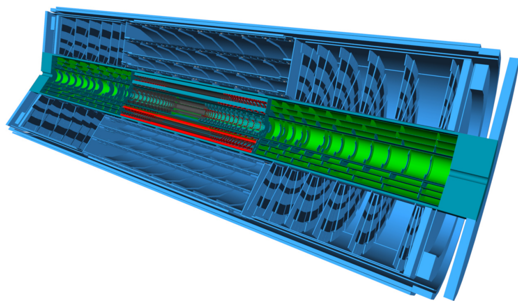
Figure 2.3: Visualization of particles inside the ATLAS's sub-detectors [8]

Muon detector As shown in Figure 2.1, The Muon detector is ATLAS's largest and outermost part. It is divided into an endcap Muon chamber, barrel Muon chambers, and a New Small Wheel (NSW) Muon chamber. The Muon detector detects the momentum and energy of the muon particles, which pass through all the inner detectors without any interaction. The barrel region measures the muon tracks using three cylindrical layers around the beam axis. The endcap chambers have three layers perpendicular to the beam axis on each side. The information generated by the muon detector is also used for the trigger system[6]. New Small Wheel (NSW) endcaps have been integrated recently into the muon spectrometer to cope with the HL-LHC environment and for better resolution [9].

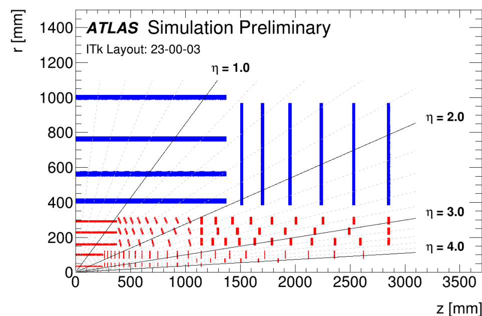
Magnet system The ATLAS experiment has four large superconducting magnets with a combined stored energy of 1.6 GJ. The ATLAS magnet system is divided into two main parts. A solenoid that is cylindrical around the beam axis and provides an axial magnetic field for the Inner Detector (ID). The solenoid magnet can be charged and discharged in just 30 minutes. A barrel toroid and two endcap toroid magnets provide deflection power for the muon detector. The barrel toroid generates a magnetic field of 0.5 T. The two endcap toroids combined produce a magnetic field of 1 T [6]. The whole magnet system is steered and operated in different modes by the ATLAS detector control system, as explained in Chapter 3.

2.2 The ATLAS ITk Pixel Detector

The complete Inner Detector of the ATLAS experiment will be upgraded and replaced by an all-silicon Inner Tracker (ITk) during the Long Shutdown (LS) 3 of the LHC. The upgrade is required to cope with harsher radiation environments of up to a fluence of 2×10^{16} n_{eq}/cm^2 and to provide more precise measurements operating under the HL-LHC. Shown in Figure 2.4(a) is a software-rendered overview of the complete ITk, whereas Figure 2.4(b) shows the layout for one quadrant. The blue lines show the Strip part, whereas the red lines represent the Pixel part of the detector. In this thesis, only details regarding the Pixel part will be discussed because the MOPS chip has been developed to be used only for this part. The new Pixel detector will have five layers surrounding the beam pipe and several layers as rings known as Endcaps. Each layer is loaded with detector modules. A module comprises a sensor to detect particles and a readout chip to communicate data. The whole ITk will cover an instrumented area of $13\,m^2$ with five billion readout channels [10]. The innermost layer is only at a distance of 34 mm from the beam pipe. Because of the radiation damage caused by an ionizing radiation dose of 500 Mrad, the innermost two layers will be replaced after five years of operation [11]. This allows for replacing damaged components due to radiation and integrating the newest available technology. The system will provide a pseudorapidity coverage of $|\eta| < 4.0$. 3D sensors will be used in the innermost layer with a pixel size of 50×50 µm^2 and 25×100 µm^2 whereas planar sensors will be used in the outer four layers with a pixel size of 50×50 µm^2. The planar sensors have a thickness of 100 µm for the second layer and 150 µm for the outer three layers. The readout system will use the ITkpix chip providing 400×384 pixels. Each chip has four readout channels at a rate of 1.28 Gbps. Approximately 10000 modules will be used in the system to host the ITkpix readout chips. The readout chips on the modules are powered in parallel [10].



(a) Software rendered image of the new Inner Tracker [11]



(b) Layout of one quadrant from the point of interaction (origin) [12]

Figure 2.4: The ATLAS Inner Tracker layout

2.3 Serial powering scheme for the detector modules

The new Pixel Detector uses a new serial powering scheme to reduce the material inside the detector volume and decrease cable power losses. The total power loss in the cable should be less than 30 % of the total required power [11]. Figure 2.5 shows the new serial powering scheme. The concept of a serial powering chain has not been used in earlier generations of the detector. The complete chain is powered by a constant current source labeled LV. All the modules hosting the readout chips are connected in series, although the chips themselves are powered in parallel on the modules. According to the Pixel TDR [11], a single chain can have a maximum of sixteen modules, which is reduced to thirteen in the subsequent system planning. Each module can have a maximum of four FrontEnd (FE) chips [13], but a lower number is also used in some chains. Every FE chip is powered using two shunt-LDO regulators [14][15], which provide a constant voltage supply for the chip and can also shunt extra current in the case when the chip is working in the low power mode where the consumption goes down significantly. The shunting capability of the regulator also helps in case one of the FE chips stops working and becomes a high ohmic path. The regulators from the other FE chips can shunt the extra current to the ground. The regulator can shunt the current as high as double the amount during nominal operation. To ensure reliability using the serially powered chain of modules, the modules must be protected against over-temperature and over-voltage conditions. This requires a radiation-hard independent monitoring system. A serial power chain is the smallest unit, which can be controlled individually from the power supplies. In case of over-temperature and over-voltage conditions reported by an independent monitoring system, the problematic modules can be configured so they can be bypassed to prevent loss of the complete chain.

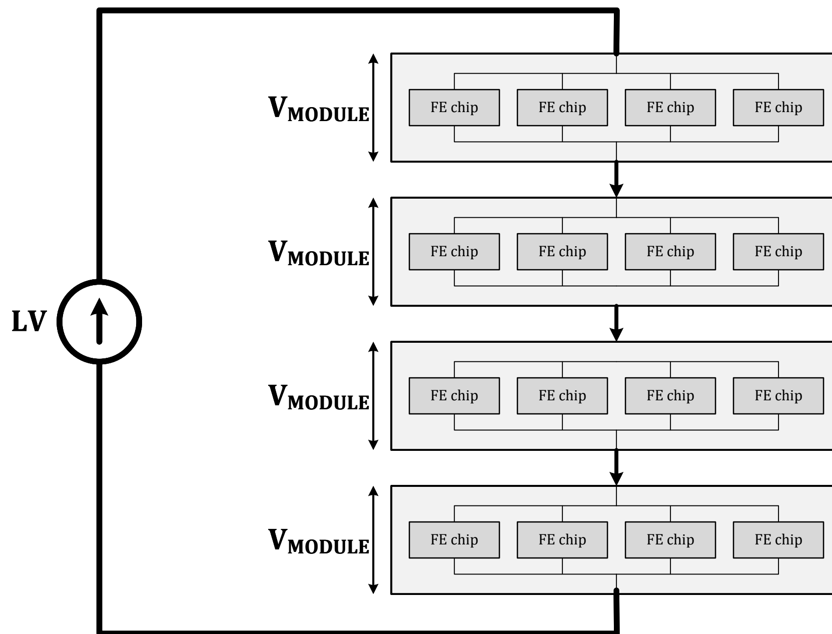


Figure 2.5: Serial powered chain for the ATLAS ITk Pixel detector

Chapter 3

Detector Control System (DCS) for the ATLAS ITk Pixel Detector

A sophisticated Detector Control System(DCS) for the ATLAS ITk Pixel Detector is necessary to ensure reliable data collection and safe operation of the detector itself and the safety of the operating personnel. The DCS monitors parameters like voltage, temperature, and other signals from different sub-systems to assess the experiment's state.

3.1 Requirements for the new DCS system

The system is required not only for nominal operation but also during the commissioning of the new subsystems. The DCS must have independent power and communication links/protocols to ensure that it is available at all times. This allows monitoring, control, and safety of the detector independent of its operational mode or whether the front-end detector modules can communicate.

3.2 Proposed DCS concept of the Pixel Detector

The Technical design report (TDR) of the ATLAS ITk Pixel Detector [11] presents a detailed concept of the DCS. There are three different independent paths for the DCS. They differ in terms of precision, availability, granularity, and reliability. The block Figure 3.1 shows the revised design.

3.2.1 Safety path

The safety path consists of the interlock system and acts as the last line of defense against any critical detector malfunction. The interlock system provides less precision but the highest reliability and availability. The system must be available and ready to act at all times. Figure 3.2 shows the topology of the Interlock system. The input from the temperature sensors is processed by two independent instances inside the interlock crate. The instance FPGA Interlock Matrix processes the information from the temperature sensors using a hardwired logic in a binary way. If the temperature rises above a certain threshold, the system will directly act on the power supplies or any interlock-controlled device. This means that the system is either in a safe

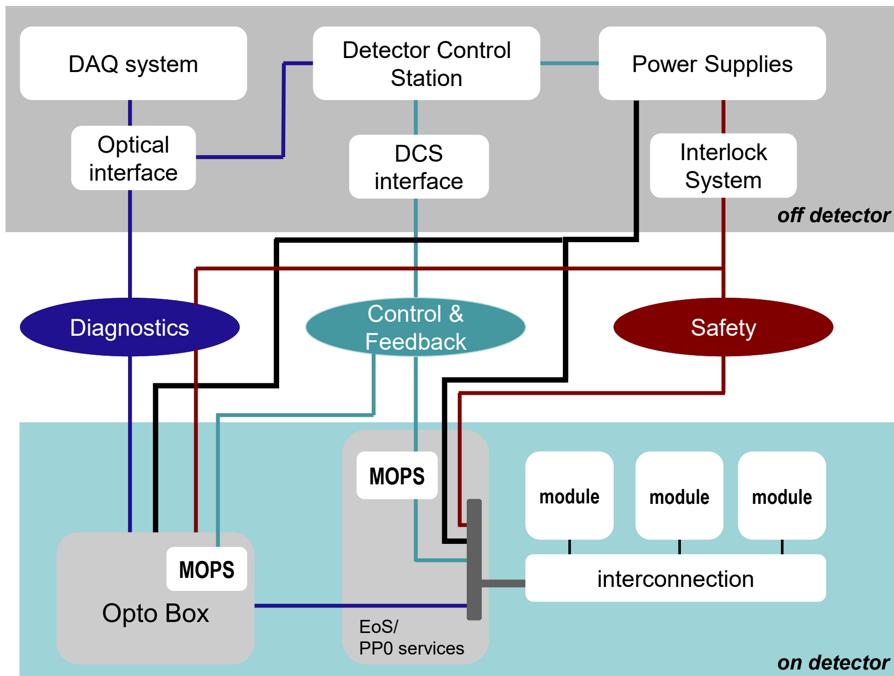


Figure 3.1: Overview of the ITk Pixel Detector DCS [11]

state or not. The same input signal from the temperature sensors is also sampled by an ADC and fed to the Monitoring-FPGA for monitoring and debugging the interlock system. Each module in the serial powering chain hosts an NTC resistor to measure the module's temperature. The interlock system uses one of the several NTC resistors available in a single serial powering chain. This allows the interlock system to have a granularity per serial power chain. The exact location of the Interlock NTC resistors in a serial power chain is different for sub-systems. A simple two-wire readout topology reads out NTC resistors, and all the signals are driven directly to the counting room. In the counting room, a 3U 19-inch crate called Local Interlock Safety System (LISSY) [16] is responsible for receiving and processing all the signals coming from the interlock NTC resistors, as well as it hosts the interlock-FPGA and the Monitoring-FPGA The LISSY are placed inside the counting room to make them safe from radiation effects. The interlock system not only acts on the temperature signals coming from the NTC resistors but also provides the possibility to act on external signals. These external signals can be, e.g., from the cooling plant or the beam interface system for a safer operation. The system acts directly on the power supplies using hardwired logic independent of any software [16][11]. .

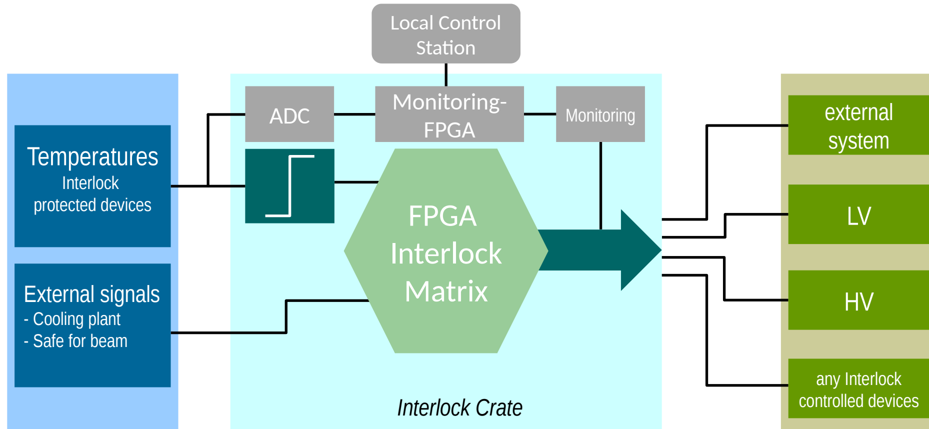


Figure 3.2: Concept of the interlock system used in the Safety path of the ITk DCS [16]

3.2.2 Control & feedback path

Figure 3.1 shows the control and feedback path. The control and feedback path of the DCS provides an operator with an interface to monitor the actual state of the detector and then act accordingly to control sub-detector parts. The control here mainly refers to controlling power to the sub-systems to ensure safe operation and reliable data taking. The power supplies directly provide the control and feedback per SP chain. However, the feedback per detector module is provided by the MOPS chip in the form of the temperature and the voltage of individual detector modules. The MOPS chip is placed on the end of the sub-structure. The control and feedback is a highly reliable system and must also be available when the detector is not running. This sub-system will be used during the commissioning to calibrate and debug services to the detector modules. Another significant feature of this sub-system of the DCS is that it has its own powering and communication lines independent of the serial power chains of the ITk Pixel Detector. This ensures the monitoring feature is available even when the detector is not in regular operation. The interconnection topology between the Monitoring of Pixel System (MOPS) chip and a module in the serial powering chain shown in Figure 3.1 is elaborated in Figure 3.3. The connection between the MOPS chip and the local control station is shown in Figure 3.4. The MOPSHUB is an FPGA-based system aggregating data from the MOPS chip and sending it to the Embedded Monitoring and Control Interface (EMCI)[17]. The EMCI then sends the data over an optical link to the local control station. The Embedded Monitoring Processor (EMP) [17] is responsible for receiving the DCS data on the other end provide it to the DCS server. The control and feedback path requires a refresh rate of 5 seconds [18]. By providing 32 ADC channels, each single MOPS chip can monitor the voltage and the temperature of up to 16 modules in a single serial power chain.

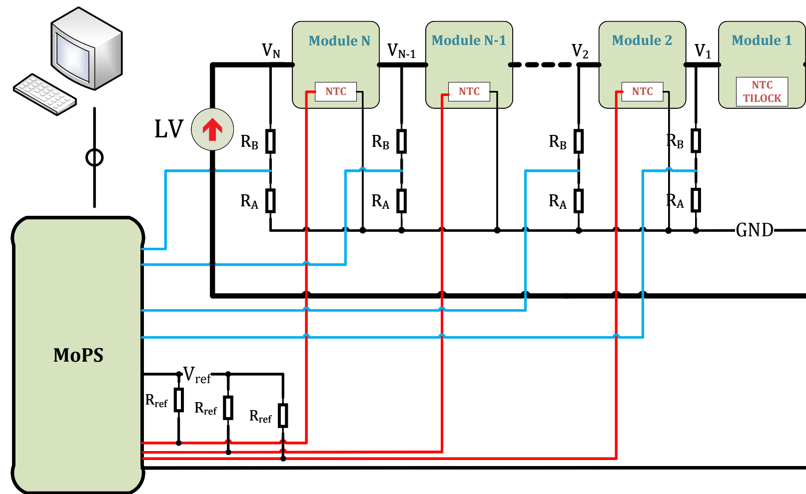


Figure 3.3: MOPS connection with modules in the serial powering chain [19]

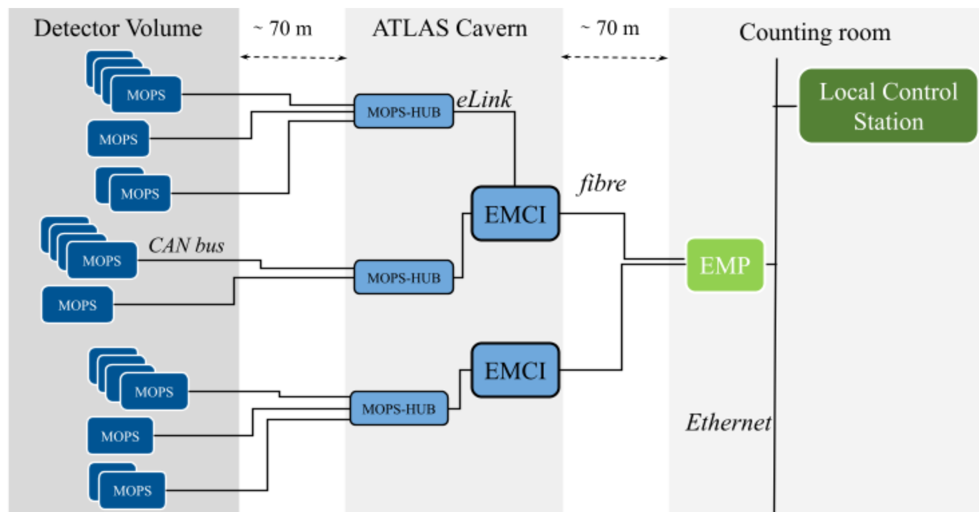


Figure 3.4: Control/monitoring path of the ITk DCS [20]

3.2.3 Diagnostics path

The diagnostics path of the DCS allows for fine-tuning the detector's performance by providing additional monitoring and debug information. Detailed information is collected from each front-end chip and transferred to the central DCS server over the optical links connected to the Opto-box shown in Figure 3.1. The communication channels and data streams of the detector modules are used for this purpose, which means that this additional information is only available when the detector is operational.

3.3 Current monitoring technology and its limitation

In the current system, each module has its own sense lines for voltage and temperature monitoring. All the sense lines are routed outside the detector volume to a point far from the modules, up to 70 m in length. The sense lines are fed into the Embedded Local Monitor Board (ELMB). The ELMB is used at CERN for different experiments and facilities. It is also used in the current ATLAS experiment to provide monitoring data for different sub-detectors [6]. This is a general-purpose board of size 50×50 mm^2 that can be theoretically placed directly on the FE modules or patch panels used for IO signals, but in reality, the board is too large for the detector modules and also lacks sufficient radiation hardness. The ELMB can withstand a maximum TID of up to 8 krad, provides 64 16-bit analog ADC input channels and several other general-purpose digital/analog IO channels, and has a CAN transceiver to communicate data using the standard 5 V physical layer[21]. Although more radiation-hard than the most commercially available monitoring boards, the ELMB had to be placed outside the Calorimeter of the ATLAS experiment to protect from harsher radiation. The radiation hardness required for the innermost layer of the new Pixel detector is 500 Mrad. This makes ELMB very unsuitable for monitoring granularity per module per serial power chain because to have such a system, an enormous amount of cables/-material must go inside the detector. The ELMB is better suited for environmental monitoring where the radiation levels are below the maximum tolerated dose level of the board. A newer version of the ELMB has also been developed and produced by a CERN group, which is more radiation tolerant but still does not meet the radiation requirements of the new Pixel detector.

3.4 Available commercial solutions

Due to its robustness and reliability, the CAN protocol has gained popularity for space applications in recent years. Under the umbrella of the European Space Agency, the European Cooperation for Space Standardization formulated a new standard that specifies the requirements on top of the existing CAN protocol for space applications [22]. For the application layer, the standard optionally specifies the CANopen standard and its limited implementation in the hardware to build CAN-compliant

controllers that can be used in space. A minimal implementation of the CANopen is also defined where the Object Dictionary of a CANopen device does not have to be dynamic, but it can be hardwired, and many communication objects can be dropped. Most commercial vendors now use this standard to build CAN controllers for space applications; however, certain limitations prevent them from being used in the DCS.

- Although the CAN-controller-based microchips built for space applications are radiation-hard, their radiation tolerance is as little as nothing for the ATLAS ITk DCS application. Most commercial controllers are radiation hard up to an Ionizing dose of $\approx$ 100 krad, e.g., Intersil's ISL7202xSEH which is tolerant only up to 75 krad at a dose rate of 0.01 rad/s [23]. The TID requirement for the innermost layer of the ATLAS ITk detector is 500 Mrad.
- As this is an extension of the original CAN protocol for space applications, it does not change anything in the original protocol. This means all the controllers must use a standard CAN physical layer, which is impossible with available radiation hard libraries for the targeted IC process.
- Most commercially available ICs do not offer all-in-one solutions. They need extra peripherals, e.g., reference voltage generators, regulators, oscillators, etc., to operate. These external peripherals are also unavailable for required radiation tolerance and require a larger space.
- Size and power are also important factors because no active cooling is foreseen for a component used for monitoring inside the detector volume. This requires very low power consumption for the chip used for monitoring.

3.5 Motivation to develop a new monitoring chip

- As mentioned in the earlier sections, the current monitoring systems from CERN and other particle physics experiments do not meet the new Pixel detector's versatility, space, power, and radiation requirements. Also, the available commercial solutions lack the necessary radiation tolerance well, and they are too general and large with added complexity to integrate into the Pixel detector.

- The tracking performance of the ITk is influenced significantly by the amount of material inside the detector volume. Some of the optimizations can be achieved by optimizing the inclination angle of the modules by doing a simulation of the tracking using the GEANT4 [24] framework to see how particles move through different materials. Less material inside the ITk than the current ID reduces the probability of electron charge misidentification by at least a factor of 3 [11]. Developing a new custom-made chip helps reduce the amount of material that goes inside the detector by saving on externally required peripheries and services and reducing the size using only essential functionality.

- Quick OPC-UA Server Generation Framework(quasar) is widely used at CERN to generate and easily manage Open Platform Communications-Unified Architecture (OPC-UA) servers. The existing DCS of the ATLAS experiment makes use of this ecosystem based on the WinCC OA SCADA platform [25]. The ELMB boards, which the current DCS uses, communicate with the OPC server using the CANopen protocol [6]. Developing a new chip using the CAN/-CANopen communication protocols will allow easy integration into the current system. It will save a lot of resources required to develop a new infrastructure from scratch.

- In addition to radiation hardness, commercial CAN controllers that implement CANopen in hardware also lack flexibility. Due to Intellectual Property (IP) rights, it is not possible to modify the design to meet the DCS-specific requirements, e.g., Triple Modular Redundancy (TMR) to harden the design against SEE or to add more custom functionality on top of the existing CAN/CANopen protocols.

- A CANopen-based general-purpose monitoring chip can be extended for more functionality in the future and used in other physics experiments or in any high-radiation environments.

Chapter 4

Integrated circuit development and radiation tolerance

4.1 Development of Integrated Circuits (ICs)

Application Specific Integrated Circuits (ASICs) are highly customized integrated electronic circuits that are developed to provide a very specific functionality. These integrated circuits are then mostly packaged and produced in large numbers, to be found in almost every electronic device these days. ASICs are categorized into two main domains: analog and digital circuits. Most of the ICs these days include both domains, so they are labeled as Mixed-signal circuits. Primary examples of mixed-signal circuits are the Digital-to-Analog (DAC) and Analog-to-Digital (ADC) data converters. Figure 4.1 shows some general steps involved in the design of a CMOS IC. Some more sub-processes are involved or may differ depending upon the type of IC.

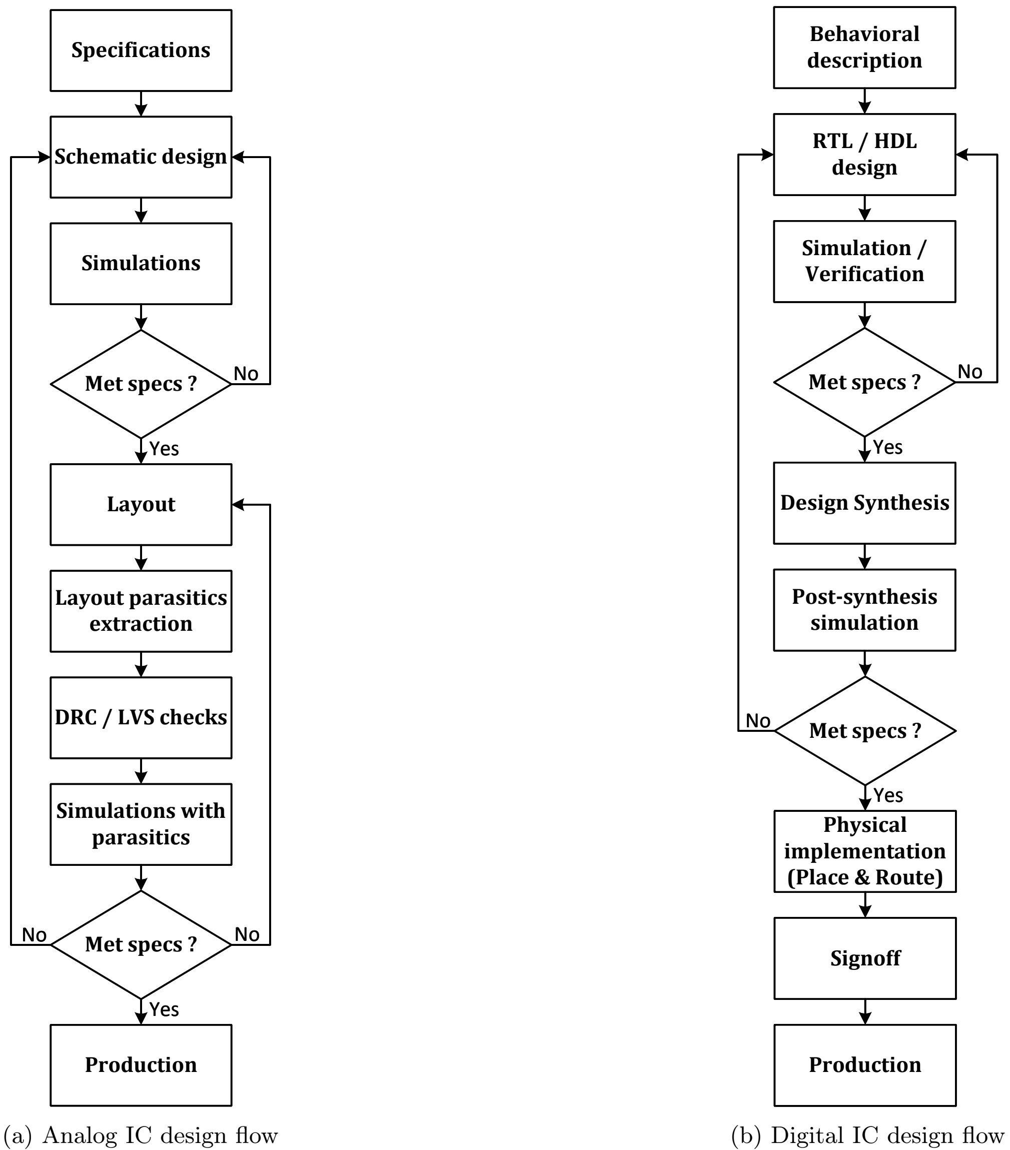
ASICs can be further categorized into three main types.

- Full-custom ASICs
- Semi-custom ASICs
- Programmable ASICs

Full-custom design ASICs require a lot of time and effort for the development and verification of the desired functionality as they are highly customized, and most of the logic building blocks, analog circuits, and layouts are done from scratch. Power consumption, size, and speed are the main driving factors in designing full custom ASICs. In addition, tolerance to ionizing radiation and Single-Event Effects (SEEs) are also very important parameters for the full custom ASICs used in particle physics experiments and the space industry.

Semi-custom ASICs can be produced a lot faster than full-custom ASICs because a lot of building blocks already exist. A developer does not have to start layouts and definitions from the transistor level. The IC manufacturers provide a lot of standard cell libraries for commonly used logic blocks, e.g., logic gates, Random Access Memories (RAMs), multiplexers, flip-flops, etc. Many custom-made ASICs produced these days belong to this type.

Programmable ASICs are the most flexible, fastest, and economical variant of all



(a) Analog IC design flow

(b) Digital IC design flow

Figure 4.1: ASIC design flow

three different types to design and produce. They are usually categorized into Programmable Logic Devices(PLDs) and Field Programmable Gate Arrays(FPGAs). These devices are built with configurable logic blocks that are not hardwired. These devices can be programmed and configured after production using design tools provided by the IC vendors. As the logic is programmed by defining Look-up-tables (LUTs), logical wires, and logic gates, the devices can normally be programmed more than once. This allows easy and very cost-effective upgrading.

4.1.1 Analog IC design

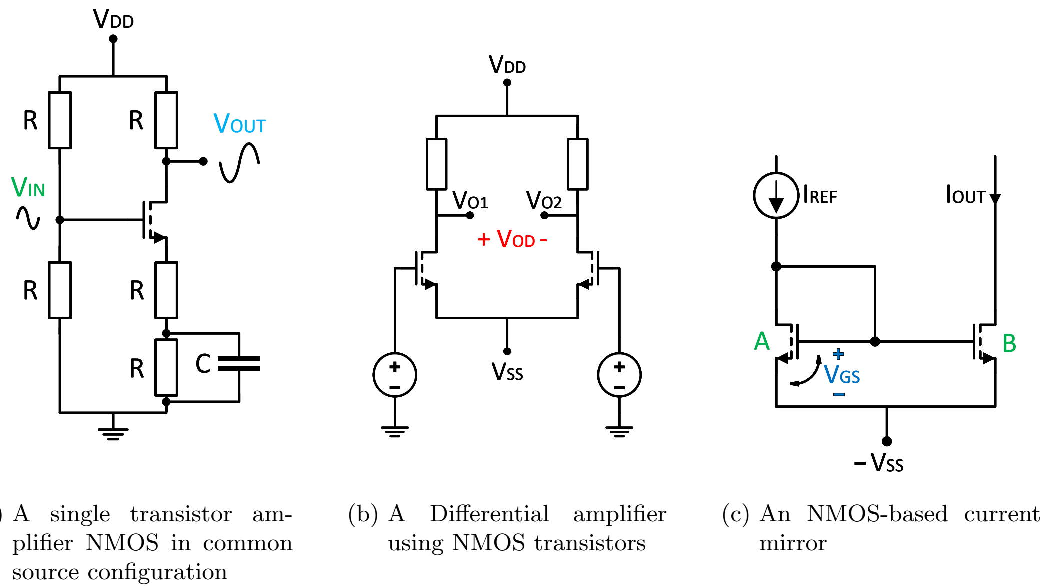
Although digital information processing has increased enormously over time, almost all the signals existing in nature are continuous/analog signals. These analog signals are often sampled to get rid of noise, digitized to increase processing speed, and then driven back to the analog world. This is the reason why many ICs are mixed-signal, where both analog and digital information is processed, e.g., transceivers for wired/wireless communication, audio/video processing, sensors, actuators, etc. A lot of analog signals are so small and noisy that they require amplification and filtration before they can be processed by a complex digital logic on the chip. In the case of mixed-signal ICs, the signals are then converted using an ADC to be processed by some Digital Signal Processor (DSP) on the chip. In the end, the digital signal is once again converted back to an analog signal by using a DAC and then provided to a driver circuit to drive an analog medium.

Single-stage amplifiers are a type of circuit topology where a single transistor is used for signal amplification. The circuit requires external biasing components to define the operating point of a transistor. Single transistor amplifiers can be biased in inverting, non-inverting, or follower configurations where each configuration has its own merits/demerits defined in terms of voltage/current gain, input/output impedance, signal inversion, frequency response, etc. Figure 4.2(a) shows an NMOS transistor connected in a common source configuration. Some more circuitry is required to couple the input and output without disturbing the DC operating point of the amplifier.

A differential amplifier is one of the most important basic building blocks of an Analog IC. Shown in Figure 4.2(b), the circuit amplifies a differential signal, whereas it attenuates the common-mode signal. One of the very important parameters of a differential amplifier is the matching of the two transistors to get the maximum performance. Matching is ensured not only by using transistors of the same size but also by the orientation and nearby structures in the layout, which influence how well the two transistors are matched after fabrication. The differential output is given by:

$$V_{OD} = V_{O1} - V_{O2} \tag{4.1}$$

Some of the basic building blocks of analog integrated circuits are mentioned below:



(a) A single transistor amplifier NMOS in common source configuration

(b) A Differential amplifier using NMOS transistors

(c) An NMOS-based current mirror

Figure 4.2: Basic circuits to build Analog ICs

- Single-stage amplifiers
- Differential amplifiers
- Current mirror

Figure 4.2(c) shows a current mirror. The current mirrors are used in building analog circuits to work as a precise current source, which is not affected by load conditions. A good current mirror would have a very high output resistance so it is not disturbed by varying load, a very low input impedance, good frequency response, and, very importantly, good precision to copy the reference current. The output current is given by:

$$I_{OUT} = I_{REF} \frac{K_{nB}(1 + \lambda V_{DSB})}{K_{nA}(1 + \lambda V_{DSA})} \tag{4.2}$$

Where $K_n = \mu_n C_{ox} \frac{W}{L}$

$$I_{OUT} = I_{REF} \frac{\frac{W_B}{L_B}(1 + \lambda V_{DSB})}{\frac{W_A}{L_A}(1 + \lambda V_{DSA})} \tag{4.3}$$

4.1.2 Digital IC design

Logic gates, e.g., AND, OR, NAND, etc., are the core elements of a digital IC. Connected together in a complex way, they process information by using only binary

signals, where a signal is defined as low or high. In addition to logic gates, digital ICs also use other basic building blocks e.g, flip-flops to store information, multiplexers to reduce resources and channel information efficiently, and Arithmetic Logic Units (ALUs) to do arithmetic tasks, etc.
Figure 4.1(b) shows the main steps involved in the design of a digital IC. The very first phase is the behavioral description. Hardware Description Language (HDL), e.g., VHDL or Verilog, is used to define hardware elements, and afterward, verification is done to confirm the behavior. During the synthesis phase, standard cell libraries from the desired IC process are used, timing constraints are defined, and some generic optimization is done. In the implementation phase, floor-planing, clock tree synthesis, design placement, and verification are done.

4.2 Effect of radiation on Integrated Circuits

Electronic circuits are prone to damage caused by radiation. The undesirable effects can be categorized into two broad categories, i.e., cumulative effects and single-event effects (SEE). Depending on the total dose, dose rate, type of radiation, and the target IC type, the damage can cause an IC to stop working completely or shift from the optimal operational point and lose precision over time. The damage caused may or may not be recoverable by annealing. These are very vast topics on their own and not the main scope of this thesis. In this thesis, the radiation effects are only briefly described to characterize and qualify the MOPS chip to meet the defined specifications.

4.2.1 Cumulative dose effects

When electronics, or more specifically integrated circuits, are exposed to radiation, the damage caused by radiation has a cumulative effect. The longer an electronic component is exposed to radiation, the more damage it inflicts on the component. Cumulative radiation damage is further categorized into two different categories. A Total Ionizing Dose (TID) effect is due to Ionizing radiation, and the displacement damage is caused by Non-Ionizing radiation.

Degradation due to Total Ionizing Dose (TID) Ionization is a process where an electron sitting in the valence band absorbs enough energy to jump into the conduction band. This creates an electron-hole pair. If a material is under the influence of an electric field, then this newly created electron-hole pair may not recombine. The movement of these extra charge carriers also introduces a parasitic current in the device. Linear Energy Transfer (LET) is used to define the amount of energy absorbed by the material during this ionization process. How much energy gets transferred to the material by the highly charged particles depends upon the energy, flux, angle of incidence, and the material itself. Because of lower mobility for charge carriers in the

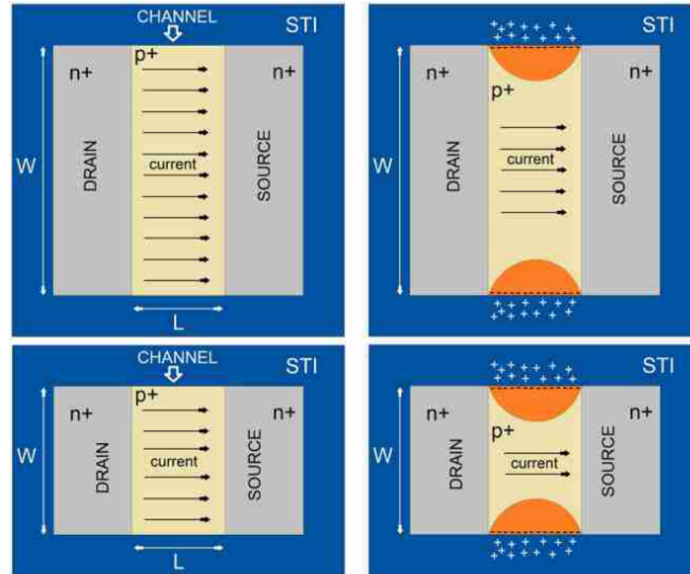


Figure 4.3: Radiation Induced Narrow Channel Effects (RINCE) [26]

insulators, it is difficult for the electrons and holes to leave the region. Compared to the holes, the higher mobility of electrons lets them escape from the silicon dioxide, whereas the holes remain trapped. This gradual accumulation of holes creates a net positive charge in the region, which is responsible for the change of threshold voltage, noise, leakage current, etc. [27]. Commercial CMOS electronics can typically withstand up to 5 krad of dose [23]. Two of the main reasons for TID effects in electronics are the trapped positive charges in insulating parts of a MOSFET, and the second one is the creation of defects at the interface between silicon and silicon dioxide due to the same trapped charges. With the decreasing thickness of gate oxide in the newer IC technologies, IC technology is inherently becoming more and more tolerant to radiation, but some other effects have started to appear. The defects in the spacers and Shallow Trench Isolation (STI) used to isolate transistors contribute significantly towards degradation due to radiation. Positive charge trapped in the spacers can change doping levels and have an impact on the effective resistance of the channel. This is especially true for devices with smaller sizes. The degradation due to this phenomenon is called the Radiation-Induced Short Channel Effect (RISCE) [28]. As shown in Figure 4.3, The term Radiation Induced Narrow Channel Effects (RINCE) was first coined in [29]. The electric field due to charges trapped in STI affects the current flowing through the channel. Devices with narrow channels/smaller widths are affected more than the devices with wider channels. The charges trapped in STIs are also responsible for the leakage current in the device because of the creation of the parasitic channels. TID effects are studied when an electronic component is under nominal bias conditions. This is due to the reason that an electron-hole pair created by the ionization process has a lower probability of recombining under an

applied electric field. TID is defined by the SI unit Gy as well as using the old unit rad where 1 Gy is equal to 100 rad [30]. TID-induced degradation in electronics for very large doses is dependent on the dose rate, transistor size, biasing voltage, and operational temperature [28]. For the TSMC 65 nm process, the studies have shown that more damage has been done at low dose rates of 35 krad/h than at much higher dose rates of higher than 2 Mrad/h. The dose rate of 35 krad/h is comparable to what is expected for some of the inner detectors at the LHC; however, it might still be higher for the future ITk Pixel detector [31].

Displacement damage Displacement damage occurs to an electronic device when it is exposed to non-ionizing radiation. When high-energy particles hit the material's lattice, they can displace an atom, which can displace even more atoms in the lattice. This causes defects that change a material's electrical properties, doping concentration, etc. In CMOS technology, the TID effects constitute the major damage caused by radiation. No displacement damage studies have been done during the course of this thesis.

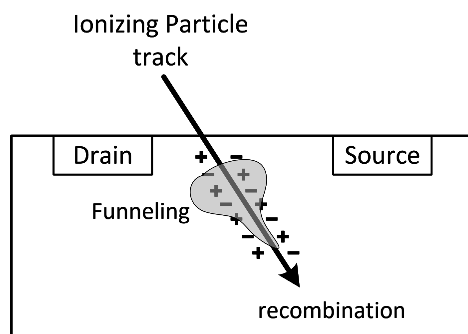


Figure 4.4: Single-Event Effect (SEE)

4.2.2 Single-event Effects (SEE)

Single-event effects (SEE) in a semiconductor chip were first reported in [32]. In comparison to TID effects, SEEs are caused by a single high-energy particle hitting a device, which creates an ionization track similar to that shown in Figure 4.4. Because of the electric field, the charges generated near reverse biased p/n junctions/depleted channels are quickly collected by the drain and source regions. This is responsible for the generation of a current spike. Charge collection in the depleted region happens very fast. However, a slow charge collection also happens outside and far from the depleted region. This is shown in Figure 4.4 as a Funnel until it reaches the bulk, where most of the created electron-hole pairs start to recombine. Any single ionizing particle randomly hitting a device may not generate a SEE. Two conditions are required for a SEE to happen: the highly energized particle must hit a specific region in a device defined as Sensitive volume, and the charge deposited by a particle hit

must also be larger than the required Critical charge to create an upset. SEEs are not accumulative, and the damage done by them can be a mere corruption of some data or a complete malfunction or bad configuration of the device. In severe cases, an SEE can also damage a device permanently. SEEs can be categorized into two broad categories, which are further divided into several different types of effects [30]. Here, only a few effects are discussed:

- Soft errors
  - Transients: In this case, a transient happening on some points gets propagated in the circuit as false information, eventually corrupting information, or in the case of Analog design, they can disturb the operation point of a circuit.
  - Static errors: here, information stored in a single memory cell can change.
- Hard errors
  - These types of errors can damage a device permanently if not corrected quickly.

Single-event Transients (SET) A Single-event Transient (SET) is a glitch or voltage spike that occurs when a highly energetic subatomic particle hits an electronic device. The sudden voltage spike generated due to the hit can disturb the operating point of a node in an analog circuit, or it can propagate through the combinational logic of a digital design within one clock cycle, creating logical errors. A SET can become very serious, e.g., if it happens on an asynchronous reset signal or during the critical time when a combinational input is sampled and stored in a flip-flop. In circuits with very high-speed clocks, SET can also result in an SEU [33].

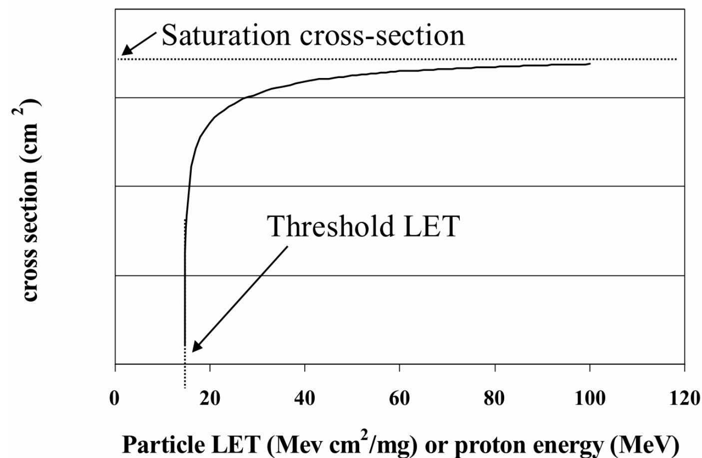


Figure 4.5: SEU sensitivity of an electronic device [30]

Single-event Upsets (SEU) A Single-event Upset (SEU) is an event where a bit is stored in a storage element, e.g., flip-flop, toggles from low to high, or vice versa. SEU can change stored data or, more importantly, can cause corruption in the configuration memory of a device. To estimate the SEU rate and characterize a device, a cross-section plot is calculated at different LETs in case of irradiation using heavy ions [34]. As Shown in Figure 4.5, a SEU does not happen at energies lower than the threshold LET. The plateau of the curve indicates the total area of a device sensitive to SEUs. For any given LET, the area can be divided by the total number of sensitive nodes in a device to get an estimate of the sensitive area per node.
SEU cross-section is defined as:

$$\sigma = \frac{N_{upsets}}{\Phi \cdot N_{nodes}} \tag{4.4}$$

Where N_{upsets} are the total number of SEUs that happen, and N_{nodes} is the total number of storage cells or sensitive nodes in a device. Φ represents time-integrated particle flux or total fluence in $\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Previous studies have shown that an increase in the operational clock frequency on a chip will induce more SETs in the combinational logic, and a low supply voltage can make flip-flops more vulnerable to SEUs. Therefore, modern CMOS processes working on low voltage and high frequency are more prone to SEUs [35]. SEU cross-section calculation for different logic circuit implementations using the TSMC 65 nm process, different radiation types, and the factors affecting it have been investigated in [36][37].
Cross-section obtained by irradiating an electronic device using heavy ions can be translated to the expected rate in the LHC environment using the computational method defined in [38].

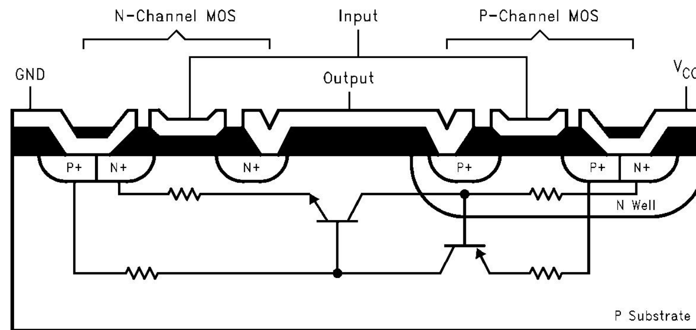


Figure 4.6: Parasitic BJTs in a CMOS device causing a Single Event Latch-up (SEL) [39]

Single-event Latch-ups (SEL) Single-event Latch-up (SEL) is a type of hard error. If not corrected swiftly, an SEL damages a device permanently. In a CMOS process, an SEL happens due to the opening of a low impedance path between the supply

voltage and the ground potential due to parasitic PNP and NPN transistors shown in Figure 4.6. In case of an over-voltage / thermal stress or due to an ionizing particle hitting the device, a positive feedback path is created where the collector current of the first parasitic transistor feeds the base current of the second one and vice versa. An abnormally large amount of current is drawn due to this path creation. To save the device from permanent damage, the power supply must be cut promptly.

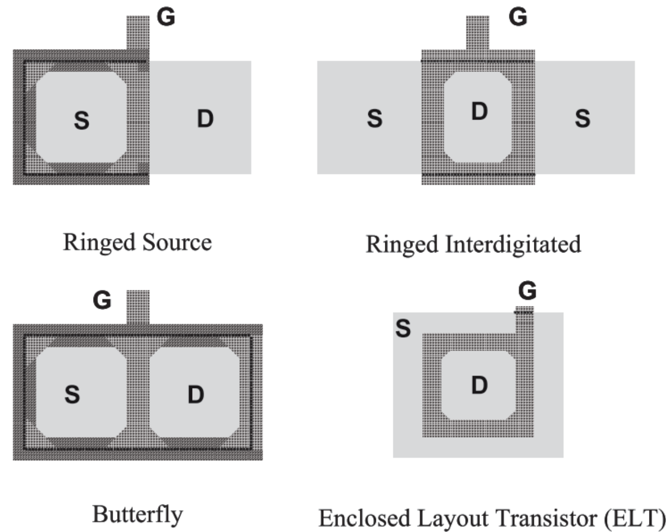


Figure 4.7: MOSFET layout techniques to reduce leakage current between source and drain [40]

4.3 TID tolerance

Radiation tolerance for electronic devices can be achieved by either using the approach Radiation Hardening by Process (RHBP), Radiation Hardening by Design (RHBD), or a combination of both. Since RHBP is very expensive, RHBD is normally used in modern CMOS ICs. The following text explains some of the important techniques.
As explained earlier in this chapter, the main cause of the TID effects in a CMOS process is related to oxides used in the gate or STI, etc. Thin gate oxide transistors are very tolerant to TID effects and for thicknesses less than 10 nm, the radiation effect due to gate oxide becomes insignificant [41] [42]. Scaling down the CMOS process also reduces the gate thickness, which makes the modern CMOS technology inherently radiation-hard.
Another problem with TID is the leakage current due to trapped charges in the STIs, which are responsible for opening the parasitic channels between the source and the drain. The leakage current due to parasitic channels increases with the increasing total dose until the point where normal operation of the circuit stops. A solution to this problem is to enclose either the source or drain of a transistor using thin gate

oxide, as shown in Figure 4.7. The most commonly used Enclosed Layout Transistor (ELT) implementation and its effectiveness are further discussed in [43]. The leakage current between neighboring transistors can be eliminated by using heavily doped guard rings, e.g., a p+ guard ring between n+ diffusion regions. Due to the custom nature of analog IC design, the TID-induced damage, which is dependent on transistor sizing, e.g., RINCE and RISCE, can be reduced by choosing wider and longer channel devices. The design parameters used to increase the radiation tolerance of devices in the analog design are difficult to control in the digital IC design because standard cell libraries available for commercial IC processes mostly use the minimum possible length and width for the transistors. Also, it requires a great effort to produce numerous standard cells using ELT and guard rings.

4.4 SEE mitigation

Because the SEEs are caused by single high-energy ionizing particles, to make circuits tolerant, the application environment of an electronic device plays an important role in defining a mitigation strategy. Devices used in the LHC experiments experience particles and their energies differently from the devices used for space applications. As explained earlier in this chapter, an ionizing particle must deposit enough charge in a sensitive volume of a node to create undesired effects. Adding capacitance to the sensitive node can provide a very simple solution, but it has the drawback of more power consumption and loss of metallization options at the top level.
To protect against SETs, de-glitching circuits at the cost of sacrificing speed can be used as well as redundancy in combination with voters can be used in the combinational logic to prevent SETs from propagating in the logic.
Protection against SEUs can be achieved by duplicating information stored at the node level by using architectures like Heavy Ion Tolerant (HIT) proposed in [44] and Dual Interlock Cell (DICE) in [45]. However, the effectiveness of these architectures at the node level is not outstanding for modern CMOS processes due to the fact that smaller transistor sizes in a modern CMOS process imply larger density. The two sensitive nodes of a DICE must be placed far apart in the layout to ensure that they are not hit at the same time. W.r.t. a standard cell, DICE could achieve only a tenfold improvement in a 90 nm process [40]. Another approach is to use redundancy for the stored information. Triple Modular Redundancy (TMR) is widely used in ICs to protect against SEUs. As shown in Figure 4.8, every storing element, e.g., a flip-flop, is triplicated, where each storing element contains a copy of the same data. A voter is used in front to decide the correct value by majority voting. To prevent multi-bit upsets from happening, the triplicated cells must be placed far apart from each other. In the circuits operating at high frequency, the SETs can easily propagate into the storing elements. There are two ways to mitigate this: using Temporal sampling, where a clock skew is used for three triplicated cells to filter out glitches, or by triplication in the combinational logic. Using Temporal sampling can make it very difficult to handle correct timing in the design, whereas triplication in the

combinational logic can significantly increase the required area. Error detection and correction techniques can also be used to cope with SEUs, e.g., hamming encoding.

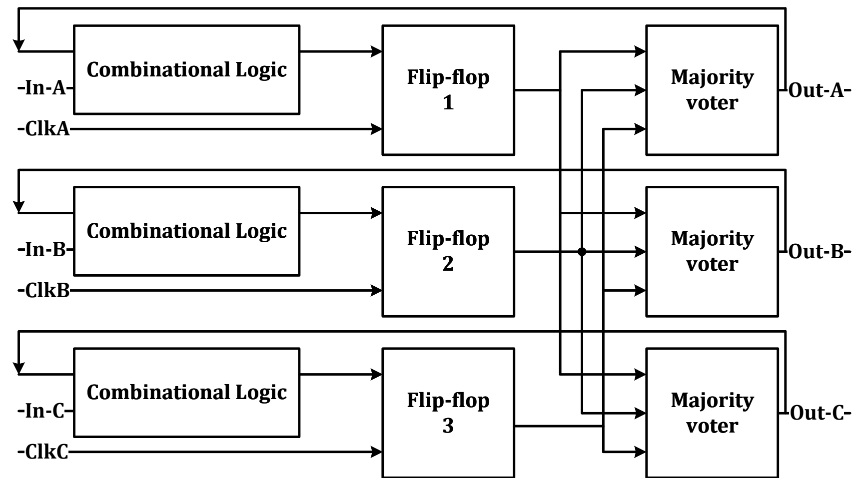


Figure 4.8: Full triplication of a digital logic

Chapter 5

First test prototype

5.1 Purpose and components of the chip

A first test chip was submitted to study and verify the behavior of the analog circuits required for the actual MOPS chip.

- Three regulators with a regulated output voltage of 1.2 V, 2.4 V, and 3.6 V are powered using 5 V power supply. The 1.2 V regulator was intended for the digital part of the chip, while the other two were required by the standard CAN physical layer
- Standard CAN transceiver using a supply voltage of 5 V
- Serial Control Bus (SCB) physical layer
- 3000-bit shift registers to study SEU cross-section

The chip was built using the TSMC 65 nm process, which allows a maximum of 1.2 V for the transistors. The high-voltage circuits were built using transistors in a cascoded topology to sustain a voltage higher than what is specified by the fabrication technology. For the analog part, the regulators were developed by Michael Karagounis (FH Dortmund), and the other components on the chip were a joint effort from the people from FH Dortmund and the University of Wuppertal. The Serial Control Bus (SCB), a physical layer, was also used on the chip to test communication with the PSPP chip [46].

5.2 3000 bits shift register for SEU studies

The digital part of the test chip included only a 3000-bit long shift register logic to study SEUs. This is the same logic that was also implemented in the Pixel Serial Powering & Protection (PSPP) chip [46] and was integrated into the MOPS chip as well for SEU studies. Two instances of the 3000-bit long shift register are included in the chip. One instance is the simple shift register, while the other uses full triplication. A simplified schematic of the shift register logic is shown in Figure 5.1.

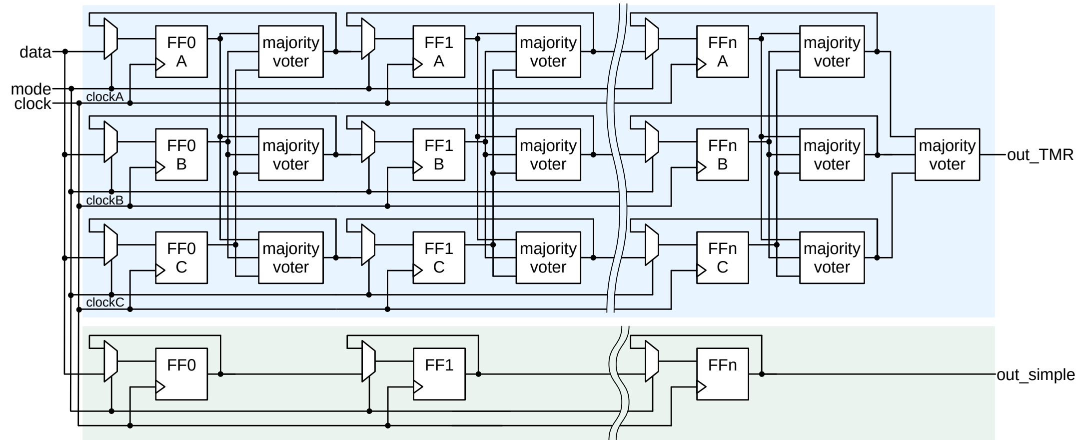


Figure 5.1: TMR shift register schematic [46]

5.3 Problems seen on the chip

A mistake was made regarding the IO pad selection for the high-voltage IO signals from the regulators and the CAN physical layer. The pads used in the chip for high voltage signals allow a maximum signal of 2V. If the voltage exceeds 2V, then the ESD protection circuit gets activated, and the high voltage signal is shorted to either supply voltage or ground, depending on the polarity. Because of this problem, testing the high-voltage circuits was no longer possible. A special procedure called Focused Ionizing Beam (FIB) was used to cut the ESD structures. The intention was to eliminate the ESD protection circuit, although it was not desired in normal circumstances. As the FIB procedure cannot guarantee that only specific metal layers are destroyed, the procedure done to chip created short circuits. It was later decided in the revised baseline that high voltage regulators and the CAN Physical layer must be omitted in the chip to avoid technology limitations and mitigate radiation damage, which is significantly higher at high voltages.

5.4 Outcome and lessons learned

Although the results of the analog circuitry were not promising, they still helped to understand some design problems, technology limitations, and shaping decisions that influenced the design and development of the succeeding versions of the MOPS chip. The on-chip digital part included only the shift register for the SEU studies. These chips were then used for the SEU studies carried out in Leuven. The results are explained in the chapter 9.

Chapter 6

Monitoring of Pixel System (MOPS) chip

The Monitoring of Pixel System (MOPS) chip is an Application Specific Integrated Circuit (ASIC) designed to be used in the DCS to independently monitor the voltage and the temperature across the detector modules. The detector modules constitute the front-end electronics responsible for tracking and data read-out. Chapter 3 explains the concept of the DCS for the Pixel detector, and Figure 3.3 shows the topology of the MOPS chip's connection in a serial powering chain. The chip has been developed using the TSMC 65 nm CMOS process. CERN has put a tremendous amount of effort into studying the radiation tolerance of the technology in detail for future upgrades. The TSMC 65 nm CMOS process itself is inherently radiation-hard, but to make it more radiation-hard to be able to tolerate radiation levels for different experiments, CERN provides additional custom libraries Hardened by Design (HBD) for different fundamental building blocks and also provides simulation corners to characterize circuits for TID.

6.1 Requirements for the chip

Several requirements for the MOPS chip are defined in the specification documents [18] and [47] related to monitoring precision, radiation hardness, operational temperature, size, packaging, etc.

Voltage monitoring The chip must be able to monitor a maximum of 16 modules in a single serial powering chain [11]. During regular operation, every detector module has a nominal voltage drop of 2 V. This makes a maximum of 32 V in a single chain. The MOPS chip must provide a relative precision of 15 mV for the voltage measurement within its operational temperature range.

Temperature monitoring Every detector module in the serial powering chain hosts a Negative Temperature Coefficient (NTC) resistor to measure the temperature. The reference voltage for this resistor must be provided by the MOPS chip. The chip should provide a relative temperature monitoring precision of 1 K.

Radiation hardness Radiation hardness is one of the most essential requirements for the MOPS chip. The chip will also be operated in the innermost layer of the Atlas ITk Pixel Detector, so it has to qualify for radiation levels of up to 500 Mrad of TID.

Operational temperature The operational temperature range for the chip is −40 °C to 60 °C.

SEE tolerance The chip must be tolerant of SEEs. An SEU in the monitoring data can be tolerated but can be fatal and unacceptable in the configuration memory of the chip. Frequent SEUs in the configuration memory can cause the chip to require more power cycles to provide reliable monitoring data. This introduces transients in the system, so the amount of transients must be reduced as much as possible. In addition to that, the chip must also be tolerant towards SET and SEL, as explained in Chapter 4.

Independent powering regulator The chip must have an on-chip voltage regulator to ensure a stable power supply to the chip and to provide a reference voltage for the NTC resistor to monitor the temperature reliably. The Voltage regulator must be able to compensate for long power lines, which can be up to approximately 70 m in length. The current consumption of the chip varies with bus activity, which also causes varying voltage drop on the long power lines. The regulator must be able to regulate for a large input supply voltage range.

Communication protocol A robust and reliable communication protocol must be chosen to communicate over long distances. The number of service lines required by the communication protocol must be as small as possible. Therefore, the chip implements CAN and CANopen protocols, which are explained in sections 6.3.1 and 6.3.2. The chip must also be able to drive the communication bus of 70 meters in length with included filter capacitors of 10 µF.

On-chip oscillator If there is no clock available on the communication lines or can not be extracted from the data, a local on-chip oscillator is required to generate frequency for the digital part of the chip. The oscillator should provide a possibility to be trimmed remotely after installation. Trimming is necessary to compensate for process variation and radiation and for variation in operational conditions.

6.2 Chip versions

The first test prototype of the chip is called DCS-controllerv1. At the time of submission of the first version, the digital part of the chip was still not mature enough to be fabricated, so it was programmed on an FPGA [48]. The digital part also included the logic to communicate with the PSPP chip [46], which was defined in the original ITk Pixel Detector TDR [11] but was later dropped in the revised baseline of the

Pixel project. The Analog part of the chip included the voltage regulators and the standard CAN physical layer. More details about this first test chip are provided in Chapter 5.
This chapter discusses the two complete versions of the MOPS chip, the MOPSv1 and the MOPSv2. The MOPSv2 is essentially an improved version of the MOPSv1 with some added functionality, e.g., automated oscillator trimming more watchdogs to increase SEU tolerance and malfunction mitigation. The watchdogs allow for resetting the core state machines and frequent configuration reloading to prevent a high number of power cycles.

6.3 MOPS communication protocol

The chip makes use of two well-defined communication protocols: the Controller Area Network (CAN) [49] and the CANopen [50] standard. Figure 6.1 shows the Open Systems Interconnection (OSI) model. The CAN protocol is only defined for the physical and the data link layers. To handle communication effectively between different nodes on a CAN bus, the CANopen is one of several protocols defined for the rest of the upper layers. The CANopen mainly covers the transport and the application layers because the definitions in others are not required in a CAN network.
The MOPS chip implements more functionality on top of both CAN/CANopen base standards and does some customization. Below mentioned are some important differences:

- Although the digital part of the chip's CAN node complies with standard ISO 11898-1:2015 [49], the physical layer uses different analog signal levels. Therefore, the physical layer signaling is incompatible with the standard/commercial controllers without translating the logic/voltage levels.
- The on-chip oscillator can be done at the start-up or after the remote reset command. During the calibration phase, the chip listens to the bus like any other CAN node but does not actively participate in the communication.
- The chip is not fully CANopen compliant. It only implements a minimal set of SDO and NMT communication objects.
- The minimal CANopen implementation in the hardware strategy used on the MOPS chip is similar in approach but completely different from what is defined in [22].

6.3.1 CAN bus communication protocol

As shown in Figure 6.2, CAN is a serial communication bus where all the nodes are connected to a single bus terminated by a termination resistor at both ends. A CAN bus requires only four lines in total. Two lines are required for powering, and the other two are used to communicate using differential signaling. The CAN protocol

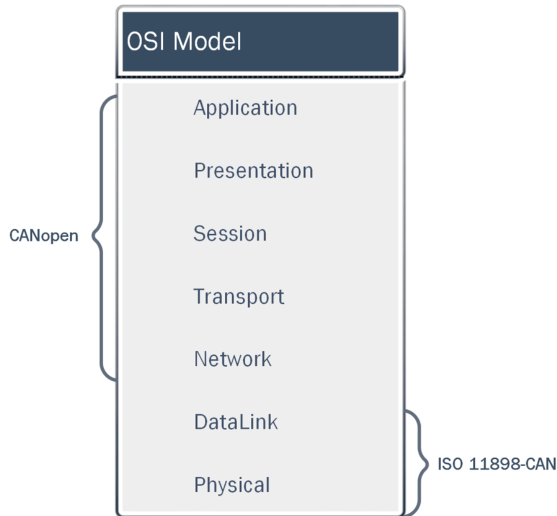


Figure 6.1: The layers defined in the Open Systems Interconnection (OSI) model [51]

states no limit for the maximum number of nodes allowed on a single bus; however, the bus load limits the number. There is no single master on the bus, so every node is allowed to send messages at any time. Real-time non-destructive arbitration happens whenever more than one node tries to send a message simultaneously. A frame with the highest priority gets access to the bus. The priority of any frame is solely defined by the 11-bit identifier sent at the beginning.

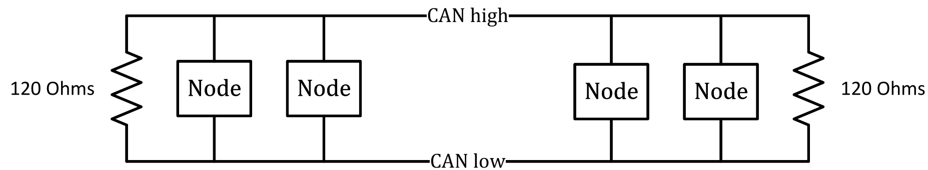


Figure 6.2: Controller Area Network (CAN)

Some features of the protocol are:

- Emphasis is placed on the priority of the messages where all nodes have unrestricted access to the bus
- Message arbitration is non-destructive
- All nodes can listen to all messages on the bus and decide for themselves whether the message is important for them or not
- Data integrity is ensured by robust error detection features
- Differential signaling to provide noise immunity

SOF	Arbitration	Control	Data	CRC	EOF
1 bit	11 bits or 29 bits (extended)	4 DLC and few other specific bits	8 bytes	15 bits	1 bit

Figure 6.3: CAN classic frame format

- Data can be requested remotely between different nodes
- Automatic re-transmission of the messages that lost arbitration

The format of a classic CAN message frame can be seen in Figure 6.3.

- SOF/EOF

  These fields define the start of a frame and the end of a frame.

- Identifier / Arbitration field

  The 11-bit identifier uniquely identifies a message on the CAN bus. This is used to do arbitration where a CAN frame with the highest priority gets access to the bus. If more than one node tries to send a message on the bus simultaneously, then the message with the highest priority will be delivered. It also serves the purpose of message filtration, where every node on the bus can listen to any message but decides for itself whether it is important or not.

- Control field

  The control bits section of a CAN message defines the length of data in a message and some other features, e.g., whether a message is a remote request or a standard message that includes data, length of identifier, and some reserved bits, etc.

- Data field

  This field of a CAN message holds the actual data. In the classical frame format shown in Figure 6.3, the data field can have no data or a maximum of up to 8 bytes.

- Cyclic redundancy check (CRC) / error correction field

  This part of the frame holds the CRC checksum bits and the acknowledgment bit to prove the integrity of the message.

6.3.2 CANopen protocol

The CANopen is an application-level protocol that can be used in conjunction with the CAN protocol. Figure 6.4 shows the model for each MOPS chip on a network. CANopen is a device and manufacturer-independent communication protocol defined

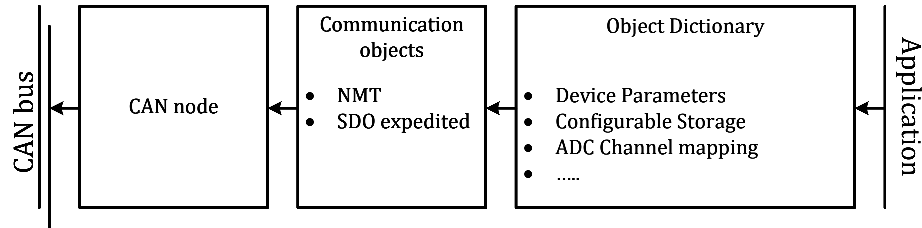


Figure 6.4: CANopen device model of the MOPS chip

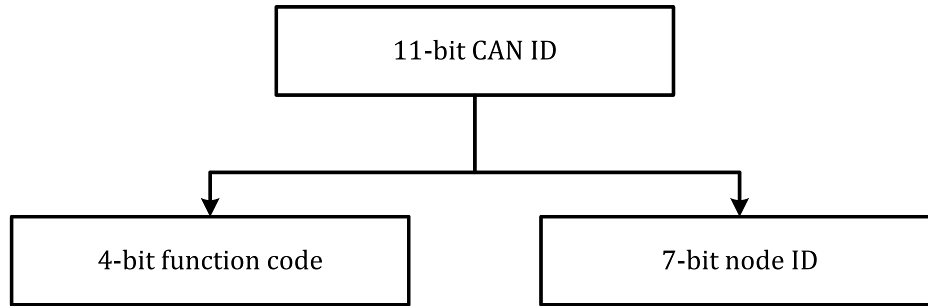


Figure 6.5: COB-ID in CANopen

for the application layer in the Open Systems Interconnection (OSI) model. As shown in Figure 6.1 the CANopen covers the network to application layers of the OSI model. Due to the architecture of the CAN protocol, no definition is required for the presentation, the session, and the network layer of the OSI model. The CANopen mainly implements the transport and the application layer. The protocol uses the CAN identifier field defined in Figure 6.3 to distinguish between different communication objects and address nodes connected to the network as shown in Figure 6.5, seven of the eleven identifier bits are used to address different nodes on the bus. This implies a maximum of 127 CAN nodes with distinct identifiers can be connected to a single bus in a CANopen network. The CAN protocol does not define a maximum number of CAN nodes. Theoretically, more than 127 nodes can be connected to a CANopen network, but they can not be addressed uniquely. The nodes without unique IDs can still read and broadcast messages on the bus. The protocol offers the possibility of synchronization on a CAN network. CANopen uses predefined communication objects to transfer information between different nodes. The predefined communication objects are categorized into the following types:

- Network Management (NMT) to manage/analyze the state of the network
- Process Data Objects (PDO) to transfer real-time process data
- Service Data objects (SDO) to configure nodes on a network
- Synchronization objects (SYNC) to synchronize timing and coordination between the different nodes

- Emergency objects (EMCY) to report malfunctioning by the nodes
- Time stamp objects (TIME) for time-critical applications

Due to its complexity and size, a complete implementation of the CANopen in hardware requires large storage on individual nodes and also adds complexity in the logical part. The CANopen is almost always defined at the software level for the standard CAN controllers.
In the MOPS chip, CANopen is embedded into the hardwired digital logic. The chip provides no dedicated logic to store the definition of the communication objects. For the following reasons, a modified, reduced subset of CANopen is implemented using Network Management (NMT) and Service Data Objects (SDO).

- The chip must be radiation hard up to an ionizing dose of 500 Mrad. Increasing storage elements on the chip requires more resources and complex logic to protect against SEEs.
- The final chip size can only be 2×2 mm^2. The size is limited by the cost, space, and material budget available in the final system. A complete CANopen implementation requires a significant increase in the fabricated chip size, which increases the cost with no added benefit; instead, the chip will become more vulnerable to the radiation effects.
- The DCS refresh rate requirement of 5 s [18] is very relaxed. Therefore, there is no need to implement PDOs to expedite the monitoring data.
- The system topology requires the chip to send the monitoring data only upon request and stay silent otherwise.
- Expedited transfer offered by the Service Data Objects (SDOs) with a bus speed of 125 kbps is sufficient to meet the requirement for the data rate, data length, and refresh rate of the whole system.

Network Management Object (NMT)

Three items are implemented in the chip for this type of communication object. One of the nodes connected to the network acts as a logical master. The master node doesn't need to have a COB-ID.

- Sign-in message
- Node guarding
- Remote reset

Sign-in message As the name suggests, whenever a chip is connected to the bus and powered on, it sends a sign-in message over the bus. Each node on the bus generates a single sign-in message when the power is supplied. The structure of this sign-in message is the same as the node guarding. It is the same node guarding message but is sent only once during the start-up by the remote node despite no request from the master node. Following the CAN protocol, a node keeps repeating a sign-in message until it is acknowledged. Figure 6.6 shows the structure of a sign-in message.

Node guarding The Node guarding is another NMT object implemented in the MOPS chip. The Node guarding message allows a master node in the CANpoen network to check whether a node is still alive and operational. Again, this protocol part is simplified to implement what is absolutely necessary.
Whenever there is a message on the bus with the identifier '0x700 + node-id', the respective node will respond with a single byte of data where the MSB should toggle for every new request. If the master node finds no response from the slave node or the MSB of the response message does not toggle for every new request, there is something wrong with that node. Either it is not working, or the configuration values in the registers have been changed. A reset request will then be required to return the node to the operational state. All other status messages are not implemented.
Figure 6.6 shows the format of the Node guarding.

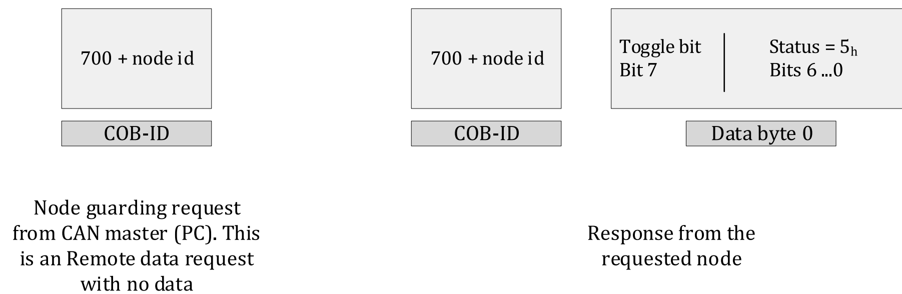


Figure 6.6: Node guarding/sign-in message in the MOPS chip

Remote reset request At any time, a MOPS chip can be in one of the three states: non-operational, operational, and configuration. When the chip is working normally, it is in the operational state. The chip is in the configuration state when the chip is doing automated trimming upon power-up or on demand using a remote reset command. Whenever a chip must be reset remotely, an empty message with an ID '0' is sent over the CAN bus. The CANopen standard defines this as node-dependent, but to simplify our application, every node will reset itself whenever an ID '0' is detected on the bus. After the reset, default configuration values, e.g., timing, etc, for the CAN node are reloaded from hardwired combinational blocks, and all the state machines will be returned to a known state.

Service Data Objects (SDO)

The Service Data Objects (SDO) provide access to all the entries of an object dictionary in a CANopen device. The SDO communication is available during pre-operational mode. It is used to configure a CANopen device, but it is also possible to read out a particular entry using the SDO read protocol.
The CANopen protocol always confirms the read/write operation when using the SDO communication objects. The chip implements service data objects of the CANopen standard explained in section 6.3.2, but only the expedited transfer mode is implemented. The Object dictionary is defined so its entries do not exceed four bytes. All the object dictionary entries can be accessed using expedited data transfer of SDOs, which allows a maximum of four bytes of data to be sent in a single CAN message. In comparison, the four remaining bytes are used for other task details, i.e., index, sub-index, and SDO operation details.
Different types of SDO frames that are used to communicate with the MOPS chip are shown in Figure 6.7 to Figure 6.11.
The following terms are mentioned in the figures.
scs: Command specifier
N: n = 4 - Data size
T: Toggle bit (unused)
E: Expedited transfer is used
S: Data size is indicated
Table 6.1 shows the message encoded with each abort code. All values are in hexadecimal.

600 + node id	Cmd=40_h	Index	Subindex	0
COB-ID	Byte 0	Byte 1&2	Byte 3	Byte 4 ... 7

Figure 6.7: SDO read request to the MOPS chip

580 + node id	Scs=010_b Bits 0..2	T=0 Bit 3	N Bit 4..5	E=1 Bit 6	S=1 Bit 7	Index	Subindex	Data
COB-ID	Byte 0					Byte 1&2	Byte 3	Byte 4 ... 7

Figure 6.8: MOPS response to the SDO read request

Table 6.1: SDO abort codes

Abort code	Description
0504 0000	SDO protocol timed out.
0504 0001	The client/server command specifier is not valid or unknown.
0601 0000	Unsupported access to an object.
0601 0001	Attempt to read a write-only object.
0601 0002	Attempt to write a read-only object.
0602 0000	The object does not exist in the object dictionary.
0606 0000	access failed due to a hardware error.
0606 0007	timeout of communication occurred.
0609 0011	Sub-index does not exist.
0800 0000	General error

600 + node id	$Scs=001_b$ Bits 0..2	T=0 Bit 3	N Bit 4..5	E=1 Bit 6	S=1 Bit 7	Index	Subindex	Data
COB-ID	Byte 0					Byte 1&2	Byte 3	Byte 4 ... 7

Figure 6.9: SDO write request to the MOPS

580 + node id	$Cmd=60_h$	Index	Subindex	0
COB-ID	Byte 0	Byte 1&2	Byte 3	Byte 4 ... 7

Figure 6.10: Reponse of the MOPS chip to an SDO write request

SDO COB-ID	$Cmd=80_h$	Index	Subindex	Abort code
COB-ID	Byte 0	Byte 1&2	Byte 3	Byte 4 ... 7

Figure 6.11: SDO abort message in case of an error

6.4 Digital block

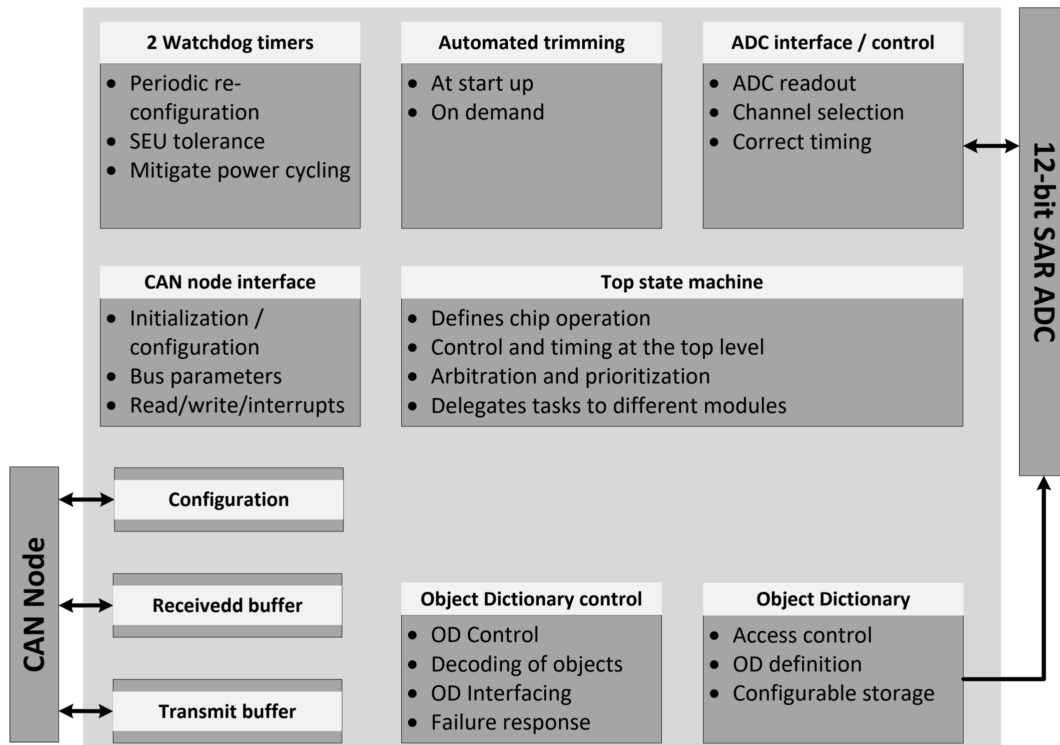


Figure 6.12: Abstract view of the digital logic on-chip

Alexander Walsemann did the physical implementation part of the digital design from Fachhochschule Dortmund. The chip's digital part is designed to keep it as small as possible, i.e., to implement only constructs that are absolutely necessary for the DCS application. This also reduces the complexity of the design. The logic, however, allows easier extension to include more constructs in the future if required. The digital part of the MOPS chip provides everything related to the CAN and CANopen protocol implementation, ADC interfacing, Automated trimming control unit, etc. The Moore Finite State Machine (FSM) concept is used everywhere in the logic for the state machines, which means the output is defined by the current state only. Mentor Graphics's HDL designer [52] and Questasim [53] have been used extensively to define the state machines graphically and to verify the design, respectively. Verilog 2005 [54] has been used for the complete design, while Systemverilog [55] has been used for verification purposes.
Figure 6.12 shows an abstract view of the complete digital logic.

- The hierarchical topmost logic that controls the complete behavior of the chip is the Top-state machine. A simplified abstract view is shown in Figure 6.15.

It defines the top-level chip operation, arbitrates, delegates tasks, and defines priorities for operation among other state machines and digital blocks.

- The Object Dictionary and the Object Dictionary control blocks are a combination of state machine, sequential, and combinational blocks to realize the CANopen in hardwired logic. Shown in Figure 6.16 and Figure 6.17 is an overview of the sub-blocks. The implemented CANopen logic is flexible and allows future integration of other CANopen constructs to enhance functionality.

- The ADC interface logic takes care of the timing and signals to ensure the correct read-out of the ADC data.

- There are two watchdog timers on the chip, which ensure safer operation and mitigate SEU effects to avoid frequent power cycles or data corruption. They are triggered by malfunctioning or inactivity on the chip.

- The CAN interface unit is responsible for initializing, configuring, and controlling the CAN node. There are two buffers to hold the incoming and outgoing messages.

More details about the blocks are described in the following sub-sections.

6.4.1 Initialization scheme

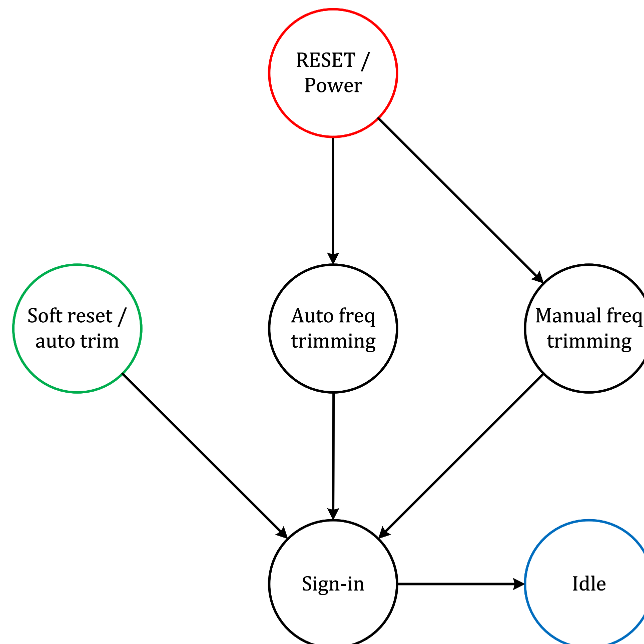


Figure 6.13: Initialization scheme at the top-level logic

Figure 6.13 shows the initialization scheme at the top-level Finite State Machine (FSM). The chip is initialized after the power-up to have the correct information related to the CAN bus timing and other registers, along with important information for proper functionality. Although the CAN node part of the chip allows different configurations of the bus timing by providing configuration registers, the top-level logic of the chip loads these configuration registers during power-up using hardwired values defined in a combinational block shown as Configuration in Figure 6.12. The reason for loading configuration registers using hardwired values from another block is to initialize the chip itself without any external signals/communication protocol. If required, this also provides the flexibility of changing the timing values quickly at the top level in later versions of the chip. In addition to that, hardwired values make the chip more tolerant to the SEUs by refreshing the configuration periodically. The chip does frequency trimming either manually by reading values defined on the external pads or automatically by reading incoming CAN messages. If the automated frequency trimming procedure is enabled, the chip loads configuration by decoding the incoming CAN message but only sends a sign-in after the trimming. If the feature is enabled but no message is sent over the bus within ≈ 4 to 6 s, depending on the default frequency, the watchdog timer forces the chip to use the default frequency on-chip and then generates a sign-in message. The simulation in Figure 6.14 shows

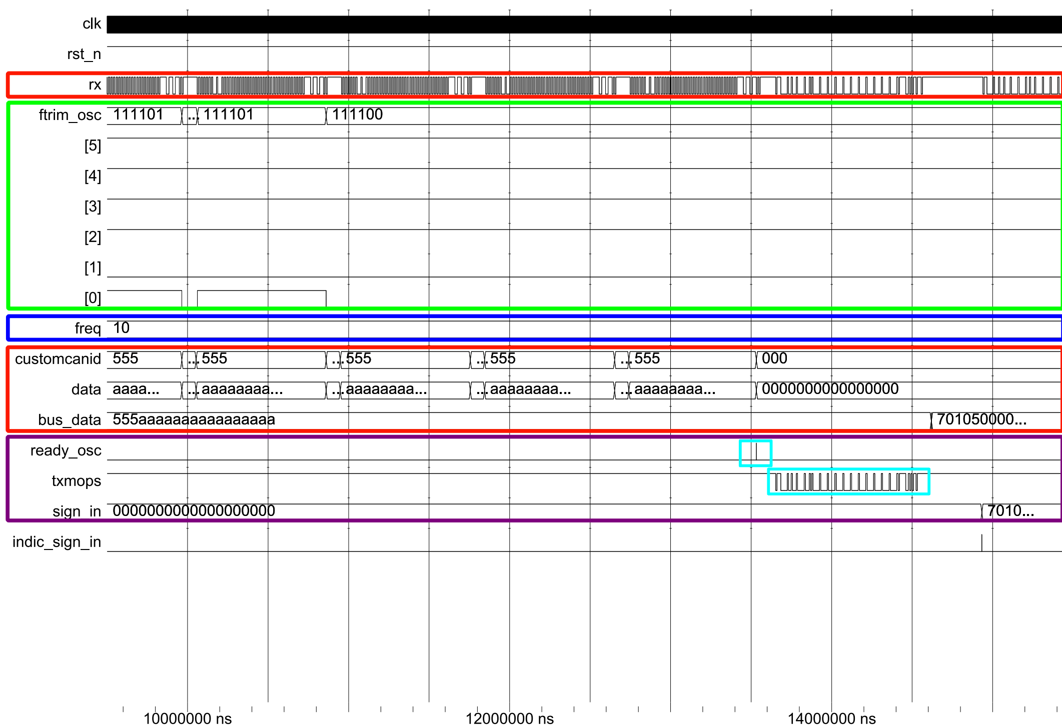


Figure 6.14: Sign-in after the automated trimming procedure

when Automated trimming is enabled during chip powering. Signals in the red blocks show transition on the CAN bus and corresponding data. In the automated trimming

configuration mode, the chip requires frequent transitions on the bus to detect the mean frequency. This can be realized by sending alternating bits on the CAN bus. The blue block shows a trimmed frequency of 10 MHz on the bus. An active high 'ready_osc' signal in the cyan-colored block indicates when the chip is ready, and 'txmops' represents the signal where the MOPS chip drives the bus to send the sign-in message. The sign-in message from the MOPS gets decoded on the bus with an ID of '701'.

6.4.2 Top level state machine

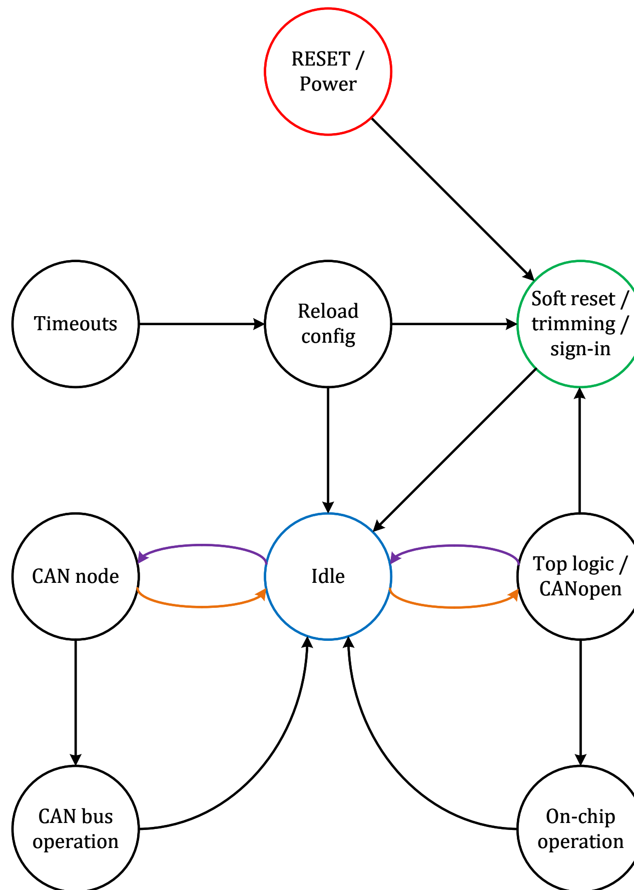


Figure 6.15: Top-level FSM to define the operation of the MOPS chip

A simplified abstract view of the top-level FSM, which controls the behavior of the MOPS digital part, is shown in Figure 6.15. It defines the overall operation of the chip, delegates tasks to the other state machines in the logic, and ensures that the chip is always in listening mode, even during the sampling of an ADC channel. It bridges the CAN bus logic, the CANopen logic, and the ADC on-chip. After the initialization phase shown in Figure 6.13 ends, the chip goes into the 'Idle' state. The

chip stays in this state until an interrupt signal tells the FSM to read or send a new message. Whenever a new message is ready to be read/written to the CAN bus or the CANopen side, the FSM delegates these tasks to corresponding logic blocks and returns to the 'Idle' state. Both watchdogs on the chip can bring the top FSM back to the 'Idle' state.

6.4.3 CAN node interface

The CAN node has a register-based interface to store timing and masking configuration specific to the bus. The top-level logic has three blocks to interface with the CAN node.

- An interface FSM to control operation and handshake signals in a synchronous manner
- An interface block that has both sequential and combinational logic to provide data buses to read/write CAN node as well as to get configuration data from the initialization block
- The third block is purely combinational to prioritize the incoming messages

The CAN node takes care of the ID arbitration over the bus, which is insufficient. This only defines which message has the highest priority at any given time, so it gets access to the bus first. In the case of the MOPS, the processing time of a single message on the chip is approximately 1.3 ms because of the slow ADC clock. If a new request arrives at the chip when it is already handling the previous request, then the chip must be able to handle the priority based on the COBID shown in Figure 6.5. The SDOs get priority over PDOs, and especially in the case of remote reset requests, the chip will stop doing everything to listen to the bus and automatically trim the oscillator.

6.4.4 On-chip CANopen implementation

Implementing the CANopen protocol requires an Object Dictionary (OD) definition. This is common for the server and all the CANopen nodes on the network. The object dictionary defined for the MOPS chip specifically meets the requirements of DCS monitoring. The requirement was to make the design small and as simple as possible to remain within the space and cost budget defined for the chip. To meet this goal, unnecessary generalized OD entries are not implemented. As explained in section 6.3.2, the CANopen standard uses predefined communication objects to communicate over the CAN network, but not all are implemented in the chip. The CANopen digital block is divided into two sub-blocks. One block defines the complete OD, while the other sub-block implements the interface between OD and the rest of the digital logic. As shown in Figure 6.16, the interface block is further divided into

four sub-blocks that are explained below:

- FSM
- Message type decoder
- Failure response
- Object Dictionary interface

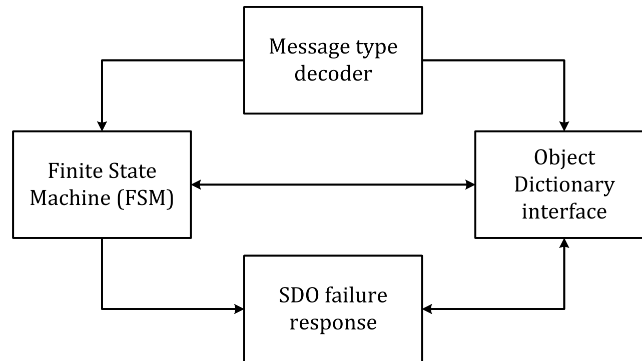


Figure 6.16: CANopen realization in the digital logic

The FSM is responsible for handling tasks related to CANopen communication objects. It controls the signals to instruct other blocks to decode and categorize incoming messages from the received buffer into different communication objects, and it also prepares responses to be written to the output buffer. After receiving the decoded information from other blocks, the FSM defines the handling procedures for different communication objects. It defines SDO expedited transfer and NMT objects in detail. Although PDO, SYNC, and EMCY are the communication objects that are not used in the chip, they are still defined in a limited way, so they can be easily integrated if required in the future.
The 'message type decoder' is a combinational block identifying a newly arrived message in the received buffer. This block generates signals for the FSM to indicate the type of the communication object and provides an index/sub-index to the interface block.
The 'SDO failure response' block is also a purely combinational block that generates failure information in case of an SDO communication failure. A complete list of codes is shown in Table 6.1.
The block 'object dictionary interface' has read and write access to both the received and transmitted message buffers. This block also has the interface to communicate with the OD. The commands to read or write the OD or the data buffers come directly from the FSM. The OD interface block consists of both sequential and combinational modules.

6.4.5 Object dictionary

The Object Dictionary defined in the MOPS chip consists of three blocks, as shown in Figure 6.17. The logic is separated into three units to define entries, access control, and data storage separately. The block that defines all the OD entries for the chip is a purely combinational and very large multiplexer. It gets input signals from the interfacing blocks to address all the entries defined in the large multiplexer. All the constant values are defined as hardwired values, while the writable values are read directly from the block 'stored OD entries'. For each entry in the OD, the large multiplexer also sets appropriate asynchronous access signals, which are then passed to the block 'Access control'.
The 'Access control' block generates synchronous control signals to allow writing new information to the writable registers defined in the OD.
The block 'stored OD entries' holds all the sequential registers defined in the OD. It reads the content of the register passed directly by the multiplexer block and acts on it using the access control signals defined by the 'Access control' block. Values are driven back as feedback to the multiplexer block.

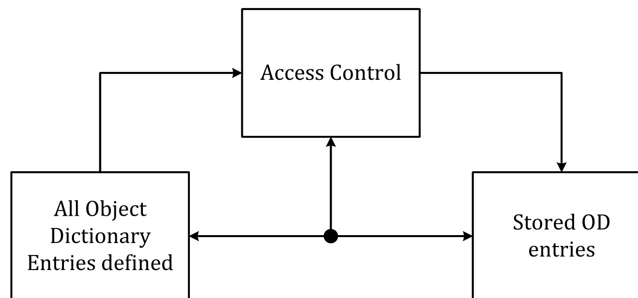


Figure 6.17: Object dictionary to define communication objects

6.4.6 ADC Interface

The MOPS chip does not store ADC values except the current value in the transmit buffer register. The current value is stored for a very short time before transmitting it over the CAN bus. The chip uses SDO expedited transfer to transmit monitoring values, so at any given time, a single CAN message can hold information for only one monitored value. The OD defines separate entries/indexes for each monitoring channel. The ADC on-chip works using a 10 kHz signal which is scaled down from the main clock of 10 MHz. Only one of the twelve ADC bits is sampled during a single clock cycle. This makes the ADC very slow compared to the rest of the digital logic and CAN communication; therefore, storage of monitoring data is not required. This reduces the size of the digital logic and the probability of monitoring data corruption due to SEUs. The ADC interface has an FSM to respect signal timing and a combinational block to translate OD indexes to select a respective ADC channel. 35 out of 40 channels are used on the MOPS chip. Instead of using a multiplexer, the ADC

on-chip uses 40 separate lines to activate one of the channels. After a new message arrives in the received buffer register, the index and sub-index of the OD are directly defined and mapped to the respective ADC channel. To ensure correct read-out, a channel is selected many clock cycles before the start of the conversion signal.

6.4.7 Watchdog timers

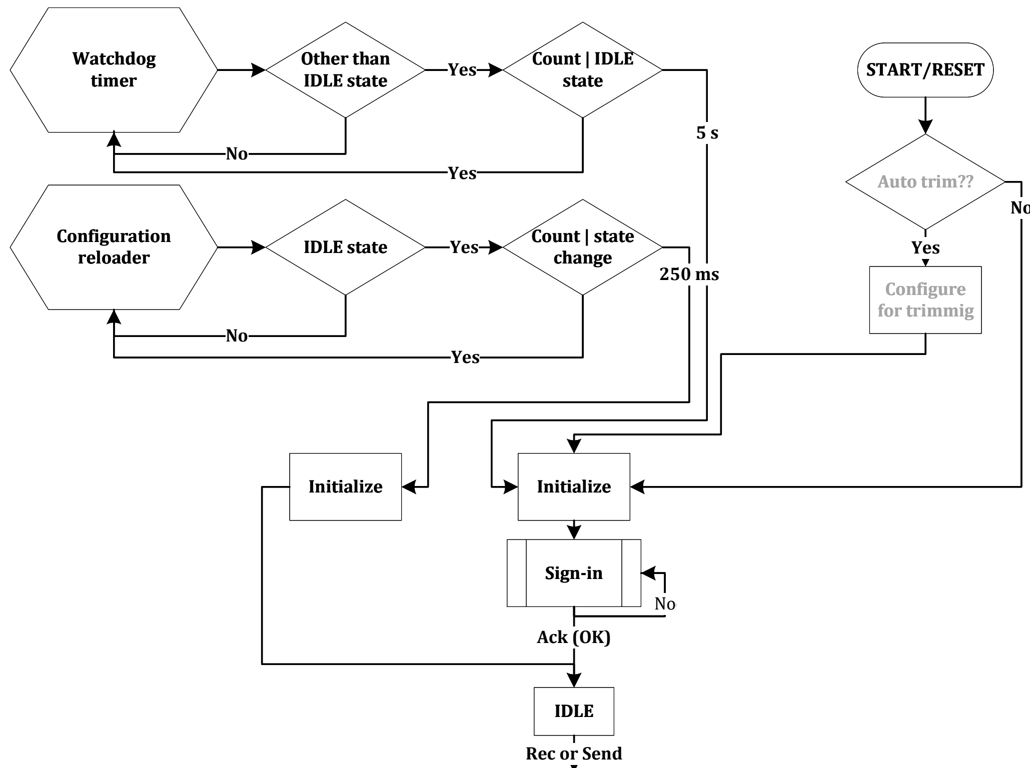


Figure 6.18: Watchdog timers available on the chip

Figure 6.18 explains the logic of the watchdogs available on the MOPS chip. Two watchdogs are available on the chip: the watchdog timer and the configuration reloader. The times mentioned in the figure are w.r.t. the on-chip frequency of 10 MHz. An important point about the watchdogs is that none of them takes the chip into the mode that requires Automated trimming once again. This is to avoid the scenario where the MOPSHUB [20] does not know that the chip has gone into the trimming mode. Both watchdogs do not reset configurable storage in the OD, which also holds values for the oscillator trimming and trimming of the DAC network inside the ADC. Upon activation, the watchdog timer triggers a sign-in message, but the configuration reloader reloads without indication.
The watchdog timer mainly looks for any malfunction in the internal logic of the

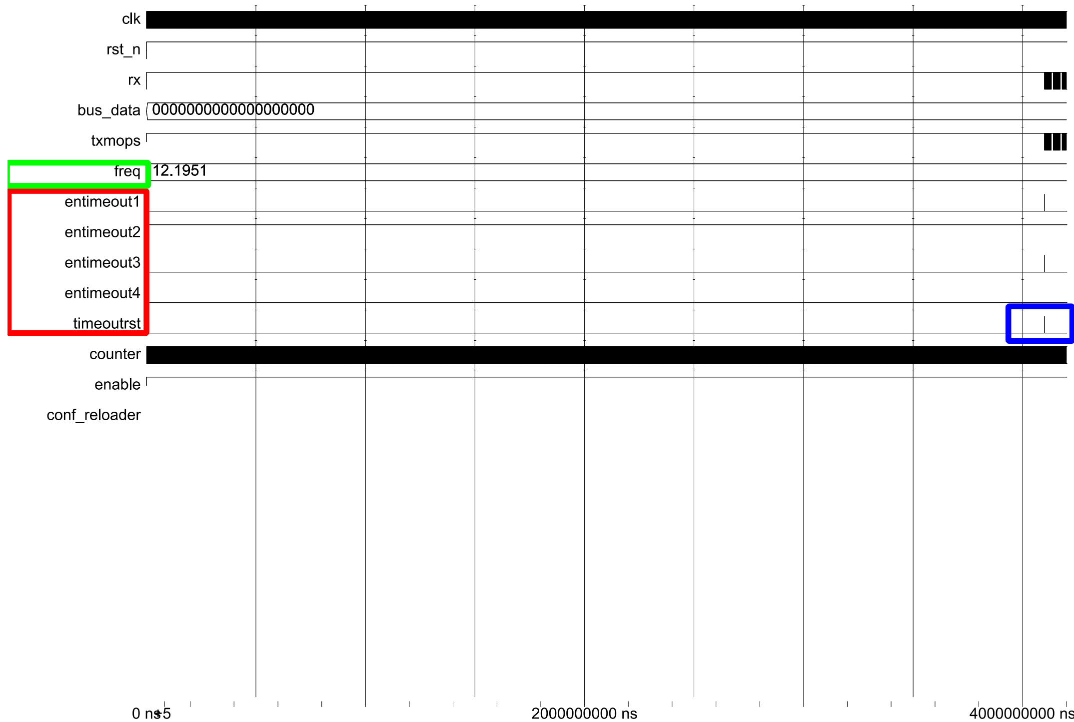


Figure 6.19: Watchdog timer on the MOPS chip to reset the state machines

chip by continuously monitoring all the state machines at the top level. If any of the top-level state machines remain in a state other than 'Idle' for more than 5 s, then the watchdog timer triggers a soft reset. Depending on the frequency, the watchdog timer releases a soft reset signal for all the state machines after 5 s given the condition that the on-chip frequency is 10 MHz. The timeout counter changes accordingly if the frequency is other than 10 MHz on the chip. After the reset, the chip initializes itself and sends a sign-in message. The watchdog timer makes sure that all the state machines never remain stuck in a locked state due to a bug or an SEU. Shown in Figure 6.19, the red block shows four 'entimeout' signals generated from all four state machines at the top-level logic to indicate their current state and the green box shows the current frequency of the chip. There is a logic 'OR' between all four signals. If any of the four signals is 'True', the output will become 'True'. Here, the 'entimeout2' is True while the other three are 'False'. Around ≈ 4.125 s, the 'timeoutrst' signal in the blue block is generated to trigger a reset for all the state machines. Figure 6.19 shows the scenario where no trimming configuration was provided to the chip after a power-up. The watchdog timer prevents the chip from waiting forever for the automated trimming. The configuration for the chip is loaded in the same way as shown in Figure 6.21(explained in the next paragraph).
The configuration reloader is a second watchdog available on the chip. It checks for conditions opposite to the watchdog timer where a state machine remains in the 'Idle' state for too long. This indicates no activity happening in the digital part of the chip.

This is normal but can also be due to the lack of CAN communication on the CAN bus. An SEU can change the timing configuration on the CAN node, which results in errors on the bus, ultimately leading to the Bus-off state where the CAN node remains silent and does not participate actively. The configuration reloader reloads the CAN node configuration and resets all the state machines after every 250 s of no activity in the digital part. This process does not interrupt the CAN message reception because the reload time is less than one bit wide on the CAN bus and is completely independent of the process happening on the CAN node to decode bus communication. As shown in Figure 6.20, the red box shows the important signals from the register-based interface of the CAN node. The signal 'addr' represents the address of the registers holding configuration, 'data_init/config' are values provided to the registers, whereas 'write' is the control signal. The green box shows the four 'reload' signals fed by the four state machines to indicate the current state. There is an 'AND' logic between the four signals. The 'reloadconf' marked in the blue box goes high around 267 ms of simulation time. The exact time is dependent upon the on-chip frequency. A zoomed-in simulation of the actual configuration reloading is shown in Figure 6.21. The red block shows the write signal, address, and data written to the CAN node. The counter shown in the blue box starts counting again after the reloading is finished.

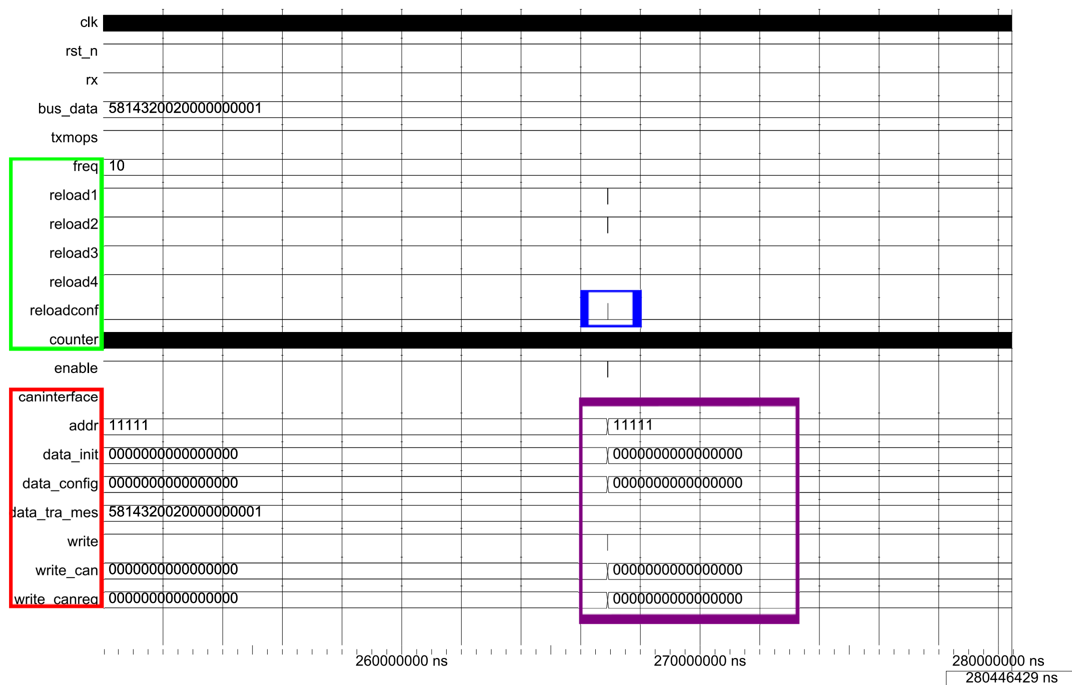


Figure 6.20: Configuration reloader activation due to no activity on the bus

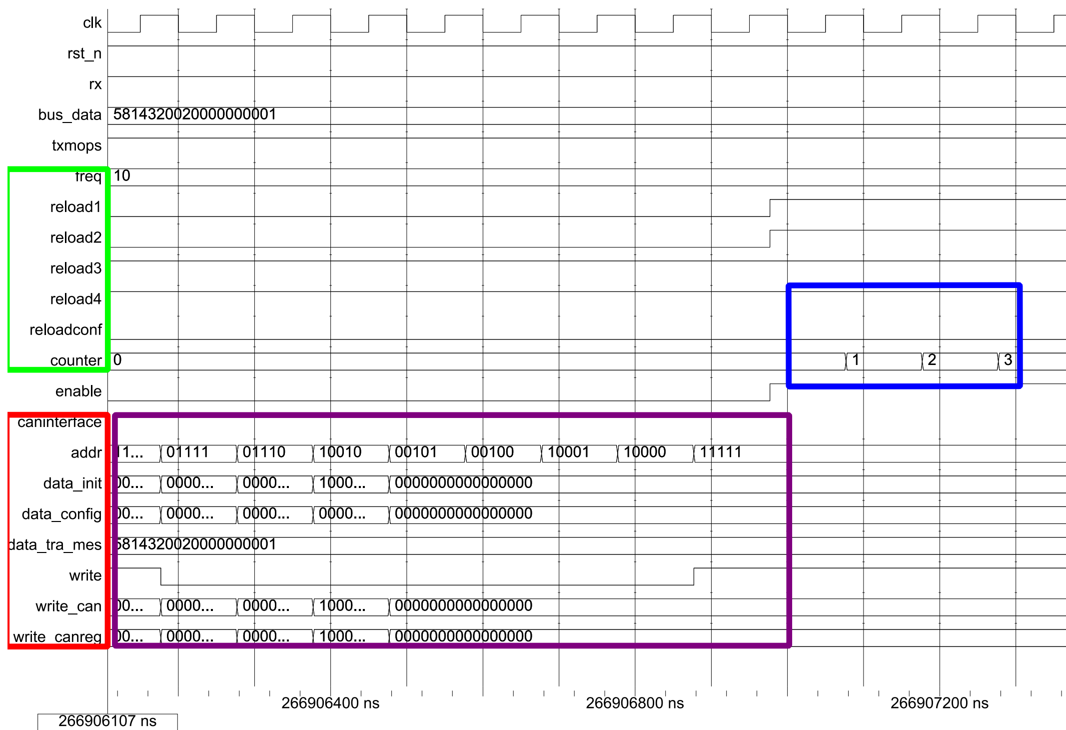


Figure 6.21: Configuration reloader signals to reload the CAN node configuration and resets state machines

6.4.8 Automated Oscillator trimming

The Automated trimming is only done after the power-up and after the remote reset request explained in section 6.3.2. Non other than the above two conditions can make the chip go into automated trimming mode. After a remote reset request, automated trimming is done to mitigate power cycling due to an SEU or a frequency shift due to temperature/radiation effects. Figure 6.22 explains the logic flow for two scenarios when the automated trimming is triggered. After the power-up, the chip enters the configuration mode if automated trimming is enabled. After finishing the trimming, the chip initializes, sends a sign-in message, and then remains idle. A second scenario is when a chip receives a message that does not match its node ID. If the ID of the message is zero, the chip understands it as a remote reset command, irrespective of the data in the frame. This remote reset brings the chip into configuration mode. A prerequisite for the remote reset is that the deviation in the on-chip frequency must be within 3 % of the mean frequency of 10 MHz. If the frequency shift happens on the chip, then this can be very easily detected by the MOPSHUB [20] by looking at error counters on the bus. In case of large error counters, the MOPSHUB can initiate a remote reset request autonomously and independent of the central DCS. This can trim the oscillator on-chip, eventually saving an extra power cycle. The remote reset command has proven helpful during the irradiation and temperature tests. Details are described in Chapters 8 and 9. The control block for the Auto trimming feature is designed by Michael Karagounis (FH Dortmund), whereas the top-level and OD integration are done within the scope of this thesis.

The automated oscillator trimming procedure makes use of the information provided by the bit timing block in the CAN protocol unit. As shown in Figure 6.23, the CAN standard splits bits into several-bit time quanta. These bit time quanta are grouped into segments. The falling edge of a new dominant bit is expected to happen on the CAN bus during the synchronization segment. If the falling edge arrives in phase segment 2, then it is considered early, and a negative phase error is assigned. If the falling edge occurs in the propagation segment, it is considered delayed, and a positive phase error is attributed. In the CAN bit timing unit, this phase error is used to enlarge or shorten the bit-time accordingly to ensure phase synchronization between the sender and receiver.

As shown in Figure 6.24, in the MOPS chip, the phase error e extracted by the CAN bit timing unit is forwarded to the control block of the automated trimming system, which is implemented as a digital Proportional–integral (PI) compensator. The phase error e is multiplied by a configurable constant K_P and, in addition, integrated into a special accumulation register and multiplied afterward by the configurable constant K_I. The result of this operation is forwarded as a 6-bit trimming code to the relaxation oscillator. The oscillator output clocks the whole MOPS chip and, in addition, is scaled down by a prescaler to the frequency, which gives rise to the required CAN bus data rate. The pre-scaler clocks the CAN bit-timing unit, which defines the correct time point to sample the CAN bus or transmit a new bit on the CAN bus.

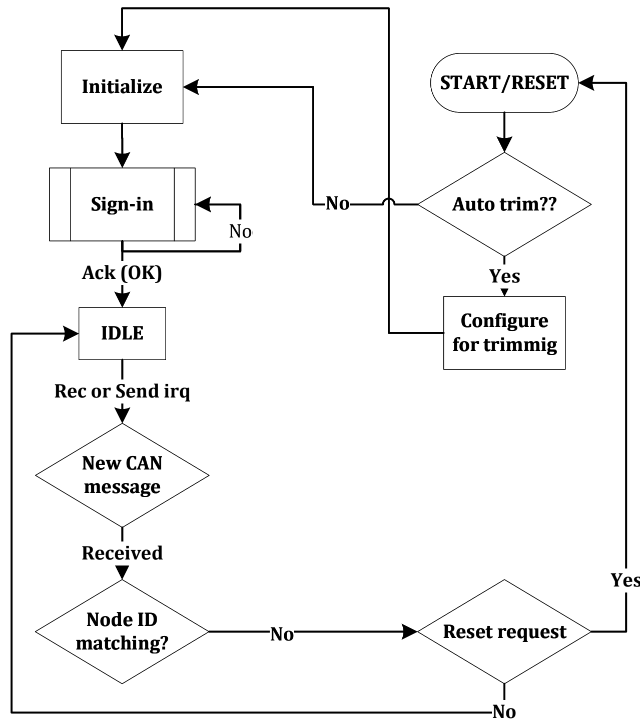


Figure 6.22: Automated trimming procedure of the MOPS chip

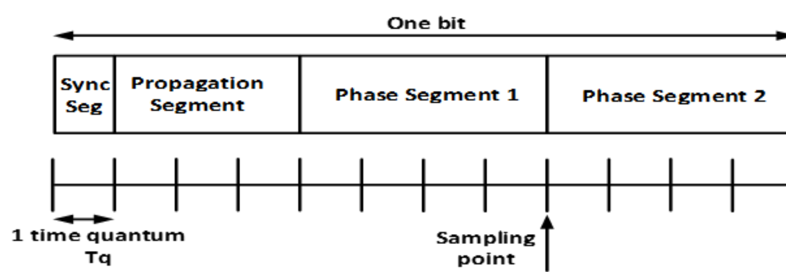


Figure 6.23: Bit Timing defined in the CAN protocol

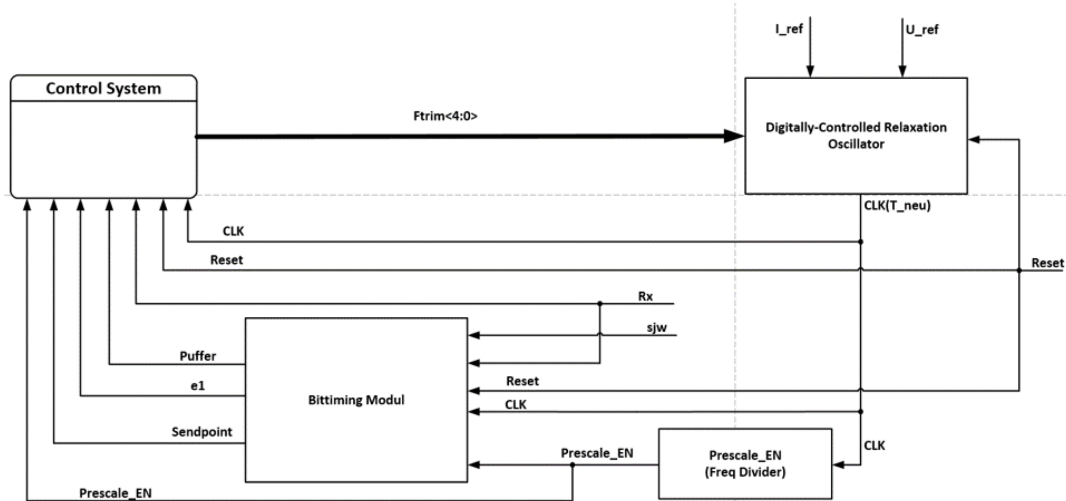


Figure 6.24: Block diagram of the automated frequency trimming system

When a pad signal configures automated trimming, the procedure starts after power-on-reset and lasts for fifteen CAN frames. After fifteen CAN frames, the trimming procedure is switched off. The trimming procedure can be restarted using the remote reset command by sending a message with ID '0' over the bus [56].

Figure 6.25 shows the trimming of the oscillator after power-up. The green box shows six trimming bits, while the blue box shows the actual frequency. Here, a digital model of the oscillator is used for simulation purposes. The 'rx' signal in the red box shows CAN bus transitions while the 'bus_data' shows the actual message in hexadecimal. Figure 6.26 shows the automated trimming upon remote reset. The first instance of trimming is done after power-up and then upon remote reset command. The cyan-colored box shows the 'read_osc' signal going high after fifteen CAN frames on the bus to indicate the end of trimming.

6.4.9 Controller Area Network (CAN) protocol unit

The CAN protocol unit of the MOPS chip is called Canakari. Michael Karagounis developed it during his studies at the FH Köln [57]. The design was later improved over the years within the scope of the Bachelor's/Master's thesis. The digital logic was written in VHDL but later translated into Verilog by Philip Ledüc during his studies at FH Dortmund. The reason for translating the design into Verilog was to achieve Triple Modular Redundancy (TMR) implementation as the TMRG tool [58] available from CERN only takes Verilog designs as input. Alexander Walsemann and Philip Ledüc from FH Dortmund contributed to verifying the CAN node part in the MOPS chip.

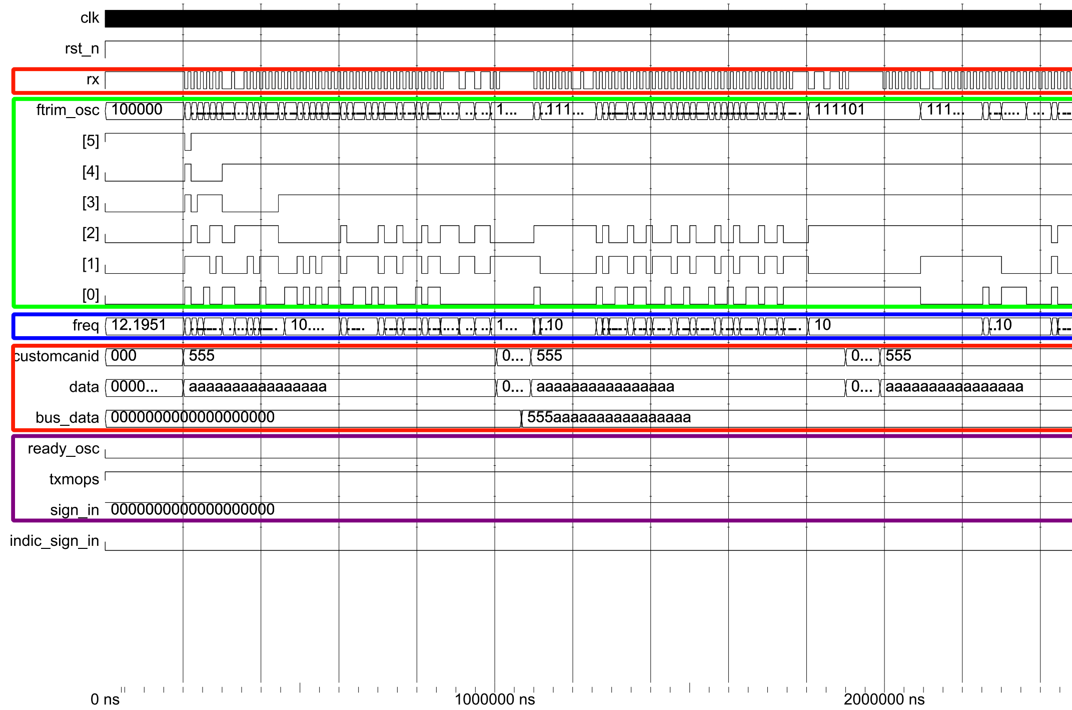


Figure 6.25: Automated oscillator trimming after power is supplied to the chip

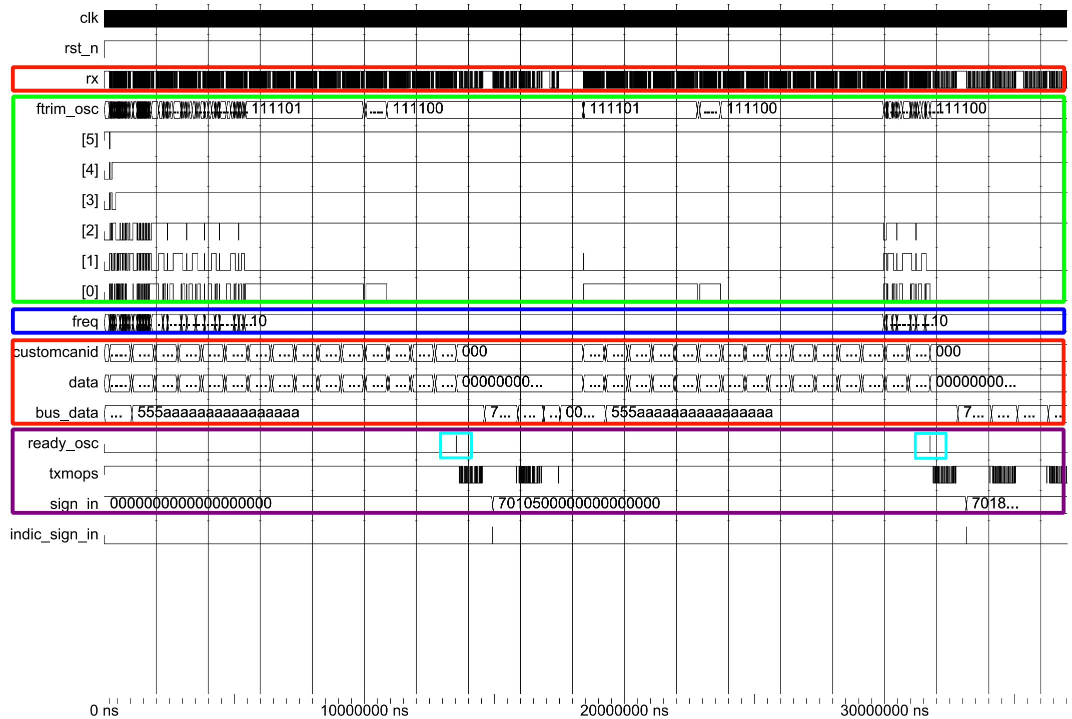


Figure 6.26: Automated trimming after a remote reset command

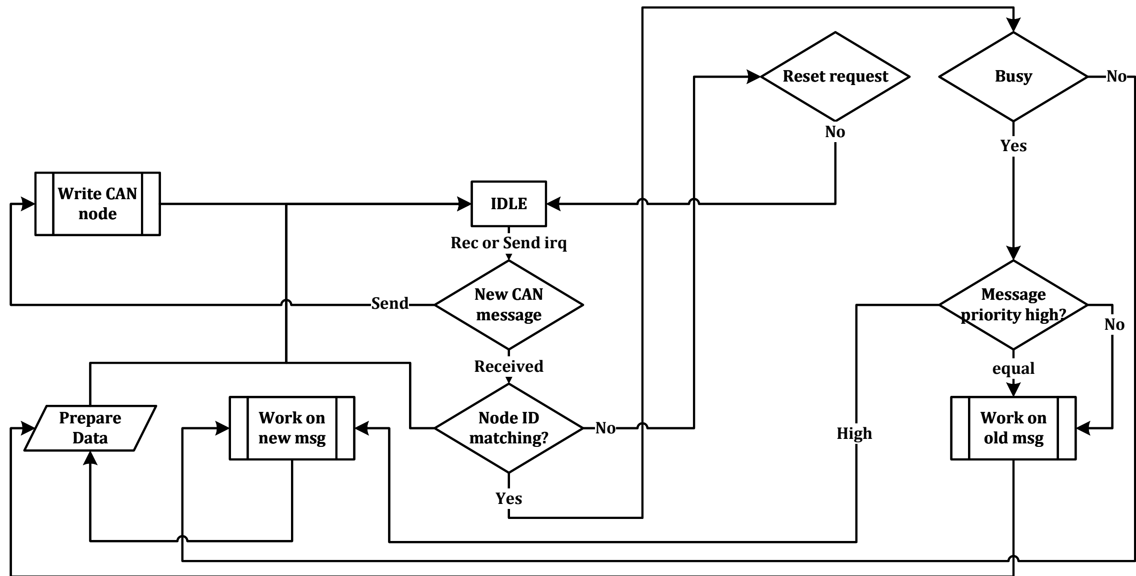


Figure 6.27: CAN message handling by the MOPS chip

6.4.10 Data buffers

There are two data buffers in the chip to send and receive data. Both buffers are 75-bit wide to store the CAN frame identifier and actual data without the protocol overhead. Like the other digital logic, data buffers are also completely triplicated to protect against SEUs. Figure 6.27 illustrates the chip's handling of incoming messages. If there is no ID match, the frame is checked for the remote reset command. If the ID of the node matches, the chip compares the message that is currently worked upon with the incoming message to decide priority. At any given time, the chip works on a single message with the highest priority.

6.5 Design techniques for a robust MOPS digital logic

The MOPS chip was developed entirely using industry-standard tools and known methods to implement a digital IC. However, the development of the complete logic at every stage of the development process is inspired by the fact that it should be very tolerant of SEUs and other failures. The SEU tolerance here refers more to the system-level reliability and operational stability than the mere corruption of some monitored values. Another important point is to make the logic small and as simple as possible to keep it economical regarding size, cost, and power consumption. Below are some important points about the MOPS digital part to make it robust.

- The complete digital design has been triplicated to make the chip tolerant to SEUs [58]. Figure 4.8 shows the actual implementation. Every combinational

signal is triplicated and then fed to the sequential logic. There are three voters instead of just one to reduce further the probability of a Single Event Transient (SET) happening at the output of a single voter. In addition, the triplicated cells are placed with at least 15 µm [36] apart to defend against multiple-bit upset where data of more than one storage cell gets corrupted, and there is no longer a possibility to correct it.

- Two watchdogs continuously monitor all four state machines on the chip. Their operation in detail is explained in Section 6.4.7. They protect against both cases where either the top-level logic gets locked due to an SEU/error or the CAN node configuration changes. Only the watchdog timer can send a sign-in message, but this can happen earliest after 5 s, the maximum time frame for all the DCS monitoring values to get updated. In case of an unknown failure, the watchdog timers can not spam the bus with unnecessary sign-in requests.
- A change in the frequency due to radiation/temperature changes can be detected by the MOPSHUB. The error registered by nodes on a CAN bus depicts the state of the communication. Due to a frequency change, many errors appear on the bus. A remote reset request from the MOPSHUB can be used to trim the chips once again without a power cycle. The automated trimming feature in the MOPS chip is a completely customized solution not defined by the CAN or CANopen protocol.
- Initialization of the digital logic is partly hardwired. Although the CAN node configuration must be written to the registers, it is defined using hardwired values in a combinational logic. These values are loaded during power-up, time-outs, or on a custom remote reset command. The chip neither requires a flash memory nor depends on any external interface/protocol to initialize.
- The design is kept modular for the CANopen implementation, the CAN node, OD, and the ADC to allow for easy integration of other constructs in the future. The functionality can easily be extended in the future.
- The digital design of the chip and the physical layer to communicate over the bus are independent of each other. This allows the user to choose an external standardized physical layer, and a commercial CAN controller can use the low-voltage MOPS physical layer.

6.6 Improvements in the digital design and new features in the MOPSv2

The digital logic of the MOPSv1 chip had some functional problems. The problems in the MOPSv1 were not large enough to hinder the core functionality.

- The sign-in message is described in Section 6.3.2. Shown in Figure 6.6, the MSB of the sign-in message must be 0, and it toggles every time a new node

guarding request is sent. The MOPS chip sends a sign-in message with the correct MSB, which is 0 and keeps sending this on the bus until it receives an acknowledgment. It is observed during the testing that if MOPS doesn't get an acknowledgment, then after a couple of sign-in messages on the bus, the bit toggles automatically, which should not be the case.

- There was a problem with the remote reset request functionality of the MOPSv1 chip. When an ID '0' is sent over the bus, then it should cause every MOPS chip connected to the bus to reset its state machines. After working on the reset request, the chip should respond with a node guarding response explained in Section 6.3.2, but the MOPSv1 chip sends back the last message stored in the buffer register. If the last message sent out by the MOPS chip was a node guarding message, then the MSB toggles for every new reset request.
- The watchdog timer on the chip acts only on the top-level state machine instead of all four state machines in the design.

In addition to all the bug fixes required for the MOPSv1, the chip also introduces some new features, which are listed below:

- Automated trimming of the Oscillator
- Refresh configuration registers automatically if the MOPS chip remains idle for more than 250 ms
- In case of a frequency deviation, there is a remote reset request to trim the oscillator without a power cycle

6.7 Digital logic verification and full-netlist simulation

As shown in Figure 6.28, the block diagram of the testbench has been written in the SystemVerilog to verify the chip's digital logic and run a full-netlist simulation of the whole chip before fabrication. The scheme of the testbench is such that a virtual CAN bus is defined as one that connects all four main entities. .

- A driver/generator acts like a master node that generates requests for the MOPS chip and generates constrained randomized messages. This module is very generalized and needs input about the message content from another block to generate CAN messages according to the standard.
- A large GUI-based FSM is defined using the Mentor Graphics HDL designer. The FSM can be easily modified using the GUI tool to change test scenarios, content and type of messages, randomization, and timing of the frames presented on the virtual bus.
- The MOPS chip is connected to the virtual CAN bus, where it reads every frame sent by the generator. The chip decides for itself whether the message

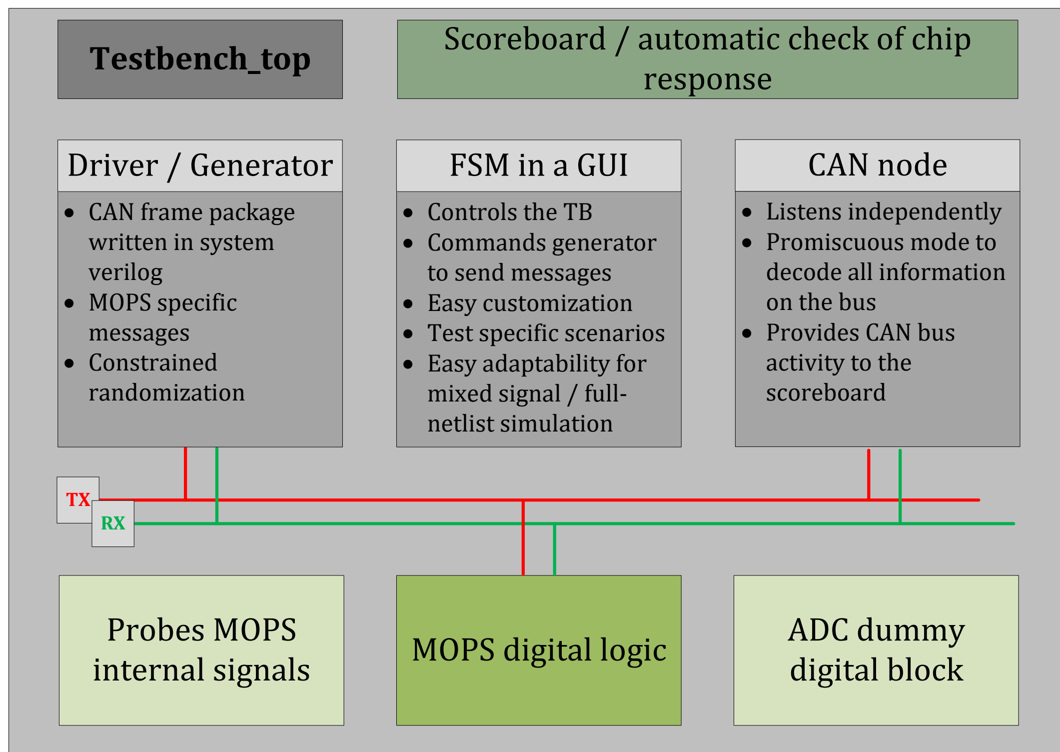


Figure 6.28: Abstract view of the full chip test bench

is important or not. If a message is important to the chip, it acts on it and responds.

- A third independent CAN node is also connected on the virtual bus to decode frames from either the generator or the MOPS chip.

An ADC dummy module provides values to each ADC channel on the chip, whereas another module probes other essential signals from the chip. The testbench generates thousands of CAN messages to test the chip's response. Some messages are targeted to test particular responses or functionality of the chip. In contrast, constrained randomized messages are also used to ensure the chip does not go into a bad state. A scoreboard is defined to automatically verify the functionality without looking into each signal in the simulation. The scoreboard prints all activity on the CAN bus and categorizes the MOPS response into good or bad.

6.8 Analog block

The analog part of the chip includes a power-on-reset circuit to ensure the digital part is in the correct start-up state. A bandgap reference circuit and a voltage regulator provide the chip with a stable reference voltage and supply voltage, respectively. The chip also includes an oscillator to locally generate a clock signal for the digital part. There is also a CAN physical layer to convert digital logic levels to appropriate voltages over the bus.

6.8.1 Power-on-Reset generator

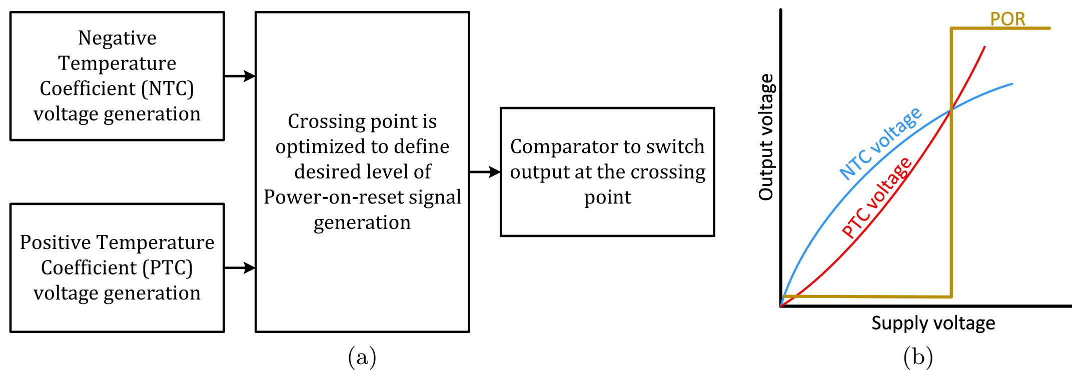


Figure 6.29: Generation of an on-chip temperature and process independent Power-on-reset signal

A Power-on-Reset(POR) circuit on the chip ensures that the complete digital logic starts in a known good state. It generates a reset signal when the power to the chip is applied. The reset signal is kept in an active state until the supply voltage is completely stabilized. A process and temperature tolerant Kuijk cell bandgap reference

[59] based POR using Dynamic-Threshold(DTMOS) transistors for better matching [60] has been developed for the MOPS chip. The concept of the POR is partly derived from [61]. Figure 6.29 shows the basic circuit topology to implement the design where a Negative Temperature Coefficient (NTC) voltage and a Positive Temperature coefficient voltage (PTC) voltage are generated. The crossing point of the PTC and NTC voltages can be used to invert the output of a comparator circuit. Since the crossing point of PTC and NTC define the release point of the reset signal, the output of the POR circuit is temperature-independent. A temperature-independent source is mostly also process-independent because most of the process parameters are dependent on temperature [62]. The original POR using this approach was designed in [51] for the PSPP chip [46] using the Global foundries 130 nm CMOS process. This is a reuse of the original circuit adapted to TSMC 65 nm CMOS process.

A current through a forward-biased base-emitter of a bipolar transistor or a PN junction diode is defined as:

$$I_c = I_s \exp \frac{V_{BE}}{V_T} \tag{6.1}$$

Where
V_T is the temperature voltage which is equal to $k\frac{T}{q}$.
Here, k is the Boltzmann's constant and q is the elementary charge.
I_S is the saturation current which is proportional to $\mu k T {n_i}^2$.
μ is the mobility of minority carriers and n_i is the intrinsic carrier concentration. Both μ and n_i are temperature-dependent quantities.

$$\mu \propto \mu_0 T^m \qquad with \qquad m \approx \frac{-3}{2} \tag{6.2}$$

while

$${n_i}^2 \propto T^3 \exp \frac{-E_g}{kT} \qquad with \qquad E_g \approx 1.12eV \tag{6.3}$$

Whereas the saturation current is

$$I_s = bT^{4+m} \exp \frac{-E_g}{kT} \tag{6.4}$$

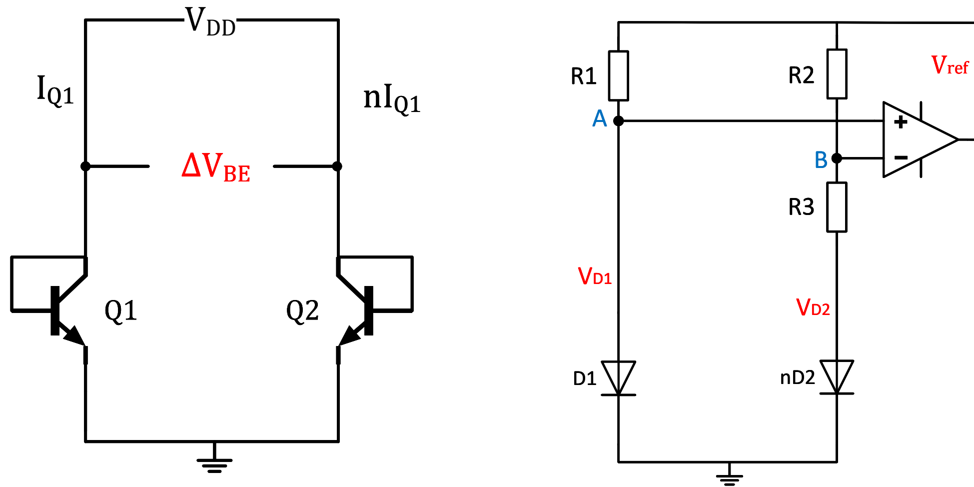
To find the variation of V_{BE} concerning temperature, we can take the partial derivative of base-emitter voltage, which is

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \tag{6.5}$$

The partial derivative concerning temperature will be

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - \frac{E_g}{q}}{T} \tag{6.6}$$

With $V_{BE} \approx 750mV$ and $T = 300K$ equation 6.6 gives us the negative temperature coefficient of $\approx -1.5\frac{mV}{K}$. A $\approx +1.5\frac{mV}{K}$ is required to cancel the effect of the NTC and make it temperature independent [62].
Shown in Figure 6.30(a), the difference of the base-emitter voltage of two transistors operating at different current densities is directly proportional to the absolute temperature, so the voltage V_{BE} calculated in equation 6.9 is a PTC voltage [63].



(a) Positive Temperature Coefficient voltage generation

(b) A basic circuit to generate a bandgap voltage reference independent of temperature

Figure 6.30: PTC voltage and a basic bandgap reference voltage generation circuits

$$\Delta V_{BE} = V_{BEQ2} - V_{BEQ1} \tag{6.7}$$

$$\Delta V_{BE} = V_T \ln \frac{nI_{Q1}}{I_{S2}} - V_T \ln \frac{I_{Q1}}{I_{S1}} \tag{6.8}$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n \tag{6.9}$$

Equation 6.9 exhibits a positive temperature coefficient.
In case more than one transistor is used in parallel, where m is the number of transistors, Equation 6.8 then can be written as:

$$\Delta V_{BE} = V_T \ln \frac{nI_{Q1}}{I_{S2}} - V_T \ln \frac{I_{Q1}}{mI_{S1}} \tag{6.10}$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln(nm) \tag{6.11}$$

Assuming that a temperature-independent voltage can be described by the following equation

$$V_{TC0} = \alpha_1 V_{BE} + \alpha_2 (V_t \ln n) \tag{6.12}$$

Where $V_t \ln n$ is the PTC voltage, which results in the difference of base-emitter voltages. Then the values of α_1 and α_2 can calculated as explained below:

At room temperature equation 6.12 gives us $\frac{\partial V_{BE}}{\partial T} \approx \frac{-1.5mV}{K}$ and $\frac{\partial V_T}{\partial T} \approx \frac{+0.087mV}{K}$
Supposing $\alpha_1 = 1$, α_2 must be chosen such that $(\alpha_2 \ln n)(0.087\frac{mV}{K}) = 1.5\frac{mV}{K}$. This requires $\alpha_2 \ln n \approx 17.2$

Equation 6.12 then can be written as

$$V_{TC0} \approx V_{BE} + 17.2 V_T \approx 1.25 \tag{6.13}$$

The circuit shown in Figure 6.30(b) can be used to add the NTC and the PTC, which are V_{BE} and $17.2V_T$, respectively. For simplicity, the transistors can be replaced by diodes. As shown in Figure 6.30(a) if the voltages V_{BEQ1} and V_{BEQ2} are equalized then the voltage across resistor $R3$ in Figure 6.30(b) will be

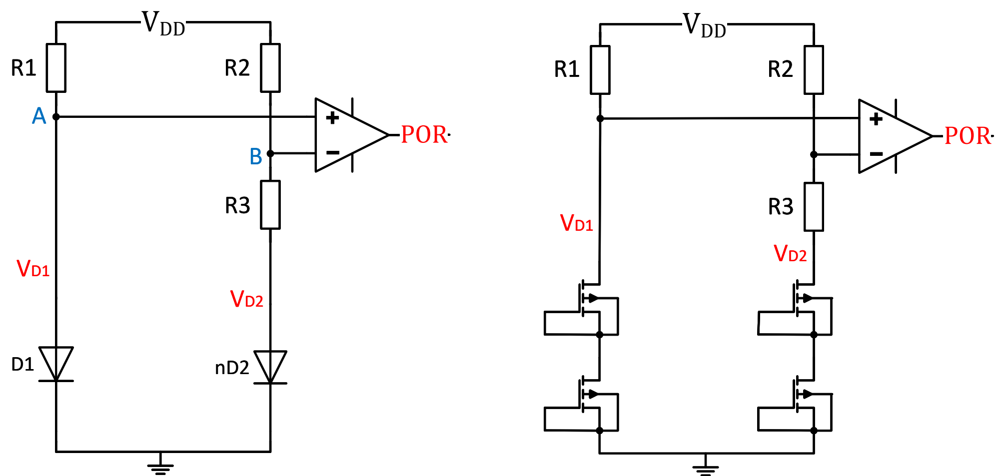
$$V_{R3} = V_{BE1} - V_{BE2} = V_T \ln n = V_{d1} - V_{d2} \tag{6.14}$$

An equal R_1 and R_2 ensure that the voltage at points A and B are approximately equal. From the circuit in Figure 6.30(b), the V_{REF} can be obtained as [62]:

$$V_{REF} = V_{d2} + \frac{V_T \ln n}{R_3}(R_3 + R_2) \tag{6.15}$$

$$V_{REF} = V_{d2} + (V_T \ln n)\big(1 + \frac{R_2}{R_3}\big) \tag{6.16}$$

The bandgap reference circuit shown in Figure 6.30(b) can be used to generate a temperature and process independent POR signal for the digital part. To generate a POR signal, the feedback path can be removed, and a comparator can be used instead of an opamp to switch the output signal at the crossing point of PTC and NTC voltages. Figure 6.31(b) shows the actual implementation in the chip where DTMOS



(a) Power-on-reset circuit based on bandgap reference using diodes

(b) Power-on-reset circuit based on bandgap reference using DTMOSFETS

Figure 6.31: Power-on-reset generation circuit for the MOPS chip

transistors are used for better matching. Two transistors in series are placed to achieve the desired voltage level. The circuit generates an asynchronous reset signal, which is released when the supply voltage to the digital part reaches approximately 930 mV. A comparator circuit designed by Tobias Froese for the CAN physical layer has been reused:

$$V_p > V_n \quad then \quad V_{OUTPUT} = Logic\,high \quad or \quad V_{DD} \tag{6.17}$$

else

$$V_n > V_p \quad then \quad V_{OUTPUT} = Logic\,low \quad or \quad Gnd \tag{6.18}$$

6.8.2 On-chip shunt LDO regulator

An on-chip LDO regulator with a PMOS pass-device that generates a 1.2 V output voltage for load currents of up to 200 mA was designed by Michael Karagounis (FH

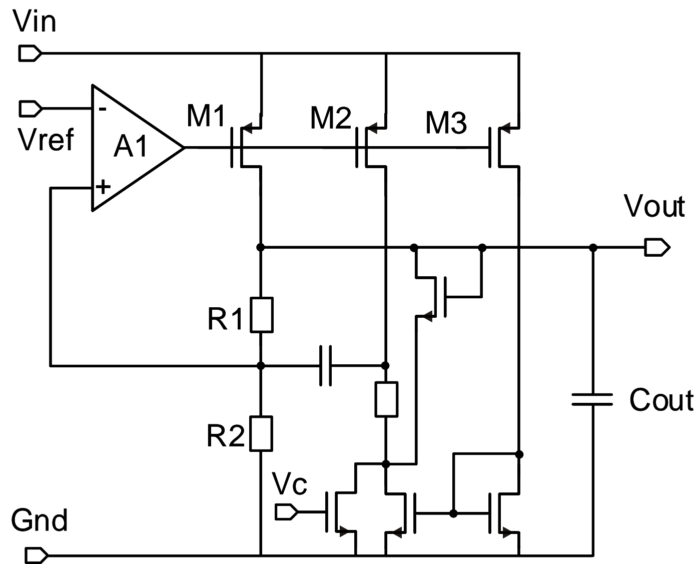


Figure 6.32: Low-Drop Out Regulator [14]

Dortmund). The minimum drop-out voltage is 200 mV, and the circuit is fully cascoded and can tolerate supply voltages up to 2 V. It is an adapted version of the regulator integrated into the pixel chip of the RD53 collaboration with reduced pass-device width [14][15]. As shown in Figure 6.32, the output voltage drop across the resistor R2 is fed to the non-inverting input of the error amplifier A1. The operational amplifier A1 compares the voltage to the reference voltage of 600 mV provided by a bandgap voltage reference circuit. For stabilization, an on-chip compensation circuit is integrated, which injects a charge into the middle tap of the resistive divider whenever a load or input voltage change happens. By this means, the circuit can be stabilized with an external low Equivalent Series Resistance (ESR) capacitor of 2.2 µF [56].

6.8.3 Bandgap reference generator

The bandgap voltage reference circuit is a reuse of the RD53 pixel chip [64]. It has a two-stage architecture to provide over-voltage tolerance and trimming capability simultaneously. The first stage is a bandgap reference voltage circuit with fully cascoded transistor structures that can tolerate supply voltages up to 2 V. Since trimming reduces the over-voltage tolerance, this bandgap reference avoids any trimming functionality, which results in low precision due to uncompensated process variations. This circuit is used as a reference of an LDO pre-regulator, which generates an output voltage of approximately 1.2 V and needs a 100 nF external compensation capacitor

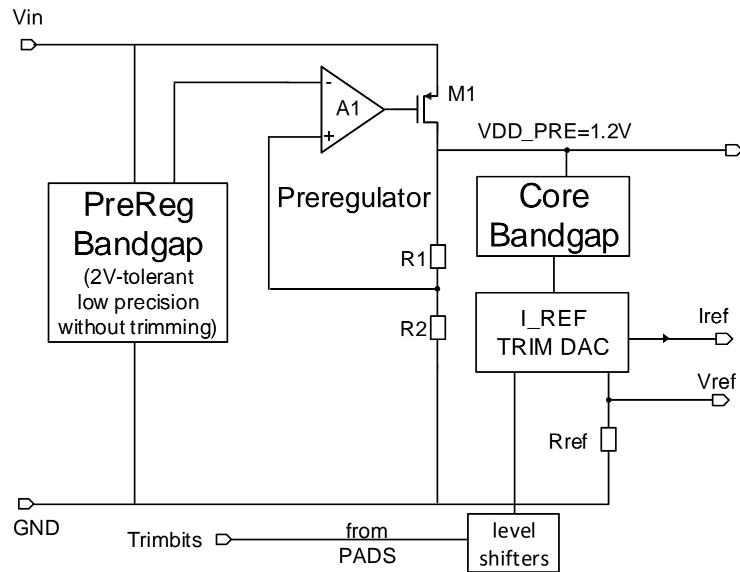


Figure 6.33: 2-stage bandgap voltage reference circuit [56]

at its output. The pre-regulator supplies a high-precision bandgap voltage reference circuit, which generates a reference bias current Iref and the primary regulator reference voltage Vref by means of an external resistor. Due to its high Power Supply Rejection Ratio (PSRR), the high-precision bandgap circuit can tolerate substantial supply voltage variations generated by the low precision of the pre-regulator bandgap. The high-precision bandgap output voltage can be trimmed in a region between 1.0 V and 1.32 V by a 4-bit trimming code provided externally via trimming pads. To avoid any parasitic feedback loop from the supply voltage of the trimming pads to the regulator, because the trimming pads are supplied by the regulator itself, level shifters were introduced [56].

6.8.4 On-chip oscillator

Since in CAN signaling, data is transferred without propagating a clock; the MOPS chip needs its own oscillator for communication and clocking of sequential digital circuits. This clock signal is generated by the relaxation oscillator designed by Michael Karagounis. The circuit diagram is shown in Figure 6.34. The reference current I_{ref} provided by the bandgap reference is steered to charge one of the two capacitors C_1 or C_2. Assuming the signal Q to be low, the capacitor C_1 is charged until the voltage V_{C1} across capacitor C_1 reaches the voltage V_{ref}, which is also provided by the bandgap reference. The voltage V_{C1} is monitored by a comparator and asserts a logical high output signal as soon as the reference voltage is reached. This triggers a D-FlipFlop wired to generate set-reset functionality, which in turn sets the signal Q

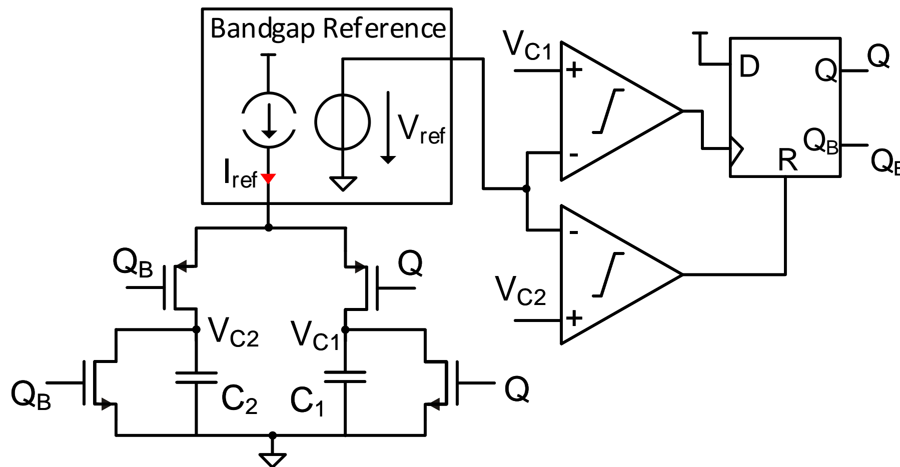


Figure 6.34: Relaxation Oscillator [56]

while it resets the signal Q_B. As a result, the current flow is steered towards capacitor C_2 while the capacitor C_1 is discharged by activation of the parallel connected NMOS. As soon as the voltage V_{CS2} across capacitor C_2 reaches the voltage V_{ref}, a second comparator generates an output pulse which resets the D-FlipFlop and restarts the procedure described above, giving rise to an oscillation with a frequency of 10 MHz. The frequency can be calculated in general by the following equation:

$$f = \frac{I_{ref}}{2CV_{ref}} \tag{6.19}$$

The CAN protocol includes a bit timing re-synchronization mechanism, which allows for stable communication as long as the frequency deviation between the sending and receiving CAN node is less than three percent. To compensate for process variation influencing the oscillation frequency, a trimming option has been introduced. As shown in figure 6.35, the capacitors in the relaxation oscillator, which are charged and discharged during the oscillation operation, are split into a fixed and a configurable part. The configurable part consists of six capacitors of binary weighted capacitance with an NMOS switch transistor in series, resulting in a 6-bit trimming code. This trimming code can either be applied manually by a bonding option on the package level or automatically by a digital control loop that compares the phase shift between the incoming CAN data stream and the oscillator signal. The automatic procedure also allows for compensation of radiation and temperature-induced frequency shifts [56].

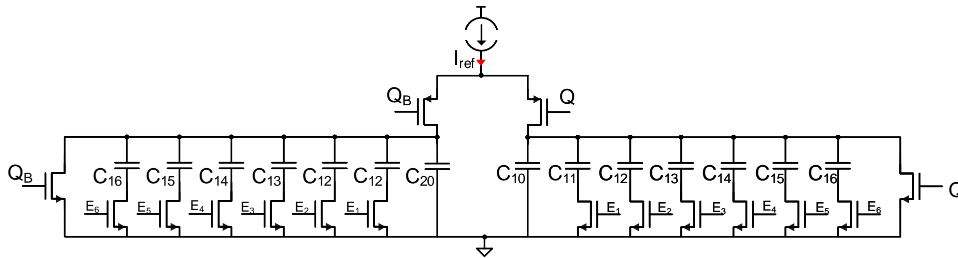


Figure 6.35: Oscillator Trimming Option [56]

6.8.5 Custom low voltage CAN physical layer

The chip communicates over the CAN bus using the standard CAN bus communication protocol defined in the standard [49] and explained in Section 6.3.1, but the electrical signals on the bus are not standard compliant. MOPS communicates using non-standard CAN high and CAN low signals. A level shifter is required to translate and isolate signals from a standard CAN physical layer to the MOPS physical layer.

- Recessive state > logic 1 > $CAN_H = CAN_L = 600\,\mathrm{mV}$
- Dominant state > logic 0 > $CAN_H = 1.2\,\mathrm{V}$ and $CAN_L = 0\,\mathrm{V}$

A low-voltage 1.2 V CAN physical layer has been developed by Tobias Fröse (FH Dortmund) for the chip to communicate over the CAN bus. The reason for the deviation from the standard is the incompatibility between the 5 V high-voltage signals as they are defined in the CAN standard, which require MOS transistors of thicker gate-oxides and radiation hardness demands which require MOS transistors of thinner gate-oxide.

The CAN receiver circuit shown in Figure 6.36 is based on the LVDS receiver design of the FE-I4 pixel chip [65] and consists of two parallel-operated comparator circuits with an NMOS and a PMOS input differential stage to allow a rail-to-rail common-mode input signal range. The transistors M4-M7 and M11-M14 in the decision circuit are not equally sized to introduce a hysteresis of at least 35 mV. The second stages, made of transistors M15-M18 and M19-M22, translate the low-swing signals from the first stages into full-swing CMOS signals and merge the two signal paths. A resistive divider is added to the CAN_H input port to safely detect a recessive bus state for differential input voltages lower than at least 30 mV. To match the RC-time, which is formed by the resistors at the CAN_H network and the parasitic capacitances of the input transistors, an additional resistor R_L of the same resistance is connected to the CAN_L port.

The CAN driver circuit shown in Figure 6.37 consists of a PMOS and an NMOS transistor, which are closed simultaneously to generate the dominant bus state and

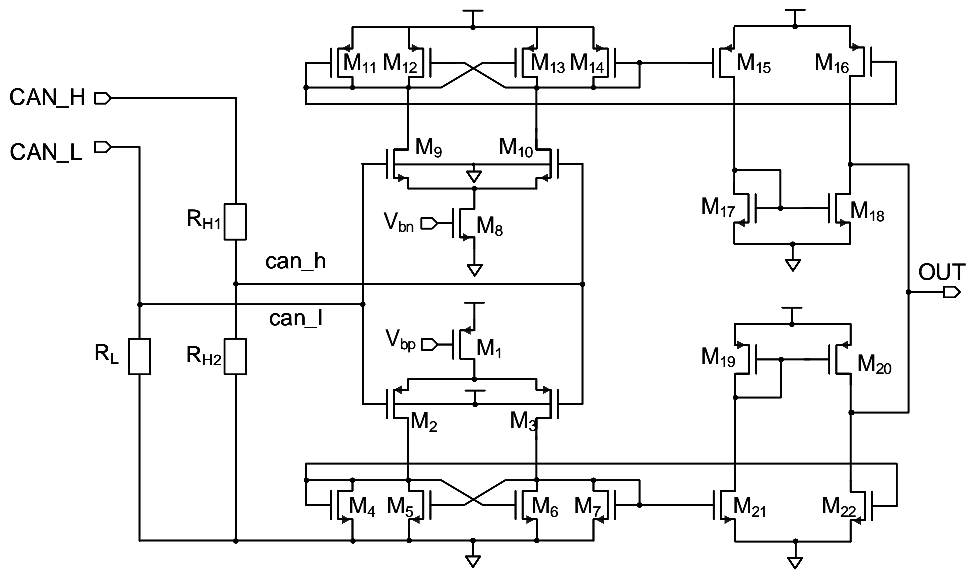


Figure 6.36: Low-voltage CAN receiver circuit [56]

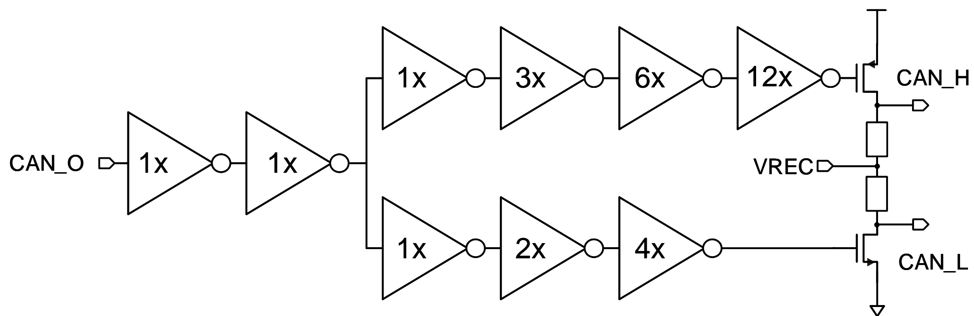


Figure 6.37: Low-Voltage CAN driver circuit

to drive CAN_H to 1.2 V and CAN_L to 0 V. Both transistors are opened in the recessive bus state, and the bus lines reach the VREC potential of about 0.6 V, which is introduced to the driver using two high-ohmic resistors. To provide the same current drive capability, the PMOS transistor has been chosen three times wider than the NMOS to compensate for the lower charge mobility in PMOS transistors. As a result, a three times larger driver strength is chosen to control the PMOS gate than the NMOS gate, which is implemented by inverter chains [56].

6.8.6 Analog to digital converter

To sample voltage monitoring values, the MOPS chip hosts a 12-bit Successive Approximation Register (SAR) based Analog-to-Digital Converter (ADC). The circuit is provided with a reference voltage of 900 mV, which provides a theoretical resolution of 219.72 µV per ADC count. The ADC is silicon proven to be radiation hard up to an ionizing dose of 500 Mrad. The circuit has been designed and tested by the CERN RD53 collaboration [66]. Shown in Figure 6.38 is the block diagram of the MOPS ADC. It provides 40 channels. The MOPS digital logic can address all of them, but due to the limited number of pads available on the package, only 32 are used for external inputs.

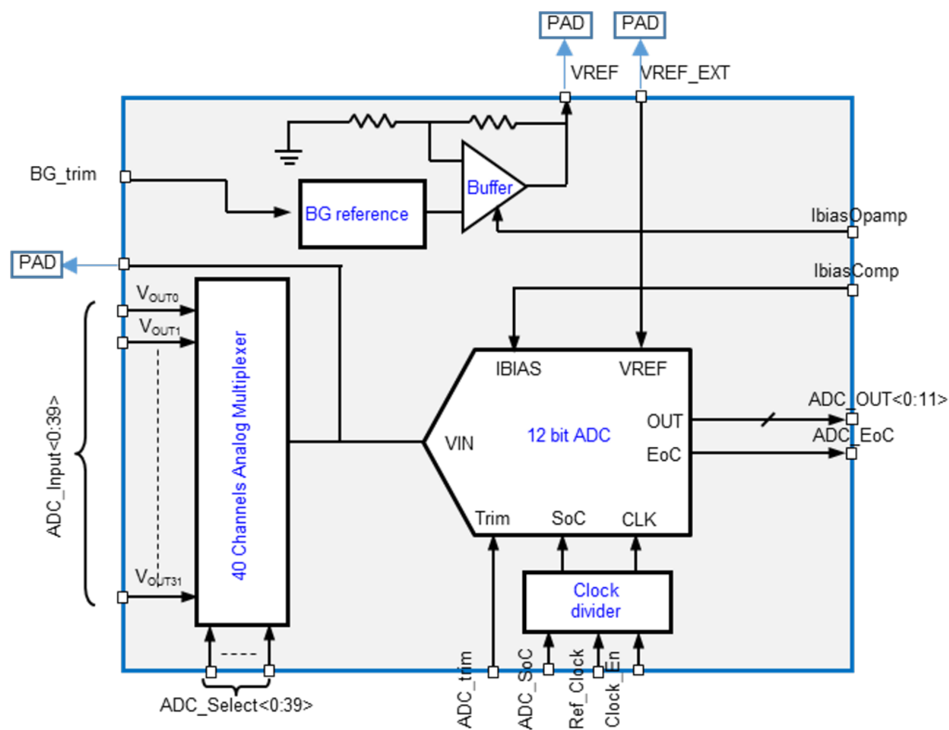


Figure 6.38: Block diagram of the ADC used on the MOPS chip [67]

6.9 Analog block modifications and improvements in the MOPSv2

- It was observed during testing of the MOPSv1 chip that the regulator had a problem with a fast variation of the load current. The regulator did not react fast enough to changes in the current consumption due to communication on the CAN bus. A transistor mismatch in the compensation circuitry of the regulator contributed to this problem. This has been corrected in the MOPSv2.
- The ADC requires a reference of 450 mV but it was supplied with 600 mV instead. This does not break the functionality completely but causes a large gain error, further reducing the ADC range at large input values.
- The MOPSv1 struggles to start at low temperatures when the ramp-up time of power is not very fast [19]. The slowest possible ramp-up time was 30 ms at −15 °C. The exact reason for this behavior is not clear. The problems mentioned in the following three points could have contributed to the start up problem on the chip.
  - Level shifters are missing on the bandgap trimming pads
  - ESD protection configuration done on the bandgap trimming pad is incorrect.
  - Parasitic voltage on different pads due to the fact that trimming bits are supplied by an external regulator, which is incorrect. They should be applied by the internal regulator. Connecting trimming bits to the external regulator means that even when the power is not supplied to the chip, the ESD protection diodes on the pads get activated. This can cause leakage current and parasitic voltage.

The start-up problem seen in the MOPSv1 was solved in the MOPSv2. As explained in Chapter 8, none of the MOPSv2 tested for the complete operational temperature range experienced any problems with the start-up.

6.10 Required external components and monitoring precision

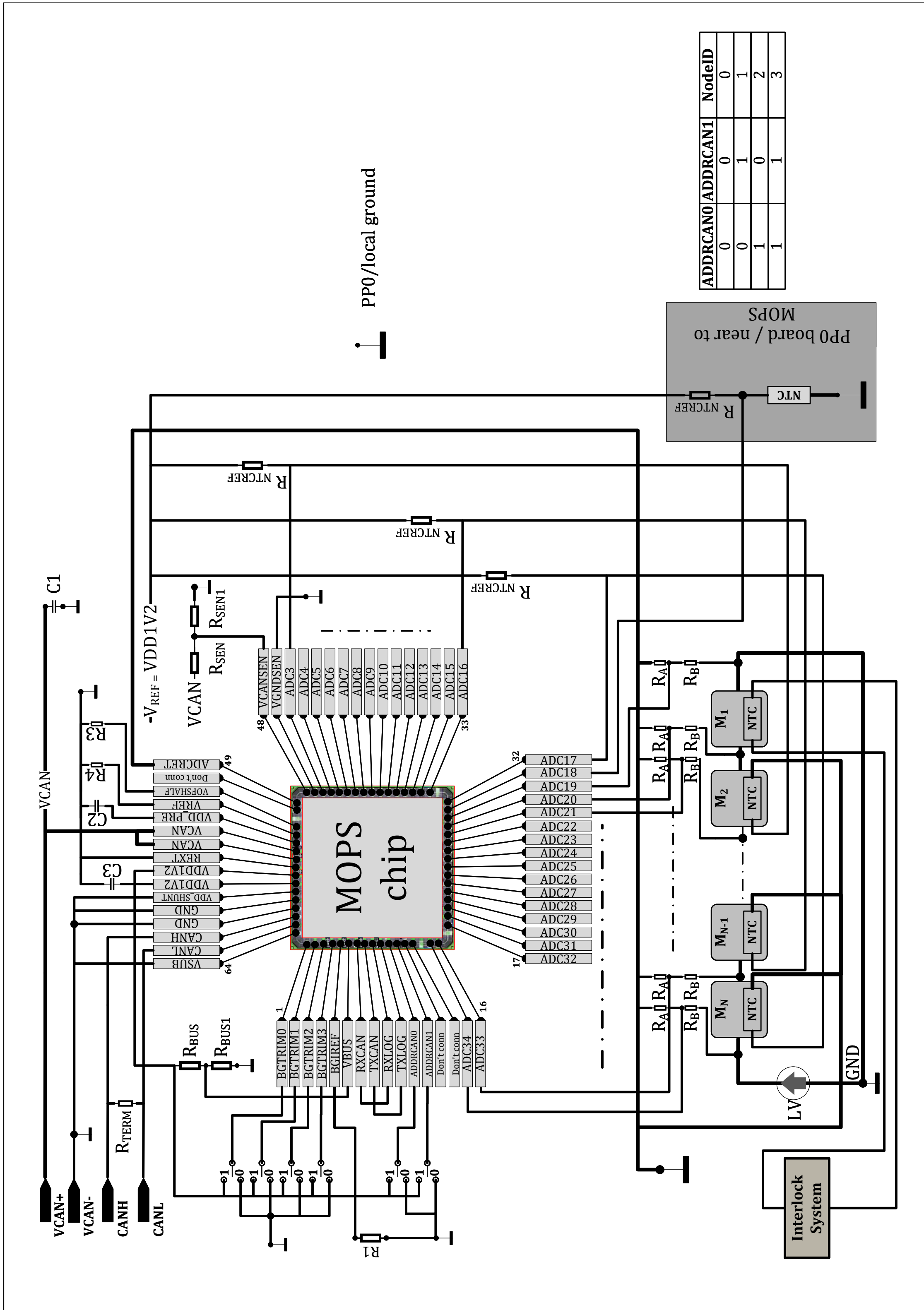
The chip requires external passive electronic elements to correctly define the operation point and modes for different sub-blocks to monitor the serial powering chain. The monitoring precision of the chip is affected by several factors, among which the most important are below:

- The tolerance and topology of the required external components, e.g., resistor network, to translate large voltages from the serial chain to the input range of the ADC.

- Precision/stability of the reference voltage provided to the NTC resistors on the modules to measure the temperature.
- Radiation dose and the operational temperature of the chip. Both of these effects change the Bandgap reference voltage on the chip. A variation of voltage X in the bandgap reference results in a change of 2X in the voltage regulator output and 1.5X in the ADC reference.
- Integral and differential non-linearity of the on-chip ADC if not calibrated.
- Stable communication on the CAN bus. Errors on the bus can hinder real-time updates of the monitored values.

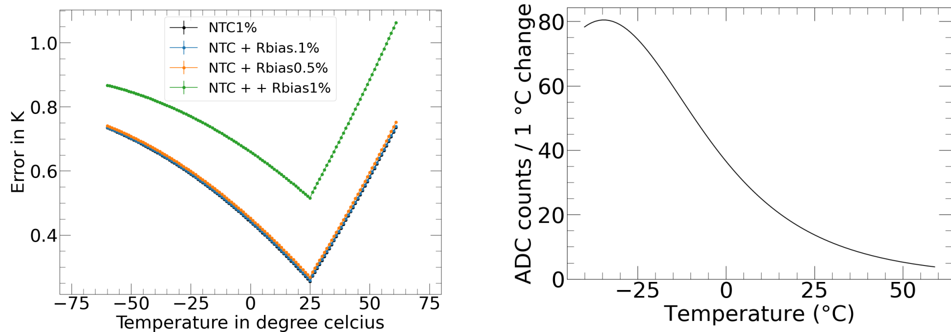
To meet the requirements described in Section 6.1, tolerance of the required external components is mentioned in Table 6.2. The absolute precision of the monitored values depends on the tolerance of all the components involved in the monitoring lines; the relative precision is much more important at the system level to follow precisely any changes in the temperature and the voltage of the modules during normal operation. For the voltage monitoring, the worst-case absolute error is expected in the last module in the chain due to a large dividing factor. Shown in Figure 6.39, the resistors R_A and R_B can have tolerances in the opposite direction. A negative tolerance of just 0.1 % in R_B with a nominal value of 39 kΩ equates to a real value of 38.961 kΩ while a positive tolerance of 0.1 % in R_A with a nominal value of 1 kΩ equates to a real value of 1.1 kΩ. In the final system, a serial chain can have a maximum of 13 modules, which means the 13th module will have 26 V during the normal operation. Using the above tolerances, the chip will read 651.26 mV instead of an ideal 650 mV. An error of just 1.26 mV translates to an error of 50 mV at the module level due to a dividing factor of 40. Another significant problem is the change of reference voltage on the chip. As described in detail in the chapters 8 and 9, the change of bandgap reference voltage due to temperature/radiation can introduce an absolute error of up to 300 mV in the worst case at the chain level. This must be calibrated to ensure precise monitoring.
Similarly, for temperature monitoring, the absolute error due to the tolerance of the resistors can be calculated. Figure 6.40(a) shows the absolute error in temperature measurements due to the tolerance of the NTC resistor as well as the biasing resistor, which is referred to as R_{NTCREF} in the Figure 6.39. The x-axis represents the temperature of the modules in a serial powering chain, whereas the y-axis shows the maximum absolute error in °C using an NTC and the bias resistor of 1 % tolerance. Figure 6.40(b) shows the measurement resolution at different temperatures. Here, the NTC's biasing resistor value is 130 kΩ. The value is chosen to cover the complete temperature range and provide the maximum resolution at the expected operating temperature of −25 °C for the experiment.

The relative precision is affected a lot by the radiation damage to the ADC itself; bandgap reference changes over time due to radiation/temperature and the non-linearity of the ADC. Section 7.4 describes the ADC characterization results in detail, considering all these factors.



ADDRCAN0	ADDRCAN1	NodeID
0	0	0
0	1	1
1	0	2
1	1	3

Figure 6.39: Required components/topology in the system for the chip



(a) Absolute error in the temperature measurement due to component tolerances

(b) Measurement resolution at different temperatures

Figure 6.40: Factors affecting absolute precision of the temperature monitoring values from the MOPS chip

Table 6.2: Properties of the external components required by the MOPS chip

Name	Value	Max. Voltage	Max.Power	Tolerance	Temp. Coefficient
R_A	51 kΩ	32 V	1.3 µW	0.10 %	25 ppm
R_B	2 MΩ	32 V	487 µW	0.10 %	25 ppm
R_{NTCREF}	130 kΩ	2 V	40 µW	0.10 %	10 ppm
R_{BUS}	20 kΩ	2 V	200 µW	1 %	100 ppm
R_{BUS1}	20 kΩ	2 V	200 µW	1 %	100 ppm
R_{SEN}	360 kΩ	2 V	4.8 µW	1 %	25 ppm
R_{SEN1}	200 kΩ	2 V	3.2 µW	1 %	25 ppm
R_{TERM}	100 Ω	1.2 V	15 mW	1 %	100 ppm
R_1	24.9 kΩ	2 V	160 µW	0.10 %	10 ppm
R_3	20 kΩ	2 V	200 µW	0.10 %	10 ppm
R_4	30 kΩ	2 V	135 µW	0.10 %	10 ppm
C_1	6.8 µF	6 V		10 %	NPO
C_2	100 nF	6 V		10 %	NPO
C_3	2.2 µF	6 V		10 %	NPO

Chapter 7

Measurement setup and test results

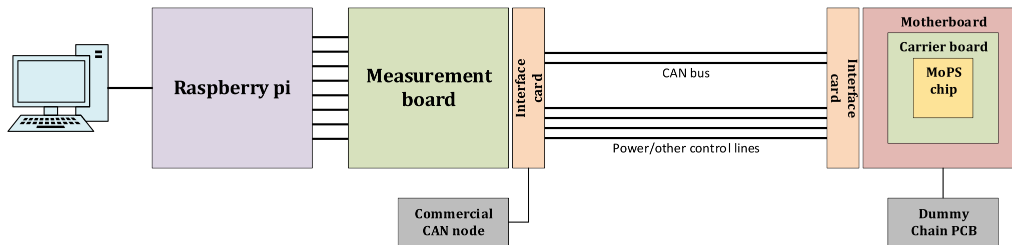


Figure 7.1: Block diagram of the main testsetup used to test the MOPS chip

Several measurement setups have been used to characterize the chip depending on the environment and requirements of particular tests. Figure 7.1 shows the concept of the main measurement setup, which was deployed for temperature measurements, irradiation, and ADC characterization. Because of the modular design, the setup could easily be disintegrated so that different boards could be connected via cables. This allows to put the board that hosts the chip inside a machine used for irradiation or temperature testing, whereas the other boards hosting all the commercial components could be placed on a desk next to the Raspberry Pi board. The same setup has been used to test other parameters at room temperature, e.g., automated trimming, testing with realistic services, and validation of the digital logic. Peter Kind did the layout for most of the required Printed Circuit Boards (PCB). Working towards their bachelor thesis, Julia Besproswanny and Dennis Neuhaus prepared different software required to test the MOPS chip [68].
In addition to the main test setup, the regulator characterization is done using the existing test stand available in FH Dortmund. This was developed for the FE chip to test the regulator.

7.1 Hardware/software parts of the testsetup

The test setup consists of several hardware components like PCB boards, power supplies, and computers. The different boards are explained below:

- Raspberry Pi

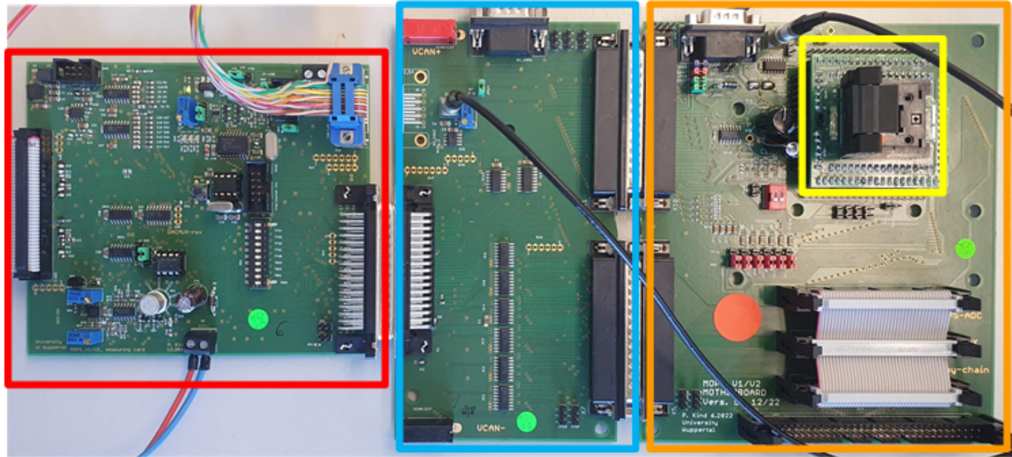


Figure 7.2: Test boards to host commercial components and the MOPS chip

A Raspberry Pi [69] was chosen to benefit from the flexibility of the Linux system and already existing packages to speed up development and its small size to relocate the setup easily to different test facilities. Standard Python libraries are already available to communicate with commercial SPI devices, e.g., ADCs, DACs, MUX, and CAN controllers.

- Measurement Board

  Seen in Figure 7.2(red box), this board hosts all the commercial ICs, e.g., DACs, ADCs, and communication controllers, to generate dummy signals for the MOPS chip and then sample the behavior. The board also offers a custom-built DAC-controlled power supply to control the chip power remotely.

- Motherboard

  As shown in Figure 7.2(orange and blue boxes), the motherboard provides the interface on one side to the carrier board of the chip and on the other side to the measurement board. The board also has connectors to offer the possibility of connecting a dummy chain board.

- Carrier Board

  The carrier board of the test setup is the one that hosts the actual chip. The board is shown in Figure 7.2(yellow box). This has fan-out connections, which are used to wire-bond the chip. The board also hosts decoupling capacitors and resistors in the near vicinity of the chip.

- Dummy chain board

  Shown in Figure 7.3, this board mimics the construction of an actual serial power chain. The board has variable resistors to depict detector modules and

NTCs to provide temperature measurements as if they are on an actual module detector.

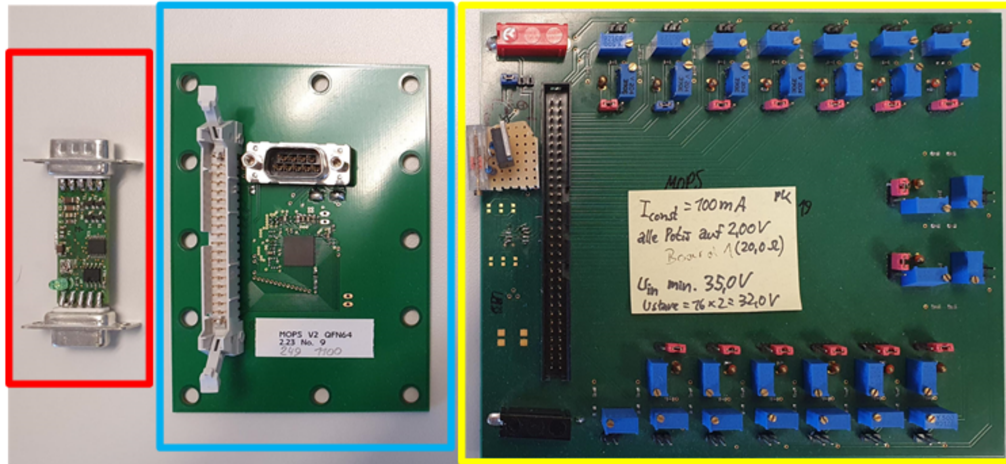
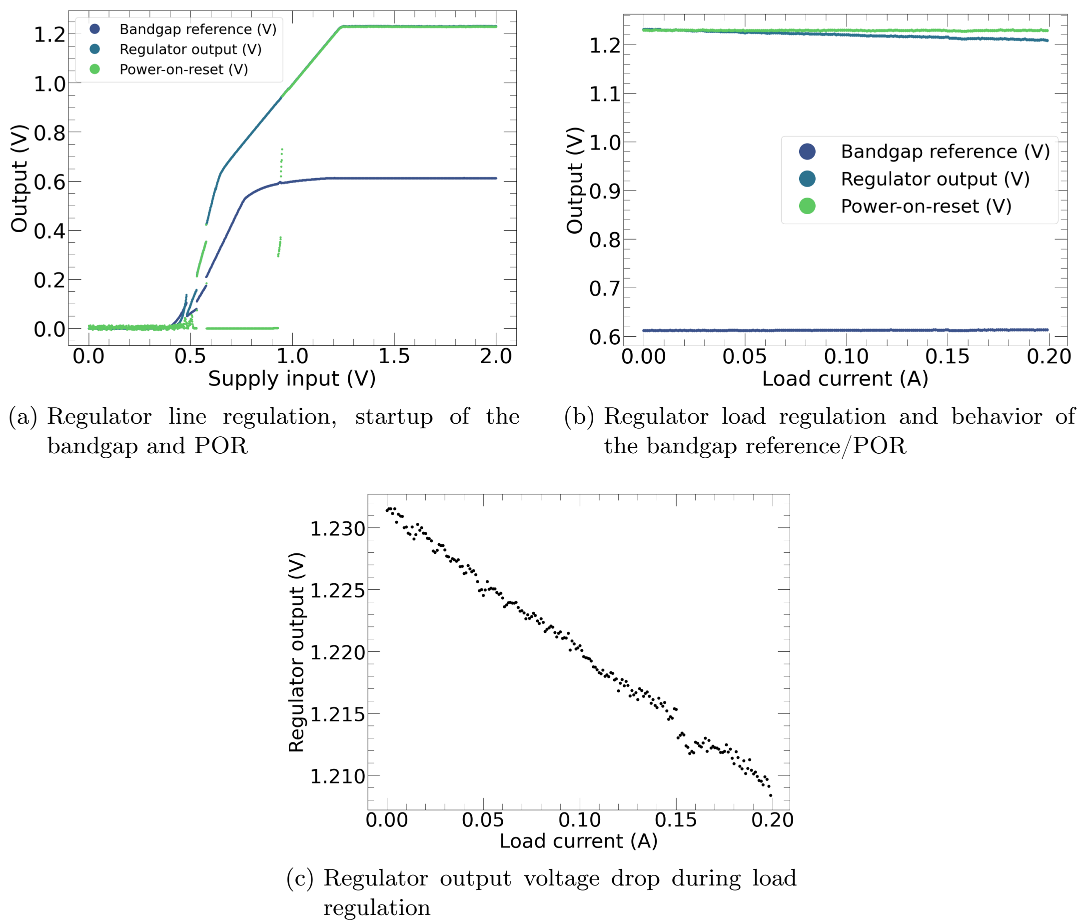


Figure 7.3: Test boards to host MOPS, translate CAN signals and provide test signals

7.2 Regulator, Bandgap reference and POR measurements

The regulator on the chip has been tested to pass the line and load regulation tests, and the startup behavior of the analog component has been sampled. All the plots shown in this section are only about the MOPSv2. Figure 7.4(a) shows the line regulation measurements. The input supply voltage to the chip was increased from 0 V to the maximum tolerable range of 2 V. The regulator output rises when the supply voltage reaches ≈ 0.5 V. The regulated output starts already at ≈ 1.25 V and then stays constant until the supply voltage reaches 2 V. The bandgap reference also starts up as expected and then stays constant. The POR output is also very important during the line regulation to ensure a good known state for the digital logic during startup. Its output stays low until the supply voltage reaches ≈ 930 mV. The POR then follows the regulator and stays constant.
Shown in Figure 7.4(b) is the load regulation. The load current drawn by the regulator is increased from 0 to 200 mA. During the normal operation, the chip requires only 10 mA of current. Shown in Figure 7.4(c), at the maximum specified current of 35 mA, the voltage drop at the regulator output is only ≈ 5 mV. The POR and the bandgap reference output remain constant during the load regulation test.
Transient testing has also been done for the regulator. This ensures the regulator can cope with the fast load current change during communication on the CAN bus. The load current changes abruptly when the chip actively participates in the communication and drives the CAN bus. Shown in Figure 7.5(a), when the current changes from



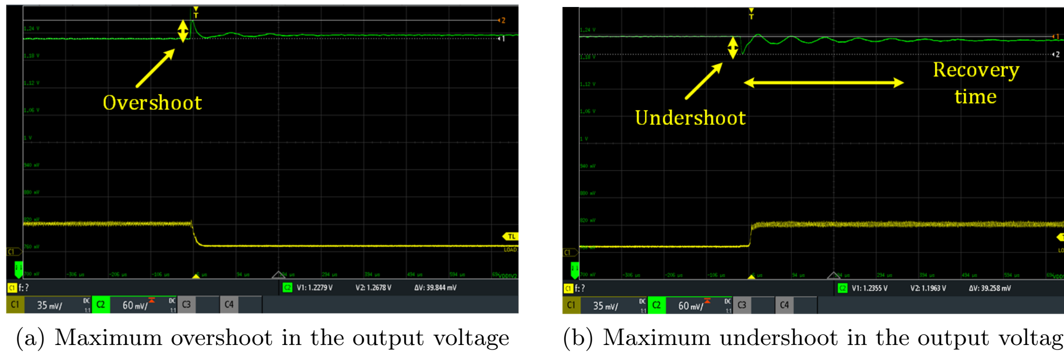
(a) Regulator line regulation, startup of the bandgap and POR

(b) Regulator load regulation and behavior of the bandgap reference/POR

(c) Regulator output voltage drop during load regulation

Figure 7.4: Output of the analog components at different supply voltages and load current

35 mA to 0 with a delay of only 10 µs, the maximum overshoot is ≈ 40 mV. Figure 7.5(b) shows the undershoot with a similar value when the load current changes from 0 to 35 mA. In the worst case, the regulator output takes 500 µs to recover. To fix this problem, more on-chip decoupling capacitance is foreseen in the next version of the chip. Figure 7.6 shows the variation in the output voltage of the bandgap reference



(a) Maximum overshoot in the output voltage (b) Maximum undershoot in the output voltage

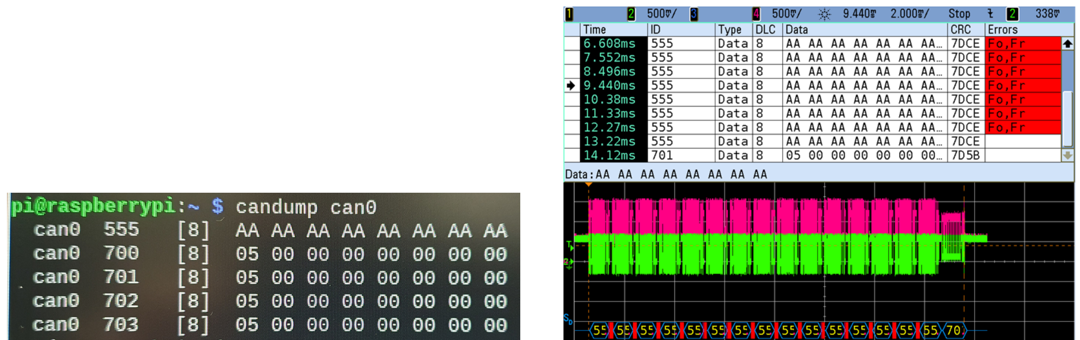
Figure 7.5: Regulator output voltage at fast changing load current

Figure 7.6: Coupling of the bandgap reference and the 10 MHz on-chip oscillator

circuit. As explained in Chapter 6, the MOPS chip used a relaxation-based oscillator. The capacitor network in the oscillator is charged by the reference current generated by the bandgap reference. The time period of noise is ≈ 100 ns, which is exactly the time period of the oscillator output frequency. A solution to this problem is to add decoupling circuitry on the chip. This is foreseen for the MOPSv3.

7.3 Digital functionality

The chip's digital logic has been rigorously tested while carrying out the temperature and radiation testing explained in Chapters 8 and 9, respectively. During temperature and radiation testing, each channel of the MOPS ADC was supplied with random values from a commercial 12-bit DAC and then read out by an independent



(a) Sign-in message sent by four MOPS on a single bus

(b) CAN bus decoding using an oscilloscope where the trimming messages and then a sign-in message by the MOPS can be seen

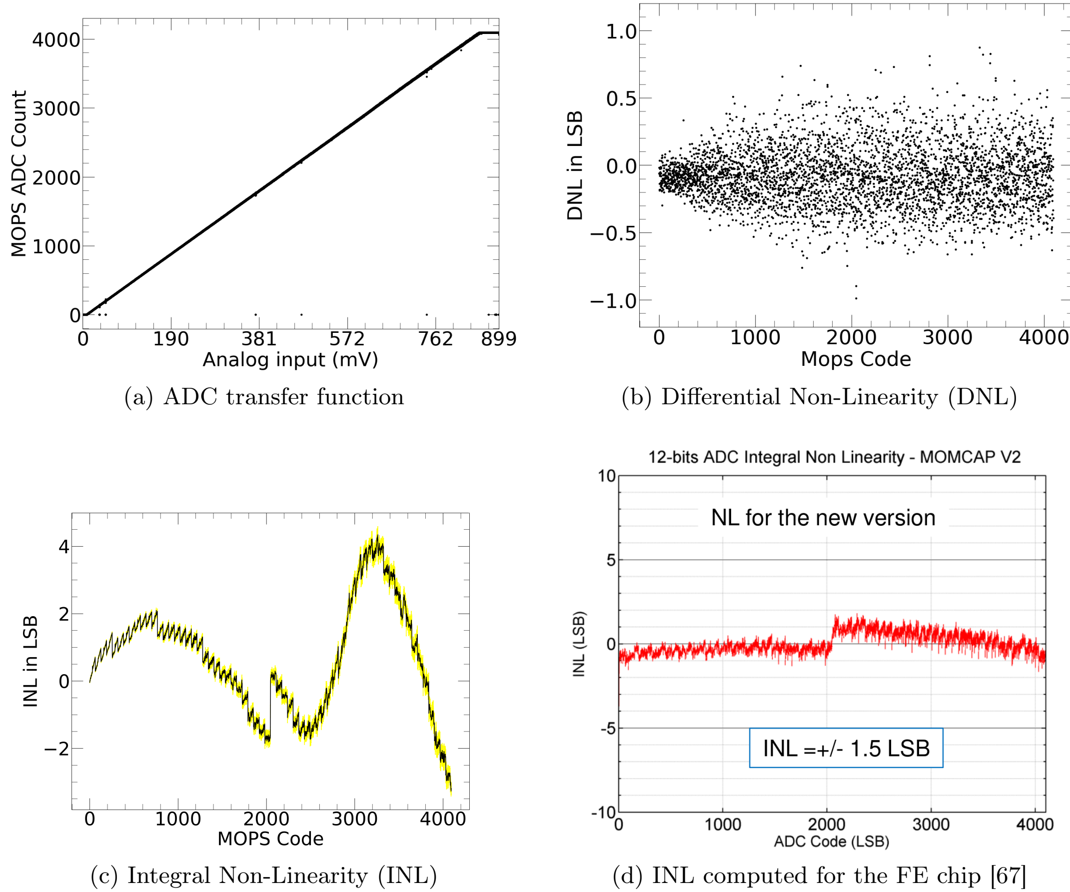
Figure 7.7: Automated trimming using four real MOPS chips on a single bus

commercial 12-bit ADC and the MOPS chip for comparison. The usefulness of the automated trimming feature introduced in the MOPSv2 was also demonstrated from results shown in chapters 8 and 9, where auto trim was used without a power cycle to correct the frequency variation. In addition, some tests have also been done at room temperature to check the robustness of digital design at the system level, e.g., Automated trimming and a maximum of four chips on a single bus. Figure 7.7(a) shows a sign-in message from four chips on a single bus. Figure 7.7(b) shows activity on the CAN bus using an oscilloscope. After powering up, messages destined to trim the MOPS are decoded but marked as red to indicate missing acknowledgment bits. When the MOPS was correctly trimmed, it acknowledged the second last message and sent a sign-in message afterward.

7.4 ADC characterization

Detailed characterization of the on-chip ADC has been done at room temperature using the setup shown in Figure 7.1 and MOPSv2 chip. A linear ramp-up method shown in Figure 7.8(a) was used. A commercial 16-bit DAC with a reference voltage of 2.5 mV was used to provide an input voltage at the MOPS ADC channels, which can be incremented by 38.14 µV per DAC count. A single ADC count from the MOPS chip itself equals 219 µV. To reduce noise and make precise edges for the ADC counts, each code sent by the DAC and sampled by the MOPS was repeated five times before jumping to the next DAC count. Before calculating the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), a histogram and an average for the MOPS ADC counts were calculated to give clear transition points. Shown in Figure 7.8(b) is the DNL. Because of the negative offset and the positive gain, the MOPSv2 loses ≈ 75 mV of measurable range. The most important takeaway from the DNL is that it stayed $-1 > DNL < 1$. This proves no skipped counts and a monotonic behavior.

The INL is shown in Figure 7.8(c). Instead of calculating the INL by DNL summation, the INL was computed using the end-point line method to cross-check the calculated DNL. The yellow trace shows the standard error on the mean. The ADC used on the MOPS chip is the same as on the FE chip, but the calculated INL is worse for ADC counts larger than 3000. The INL calculated for the FE chip was 1.5 LSB [67], shown in Figure 7.8. This could be due to the bandgap noise problem discussed in section 7.2 as the ADC reference is provided by the bandgap reference circuit on the chip with a multiplying factor of 1.5.



(a) ADC transfer function

(b) Differential Non-Linearity (DNL)

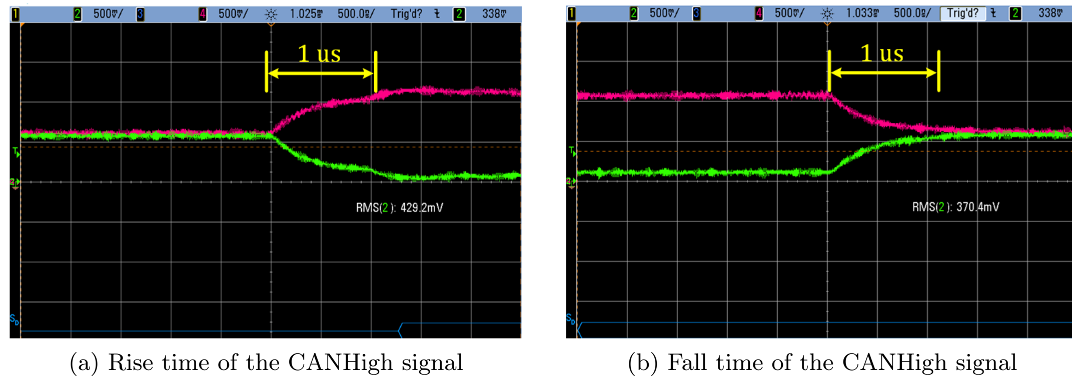
(c) Integral Non-Linearity (INL)

(d) INL computed for the FE chip [67]

Figure 7.8: Output of the analog components at different supply voltages and load current

7.5 Operation with realistic services

In the final system, a cable length of ≈ 70 m will be used to communicate data and supply power to the chip. The patch panel outside the detector volume uses 10 nF filter capacitors connecting the CANHigh and the CANLow line to the ground. They



(a) Rise time of the CANHigh signal

(b) Fall time of the CANHigh signal

Figure 7.9: Rise/fall time of the CAN bus signals including extra filter capacitors 10 nF used in the system

introduce more delay to the rise/fall time of the signals on the CAN bus. Tests for the physical layer of the chip, including the filter capacitors, have been done. Figure 7.9 shows the rise/fall time of the CANHigh/CANLow signals using an equivalent filter capacitance of 13.87 nF to the ground. The equivalent capacitance included 3.87 nF of the cable capacitance. The capacitance between the CANHigh/CANLow cables was 4.15 nF. Using a bus speed of 125 kbit s^{-1}, where each bit has a period of 8 µs, the chip proved to work reliably.

Chapter 8

Operational temperature and performance

Both MOPSv1 and MOPSv2 were tested at different temperatures inside a climate chamber. The climate chamber tests aim to prove a reliable operation of the chip for the whole temperature range defined in the specification documents [18] and [47].

8.1 Scope of measurements

The operational requirements specified in the specification document require the MOPS chip to be tested at a temperature range of -40 °C to +60 °C. However, the chip may not cover the full temperature range during the nominal operation because the detector is expected to run between −25 °C to −20 °C. For the MOPSv1, a climate chamber was used which could go from −15 °C to 60 °C whereas for the MOPSv2, Thermostream [70] was used. The Thermostream machine can change the temperature very fast and is also able to provide a broad temperature range of −80 °C to more than 100 °C. The MOPSv2 was tested for −50 °C to 60 °C. The most important points to prove the chip's reliability for the complete temperature range.

- Start-up behavior of the chip, especially at cold temperatures
- Slow ramp-up of the power supply at different temperatures
- Change of frequency and the output of analog components
- Reliability studies/aging at high temperature of 60 °C

8.2 Startup performance

8.2.1 MOPSv1

The chip responded well but struggled to start at low temperatures using a slow ramp-up supply voltage. This can be seen in Figure 8.1, where the bandgap reference represented as VREF does not rise upon the power supply. The exact reason for the startup issue is still unclear, but there could be different reasons for that, e.g

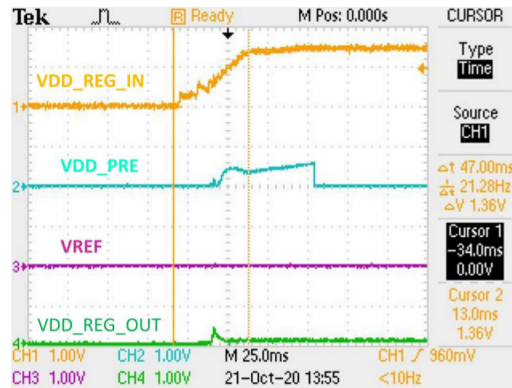


Figure 8.1: MOPSv1 bandgap reference startup problem at low temperature

- Parasitic voltage of up to 400 mV at different analog signal pads. This was due to the fact that an external commercial regulator was used to trim the bandgap.
- Level shifters missing at the input of Bandgap trimming pads

More details about the MOPSv1 start-up problem are discussed in [19]. However, it is important to mention that the bandgap circuit used on the MOPS chip has proven to work completely fine for a large temperature range [64]. This startup issue for the MOPSv1 should not cause a problem in the final system. Although the exact reason for the problem was unclear, by fixing the issues mentioned before, the MOPSv2 experienced no startup problems.

8.2.2 MOPSv2

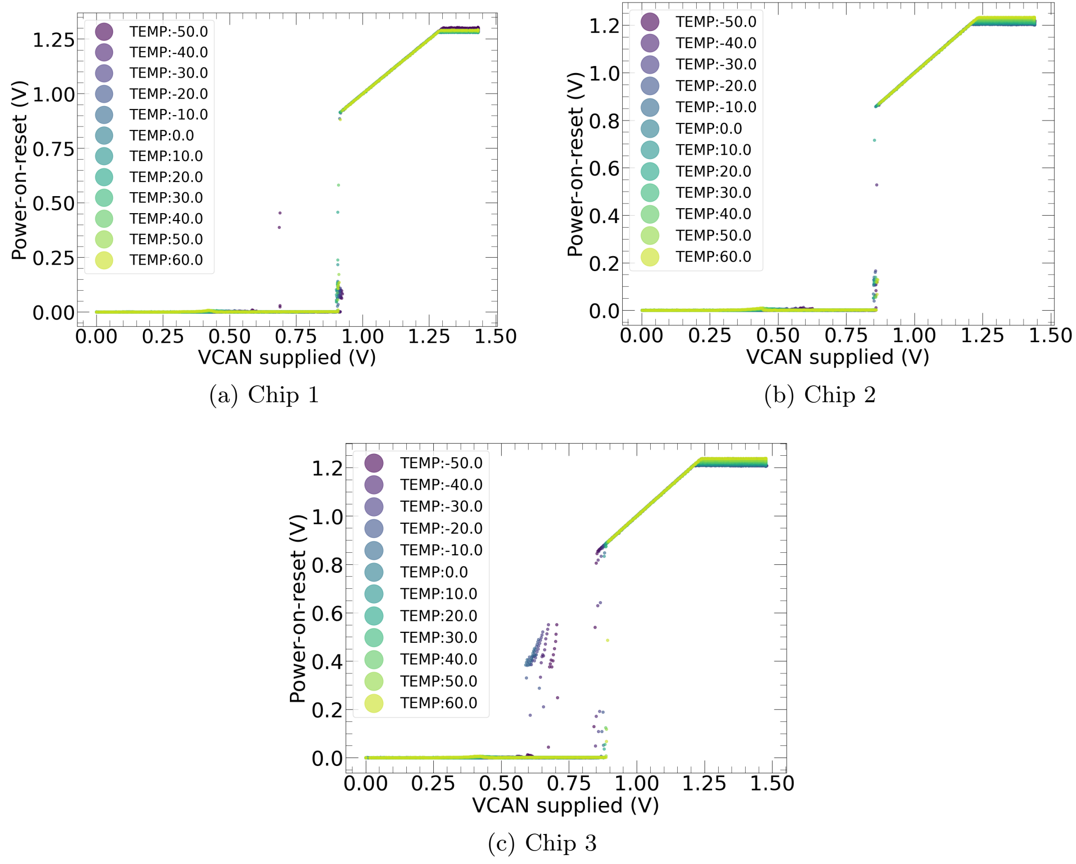
Three chips were used in total to do the startup tests. The chip was power cycled for a change of every 10 °C. A ramp-up time of minimum 600 ms was used for the power supply. None of the three chips showed any problems during the start-up.

POR

Shown in Figure 8.2 is the start-up behavior of the POR for three different chips. Chip 2 worked completely fine, whereas for chip 1, for an extreme temperature of −50 °C, the POR was released at ≈ 700 mV. Also, for chip 3, the release point of the POR output was ≈ 600 mV. This is very low to ensure proper resetting of the digital logic; however, in the final system, the chip will not be actively cooled during operation. It is very unlikely that the chip will experience temperatures lower than −15 °C during operation [71].

Bandgap

Shown in Figure 8.3 is the start-up behavior of the bandgap reference for three different chips. Two observations can be made from this plot. At colder temperatures, the

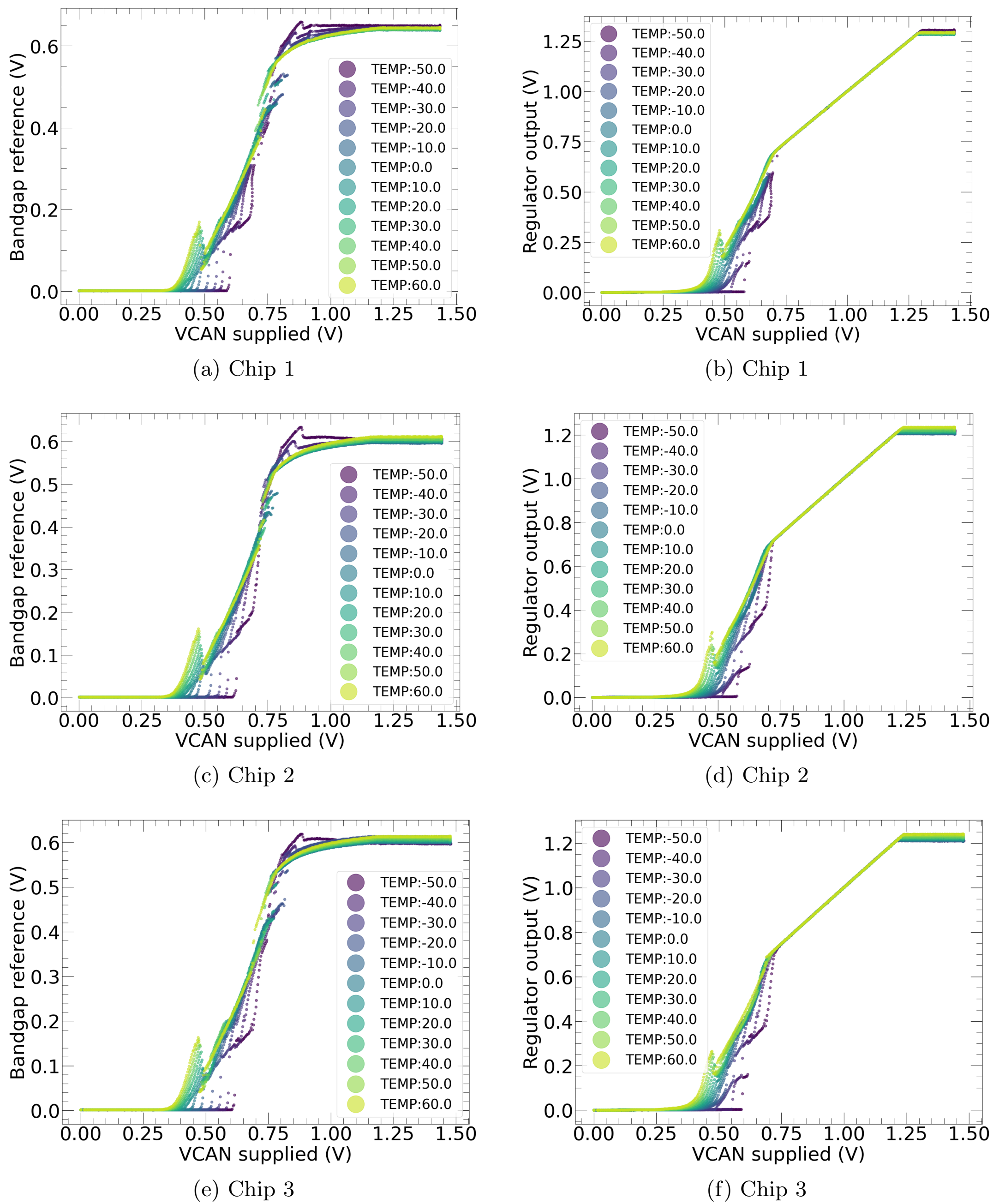


(a) Chip 1

(b) Chip 2

(c) Chip 3

Figure 8.2: POR startup behavior at different temperatures



(a) Chip 1

(b) Chip 1

(c) Chip 2

(d) Chip 2

(e) Chip 3

(f) Chip 3

Figure 8.3: Bandgap/regulator startup behavior at different temperatures

bandgap circuit starts later than at warmer temperatures. At colder temperatures, a slight overshoot occurs before the output voltage settles down to the desired value after the recovery time.

Regulator

Shown in Figure 8.3 is the start-up behavior of the regulator for three different chips. The regulator in all three chips started up perfectly fine. Because the bandgap started later at cold temperatures, the start-up of the regulator was also delayed. However, it did not cause any problems for the circuit.

8.3 Temperature cycling between $-40\,°\mathrm{C}$ to $60\,°\mathrm{C}$ during operation

The same three chips used for the startup tests were also used during the temperature cycling test. While in operation, each chip was temperature cycled from the lowest to the maximum value of the operational temperature and vice versa. This means each chip was temperature-cycled two times. Before the tests, each chip was trimmed to the desired operational frequency of 10 MHz. The rate of temperature change was $1\,°\mathrm{C}\,\mathrm{min}^{-1}$.

Oscillator

As shown in Figure 8.4, chip 1 was exceptionally good and had minimal variation for both cycles. The variation for chip 1 was small enough not to cause any communication problems on the CAN bus. The frequency deviation for both chip 2 and chip 3 shown in Figure 8.4 was large enough to cause disturbance on the CAN bus communication. The communication problem started at the point where the plot became lighter with few sample points. For the chip 2, going from $-40\,°\mathrm{C}$ to $60\,°\mathrm{C}$, it started around $5\,°\mathrm{C}$. whereas, going from $60\,°\mathrm{C}$ to $-40\,°\mathrm{C}$, it started at $-30\,°\mathrm{C}$. The plot for the chip 3 can be interpreted in the same way. Here, an important takeaway point is that the chip could communicate without errors on the bus as long as the on-chip frequency variation was not larger than 1.5 %. However, theoretically, it should be 3 %. The inflexibility of the software and incorrect setting of the level shifter used to translate the CAN bus signals were thought to have contributed towards intolerance towards change of frequency. Another interesting observation that can be made from the frequency plot is that the direction of deviation w.r.t. the temperature was not uniform for all three chips. e.g. for chip 2, going from $-40\,°\mathrm{C}$ to $60\,°\mathrm{C}$, the frequency increased whereas it decreased for chip 3.
It is important to mention that almost every time the frequency variation was large enough to cause communication errors, a remote reset command could return the chip to the right frequency as long as the communication was not completely broken.

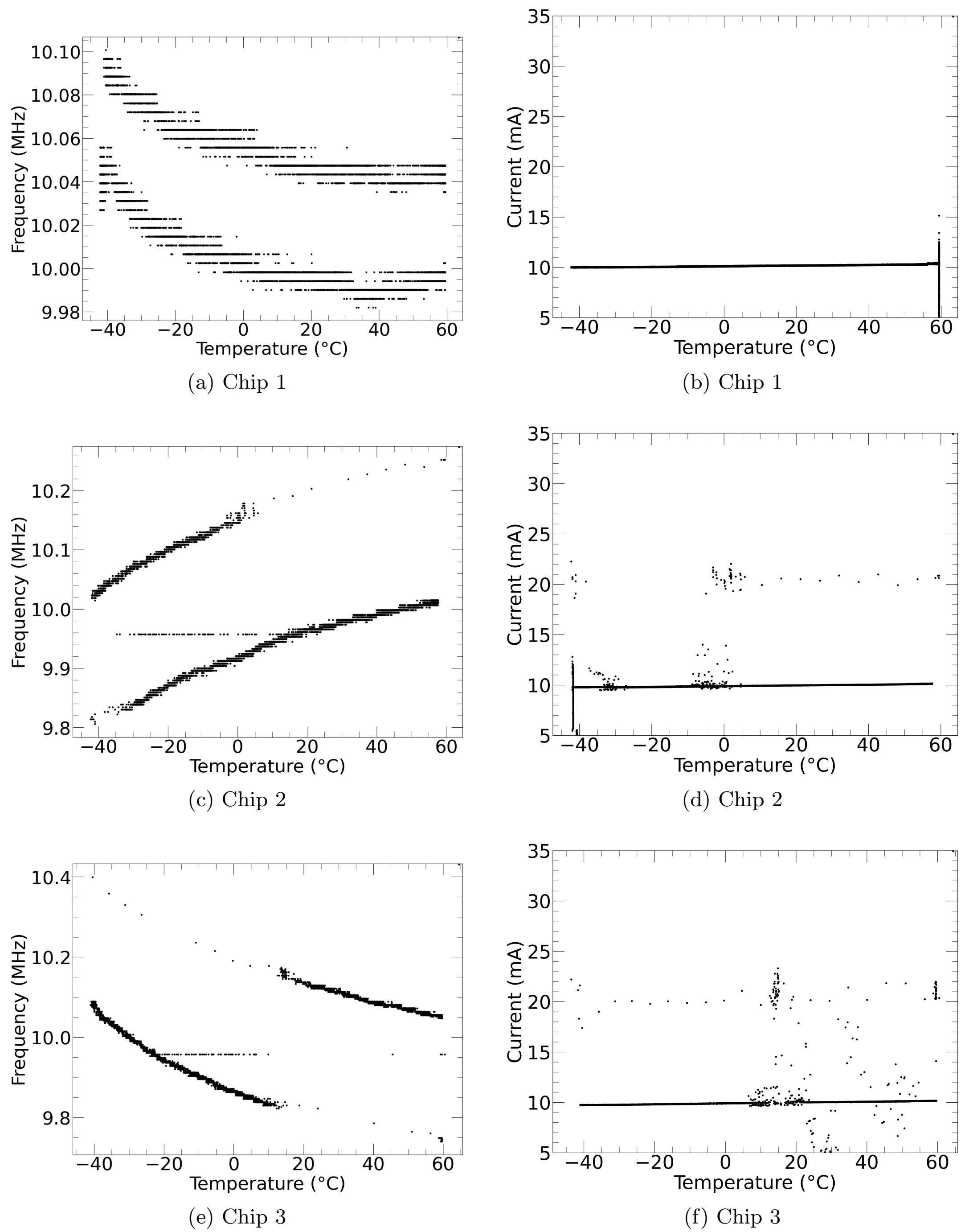


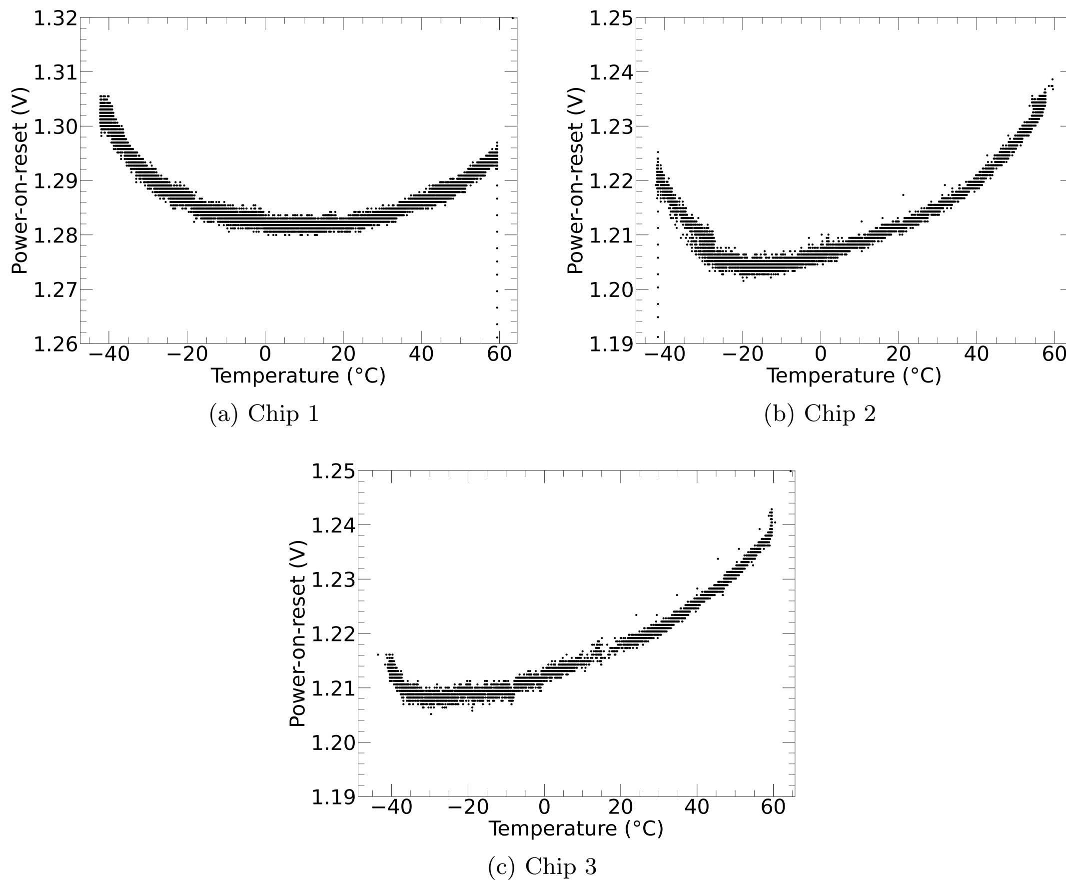
Figure 8.4: Change in the on-chip oscillator frequency w.r.t. temperature and current consumption

Current consumption

Shown in Figure 8.4 is the current consumption of the same three chips. Because chip 1 had no communication problem due to frequency shift, the current consumption remained stable throughout the test and increased by only a couple of µA. The current consumption for both chip 2 and chip 3 increased from 10 mA to ≈ 21 mA during the time of communication problem explained earlier in the oscillator paragraph. The reason for more current consumption is that the chip continuously tried to drive the bus but with the wrong frequency.

POR

Figure 8.5 shows the variation in the POR output. The POR continuously followed the regulator output. At all operational temperatures, no glitches were recorded in the output of the POR circuit.



(a) Chip 1

(b) Chip 2

(c) Chip 3

Figure 8.5: POR output voltage variation w.r.t. temperature

Bandgap

The bandgap variation shown in Figure 8.6 w.r.t. the operational temperature is critical to calibrate ADC measurements from the MOPS chip. As expected, a bandgap reference circuit is optimized for a particular temperature range where it exhibits the most temperature independence. It is evident from the plot from both chip 2 and chip 3 that voltage output shows the most temperature independence around $\approx -20\,°\mathrm{C}$, which is expected to be the operational temperature of the final detector and the FE chip. The chip 1 looks exceptionally good. However, the independence point has shifted a bit towards 0 °C to 20 °C. A maximum variation of 18 mV was recorded in the bandgap output for the entire temperature range. This is shown as V_{ref} in Figure 6.33, after the reference current generator. Variation in the Core Bandgap circuit output is much smaller, which is reported in [64].

Regulator

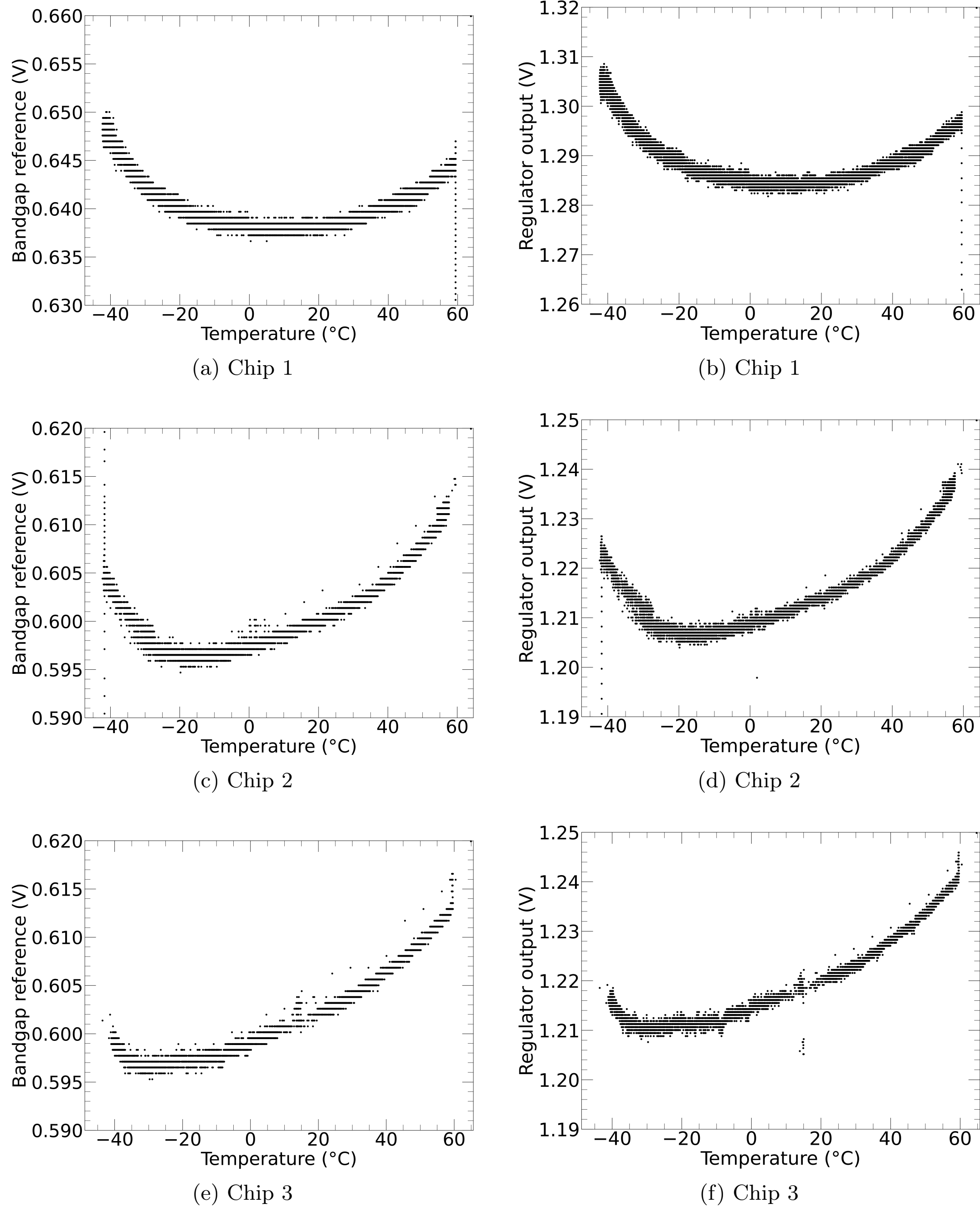
The regulator on the MOPS chip has an output voltage of two times the bandgap voltage. Shown in Figure 8.6 is the variation in the regulator output. The variation in the output completely follows the pattern of the bandgap variation. The total variation in the regulator output is almost 36 mV, which is double the variation that can be seen in the output of the bandgap regulator.

8.4 Long term stability / reliability at 60 °C

To test the reliability of the MOPS chip to continuously operate at high temperatures, one of the MOPSv2 chips is being operated in a climate chamber at 60 °C. The chip has completed more than 5000 h of operation without any problems. The tests are still ongoing.

8.5 Summary

The MOPSv2 chip met the operational temperature requirements defined in the section 6.1 without problems. None of the three chips showed any problem with startup at any temperature. At extremely cold temperatures, the POR was released earlier than desired, but this is not of great concern. The chip in the final system will not be actively cooled, so realistic operational temperature is expected to be higher than $-20\,°\mathrm{C}$ when the detector is running. If the detector is not running, the ambient temperature can drop further. If the MOPS chip is power cycled at this stage, there is a little risk that the digital part may not start in the correct state due to the problem seen in the POR startup. The shift in the bandgap reference output changes the ADC reference as well. For the module voltage monitoring, a shift of 20 mV in the bandgap output can introduce an error of 6 ADC counts even in the module-to-module relative voltage precision. Considering a voltage dividing factor of 40, this is equal to an error of 52 mV per module at the serial powering chain; therefore, the



(a) Chip 1 (b) Chip 1

(c) Chip 2 (d) Chip 2

(e) Chip 3 (f) Chip 3

Figure 8.6: Bandgap reference and regulator output voltage variation w.r.t. operational temperature

temperature dependence of the bandgap reference voltage must be taken into account to calibrate voltage monitoring values from the MOPS chip. In addition to the factors mentioned in Section 6.10, the temperature dependence of the ADC reference must be calibrated to achieve absolute precision. To know the operational temperature of the chip in the final system, an NTC resistor shown in Figure 6.39 will also be placed in the near vicinity of the chip. The value read from this NTC resistor is independent of the bandgap variation.

$$V_{NTC} = VDD1V2 \frac{R_{NTC}}{R_{NTC} + R_{NTCREF}} \tag{8.1}$$

Where $VDD1V2$ is equal to two times the bandgap reference V_{BG} output. V_{NTC} is the voltage across the NTC resistor.

$$V_{NTC} = 2 \times V_{BG} \frac{R_{NTC}}{R_{NTC} + R_{NTCREF}} \tag{8.2}$$

$$V_M = \frac{V_{NTC}}{1.5 \times V_{BG}} = 1.33 \times \frac{R_{NTC}}{R_{NTC} + R_{NTCREF}} \tag{8.3}$$

Here, V_M is the resultant voltage sampled by the MOPS ADC. Which can also be written in terms of ADC counts as:

$$ADC = 4096 \times V_M \tag{8.4}$$

From Equation 8.3, finding an approximate operational temperature of the chip is independent of bandgap variation. Hence, temperature monitoring of the modules in the serial powering chain also does not require temperature-dependent calibration.

Chapter 9

Radiation tolerance of the MOPS chip

Several MOPS chips from both v1 and v2 versions have been irradiated under different conditions to check whether they meet the radiation tolerance requirements defined in Section 6.1. The behavior of the chip w.r.t. low dose, frequent power cycling, high temperature, and heavy ions were sampled during the campaign, lasting over several months.

9.1 Irradiation using X-rays

To ensure the chip can survive 500 Mrad of TID, the chips were irradiated using an X-ray machine [72] available at the Physics Institute in Bonn.

9.1.1 MOPSv1, frequent power cycling

Two X-ray campaigns using four chips were done for the first version of the chip. The motive for the first campaign using only one chip was to check whether the chip could survive 500 Mrad at all. Further details are provided in the bachelor thesis by Julia Besproswanny [68].
In the second campaign, three chips were used. Table 9.1 shows the three different chips's dose rates, total dose, and temperature. During the campaign, the chips were power cycled frequently at different levels of accumulated dose to rule out start-up issues.

Table 9.1: Parameters for the three MOPSv1 chips to test TID tolerance

	Total dose	**Operational temperature**	**Dose rate**
Chip 1	554 Mrad	∼(0 to 5)°C	1.75 Mrad/h
Chip 2	509 Mrad	40 °C	1.75 Mrad/h
Chip 3	478 Mrad	20 °C	1.75 Mrad/h

Shown in Figure 9.1 is the variation in the on-chip frequency and the current consumption w.r.t. of the chips mentioned in Table 9.1. The frequency of chip 1 looked perfect even after accumulating a TID of 554 Mrad. The chip was power cycled multiple times, and it showed no problems at all. The deviation remained within 1.5 %.

Table 9.2: Parameters for the three MOPSv2 chips to test TID tolerance

	Total dose	**Operational temperature**	**Dose rate**
Chip 1	33.8 Mrad	0 °C	40 krad/h
Chip 1	533 Mrad	0 °C	1.75 Mrad/h
Chip 2	500 Mrad	20 °C	1.75 Mrad/h
Chip 3	500 Mrad	40 °C	1.75 Mrad/h

The current consumption of the chip remained constant throughout the process. For chip 2, the frequency plot in Figure 9.1 shows two colors. The blue trace is when the chip could communicate perfectly fine, whereas the red trace is when the chip was only powered, being irradiated but not communicating on the CAN bus. The issue was later found to be the faulty connector to the CAN bus cable. In several instances, the frequency of chip 2 deviated more than 1.5 %, which is the cause of high current consumption when communication was enabled. This is due to the fact stated earlier that the chip continuously tries to drive the CAN bus without success. The frequency dropping completely at around 420 Mrad was due to the unstable power supply. The chip 3 had no problems communicating until around a TID of 437 Mrad. At this point, the current consumption spiked once again.

Figure 9.2 shows the output of the same three MOPSv1 chips mentioned in Table 9.1 and their frequency/current is shown in Figure 9.1. For chip 1, some dropping lines in the bandgap and regulator output are sampled during the power cycles of the chip. The bandgap and the regulator on chip 1 worked without any problems. Both chip 2 and chip 3 did not go very well with power cycling and had trouble with the slow ramp-up of the power supply. The behavior resembled the startup problem mentioned in Chapter 8. No radiation-dependent startup problem has been reported about the bandgap circuit used on the MOPS chip [64].

9.1.2 MOPSv2, low dose, high temperature

Three MOPSv2 chips were used during the third campaign; Table 9.2 shows the dose rates, total dose, and temperature of the three different chips. Chip 1 was first irradiated at a critical low dose rate of 40 krad/h to accumulate a total of 33.8 Mrad of TID. Previous studies have proved more damage at low dose rates compared to higher ones [73][74]. After finishing the low dose rate campaign, chip 1 was then irradiated at a faster rate to accumulate a minimum of 500 Mrad. After accumulating the TID mentioned in Table 9.2, the temperature for both chip 2 and chip 3 was increased to 60 °C for some days to check the reliability. A vertical green line in the plots marks the point, where the irradiation stopped.

Figure 9.3 shows the frequency and current consumption for all three chips during the campaign. For chip 1, breaks in the frequency plot happened due to a bug in the

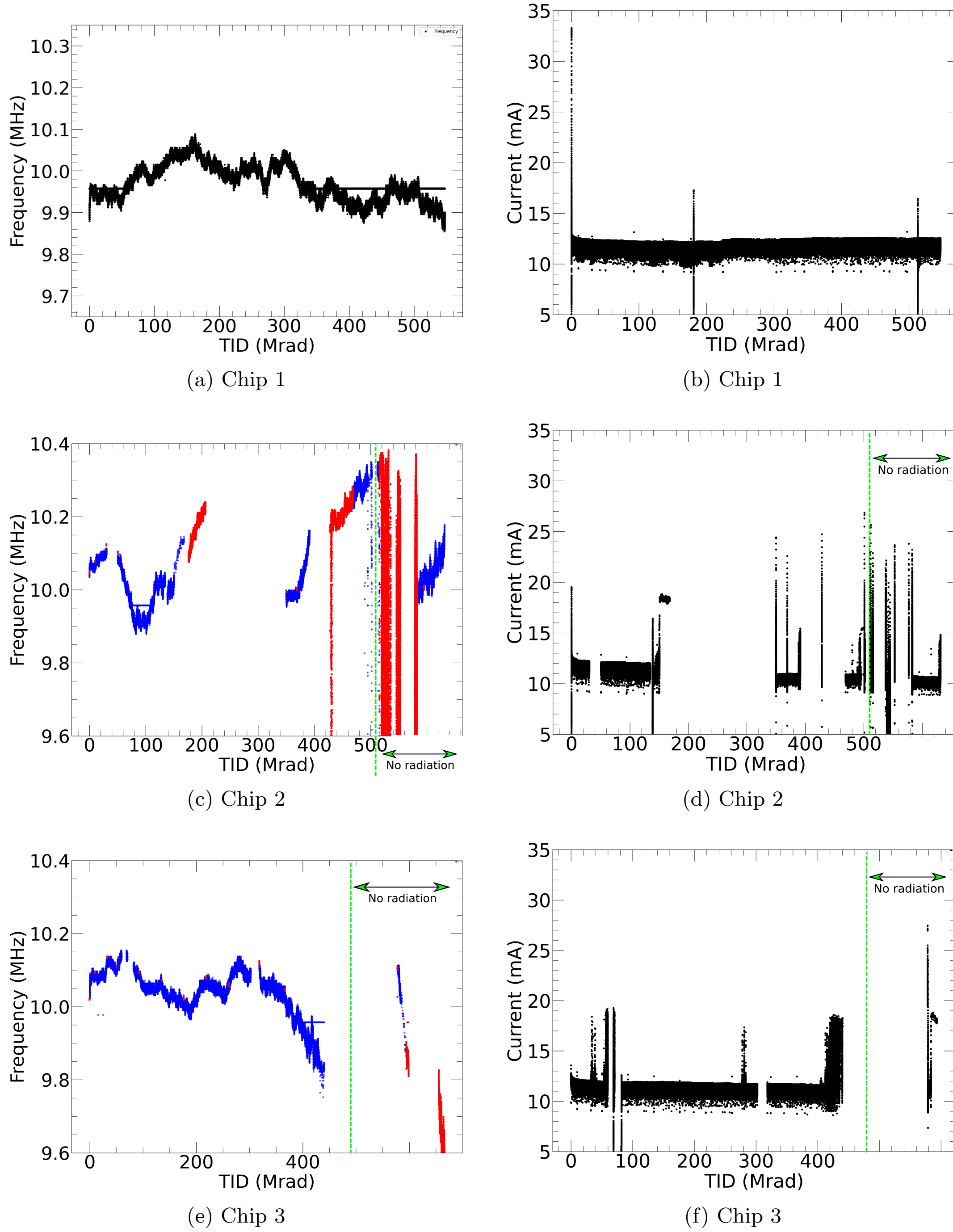
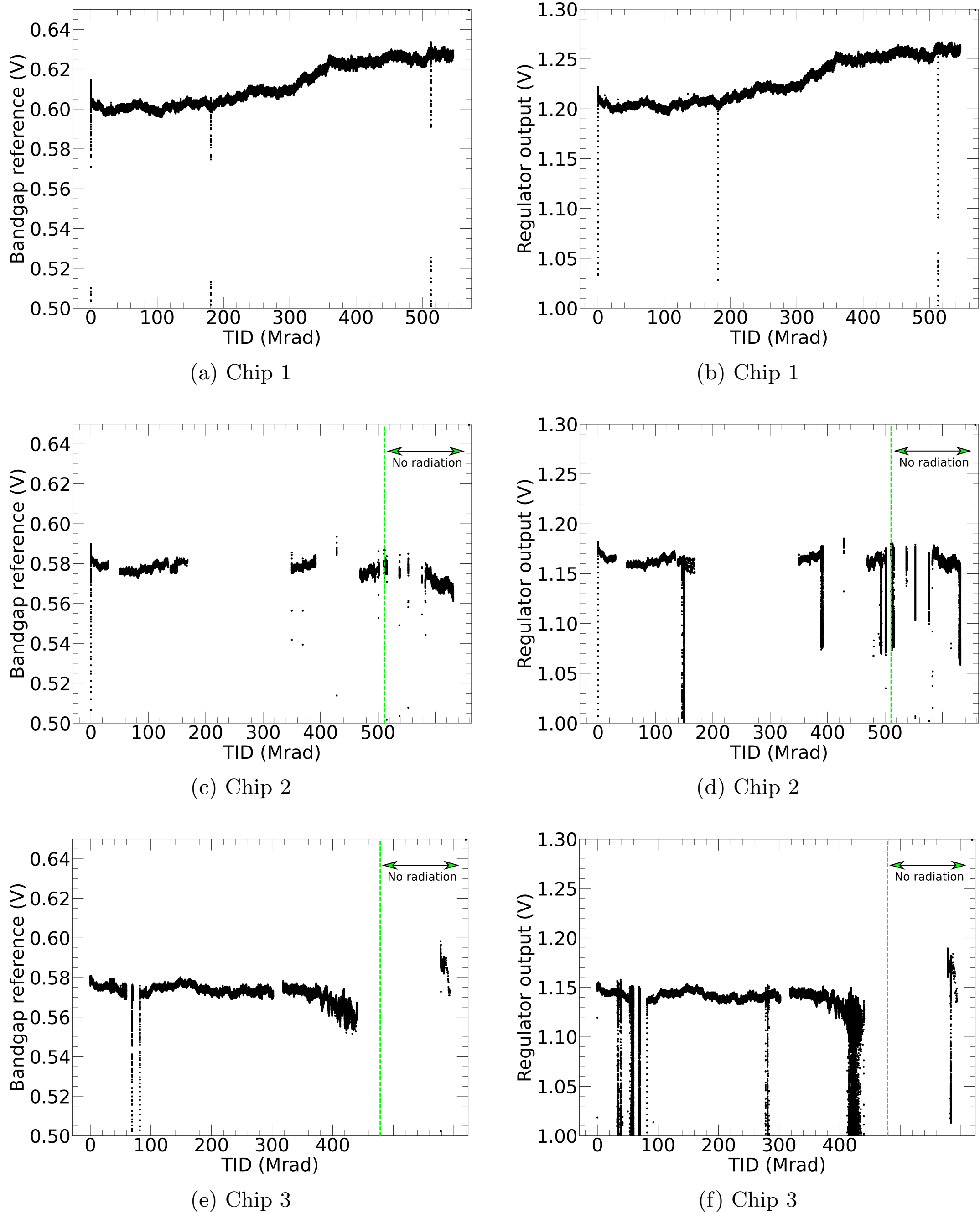


Figure 9.1: MOPSv1 current consumption and frequency variation w.r.t. TID



(a) Chip 1

(b) Chip 1

(c) Chip 2

(d) Chip 2

(e) Chip 3

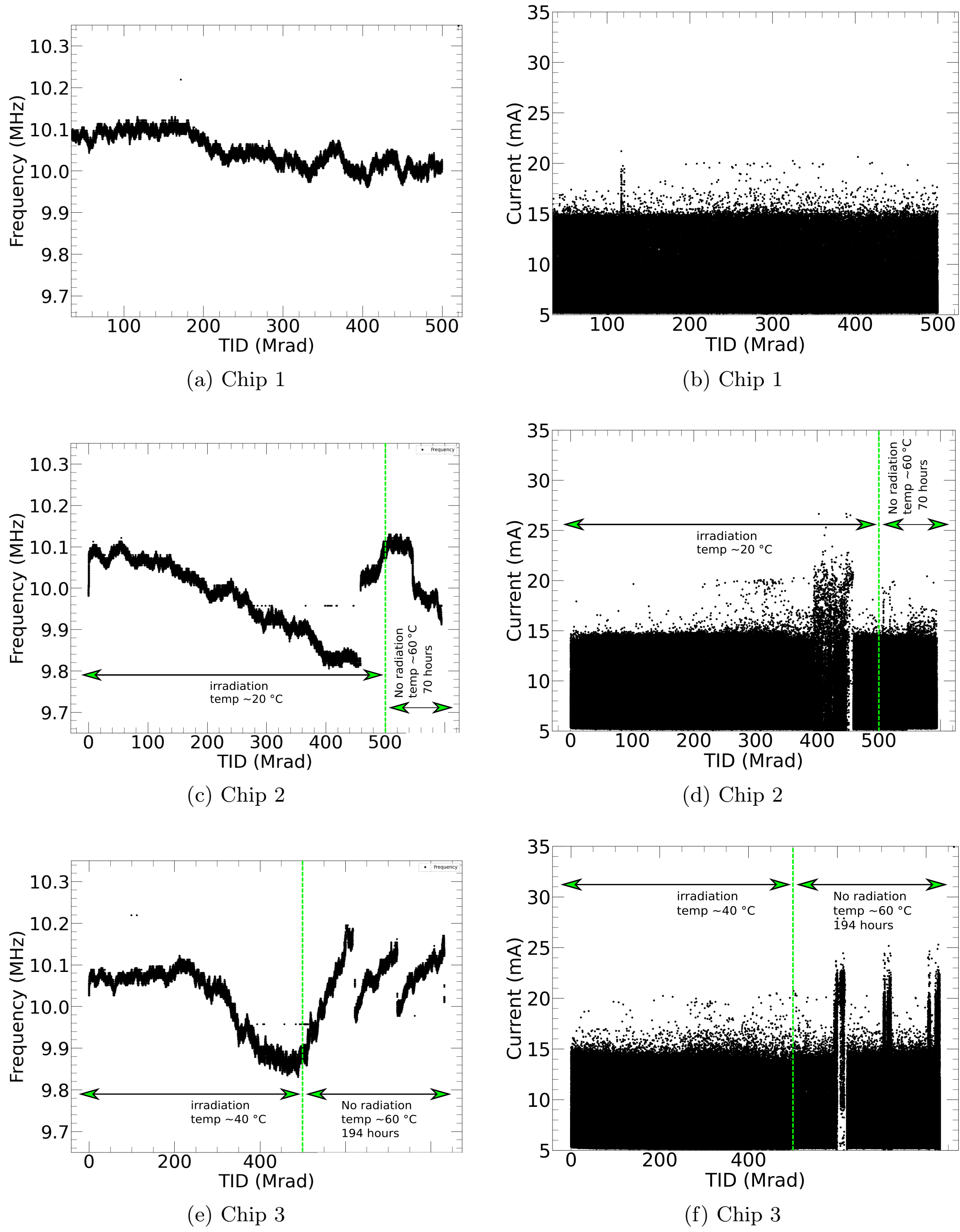
(f) Chip 3

Figure 9.2: MOPSv1 bandgap reference and regulator output voltage variation w.r.t. TID

software, but the chip itself was working completely fine and communicated the correct monitoring values. This can also be confirmed from the total current consumption plot. Compared to the MOPSv1 current consumption shown in Figure 9.1, the plot showing the current for the MOPSv2 gives an impression of the large variation in the current consumption and drops to a very low value. This was because of two problems with the test setup. The settings for the power supply on the test board were incorrect, and the sampling to log the current value was done faster than the circuit configuration could handle. For chip 2, at a TID of 455 Mrad, the deviation in the frequency increased to more than 1.5 %. At this point, a CAN communication error started to appear on the CAN bus. The behavior can also be confirmed by looking at the current consumption, which has increased. A remote reset command explained in Chapter 6 was able to bring back the chip frequency to the desired state of 10 MHz. This saved a power cycle, which is very beneficial in the final system because power cycles introduce transients and noise in the system. Chip 3 also had frequency shifts large enough to cause disturbance in communication, but every time, a remote reset command or a power cycle brought the chip back to an operational state. Change in the current consumption is the only significant difference seen between high dose rate and low dose rate irradiation for chip 1 mentioned in Table 9.2. Figure 9.6 shows the current consumption of the MOPSv2 under irradiation at a low dose rate of 40 krad/h. The plot 9.3(b) shows the current consumption of the same chip at a dose rate of 1.75 Mrad/h. Although, TID at a high dose rate is 16 times larger, an increase in the current consumption of ≈ 3 mA can only be seen during the low dose rate operation. This has not been observed in the other five chips irradiated at a high dose rate.

The output voltage from the bandgap reference and the regulator is shown in Figure 9.4. The total variation in the bandgap output after 500 Mrad is ≈ 3.33 % which is 0.58 % more than what is reported in [64] but much better than the MOPSv1 bandgap, which uses an older version of the same circuit and has a variation of as much as 5 %. Because of the $2\times$ multiplication factor between the bandgap reference and the regulator, the variation in the regulator output was double compared to the bandgap. The drop in the regulator output voltage around 400 Mrad for chip 2 and after the complete dose for chip 3 was because the MOPS regulator output was routed and also used as the supply voltage for the commercial CAN controller. There was some extra circuitry with a resistor in series, which caused the sampling problem only when the CAN communication was not good. The regulator output itself was without problems. This was confirmed from other sampled signals-

Figure 9.5 shows the POR circuit output for three MOPSv1 chips and three MOPSv2 chips. All six chips are the same, as explained in the previous sections. Apart from the powering problems that affected chips 2 and 3, the POR output strictly followed the regulator output without glitches.

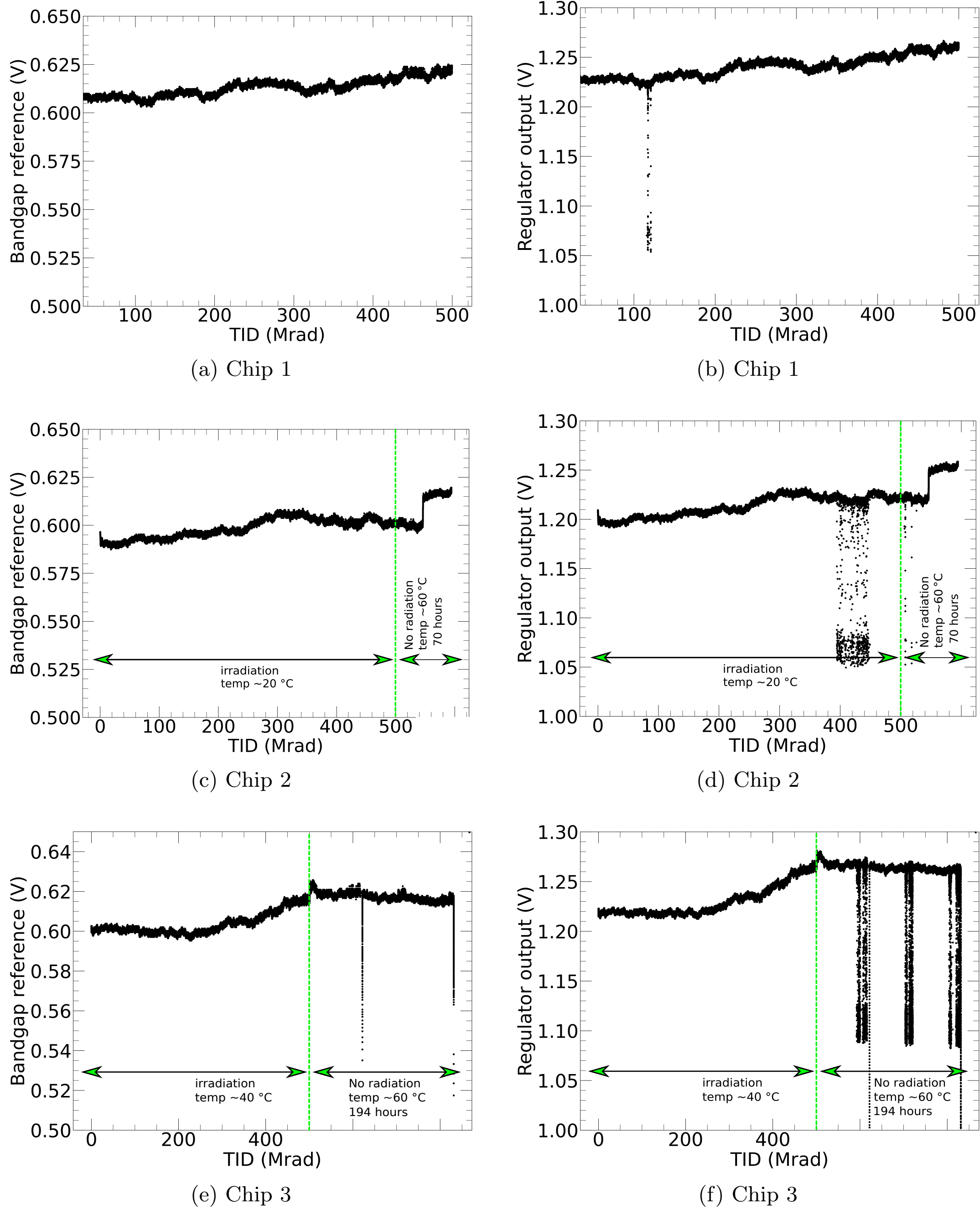


(a) Chip 1 (b) Chip 1

(c) Chip 2 (d) Chip 2

(e) Chip 3 (f) Chip 3

Figure 9.3: MOPSv2 current consumption and frequency variation w.r.t. TID

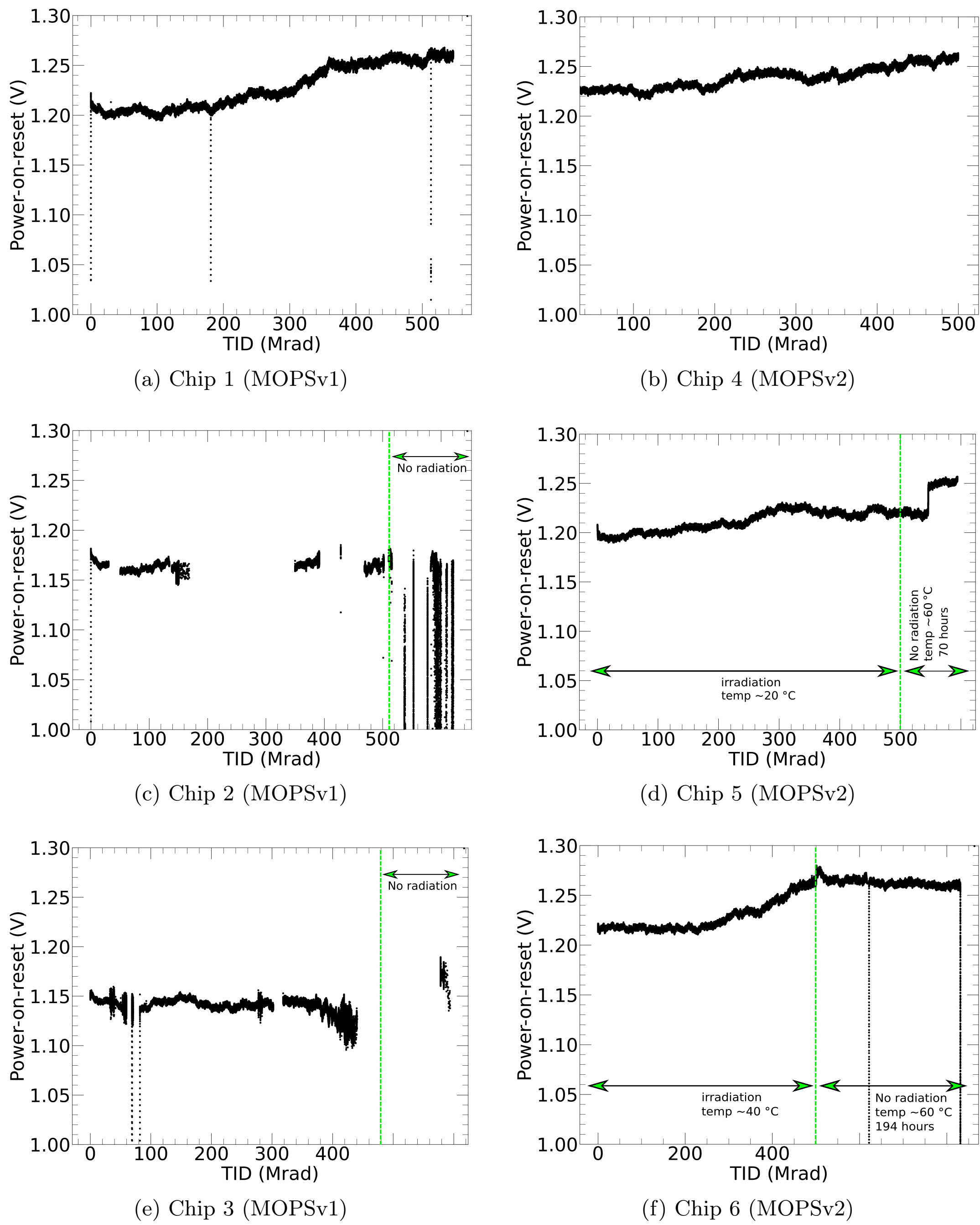


(a) Chip 1 (b) Chip 1

(c) Chip 2 (d) Chip 2

(e) Chip 3 (f) Chip 3

Figure 9.4: MOPSv2 bandgap reference and regulator output voltage variation w.r.t. TID



(a) Chip 1 (MOPSv1)

(b) Chip 4 (MOPSv2)

(c) Chip 2 (MOPSv1)

(d) Chip 5 (MOPSv2)

(e) Chip 3 (MOPSv1)

(f) Chip 6 (MOPSv2)

Figure 9.5: POR output w.r.t. TID

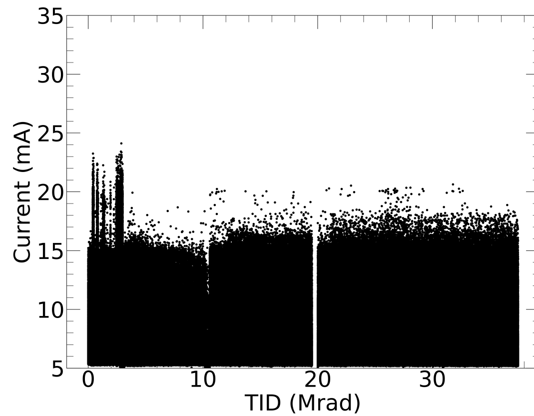


Figure 9.6: MOPSv2 current consumption under low dose rate irradiation

9.2 SEU tolerance using Heavy Ions

To calculate the SEU cross section for the TSMC 65 nm process in general and to test the tolerance of the MOPSv2 chip, heavy ions were used to irradiate the chips. The tests were done at the heavy Ion irradiation facility in Cyclotron Resource Centre (CRC), the technology platform of the Université Catholique de Louvain.

9.2.1 MOPSv2 performance

To ensure the MOPS chip can reliably provide the monitoring data, the chip must be able to tolerate the SEUs and the SETs. The digital logic does not facilitate a direct calculation of the SEU cross section for the chip because there is no real storage of monitoring data inside the chip. As soon as some new monitoring data becomes available, it stays for a very short period in a buffer before it is sent over the CAN bus. The configuration of the CAN node is the only critical storage inside the chip, but it is not possible to read it back to give an estimate of the flipped bits. The purpose of the SEU testing using heavy Ions was to confirm that the chip could survive without requiring any power cycles, latch-up, etc. For this purpose, the heaviest available Ion was chosen to irradiate the chip, which is Xenon with a LET of 62.5 MeV/(mg/cm^2) and a range of 73.1 µm. A maximum flux of 1.5×10^4 ions/s cm^2 was used during the campaign. The chip was irradiated for a total of 3.5 h. During the irradiation, the current consumption of the chip remained within range, and the chip never went into a state where it stopped communicating or required a power cycle. However, the chip displayed an undesired behavior, continuously sending sign-in messages between the normal monitoring values. The messages are highlighted yellow in Figure 9.7. Although this did not hinder the chip from communicating monitoring values, this behavior can be problematic for the automated trimming procedure. A sign-in message indicates either a real reset glitch on the chip or a bug in the digital logic. If it was a real reset glitch, this could reset the trimming

configuration, which is stored inside the chip after powering up. This can change the frequency, which will eventually cause the communication to stop. The automated trimming was not used during the irradiation campaign. Without a second SEU campaign and more verification, it is impossible to point out whether the problem is on the chip or the test boards.

```
1643960286.577297    ID: 0583   S         DLC:  8   43 00 24 11 0d 08 00 00
1643960286.607510    ID: 0583   S         DLC:  8   43 00 24 12 df 07 00 00
1643960286.635824    ID: 0583   S         DLC:  8   43 00 24 13 00 08 00 00
1643960286.649598    ID: 0703   S         DLC:  8   05 00 00 00 00 00 00 00
1643960286.663581    ID: 0583   S         DLC:  8   43 00 24 14 00 09 00 00
1643960286.686621    ID: 0583   S         DLC:  8   43 00 24 15 80 08 00 00
1643960286.711896    ID: 0583   S         DLC:  8   43 00 24 16 60 09 00 00
1643960286.734430    ID: 0583   S         DLC:  8   43 00 24 17 00 09 00 00
1643960286.757210    ID: 0583   S         DLC:  8   43 00 24 18 60 08 00 00
1643960286.779843    ID: 0583   S         DLC:  8   43 00 24 19 00 0a 00 00
1643960286.801259    ID: 0703   S         DLC:  8   05 00 00 00 00 00 00 00
1643960286.825226    ID: 0583   S         DLC:  8   43 00 24 1b 80 09 00 00
1643960286.847813    ID: 0583   S         DLC:  8   43 00 24 1c 20 09 00 00
1643960286.870477    ID: 0583   S         DLC:  8   43 00 24 1d 80 08 00 00
1643960286.893528    ID: 0583   S         DLC:  8   43 00 24 1e ff 07 00 00
1643960286.916704    ID: 0583   S         DLC:  8   43 00 24 1f 00 09 00 00
```

Figure 9.7: Performance of the MOPSv2 chip under heavy Ion irradiation

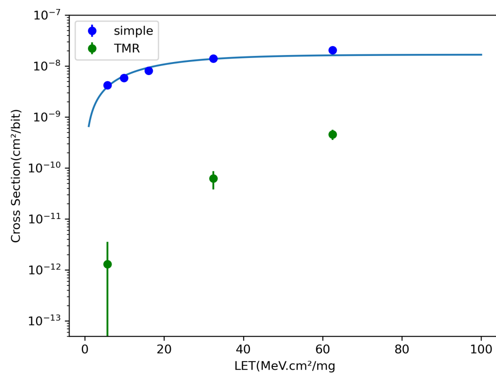
9.2.2 SEU cross section for 3000-bit shift register

The first test prototype chip, briefly explained in Chapter 5, was used for these tests. Because of the large beam diameter of 25 mm, a homogeneity of ±10 % and a small carrier board, it was possible to irradiate four chips in parallel. The deviation of the error rate between the four chips was insignificant. The cross-section for the 3000-bit shift register is shown in Figure 9.8(a). The blue line indicates the cross-section calculated for the simple shift register, whereas the green points on the plot indicate the cross-section for the register, which implements full TMR. Even though the FE chip uses clock skew to mitigate problems due to SET and a minimum distance of 15 µm between triplicated cells to mitigate multi-bit upsets, the cross-section calculated for the FE chip [36] is similar to what is calculated by using the 3000-bit shift register chip. The 3000-bit shift register chip implements full triplication without a distance between the triplicated cells and the clock skew. Limited irradiation time was the only reason that hindered getting a complete plot at different LET Ions.

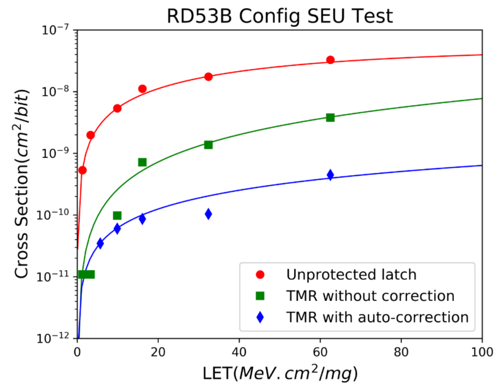
9.3 Summary

As already explained in Section 8.5, the variation in the bandgap output voltage does not affect the temperature monitoring, but to meet the voltage precision requirement to monitor the serial powering chain, calibration is required for the ADC values. The bandgap reference variation w.r.t. TID is not uniform but similar for four out of six MOPSv1/MOPSv2 chips.

As with temperature measurements, the automated frequency trimming feature introduced in MOPSv2 proved very helpful in coping with frequency variation w.r.t.



(a) SEU cross-section at different LET/ions using the 3000-bit shift register



(b) SEU cross-section calculated for the global configuration memory of the FE chip [36]

Figure 9.8: SEU cross-section for the TSMC 65 nm process

TID. The feature is beneficial for avoiding unnecessary power cycling. However, the reset glitch problem during the heavy Ion testing must be understood in more detail to not only reap the benefits of this feature but also to ensure the reliable operation of the chip.

Chapter 10

Packaging and production

10.1 Packaging experience

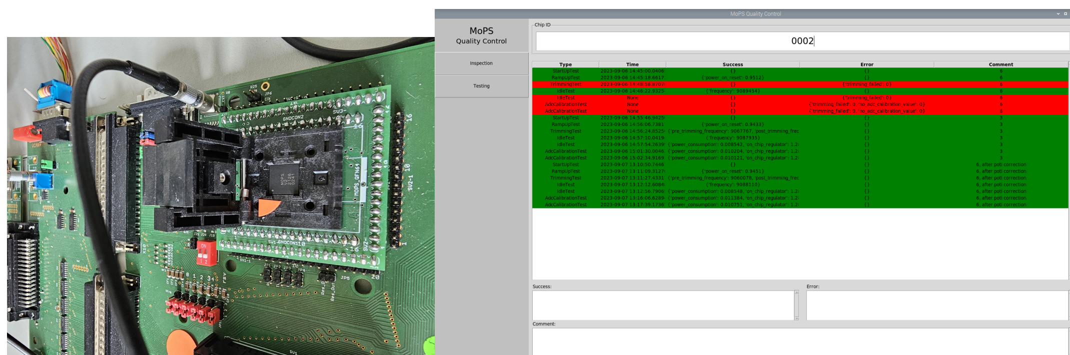
The size of the MOPS chip itself is only $2{\times}2\text{mm}^2$, the package chosen for the chip is a $9{\times}9\text{mm}^2$ QFN package that offers 64 pins. The package size is limited by the number of required pins.

MOPSv1 A total of 45 MOPSv1 chips were packaged at the University of Bonn and the University of Bern. Although with some difficulties, the overall yield was good. 39 out of 45 chips worked completely fine, giving a yield of 86.6 %. The only major problem seen for the MOPSv1 QFN packaged chips during testing was the glitches on the reset signal. Because of this problem, it was not possible to reliably communicate with the chip. The reason for the glitches was the way the test socket was used on the boards and not the chip itself. A QFN test socket was used to test the packages, but it was not pin-compatible with already available test boards. An adapter board was developed to bridge connections between the test board and the QFN socket board. This workaround created long signal lines and decoupling capacitors far from the chip pads. The problem was fixed with a new test socket carrier board.

MOPSv2 Thirty chips were wire-bonded at the University of Bern. A lot of those 30 chips saw the problem with the lid attachment. This was because not enough pressure was applied during the lid-baking process. This was easily fixed by baking the chips once again with new lids and under the weight of an approx. Forty grams of copper cube.
Due to a bug in the bonding scheme, a high current consumption of up to approx. 40 mA was seen in those chips. Some pads were configured as bi-directional inside the chip. Depending on whether automated trimming is enabled/disabled, the pads act as output/input, respectively. To provide the code manually, trimming pads acted as input when the automated trimming mode was disabled. In this mode, the current had an average current consumption of 8 mA. The results from the MOPSv2 packaged chips helped to decide the default trimming mode for the pre-production chips.

10.2 Pre-production yield and QA/QC tests

A total of 400 MOPSv2 pre-production chips were produced and packaged. ≈ 100 chips were used for different test boards required for other tests. The first commercial packaging of the MOPS chip was done using a total of 330 chips for pre-production needs packaged by IMEC. This was enough to meet demand for all the subsystems. At the point of writing this thesis, 165 out of a total of 188 tested chips worked completely fine, which gives a yield of ≈ 87.7 %. The remaining 23 chips failed the QA/QC test but may not be completely bad because it could be just a single value out of the defined good range. Shown in Figure 10.1(a) is the test socket to place packaged chips. 10.1(b) shows a screenshot of the software used to check the quality of MOPSv2 pre-production chips



(a) Test socket for the packaged MOPS chips

(b) Quality control software for the pre-production and production

Figure 10.1: Quality assurance/quality control tests of the pre-production chip

10.3 MOPSv3 for production

When writing this thesis, there is a plan to submit the third version of the chip called the MOPSv3. Most likely, this version will be used for the production as well. The MOPSv3 chip will get some updates to increase stability, and some problems in the digital logic will also be removed. Below mentioned are some of the updates:

- After the MOPSv2 fabrication, the bandgap reference circuit available from FE chip developers was updated. The new version of the bandgap has an improved Pre-regulator bandgap startup circuit. Tolerance towards SETs has been improved in the newer version. The newest version will most likely be used on the MOPSv3, but this is still under consideration.
- A 100 ns noise on the bandgap reference output is most likely because of the oscillator. A low pass filter will be integrated into the MOPSv3. This will also improve the precision of the ADC.

- A large decoupling capacitor will be used on the chip to improve the regulator output.
- TMR implementation in the digital logic will be fixed where some voters are not in the right position, and also some critical feedback paths are missing

Chapter 11

Conclusion and future work

The Monitoring of Pixel System (MOPS) chip has been developed to monitor temperature and voltage for the new ATLAS ITk Pixel Detector readout modules. The chip was developed using the TSMC 65 nm CMOS process. The TSMC 65 nm was chosen because the technology is inherently radiation-hard. The radiation hardness of the technology has been studied and characterized in detail for more than a decade by the particle physics community and chosen by CERN as the default technology for upcoming upgrades of different experiments. Three prototype MOPS chips were developed, from the first concept to the pre-production version. The chip offers a 12-bit Successive-Approximation-Register (SAR) based Analog-to-Digital (ADC) to read up to 34 channels with a resolution of 219 µV. The chip uses CAN communication protocol to communicate monitoring data over a distance of more than 70 m. In addition to compliance with the standard CAN protocol, the chip uses a non-standard low-voltage CAN physical layer that works at 1.2 V. This is especially useful for modern low-voltage CMOS processes. The chip also provides some new features on top of the existing CAN protocol, where the on-chip oscillator can be calibrated via the CAN messages to cope with the process variation and operational conditions. This can be done at startup or by using the remote reset command to avoid unnecessary power cycling. The MOPS chip provides a minimal implementation of the CANopen standard to reduce size, cost, and complexity. In addition to full Triple Modular Redundancy (TMR), reset de-glitching, and frequent configuration refreshing, the minimal implementation of the CANopen in a hardwired logic also helps protect the chip against Single Event Effect (SEE). Rigorous testing of the chip under different operating conditions explained in Chapters 7, 8, and 9 has proven the robustness of the chip to reliably provide the monitoring data and meet the requirements defined in Section 6.1. The chip has been tested for an operational temperature of −40 °C to 60 °C, irradiated for a Total Ionizing Dose (TID) of at least 500 Mrad up to a temperature of as high as 40 °C and also proved its SEU tolerance under heavy ion irradiation. The fourth prototype chip, called MOPSv3, is under development. The MOPSv3 will probably be used for the final production.

The MOPS chip can also be used as a general-purpose monitoring and control chip in other CERN experiments or high-radiation environments. The chip's digital logic has been designed to allow easy extension of other CANopen constructs to monitor and interface peripherals in the future. The chip currently only uses Service Data

Objects (SDO), but integrating the Process Data Objects (PDO) can expedite the data throughput with the least protocol overhead. Because of modular design, an ADC that provides more resolution can also be integrated with little effort for high-precision applications.

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Appendix A

MOPS IO pads description

Below-mentioned is the description of some of the pads and components:

VDD SHUNT This is used to

- enable => connection to VCAN
- disable => connection to ground

shunt-mode of the SLDO amplifier.

REXT The resistor defines the input impedance of the SLDO in shunt-mode and is connected to VCAN when shunt-mode of the SLDO is enabled.

VDDPRE output of the pre-regulator and requires a connection to a 100nF blocking capacitor against the ground.

VREF The voltage reference for the definition of the regulator output and the ADC LSB voltage requires a 30 KOhm resistor connected to the ground.

VOFSHALF Offset voltage reference which is used when the SLDO is configured in shunt-mode and requires a 20 KOhm resistor connected to the ground.

BGTRIMx These pads are used to trim the bandgap circuit. MSB which is BGTRIM3 is pulled up internally while the rest of the pins are pulled down internally.

A.0.1 Power and IO Signal Specifications

In the following section, IO and power signals are described.

Table A.1 describes all the IO signals used in the chip. Please see the footnotes of the table for hints. Further details about different pads are given in table A.4 and A.3.

Table A.1: All pads in the outer ring of the chip

Signal name	Direction	Signal type	Pad type	Description
BGTRIM0	IN	digital	CERN_IO_ mod_VSUB _PAD	Trimming bit for the bandgap circuit
BGTRIM1	IN	digital	CERN_IO_ mod_VSUB _PAD	Trimming bit for the bandgap circuit
BGTRIM2	IN	digital	CERN_IO_ mod_VSUB _PAD	Trimming bit for the bandgap circuit
BGTRIM3	IN	digital	CERN_IO_ mod_VSUB _PAD	Trimming bit for the bandgap circuit
BGIREF	-	analog	SF_1V2_FULL _LOCAL	Reference current for the bandgap circuit
VBUS	IN	analog	SF_1V2_FULL _LOCAL	CAN bus voltage in recessive state
RXCAN	OUT	digital	CERN_IO_ mod_VSUB _PAD	Received bit from CAN Phy. layer
TXCAN	IN	digital	CERN_IO_ mod_VSUB _PAD	Bit to transmit using CAN Phy. layer
RXLOG	IN	digital	CERN_IO_ mod_VSUB _PAD	Received bit to the logic
TXLOG	OUT	digital	CERN_IO_ mod_VSUB _PAD	Bit from the logic to be transmitted
ADDRCAN0	IN	digital	CERN_IO_ mod_VSUB _PAD	CAN node address

Table A.1 continued from previous page

Signal name	Direction	Signal type	Pad type	Description
ADDRCAN1	IN	digital	CERN_IO_ mod_VSUB _PAD	CAN node address
auto_trim_en	IN	digital	CERN_IO_ mod_VSUB _PAD	CAN node address
RESETD	IN	digital	CERN_IO_ mod_VSUB _PAD	External reset to reset the digital part
Reset_out	OUT	digital	CERN_IO_ mod_VSUB _PAD	Output of the POR circuit
ADC34	IN	analog	SF_1V2_CDM	ADC channel input pad
ADC33	IN	analog	SF_1V2_CDM	ADC channel input pad
* VSUB	-	-	-	-
ADC32	IN	analog	SF_1V2_CDM	ADC channel
ADC31	IN	analog	SF_1V2_CDM	ADC channel
ADC30	IN	analog	SF_1V2_CDM	ADC channel
ADC29	IN	analog	SF_1V2_CDM	ADC channel
ADC28	IN	analog	SF_1V2_CDM	ADC channel
ADC27	IN	analog	SF_1V2_CDM	ADC channel
ADC26	IN	analog	SF_1V2_CDM	ADC channel
ADC25	IN	analog	SF_1V2_CDM	ADC channel
ADC24	IN	analog	SF_1V2_CDM	ADC channel
ADC23	IN	analog	SF_1V2_CDM	ADC channel
ADC22	IN	analog	SF_1V2_CDM	ADC channel
ADC21	IN	analog	SF_1V2_CDM	ADC channel
ADC20	IN	analog	SF_1V2_CDM	ADC channel
ADC19	IN	analog	SF_1V2_CDM	ADC channel
ADC18	IN	analog	SF_1V2_CDM	ADC channel

Table A.1 continued from previous page

Signal name	Direction	Signal type	Pad type	Description
ADC17	IN	analog	SF_1V2_CDM	ADC channel
* VSUB	-	-	-	-
ADC16	IN	analog	SF_1V2_CDM	ADC channel
ADC15	IN	analog	SF_1V2_CDM	ADC channel
ADC14	IN	analog	SF_1V2_CDM	ADC channel
ADC13	IN	analog	SF_1V2_CDM	ADC channel
ADC12	IN	analog	SF_1V2_CDM	ADC channel
ADC11	IN	analog	SF_1V2_CDM	ADC channel
ADC10	IN	analog	SF_1V2_CDM	ADC channel
ADC9	IN	analog	SF_1V2_CDM	ADC channel
ADC8	IN	analog	SF_1V2_CDM	ADC channel
ADC7	IN	analog	SF_1V2_CDM	ADC channel
ADC6	IN	analog	SF_1V2_CDM	ADC channel
ADC5	IN	analog	SF_1V2_CDM	ADC channel
ADC4	IN	analog	SF_1V2_CDM	ADC channel
ADC3	IN	analog	SF_1V2_CDM	ADC channel
GNDSEN	IN	analog	SF_1V2_CDM	ADC channel
VCANSEN	IN	analog	SF_1V2_CDM	ADC channel
ADCRET	IN	analog	SF_1V2_FULL_LOCAL	Return line for the ADC
Clk_out	OUT	digital	CERN_IO_mod_VSUB_PAD	Clock output from the internal oscillator
Clk_in	IN	digital	CERN_IO_mod_VSUB_PAD	Input clock to the digital part
Vofshalf	IN	analog	SF_1V2_OVT_NOB2B	CAN transceiver local ground
Vref	IN	analog	SF_1V2_OVT_NOB2B	Reference voltage for the regulator and the ADC LSB voltage

Table A.1 continued from previous page

Signal name	Direction	Signal type	Pad type	Description
VDD_PRE	power	analog	SF_1V2_OVT _NOB2B	Output of the preregulator
* VCAN	-	-	-	-
VCAN	power	analog	SF_1V2_OVT _NOB2B	Supply voltage for the chip
Rext	-	analog	SF_1V2_OVT _NOB2B	Config resistor for shuldo
* VDD1V2	-	-	SF_1V2_POWER _CLAMP_CORE _SUPPLY	Output of the regulator
VDD1V2	power/out	analog	SF_1V2_POWER _CLAMP_IO _SUPPLY	Output of the regulator
VDD_SHUNT	power/in	analog	SF_1V2_OVT _NOB2B	enable/disable shunt mode by conn. to VCAN/GND
* GND	-	-	-	-
GND	gnd	analog	SF_1V2_ POWER _CLAMP_IO _GROUND	Ground conn. for the chip
CANH	in/out	analog	SF_1V2_CDM	CAN bus high sig.
CANL	in/out	analog	SF_1V2_CDM	CAN bus low sig.
VSUB	-	gnd	SF_1V2_ POWER _CLAMP_CORE _GROUND	Substrate conn.
* = Internally connected to the pin with similar name				

Maximum Ratings

This section specifies the maximum ratings for inputs.

- All the inputs with the pads that are connected to the 1V2 ESD ring must not be supplied more than $\pm 1.3V$. If the input goes above that value, then the ESD

protection circuit gets activated.

- Inputs using SF_1V2_OVT_NOB2B pad must not be supplied more than 2V in general but must look at individual values given in the table A.2:
- To check all the ESD protection ratings of different pads used in the chip, tables A.4 and A.3 must be consulted.

Table A.2: Maximum ratings for different input pads

Name	Min	Typ	Max	Unit
VDD_SHUNT	1.2	1.6	2.0	V
VCAN	1.4	1.5	2.0	V

Power pad specifications

Table A.3 lists all the power pads used in this chip.

Table A.3: This table lists all the pads used for powering the chip.

Name	ESD connection	Description
SF_1V2_POWER_CLAMP_IO _SUPPLY	1V2	SF_1V2_POWER_CLAMP _CORE_SUPPLY (Shorted)
SF_1V2_POWER_CLAMP_IO _GROUND	1V2	Supply ground
SF_1V2_POWER_CLAMP _CORE_GROUND	1V2	Substrate connection
SF_1V2_OVT _NOB2B	2V0	Supply voltage

IO pad Specifications

Table A.4 lists all the IO pads used in the chip.

Table A.4: This table lists all the pads used for IO connections

Name	Type	ESD connection
CERN_IO_mod_VSUB_PAD	digital	1V2 ESD ring
SF_1V2_CDM	analog	1V2 ESD ring
SF_1V2_OVT_NOB2B	analog	OVT*

Table A.4 continued from previous page

Name	Type	ESD connection
SF_1V2_FULL _LOCAL	analog	1V2 ESD ring

* Over voltage tolerant i.e. can withstand up to 2V.

Appendix B

MOPS CANopen object dictionary

Object Dictionary (OD)

Table B.1 and B.2 show communication and manufacturer-specific profile area of the object dictionary respectively. All values are hexadecimal if not otherwise stated. The information in the object dictionary is required to communicate with the MOPS chip. The placement of index/subindex and read/write commands inside the CAN message should be done as explained in 6.3.2 and 6.3.2

Table B.1: Communication profile area of OD

Index	SI	Description	Data/Object	Attr	Default	Comment
1000		Device type	U32	RO	191	Meaning: DSP-401 device profile, analogue in- and outputs, digital in- and outputs on device. Mandatory object
1001		Error register	U8	RO	0	Mandatory
1005		COB-ID SYNC	U32	RO	80	
1014		COB-ID EMCY	U32	RO	80 + NodeId	
1018		Identity object	RECORD			Mandatory CANopen object
	0	Number of entries	U8	RO	1	
	1	Vendor Id	U32	RO	12345678	Ambiguous since we will never receive an official vendor Id
1200		Server SDO parameter 0	RECORD			Define standard COB-ID for SDO
	0	Number of entries	U8	RO	2	
	1	COB-ID client to server	U32	RO	600 + NodeId	
	2	COB-ID server to client	U32	RO	580 + NodeId	
1800		TPDO communication parameter 0	RECORD			May be used for confirming a bypass command
	0	Number of entries	U8	RO	6	
	1	COB-ID	U32	RO	180 + NodeId	
	2	Transmission type	U8	RO	FE	Event driven - manufacturer specific

Table B.1 continued from previous page

Index	SI	Description	Data/Object	Attr	Default	Comment
	3	Inhibit time	U16	RO	0	
	4	Reserved	U8	RO		Unused, manufacturer specific
	5	Event timer	U16	RO	0	
	6	SYNC start value	U8	RO	0	
1801		TPDO communication parameter 1	RECORD			
	0	Number of entries	U8	RO	6	
	1	COB-ID	U32	RO	280 + NodeId	
	2	Transmission type	U8	RO	FE	Event driven - manufacturer specific
	3	Inhibit time	U16	RO	0	
	4	Reserved	U8	RO		Unused, manufacturer specific
	5	Event timer	U16	RO	0	
	6	SYNC start value	U8	RO	0	
		TPDO mapping parameter 0	RECORD			
1A00	0	Number of entries	U8	RO	1	
	1	PDO mapping entry	U32	RO	21000020	“2100”: Index; “00”: Subindex; “20” : Data length (20=32 bit)
1A01		TPDO mapping parameter 1	RECORD			

Table B.1 continued from previous page

Index	SI	Description	Data/Object	Attr	Default	Comment
	0	Number of entries	U8	RO	1	
	1	PDO mapping entry	U32	RO	21010030	“2101”: Index; “00”: Subindex; “30” : Data length (30=48 bit)

Table B.2: Manufacturer specific profile area

Index	SI	Description	Data/Object	Attr	Default	Comment
2001		ADC trimming bits	U8	RW		This entry refers to a 6 bit register for ADC trimming which is to be set via SDO when the server starts up. The value should originate from a config file.
2100		Read monitoring values of all FEs	U32	RO		Only to be used with TPDO0. This should return some SDO abort code when polled with SDO.
2310		Other monitoring values	RECORD			This object contains monitoring values which are not connected to a single FE. All values come as raw ADC counts.
	0	Number of entries	U8	RO	3	
	1	VBANDGAP	U16	RO		Bandgap output voltage
	2	VCANSEN	U16	RO		CAN sense line voltage
	3	VGNDSEN	U16	RO		Ground sense line voltage
2400		Internal ADC channels	RECORD			This entry contains all ADC channels which do not have a defined functionality up to now.
	0	Number of entries	U8	RO	40	
	01-20	ADCCh3-ADCCh34	U16	RO		