GHz Transceiver Design in Amorphous InGaZnO Technology

BERGISCHE
UNIVERSITÄT
WUPPERTAL

Dissertation

Submitted in partial fulfillment of the requirements for the degree of

Doktor der Ingenieurwissenschaften

at the

University of Wuppertal, Germany
School of Electrical, Information and Media Engineering

by

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submitted on 23^{rd} of March, 2023 in Wuppertal, Germany

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Dedicated to my wonderful family
for their love, support and encouragement
and to all my teachers
for their wisdom and inspiration.

Declaration

I, Utpal Kalita, herewith declare that I have produced this thesis without the prohibited assistance of third parties and without making use of aids other than those specified; notions taken over directly or indirectly from other sources have been identified as such. This work has not previously been presented in identical or similar form to any other German or foreign examination board.

The thesis work was conducted from 2017 to 2023 under the supervision of Prof. Dr. rer. nat. Ullrich R. Pfeiffer at the University of Wuppertal. This work was funded by the German Research Foundation (DFG) individual research grant for project '10by10.com' and as part of SPP 1796 'Flexible Communication System (FFlexCom)'.

Wuppertal, March 2023

Acknowledgements

This thesis was completed under the doctoral student program at Bergische Universität Wuppertal. The successful completion of this research resulted from the support of many people at my university.

I would like to express my sincere gratitude toward my advisor Prof. Ullrich Pfeiffer. I thank him for believing in me from the beginning and for the continuous encouragement and motivation imparted throughout the journey. He even took time from his schedule to perform measurements with me in the laboratory and familiarize me with high-frequency circuits.

I am grateful to Prof. Thomas Riedl for his valuable feedback and support at every research step. He was always proactive in replying to my queries and guided my research. I thank my project partner Christian Tückmantel for providing me with the devices and circuits necessary to complete the thesis. He was always ready to fabricate any circuit ideas that I suggested.

I would also like to thank the following persons in no particular order:

- Dr. Phillip Hillger for doing the initial work of this project and always guiding me with his immense experience.
- Dr. Vishal Jagtap for engaging me in measurements, circuit design, and publication in silicon photonics.
- Dr. Janusz Gryzb and Dr. Ritesh Jain for proofreading my publications.
- My colleagues for their encouragement.
- Mr. Wolfgang Förster, for teaching me the intricacies of probe station measurement.

Most importantly, I would like to thank my family and friends for their love and support. I am always indebted to my uncle and aunt and my parents, who prioritized my education above anything else. I can't thank my sisters enough for being such wonderful people and supporting my parents. I would like to thank Daniel Simon for proofreading this thesis. Last but not least, I would also like to thank my girlfriend, Juliane. She has made this arduous journey easy and fantastic.

Contents

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List of Abbreviations

Abbreviation	Meaning
a-IGZO	Amorphous indium-gallium-zinc-oxide
a-Si	Amorphous silicon
a-Si:H	Hydrogenated amorphous silicon
AC	Alternate current
ALD	Atomic layer deposition
BER	Bit error rate
BPSK	Binary phase shift keying
BW	Bandwidth
c-Si	Crystalline silicon
CG	Common gate
CMOS	Complementary metal oxide semiconductor
DC	Direct current
DUT	Device under test
FET	Field effect transistor
f_{max}	Maximum oscillation frequency
FoM	Figure of merit
f_T	Transit frequency
GSG	Ground signal ground
GSSG	Gate signal signal ground
HBT	Heterojunction bipolar transistor
IF	Intermediate frequency
ISM	Industrial, scientific and medical
InP	Indium phosphide
L	TFT channel length
$L_{<subscript>}$	Inductor
LC	Inductor capacitor
LCD	Liquid crystal display
LO	Local oscillator
LRM	Load reflect match
MTTF	Mean time to failure

N/A	Not applicable
NEP	Noise equivalent power
NF	Noise figure
NMP	N-Methylpyrrolidone
NQS	Non-quasi static
NRMSE	Normalized root mean square error
OOK	On-off keying
OS	Open-short
PA	Power amplifier
PAE	Power added efficiency
PCB	Printed circuit board
PDK	Process development kit
PPG	Power-power-ground
PSD	Power spectral density
RFID	Radio frequency identification
RF	Radio frequency
RMSE	Root mean square error
RO	Ring oscillator
RPI	Rensselaer polytechnic institute
SiGe	Silicon-germanium
SMA	SubMiniature A
SMU	Source meter unit
SNR	Signal-to-noise ratio
SOL	Short open load
SOLT	Short open load thru
Te	Tellurium
TFT	Thin film transistor
TMA	Trimethylaluminum
TRL	Thru reflect load
VNA	Vector network analyzer
W	TFT channel width

Publications

Journal Publications

1. **U. Kalita**, C. Tueckmantel, T. Riedl, and U. R. Pfeiffer (2023), A Multi-finger GHz Frequency Doubler based on Amorphous Indium Gallium Zinc Oxide Thin Film Transistors. IEEE Access.

2. C. Tueckmantel, **U. Kalita**, T. Haeger, M. Theisen, U. R. Pfeiffer, and T. Riedl (2020). Amorphous indium-gallium-zinc-oxide TFTs patterned by self-aligned photolithography overcoming the GHz threshold. IEEE Electron Device Letters, 41(12), 1786-1789.

3. **U. Kalita**, C. Tueckmantel, T. Riedl, and U. R. Pfeiffer (2018). Evaluation of the Beyond-f_T Operation of an IGZO TFT-Based RF Self-Mixing Circuit. IEEE Microwave and Wireless Components Letters, 29(2), 119-121.

Contributions of Others

This work was conducted at the Institute for High-Frequency and Communication Technology (IHCT), University of Wuppertal in Wuppertal, Germany. The research group is led by Prof. Dr. rer. nat. Ullrich R. Pfeiffer. The contributions made by other group members to the circuits and measurements presented in this work are listed below. Any research not included in the list was conducted by myself.

The thin-film-transistors and all the pertinent circuits used in this work were fabricated by Mr. Christian Tückmantel at the Institute for Electronic Devices (LFEB), under the supervision of Prof. Dr. rer. nat. Thomas Riedl.

- **Chapter 1:** The link-budget calculation was done by Prof. U. Pfeiffer. The goals of the supporting project were also defined by Prof. Riedl and Prof. Pfeiffer.
- **Chapter 2:** Some initial data on the performance of the thin film transistors were collected and summarized by Dr. Philipp Hillger, Mr. Wolfgang Förster, and Mr. Christian Tueckmantel.

  The improvement of the transit frequency was theorized and implemented by Mr. Christian Tueckmantel. Moreover, the choice of electrode materials with low resistivity was also made by him.
- **Chapter 3:** Prof. U. Pfeiffer wrote the code for the calibration-standard-based S-parameter de-embedding.
- **Chapter 4:** The layout of the first frequency doubler ($100\,\mathrm{MHz}$ to $200\,\mathrm{MHz}$) was proposed by Dr. Philipp Hilger and Prof. U. Pfeiffer.
- **Chapter 5:** The layout of the first detector (same circuit as the doubler mentioned above) was proposed by Dr. Philipp Hillger and Prof. U. Pfeiffer.
- **Chapter 6:** The explanation of the fabrication yield issue was assessed and revised by Mr. Christian Tückmantel.

Abstract

Metal-oxide semiconductors can revolutionize the field of biomedical communication and human-machine interaction systems. Compared to rigid silicon technology, this newly invented technology offers the substrate's thinness, recyclability, and low-cost production. The semiconductors are implemented in thin film transistors (TFTs), which have already found widespread use in display devices and some sensors.

Low device speed and power are significant roadblocks in utilizing metal-oxide technology in communication systems. Recently this issue has been addressed in the literature. However, the existing research primarily focused on building tens of MHz transmitters and receivers, with a few exceptions. A higher operating frequency, such as 1 GHz, would benefit from more compact antennas, enabling smaller transceiver sizes. Hence more insight into the reliability and capability of metal-oxide semiconductors in the GHz range is needed.

This thesis will demonstrate integrated circuits based on amorphous Indium Gallium Zinc Oxide (a-IGZO) for a GHz communication system. To this end, gate resistance optimization has dramatically increased our in-house a-IGZO transistors' maximum oscillation frequency (f_{max}).

We have also rigorously characterized and modeled the in-house a-IGZO transistors for GHz applications during the timeline. A differential frequency doubler has been designed with multi-finger TFTs to compensate for the low carrier mobility of the transistors. The device can generate a $1\,\mathrm{GHz}$ output signal from a $500\,\mathrm{MHz}$ input signal with $-29\,\mathrm{dB}$ of conversion loss. We showed that this is beyond the comprising transistors' f_{max}.

For receivers, we have also shown the utility of the doubler as a square-law detector. A record low $1.6\,\mathrm{nW}/\sqrt{\mathrm{Hz}}$ noise equivalent power is achieved at $1\,\mathrm{GHz}$. This result is a tenfold improvement from the first generation of the a-IGZO detector presented in our first paper in IEEE Microwave Components and Letter.

A complete on-off keying transceiver system based on a-IGZO has also been conceptualized and simulated with the extracted model for our record high-speed transistors. Simulation shows that data rate, system cost, and output capability results exceed the state-of-the-art transceiver performance. If a higher fabrication yield can be guaranteed, such a system can find many applications in real-time communication at a lower cost than silicon.

Zusammenfassung

Metalloxid-Halbleiter können den Bereich der biomedizinischen Kommunikation und der Mensch-Maschine-Interaktionssysteme revolutionieren. Im Vergleich zur starren Siliziumtechnologie bietet diese neu entwickelte Technologie die Vorteile, dass das Substrat dünn ist, wiederverwertet werden kann und kostengünstig in der Herstellung ist. Die Halbleiter werden in Dünnschichttransistoren (TFTs) eingesetzt, die bereits in Displays weit verbreitet waren und in einigen Sensoren Verwendung gefunden haben.

Die geringe Geschwindigkeit und Leistung der Bauelemente sind ein großes Hindernis für den Einsatz der Metalloxidtechnologie in Kommunikationssystemen. In jüngster Zeit wurde dieses Problem in der Literatur behandelt. Die bisherige Forschung konzentrierte sich jedoch hauptsächlich auf den Bau von Sende- und Empfangskomponenten im Zehn-MHz-Bereich mit geringen Betriebsbereichen (in Zentimetern), von einigen Ausnahmen abgesehen. Bei einer höheren Betriebsfrequenz, z. B. $1\,\mathrm{GHz}$, ergäben sich kompakte(re) Antennen als Vorteil, die kleinere Sendeempfänger ermöglichen. Daher sind weitere Erkenntnisse über die Zuverlässigkeit und Leistungsfähigkeit von Metalloxid-Halbleitern im GHz-Bereich erforderlich.

In dieser Arbeit werden integrierte Schaltungen auf der Basis von amorphem Indium-Gallium-Zink-Oxid (a-IGZO) für ein GHz-Kommunikationssystem demonstriert. Zu diesem Zweck haben wir durch Optimierung des Gate-Widerstands die maximale Schwingungsfrequenz (f_{max}) unserer hauseigenen a-IGZO-Transistoren drastisch erhöht.

Außerdem haben wir die hauseigenen a-IGZO-Transistoren für GHz-Anwendungen während des Zeitrahmens gründlich charakterisiert und modelliert. Um die geringe Ladungsträgerbeweglichkeit der Transistoren zu kompensieren, haben wir einen Frequenzverdoppler entwickelt und verbessert. Der Baustein kann ein $1\,\mathrm{GHz}$-Ausgangssignal aus einem $500\,\mathrm{MHz}$-Eingangssignal mit einem Umwandlungsverlust von $-29\,\mathrm{dB}$ erzeugen. Wir haben gezeigt, dass dies jenseits der Geschwindigkeit und der Ausgangsleistung der Transistoren liegt.

Bei Empfängern haben wir auch die Nützlichkeit des Verdopplers als Square-Law Detektor gezeigt. Eine Rekord-Rauschäquivalentleistung von $1.6\,\mathrm{nW}$ wird bei $1\,\mathrm{GHz}$ erreicht. Dieses Ergebnis ist eine zehnfache Verbesserung gegenüber der ersten Generation des

a-IGZO-Detektors, der in unserem ersten Verdoppler in IEEE Microwave Components and Letter vorgestellt wurde.

Ein komplettes On-Off-Keying-Transceiver-System auf der Basis von a-IGZO wurde ebenfalls konzipiert und mit dem extrahierten Modell für unsere Rekord-Hochgeschwindigkeitstransistoren simuliert. Die Simulationen zeigen, dass die Datenrate, die Systemkosten und die Ausgangskapazität die Leistung der modernsten Transceiver übertreffen. Wenn eine höhere Fertigungsausbeute garantiert werden kann, kann ein solches System viele Anwendungen in der Echtzeitkommunikation zu geringeren Kosten als Silizium finden. Darüber hinaus könnte es auch die Grundlage für die Erforschung von a-IGZO im bestehenden ISM 2,4 GHz-Band bilden, um billigere, wiederverwertbare WiFi-Kommunikationsgeräte zu ermöglichen.

Chapter 1

Introduction

1.1 Scope of this work

There has been an increasing interest in wearable and implantable electronics in the recent years [1]. By using sensors either invasively or non-invasively, the health conditions of individuals can be monitored. The advent of the Internet-of-Things (IoT) paradigm added the advantage of real-time diagnosis, measurement and monitoring of clinically relevant information such as temperature, blood pressure, heart rate and pH [2]. Wearable and implantable biomonitoring systems demand stretchable and bendable substrates that conform to the organ and skin shape. The user's comfort and the materials' transparency are also significant motivations for using flexible substrates.

A flexible biomedical implant requires sensors for measurement and integrated circuits consisting of active devices for data communication. Amorphous semiconductor materials are better suited for such circuits than crystalline semiconductors since the former can be deposited as thin film on bendable, flexible substrates. The thinness facilitates their use as large-area electronics and co-integration with other technologies [3], [4]. The large-area requirement led to the development of amorphous silicon (a-Si) transistors as control circuitry for large flat-panel displays [5]. However, compared to crystalline silicon (c-Si), their amorphous counterpart offered deficient carrier mobility. The requirement for higher mobility and large-area deposition capability led to the invention of amorphous Indium-Gallium Zinc-Oxide (a-IGZO) TFTs in 2003 [6].

A-IGZO is a new semiconductor material that has revolutionized the electronics industry. Due to its optical transparency and low-cost room temperature fabrication process, a-IGZO allows newer applications in the scientific community and the consumer industry. Some of the more prolific applications of a-IGZO semiconductors include thin film transistors (TFTs) in displays and touchscreens, sensors for various applications and memory devices based on flexible electronics [7]. Due to their higher carrier mobility than a-Si, they are now the more popular

material for TFT design. TFTs are low-priced, highly efficient, compact alternatives to expensive silicon devices.

The application of a-IGZO in wireless communication circuits is relatively limited compared to c-Si. Details on the state of the art are presented in section 1.3. If radio frequency circuits can be reliably implemented with TFTs, a lower-cost communication system can be developed with easy fabrication. Compared to the existing technologies like indium-phosphide (InP) heterojunction bipolar transistors (HBT), silicon-germanium (SiGe) HBTs complementary metal oxide silicon (CMOS) transistors, the technology is still in the rudimentary phase of development. The speed of a transistor is defined by its transit frequency (f_T). For high-frequency circuit design, the f_T of the transistors must be improved. It also affects the power gain of a transistor. Power gain is the capability of a transistor to convert DC power to radio frequency power. For a common-source transistor in a unilateral configuration, i.e., without any feedback from the output to input, power amplification at an applied frequency f_{op} is proportional to f_T/f_{op} [8]. Hence, for amplification, the f_T of the transistor must be above the targeted operating frequency. Beyond f_T, the non-linear behavior of transistors can be exploited to generate signals at the multiple of the applied input frequency. Hence, a simultaneous improvement of f_T and harmonic circuit techniques can lead to the realization of an a-IGZO-based communication system at $1\,\mathrm{GHz}$. Overcoming the gigahertz (GHz) barrier can benefit from compact antenna size and a higher data rate for communication. This perspective is illustrated in Fig. 1.1.

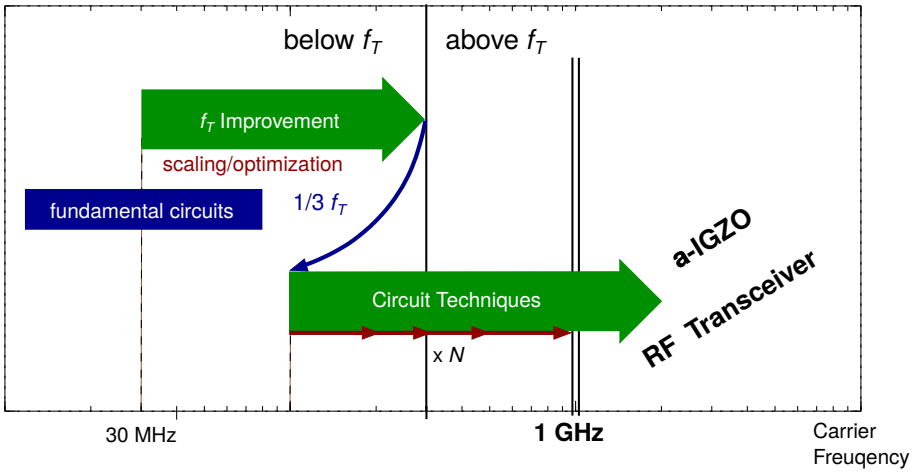


Figure 1.1: A perspective of communication system design with simultaneous technology improvement enhancing the speed of TFT and a compatible circuit technique to generate a modulated GHz signal. Image Courtesy: Project 10by10.com under the SPP 1796, funded by the German Research Foundation.

The main goal for the GHz radio frequency (RF) transceiver is to achieve a communication link at $1\,\mathrm{GHz}$ over a $1\,\mathrm{m}$ range. According to Shannon's theorem, the maximum data rate of a communication channel C is related to the bandwidth W and the signal-to-noise ratio (SNR) by the formula $C = Wlog_2(1 + S/N)$, where S and N are the signal and noise powers respectively [9]. The modulation scheme and the required bit error rate (BER) for detection at the baseband dictate the SNR. A low-order modulation scheme, such as on-off-keying (OOK) or Binary Phase

Shift Keying (BPSK), requires a low SNR.

The initial target of the flexible RF communication system is the wearable industry. For this application, the demand for the data throughput is less than $1\,\mathrm{Mbps}$ (megabit per second). Hence, a low-order modulation scheme that puts a lower demand on the transmitter power is required. Most wearable technology uses OOK modulation with a few hundred kbps data rate with OOK communication [10]–[12]. An OOK modulator is more straightforward to implement in the a-IGZO technology than BPSK. Hence, this thesis aims to design an OOK GHz frontend based on a-IGZO transistors.

In the presence of additive white Gaussian noise (AWGN), a non-return-to-zero OOK (NRZ-OOK) requires a $7\,\mathrm{dB}$ SNR for a BER of 0.001 [13]. A link budget analysis can help determine the output power required for a transmitter. The path loss can be obtained from the frequency and range by applying the Friis transmission equation. The required transmitter power can be calculated based on the path loss and the receiver's noise equivalent power NEP. Table 1.1 shows the transmitter power (Tx Power min.) specification for different NEP and data rates.

Table 1.1: Achievable range, data rates, required Tx power for OOK with a $BER = 10^{-3}$ (SNR =7 dB).

RF (MHz)	Range (m)	Pathloss (dB)	min. NEP (pW/√Hz)	Data Rate (kbit/s)	RF BW[3] (kHz)	Rx Power[1,2] min. (dBm)	Tx Power min. (dBm)
1000	1	-32.44	1000	256	512	-25.96	0.48
1000	1	-32.44	100	256	512	-35.96	-9.51
1000	1	-32.44	1000	1	2	-38.00	-11.56
500	1	-26.42	100	256	512	-35.96	-15.54
500	0.5	-20.40	100	256	512	-35.96	-21.56

[1]3-dB Tx/Rx antenna gain

[2]7dB SNR for BER=10^{-3} for BPSK (OOK) assumed

[3]Spectral efficiency 0.5 bits/Hz for OOK

The specifications in Table 1.1 set the high power requirement for a-IGZO TFT-based transmitters operating at GHz RF. The reception or detection of the transmitted signal can be done in two ways: incoherent and coherent or heterodyne. The baseband signal can be detected directly from the received modulated signal in incoherent detection. The advantage of this method is that it is simple and can demodulate an RF signal at a higher frequency than the transmit frequency of the TFT. The sensitivity of an incoherent detector is limited by its NEP.

In a heterodyne receiver, the down-conversion of the modulated RF signal is done using harmonic mixers. The mixer requires the same oscillation signal as the transmitter to demodulate the RF signal. The circuit requirements for heterodyne are complex to implement. The transmitted and received carrier frequency signal variation can affect the mixing. Hence, a heterodyne receiver needs an accurate local oscillator. However, they are advantageous

due to their higher sensitivity. As seen from the link budget calculation, a higher sensitivity is paramount for a $1\,\mathrm{m}$ communication link at $1\,\mathrm{GHz}$. Hence, this system should also be investigated with the a-IGZO-based technology.

The scope of this dissertation can be summarized as follows: to investigate the possibility of a GHz radio frequency on-off-keying (OOK) transceiver based on in-house fabricated a-IGZO thin film transistors for a communication link of a minimum range of $1\,\mathrm{m}$.

1.2 Introduction to TFT technologies

The history of TFT is almost half as old as IEEE itself. Since its conception in 1933, the research interest in this technology had disappeared and reemerged until the 70s. However, it was only within the confines of a handful of companies. However, since the 1980s, as personal and professional computers grew, the popularity of TFTs as a compact, low-power controller for active displays increased among researchers [14]. Initial materials of interest were group cadmium sulfide (CdS) and tellurium (Te). A group at the University of Dundee in 1975 demonstrated doping in amorphous Si semiconductors and, by 1983, applied the same for liquid crystal displays [15]. Following this, several prototypes were developed by different display panel manufacturers. As crystalline Si chips performed increasing functions as a microprocessor, the active display arrays based on TFTs also proliferated as input and output interfaces of the chips. As time passed, the researchers made the production process of the a-Si faster and cheaper, and the transparent glass substrates became larger and thinner. Thus, the TFT technology became synonymous with large-area electronics.

A-Si can be called the predecessor of IGZO in terms of its application. Both crystalline silicon (c-Si) and amorphous hydrogenated silicon (a-Si:H) consist of tetrahedral atomic structures, as shown in Fig. 1.2. In the case of c-Si, these tetrahedra are arranged such that the crystal lattice (a basic unit) forms a diamond-like structure. In the case of a-Si:H, although the atoms are arranged in a tetrahedral geometry, the bond length and angle between each pair of particles vary over a wide range. The structure leads to random ring sizes in a-Si. The 5–10% hydrogen atoms are connected to the empty dangling bonds at the edge of the thin silicon film [16].

In the c-Si lattice, as atoms arrange themselves in a uniform diamond ring structure, their sp^3 hybridized orbitals overlap. The orbitals split into different energy levels as multiple atoms form covalent bonds in the crystal. The closer energy level can form continuous bands, creating conduction and valence bands. A significant overlap between the relevant orbitals and a large magnitude of the overlap lowers the effective mass of the carrier, thereby increasing mobility. However, the orbitals are not continuous in a-Si:H due to structural disorders and defects. As a result, the electrons have to hop from orbital to orbital, resulting in deficient mobility[17].

1.2.1 Need for a-IGZO TFTs

Carrier mobility defines the energy efficiency and current driving capability of transistors. As demand for larger liquid crystal displays (LCD) driven by TFTs grew, the need for a cost-effective large-area amorphous semiconductor with higher mobility arose. This interest led researchers to investigate ionic metal oxide semiconductors that can provide higher mobility and drive large currents into each pixel on the screen. In the case of ionic semiconductors with a larger bandgap, such as indium oxide ($\mathrm{In_2O_3}$), the cation (In^{3+}) has a vacant s orbital ($1s^2 2s^2 2p^6 3s^2 3p^6 4s^2 3d^{10} 4p^6 5s^0 4d^{10} 5p^0$) that is spherical and spatially spread. So, the overlap of the two In^{3+} cations is insensitive to the metal-oxide bonding angle variation [18]. As a result, the amorphous thin films of $\mathrm{In_2O_3}$ show higher mobility than a-Si:H. However, pure $\mathrm{In_2O_3}$ easily forms oxygen vacancies in the crystal that give rise to large carrier concentrations, making it difficult to turn off the TFTs. $InGaZnO_4$ eliminates these vacancies by incorporating Ga ions that bond strongly with oxygen [19].

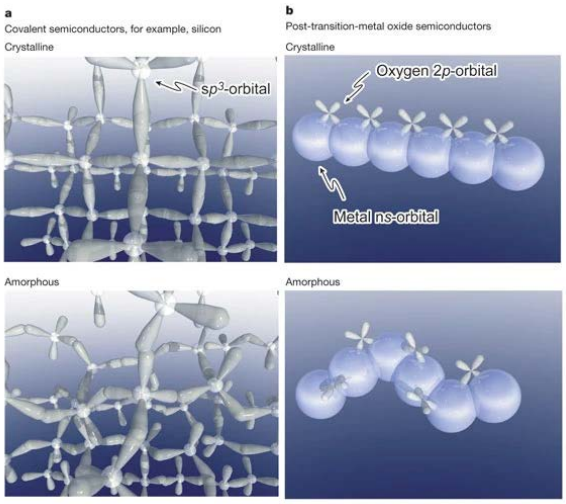


Figure 1.2: (a) Covalent semiconductors made of silicon and (b) metal oxide or ionic semiconductors [19]. Reprinted (including caption) with permission from [19], © 2004, Springer Nature.

Furthermore, optical transparency is paramount as the TFTs were meant for large-area display technologies. They should not block the light coming from the pixel that they drive. Owing to the large bandgap ($\approx 3.0\,\mathrm{eV}$) of the a-IGZO [19], the photons in the visible wavelength (frequency range 1.98–$3.26\,\mathrm{eV}$) do not have enough energy to be absorbed by the semiconductor. Hence, the visible light passes through the material with a transmittance of $> 80\%$ [19].

Amorphous IGZO was first applied as a novel semiconductor material by [19] in 2004. The study demonstrated room temperature fabrication of a-IGZO on polymer films and showed saturation mobilities of ≈ 6–$10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. A comparison of the properties of a-IGZO with c-Si and a-Si is presented in Table 1.2.

Table 1.2: Some semiconductor properties of silicon and a-IGZO.

Parameters	c-Si[20]	a-Si	a-IGZO
Bandgap(eV)	1.12	1.75[16]	3[19]
Lattice Constant (Å)	5.431	N/A.	N/A.
Breakdown field (10×10^6 V/cm)	0.3	-	-
Electron Mobility at 300K (cm^2/Vs)	1450	1[16]	10 [19]
Saturation velocity (10×10^6 cm/sec)	9	-	
Thermal conductivity (W/m.K)	1.3	-	1.4 [21]

1.3 A literature review of a-IGZO in RF applications

Although designed for display monitors, as we move towards a future with more connectivity, the idea of using transparent large-area electronics for communication circuits also got traction in the last ten years. Big corporations like Samsung, LG and Huawei have released foldable phones [22][23]. Large area-based passive RFID tags have been prevalent since the beginning of the century [24]. However, these are passive devices. Regarding active circuit components based on metal oxide TFTs, academia has achieved the following milestones.

1.3.1 Between 2005 and 2010

After Hosono discovered a-IGZO [17], Ofuji et al. presented a five-stage ring oscillator (RO) operating at $410\,\mathrm{kHz}$ and a supply voltage of $18\,\mathrm{V}$ [25]. With a propagation delay of $0.24\,\mu\mathrm{s}$ per stage, it was faster than the a-Si and organic TFT-based circuits. Zhao et al. showed a 15-stage ring oscillator with a $58\,\mathrm{ns}$ delay per stage [26]. In 2010, Suresh et al. overcame the MHz barrier by using Al_2O_3 as dielectric. They achieved a field effect mobility of $15\,\mathrm{cm^2V^{-1}\,s^{-1}}$ and demonstrated a five-stage RO with an oscillation frequency of 2.3 MHz. However, two years earlier, Sun et al. [27] achieved a similar feat with a pure ZnO-based counterpart. The same year, Kawamura et al. presented an a-IGZO-based rectifier that could rectify a 13.56 MHz wireless signal [28]. For that purpose, he used four TFTs with a semiconductor mobility of $10\,\mathrm{cm^2V^{-1}\,s^{-1}}$, two of which act as switches, while the other two act as diodes.

1.3.2 Between 2011 and 2015

In 2012, Chasin et al. presented an a-IGZO-based Schottky diode with a cutoff frequency of $1.8\,\mathrm{GHz}$ at $0\,\mathrm{V}$ forward bias [29]. They also measured a rectifier with 90% efficiency up to $100\,\mathrm{MHz}$. They modified the doping profile of the IGZO semiconductor by controlling the layer thickness and the nature of the top metal. By observing that molybdenum as a top metal induces a higher on-current than gold (Au), they concluded that Molybdenum contact induces higher doping than gold. The doping profile is independent of the work function of the metal. It depends on the thickness of the semiconductor. The same author also published an ultrahigh-frequency energy harvester based on a rectifier, a dipole antenna and a matching network in 2014 that could deliver around $1\,\mathrm{V}$ dc at a distance of $2\,\mathrm{m}$ for a transmitted power of

$33\,\mathrm{dBm}$ at $868\,\mathrm{MHz}$[30]. Shabanpour et al. presented a $762\,\mu\mathrm{W}$ cascode amplifier with $10.5\,\mathrm{dB}$ voltage gain and a 3-dB bandwidth of $2.62\,\mathrm{MHz}$ in 2013 [31]. The TFTs featured a chromium bottom gate and $10\,\mathrm{nm}$ titanium (Ti)+ $60\,\mathrm{nm}$ Au as source-drain contact. In 2015, Ishida et al. presented a fully integrated receiver on plastic comprising a four-stage cascode amplifier, a source follower and a common-source baseband amplifier for the first time. The receiver shows a conversion gain of $15\,\mathrm{dB}$ for a carrier frequency between $2\,\mathrm{MHz}$ - $20\,\mathrm{MHz}$. The baseband signal had a 3 dB-bandwidth of $400\,\mathrm{Hz}$ to $10\,\mathrm{kHz}$[32].

1.3.3 Between 2016 and 2023

In 2016, Zhang et al. demonstrated an a-IGZO-based Schottky diode with an intrinsic cutoff frequency of $20\,\mathrm{GHz}$. They further built a rectifier that showed a cutoff frequency of $4.2\,\mathrm{GHz}$ at a $15\,\mathrm{dBm}$ input signal [26].

In 2018, Li. et al. also showed the digital circuit performance of complementary inverters consisting of n-type a-IGZO TFT and a p-type tin-oxide (SnO) TFT. The inverter showed a gain of up to 112 at a supply of $10\,\mathrm{V}$. Moreover, they also presented rail-to-rail output for logic gates [33]. In the same year, Wang et al. showed the GHz frequency capability of a-IGZO TFTs with tantalum oxide dielectric. They achieved carrier mobility of $18.2\,\mathrm{cm^2V^{-1}\,s^{-1}}$ and transit and maximum oscillation frequencies of $1.24\,\mathrm{GHz}$ and $1.14\,\mathrm{GHz}$ respectively [34]. They used a high-resistive silicon substrate coated with $100\,\mathrm{nm}$ silicon dioxide. A titanium-palladium composite material was deposited with electron beam evaporation, whereas the dielectric and semiconductor were deposited through RF sputtering.

Rahaman et al. demonstrated an operational amplifier with a voltage gain of $23.5\,\mathrm{dB}$, a gain-bandwidth product of $7.5\,\mathrm{MHz}$ and a slew-rate (up/down) of $2.1\,\mathrm{V/\mu s}$ [35]. He used a combination of dual and single gate a-IGZO TFTs.

We evaluated an a-IGZO-based doubler at $1\,\mathrm{GHz}$ frequency. The TFTs had a transit frequency of $40\,\mathrm{MHz}$, but could show a responsivity of $2\,\mathrm{V/W}$ and noise equivalent power of $30\,\mathrm{nW}/\sqrt{\mathrm{Hz}}$ at $1\,\mathrm{GHz}$.

One breakthrough in signal generation with metal oxide came from Mehlman et al. in 2019, when they presented a cross-coupled LC-tank-based oscillator operating at $1.25\,\mathrm{GHz}$ with $2.8\,\mathrm{V}$ output voltage swing [36]. The inductances were implemented on a printed circuit board (PCB) with planar loops and wire bonded to the TFTs.

Another significant breakthrough was our in-house TFTs overcoming the GHz barrier with a transit frequency of $1.1\,\mathrm{GHz}$ and a maximum oscillation frequency of $3.5\,\mathrm{GHz}$ [37]. We achieved this advancement in speed by scaling and better gate electrode material selection.

In 2021, Wu et al. presented a GHz phased array by combining the oscillator presented in [36] with a $0.3\,\mathrm{m}$ aperture, thereby demonstrating beam steering with large-area-electronics [38].

In 2022, Park et al. reported a-IGZO TFTs with a transit frequency of $18.3\,\mathrm{GHz}$. They achieved this record f_T with extreme scaling of the channel length down to $12.3\,\mathrm{nm}$ as well as a novel dual-layer lift-off technique [39].

In 2023, we presented a multi-finger frequency doubler with a maximum conversion gain of $-32\,\mathrm{dB}$ for a $1\,\mathrm{GHz}$ radio frequency output signal. The TFTs showed a transit frequency of around $500\,\mathrm{MHz}$.

Thus, a significant advancement in addressing the GHz frequency range using a-IGZO TFTs has been achieved in recent years.

1.4 Design challenge and research methodology

A standardized process technology and device models help the designed circuits' reliability. The a-IGZO TFTs are not standardized and undergo repeated iterations. The technology is also sensitive to environmental conditions, material quality and impurity presence. Based on these factors, the device and designed circuit performance vary widely. Device fabrication, modeling and circuit designing must be addressed simultaneously to develop a GHz radio frequency (RF) frontend based on a-IGZO. A feasibility study must be performed to build cost-effective and reliable communication systems with a-IGZO. This study includes DC tests, S-parameter measurements, large-signal power output capability and breakdown characteristics. Moreover, the device yield has to be high enough. The effect of process variation and mismatch should also be accounted for in reliability analysis.

Hence, this work focuses on designing and characterizing the in-house a-IGZO TFTs and RF-relevant circuits in communication in the GHz frequency range. The TFTs have been fabricated in the cleanroom of the Bergische University of Wuppertal. The cleanroom is of standard Class 10, containing 10000 particles per $\geq 0.1\,\mathrm{m}$, while the photolithography section is of Class 1, containing 1000 particles per $\geq 0.1\,\mathrm{m}$ [40].

The dissertation depicts the modeling of the TFTs. A process development kit (PDK) is also created for simulation using Cadence IC. One detector and doubler was published in 2018, the first in the literature. A new, improved GHz doubler has been published in 2023.

Moreover, an on-off-keying (OOK) communication system is proposed and simulated data are shown. Due to poor yield during fabrication, we could not realize the complete communication system during the confinement of the supporting project. However, we could create multi-finger circuits like doubler and detector and present record results. The doubler achieves a conversion gain of $-32\,\mathrm{dB}$ for an output of $1\,\mathrm{GHz}$. A square-law detector has also been measured that shows a noise equivalent power of around $1.6\,\mathrm{nW}/\sqrt{\mathrm{Hz}}$.

1.5 Application and organization

This research area can potentially revolutionize the wireless communication field and open up a clutch of novel application areas for electronics. Some of the envisioned applications of TFT-based GHz communication systems are:

- Long Range or LoRa transceivers operating at near-GHz or low GHz frequency.
- Internet of Things or IoT, such as smart transmitters. RFID tags and sensors are already available.
- biomedical microcommunication for flexible transparent implantable sensors and drug delivery systems.
- Wi-Fi systems at a lower cost.
- solar-powered transceivers owing to the optical transparency of a-IGZO.

This chapter introduces the scope and challenges of this work and the state-of-the-art RF circuits based on a-IGZO or similar metal oxide TFTs.

Chapter 2 presents the state-of-the-art of the in-house transistors and the design challenges. Moreover, the relevant parameters of the transistors are also presented.

Chapter 3 shows the modeling of the TFTs. This model includes both the DC and the small signal high-frequency model. Moreover, the non-quasi-static effect is also explored.

Chapter 4 exemplifies frequency doubling with a-IGZO TFTs. The multi-finger doubler is analyzed with the derived model of TFTs.

Chapter 5 demonstrates GHz OOK detection using square law detectors. The responsivity and noise equivalent power improvement at GHz frequency are presented.

In chapter 6, we simulated and designed a GHz transceiver front-end with high-speed TFTs. The modeling and layout of the circuits have also been presented.

Chapter 7 presents the conclusion and outlook of this work.

Chapter 2

Transistor Fundamentals for Radio Frequency Circuit Design

2.1 Design requirements

For designing electronic components and ensuring the reliability and reproducibility of electronic circuits, the following components are required:

- Reliable active devices with high speed, amplification and stability
- Passive electronic elements with possibility of tunable bandwidth design
- Models for the active and passive elements
- Design and simulation capability using electronic design automation tools such as Cadence

The active devices are gate controlled metal-oxide field-effect-transistors (FETs). The goals of FETs in GHz circuits are switching, power amplification/conversion and frequency mixing.

These fundamental properties manifest themselves in a few figures of merits from the perspective of RF circuit design. They are described in section 2.2.

Passive elements in RF circuits consist of resistors, capacitors and inductors. The most challenging one in the GHz range is the inductor. In RF applications, an inductor is used primarily for impedance matching. A second application is using them as a high-frequency choke or source degeneration. Using an inductor over resistance in a common-source configuration can provide a voltage swing twice that of the supply voltage at the drain node [41]. A characterization of inductance designed on glass-substrate is described in C.1.

The in-house TFT fabrication started in the University of Wuppertal in 2015. Initially the TFTs had an f_T of $30\,\mathrm{MHz}$ for channel dimension of $500\,\mu\mathrm{m}/3.2\,\mu\mathrm{m}$ [42]. In 2020, we presented state-of-the-art TFTs that have overcome the GHz barrier in terms of f_T and f_{max} [37]. The

section 2.3 describes the fabrication steps and the fundamental ideas that helped improve these parameters.

However, a reliable design methodology encompassing high-frequency characterization and improving the known parameters was missing. Few articles in the literature describe the GHz modeling and designing procedure. The DC and RF modeling comprises a major part of this thesis and is described in the subsequent chapters.

2.2 Figure of merits for RF transistors

Before diving into the materials and the transistors, the FoMs of the TFTs must be introduced. To explore the FoMs, the transistor is considered as a two-port device. As such, we can assess the performance considering the scattering parameters of the device as the fundamental quantities. The four scattering or S-parameters are the input return loss S_{11} , the reverse insertion loss S_{12} , the forward insertion loss S_{21} and the output return loss S_{22}. Based on these S-parameters, the following FoMs become relevant for an RF transistor.

2.2.1 Stability

A two-port network is unstable when unwanted oscillations occur due to a negative real part in the input or output impedance [43]. There are two types of stability for a two port network:

- Conditional Stability: when $|\Gamma_{in}|< 1$ and $|\Gamma_{out}|< 1$ for certain range of source and load impedances
- Unconditional Stability: when $|\Gamma_{in}|< 1$ and $|\Gamma_{out}|< 1$ for all source and load impedances

The reflection coefficients for active devices such as transistors can be given by

$$|\Gamma_{in}| = |S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L}|< 1, \tag{2.1}$$

$$|\Gamma_{out}| = |S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{11}\Gamma_S}|< 1, \tag{2.2}$$

where Γ_S and Γ_L are the reflection coefficients of source and load resistances respectively.

For unilateral devices, $S_{12} = 0$. Hence from (2.1), the necessary and sufficient condition for unconditional stability is $|S_{11}|< 0$ and $|S_{22}|< 0$ at all frequencies. The simplification of these equations leads us to the figure of merit for stability, also called Rollet's stability factor K_f.

The unconditional stability criteria in this case is reduced to

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1, \tag{2.3}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|< 1, \tag{2.4}$$

for all frequencies. If $K < 1$, the device is called conditionally stable, i.e. oscillations may occur at some frequencies, where the transistor is not impedance matched.

2.2.2 Power gain

A transistor can naturally amplify current and voltages, providing power to the load. Since the source and load impedances are frequency functions, the power gain also depends on the frequency itself.

There are several definitions of power gains available. If the input and the load impedances are conjugate-matched, we can achieve maximum power gain from source to load. This power gain is the maximum available gain (G_{max}). It is the maximum gain a transistor can have without any external matching network. In case of unconditional stability i.e. $K > 1$, G_{max} is given by

$$G_{max} = |\frac{S_{21}}{S_{12}}|(K - \sqrt{K^2 - 1}). \tag{2.5}$$

It doesn't provide a meaningful result in case of conditional stability. In that case, the maximum stable gain G_{msg} is the FoM. G_{msg} equals the maximum available gain only when K=1, i.e.

$$G_{msg} = |\frac{S_{21}}{S_{12}}|. \tag{2.6}$$

In general, the actual power gain from source to load via the transistor is called the transducer power gain G_T, given by

$$G_T = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|1 - \Gamma_S\Gamma_{in}|^2|1 - S_{11}\Gamma_L|^2}. \tag{2.7}$$

In case both input and output match with zero reflection, i.e., $\Gamma_S = \Gamma_L = 0$, the transducer gain reduces to $G_T = |S_{21}|^2$.

The unilateral power gain is another frequently used FoMs for transistors. It is the power gain of the transistor, when there is no feedback from output to input, but the sources and loads are conjugate-matched. The nullification of feedback prevents oscillations. This neutralization is significant in a power amplifier, where the power at the output is high enough to influence the input via the feedback. In terms of S-parameters, the unilateral power gain is given by [43]

$$U = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|1 - S_{11}\Gamma_S|^2|1 - S_{11}\Gamma_L|^2}. \tag{2.8}$$

2.2.3 Transit frequency

The speed of transistors is primarily defined in terms of its transit frequency f_T. It is the frequency at which the short circuited current gain is unity. The dependence of transit frequency on the small signal and RF parameters can be explained by Fig. 2.1.

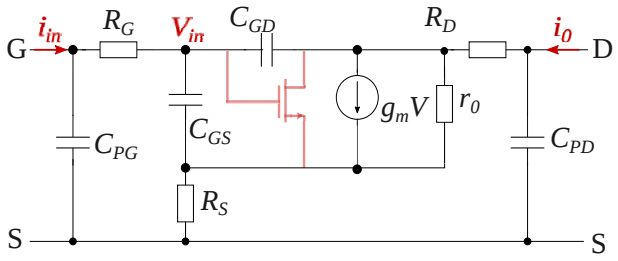


Figure 2.1: Field effect transistor with the small-signal model, ignoring the drain and source resistances.

If g_m is the transconductance of the FET and C_{GS} and C_{GD} are the gate-source and gate-drain capacitances, then the output current is given by

$$i_0 = g_m V_{in} = g_m \frac{i_{in}}{\omega(C_{GS} + C_{GD})}. \tag{2.9}$$

This leads to the current gain of

$$A_i = \frac{g_m}{\omega(C_{GS} + C_{GD})}. \tag{2.10}$$

As f_T corresponds to unity current gain, hence it is given by

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})}. \tag{2.11}$$

As we can see, f_T depends only on the transconductance and the gate-source and gate-drain capacitances. Hence, it depends mostly on the charge inducibility and the area of the gate terminal.

The channel current at any point y on the longitudinal direction, on the other hand, can be generalized by the formula $I_d(y) = Wv(y)|Q_n(y)|$, where $v(y)$ is the average carrier velocity and $Q_n(y)$ is the inversion carrier charge. So the continuous current through the channel is [44]

$$I_D = \frac{1}{L}\int_0^L Wv(y)|Q_n(y)| = \frac{W}{L}|Q_n(y)|vL = W(V_G - V_{th})C'_G v_s, \tag{2.12}$$

where, C'_G is the gate capacitance per unit area, V_G is the gate voltage, V_{th} is the threshold voltage, v is the drift velocity of carrier, $v = v_s$ i.e. saturated velocity for short channel devices. This gives the transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = WC'_G v_s. \tag{2.13}$$

The total gate capacitance can be given by the equation

$$C_{GS} + C_{GD} = WLC'_G + C_{G,par}, \tag{2.14}$$

where $C_{G,par}$ is the sum of the total gate parasitic capacitance. In case of an ideal transistor

without any parasitic capacitance i.e. applying $C_{G,par} = 0$ in eq. (2.11), we get

$$f_T = \frac{v_s}{2\pi L} = \frac{1}{2\pi\tau_t}. \tag{2.15}$$

where τ_t is the transit time across the channel length, i.e. f_T corresponds to the time carriers need to reach from source to drain for an ideal transistor with no gate parasitic capacitance. Thus f_T corresponds to the speed of a transistor.

To improve the f_T of the device, one must reduce the channel length L, as it would increase the g_m and reduce C_G. Moreover, the total gate parasitic capacitance $C_{G,par}$ should also be reduced.

2.2.4 Maximum oscillation frequency (f_{max})

This frequency concerns the unilateral power gain U of the device. The unilateral power gain is defined as the power gain of the forward path of the transistor while canceling the feedback path with a lossless reciprocal feedback network. [44] In terms of S-parameters, it is defined as

$$U = \frac{|S_{11}S_{22}S_{12}S_{21}|}{(1-|S_{11}|^2)(1-|S_{22}|^2)}. \tag{2.16}$$

In terms of device parameters, the power gain of a FET is given by

$$G_P = \frac{i_D^2 Z_L}{4i_{in}^2 R_G} = h_{21}^2 \frac{Z_L}{4R_G}, \tag{2.17}$$

where $h_{21} = A_i$ is the forward current gain and Z_L is the load impedance. If we consider a one pole approximation and frequency $f < f_T$, i.e., $h_{21}f = f_T$, we have

$$G_P = \frac{f_T^2 Z_L}{4f^2 R_G}. \tag{2.18}$$

The maximum available power gain is given by the condition $Z_L C_{GD} = 1/(2\pi f_T)$

$$G_{max} = \frac{f_T}{8\pi R_G C_{GD} f^2}. \tag{2.19}$$

This equation also represents the unilateral gain U for a common-source configuration as [44]. At f_{max}, the U of a transistor becomes unity. Hence

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_G C_{GD}}}. \tag{2.20}$$

This formula is valid for small channel resistances. However, if the channel resistance R_i is large and comparable to drain source resistance R_{DS}, then a more generalized formula for f_{MAX} can be given [37]

$$f_{max} = \frac{1}{2}\frac{f_T}{\sqrt{2\pi f_T C_{GD} R_G + g_{ds} R_G}}. \tag{2.21}$$

So to optimize f_{max}, the transit frequency f_T has to be increased while reducing the channel resistance. Moreover, the gate and source parasitic resistances R_G and R_S, as well as the gate-drain capacitance C_{GD}, must be reduced. Another important point is that C_{GD} decreases as drain voltage increases due to channel length modulation. Hence, the f_{max} also increases for higher drain voltages.

f_{max} limits the maximum operating frequency of a power amplifier. No circuit techniques can make a power amplifier operate beyond f_{max}. Moreover, no reciprocal network or matching can change the TFT f_{max} [45].

2.2.5 Noise figure

A transistor doesn't only amplify the applied signal but also the noise from the input terminal. It also generates noise and adds to the output. To describe the noise produced by the transistor, the FoM called noise figure (NF) is defined as

$$NF = 10 \log \frac{SNR_{in}}{SNR_{out}}, \tag{2.22}$$

where SNR_{in} and SNR_{out} are the signal to noise power ratios in linear scale at the input and the output terminals respectively. NF depends on matching at the input of the transistors, bias conditions and frequency. This noise-matching condition is different than power-matching conditions. Hence the design of low noise amplifiers is typically steered away from power gain and instead focused on amplifying the signal voltage without adding much noise.

For RF FETs, the higher the f_T and f_{max}, the lower the noise figure at high frequencies. Because a higher input gate resistance contributes to higher noise.

2.2.6 Output power and efficiency

These are the most important parameters for designing a power amplifier and a transmitter. They signify a transistor's maximum power handling capability for a given size and load. The power handling capability can be defined in terms of power density, i.e., maximum power over gate length for FETs or over emitter area for bipolar transistors [46].

Another FoM is power-added efficiency (PAE) for being operated as a power amplifier. A power amplifier is a power converter that consumes DC power to enhance the input RF power P_{in} and deliver it to a load P_{out}. The PAE is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}. \tag{2.23}$$

2.2.7 Failure parameters

As an RF transistor has to amplify or transfer power, it is under constant stress due to electrical and thermal effects. This stress, in turn, can lead to a lower operational lifetime of the transistor.

2.2.7.1 Mean time of failure

The reliability of a device is defined in terms of mean time to failure ($MTTF$) [46]. As supply voltage increases, high drain voltage gives rise to high temperature in the channel region and causes a defect in the oxide silicon interface due to hot carriers [46]. If the semiconductor is not highly thermally conductive, the heat generated due to current flow cannot dissipate quickly, leading to stress-induced effects. In the case of bipolar transistors, this leads to increased base currents, thereby leading to lower current gain. $MTTF$ is the time it takes for the current gain to reach 15% of its initial value. For FETs, $MTTF$ is the time for the transconductance to reach 15% of its initial value.

2.2.7.2 Breakdown voltage

The oxide layer between the gate and semiconductor sustain the applied electric field. When stressed by an applied voltage, the oxide loses its insulating properties. This generates traps inside the oxide layer, which increases the gate leakage current [47]. This leads to power dissipation through the layer path. This power dissipation could exceed a definite critical power density for a certain time. In that case, the resulting temperature melts the semiconductor and allows it to flow through oxide resulting in an ohmic-short circuit. It has been reported in [19] that the phase transition temperature of a-IGZO is around $500\,^{\circ}\mathrm{C}$ in air, while the melting point of Al_2O_3 is above $2000\,^{\circ}\mathrm{C}$ as reported in [48]. This is a hard breakdown. If the power dissipation is not above the critical power density, the leakage current through the oxide will increase. This is a soft breakdown. In this case, the post-breakdown $I - V$ curve follows a power law [47].

2.2.8 Mismatch and process variation

In FETs, the process variation is typically explained in terms of two basic transistor parameters: threshold voltage and mobility. The mismatch and variations in RF FoMs can also be expressed in terms of these two fundamental transistors parameters.

There are two possible categories of variations: systemic and random. The systemic variations are dependent on designer and their skill. Hence proper care must be taken in design and layout for symmetry. Random variations are dependent on material quality, manufacturing equipment and environmental factors such as humidity, temperature and manufacturing. Moreover, the process parameters such as fabrication time, alignment accuracy are also important, especially for a large-area technology like metal-oxide.

2.2.8.1 Causes of process variation in a-IGZO TFTs

The a-IGZO is susceptible to high process variation and mismatch. Since a-IGZO is a composite material, the deposition condition can significantly affect the electrical properties. An amorphous material lack of crystalline structure, which can result in a high density of defects and disordered regions. The process steps used for fabrication may themselves undergo variability depending

on the quality of material, operation skill or the accuracy of the equipment. This is explained in detail in chapter 7.

During characterization itself, many TFTs show different values of drain current for two different sets of measurements. Application of bias stress can cause trapping of charge carriers in the oxide, which results in drifts in TFT properties [49], [50].

2.2.9 Device yield

The a-IGZO TFT fabrication is a complex process with multiple steps involved. The thin film technology is well established for displays. However, a standardized short channel devices for RF are not well established. The fabrication steps are also primarily affected by environmental conditions such as temperature, humidity, and light [51]. The presence of many impurities also causes significant deviation in the intrinsic TFT properties. Variations in material properties can also change the threshold voltage and mobility of the carriers.

The above factors prevent the a-IGZO TFTs from consistently and reliably performing. This work compensates for the low yield by developing a reliable model for the TFT.

2.3 Designing TFTs for RF application

One of the significant challenges in designing a high-power device is the trade-off with speed. As the output current increases, the donor concentration in the channel has to be increased and the channel length has to be decreased. The lower channel length leads to a lower breakdown voltage. Hence, the allowable voltage swing between the drain and the source terminals of the transistor decreases although the speed of the device, i.e. f_T, increases. Although this is an advantage for a digital circuit, it could create a significant drawback for RF circuits where high power is needed to compensate for the loss and to transmit power over a distance. One of the significant ways to mitigate this power-speed trade-off is to reduce the device parasitics as low as possible. As we see in the following subsections, this has been done by existing circuit techniques and new process steps in fabrication.

2.3.1 In-House fabrication of a-IGZO TFTs

The following steps are used to create the in-house a-IGZO TFTs:

2.3.1.1 Deposition of gate electrode

Gate electrodes made of chromium were deposited by sputtering and patterned by photolithography on a glass substrate [42]. The gate electrode can be of different materials. Usually chromium is used since it provides sharper edges and shows good adhesion. In earlier experiments, a composite Ti/Au/Ti material was used to enhance the power amplification capability of the TFTs[37]. The latter has 25 times lower sheet resistance [37], thereby reducing the reflected power at the input.

2.3.1.2 Formation of gate dielectrics

Next the gate dielectric is deposited on top of the electrode using atomic layer deposition (ALD). The gate dielectric is chosen to be aluminum oxide Al_2O_3. It offers a relative permittivity in the range between 8.5 and 9.5. A high permittivity ensures higher control of the channel charges through the gate bias. Moreover, high permittivity also ensures a lower leakage current through the gate.

The thickness of the dielectric can be controlled during the ALD process. In [42], a $220\,\mathrm{nm}$ thick dielectric was chosen, while in [37], we presented a thickness of $50\,\mathrm{nm}$. Lower thickness also gives us the benefit of higher charge control. This results in higher speed of the transistor.

However, it has been shown in [52] that the Al_2O_3 dielectric breakdown voltage is inversely proportional to the square root of thickness. Thus a trade-off always exists between the speed and the breakdown voltage of the device. This problem is worse if the semiconductor mobility is low, which the other factor determining the speed of the transistor.

2.3.1.3 Deposition of channel material

Next, a $15\,\mathrm{nm}$-thick amorphous IGZO layer was deposited by RF magnetron sputtering at room temperature through a metal shadow mask. Sputtering was done in Ar atmosphere with 0.8% O_2 content and chamber working pressure of $6.6\,\mathrm{mtorr}$ at a plasma power of $125\,\mathrm{W}$ using a ceramic $InGaZnO_4$ (In:Ga:Zn = 1:1:1 atomic %) target [37].

2.3.1.4 Post-Deposition heat treatment

A post-deposition heat treatment or annealing is then carried out at a temperature between 250°C and 350°C. Annealing can reduce the density of defects in the semiconductor and improve electrical conductivity and stability of the material.

2.3.1.5 Self-alignment channel patterning and source drain deposition

Self-alignment means the use of the deposited gate electrode for patterning the channel and the source-drain electrodes. This method reduces the overlap capacitance between the gate and the source-drain, thereby enhancing the speed of the transistor.

The TFT channel and the source and drain electrodes are patterned by self-aligned photolithography using a positive photoresist (AZ ECI 3007, MicroChemicals). The photoresist was exposed with an Osram HBO 350 W/S mercury short-arc lamp (power density: $51\,\mathrm{mWcm^{-2}}$; exposure time: 5.5 s). A PET foil acts as a partial UV filter to reduce the overall exposure intensity and to ensure compatibility of the self-alignment process even with flexible substrates. S/D electrodes consist of 90 nm thick sputtered molybdenum [42].

In [37], a second self-aligned lithography is performed to pattern the semiconductor more precisely under the source-drain electrodes. This resulted a high speed device, overcoming the GHz f_T barrier.

2.3.1.6 Encapsulation

The TFTs were encapsulated by 90 nm ALD grown Al_2O_3 using ozone as oxidant [37].

Encapsulation hinders the interaction of the channel with the water in the atmosphere. The water molecules from the environment can cause a negative threshold voltage shift in a-IGZO semiconductors [51].

Fig. 2.2a shows the in-house bottom-gate a-IGZO TFT schematic cross section with layer stack and corresponding film thicknesses. Fig. 2.2b illustrates the self-aligned photolithography steps for patterning the S/D electrodes. A scanning electron microscope (SEM) cross-section image of the TFT is shown in Fig. 2.2c. A magnified view of the source-gate overlap length is shown in the inset. Note, in order to get a decent SEM image and to avoid charging effects, the Al_2O_3 back-channel encapsulation was omitted and the cleaved facet was coated with thin layer of gold. Fig. 2.2(d) shows the capacitance-voltage characteristics of a $250\,\mu m/0.8\,\mu m$ IGZO TFT measured at frequency of $1\,MHz$. This image is taken from [37].

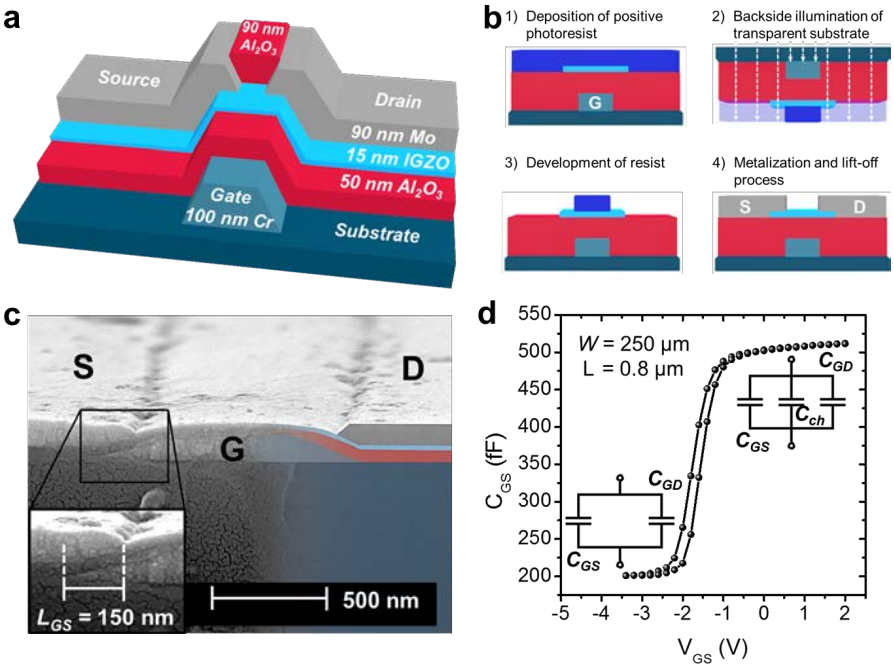
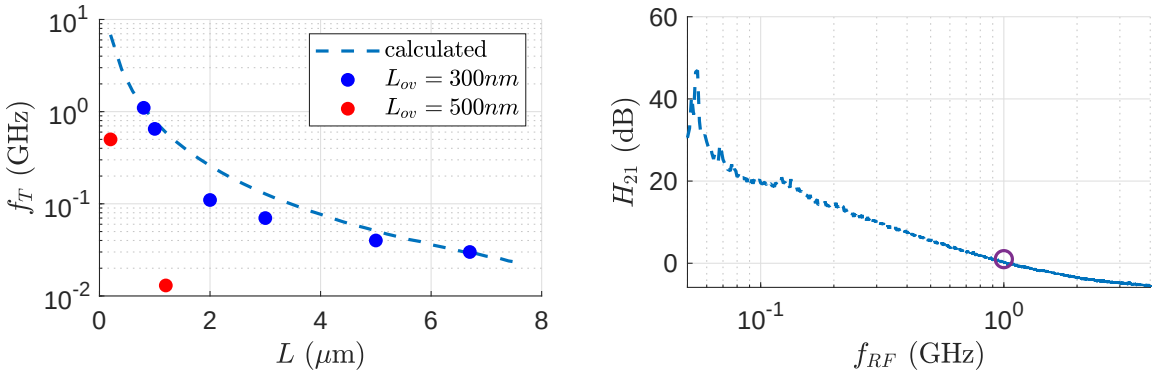


Figure 2.2: (a) Fabricated TFT layer stack with thickness, (b) fabrication steps in the self-alignment process, (c) SEM image of a fabricated TFT and (d) capacitance-voltage measurement of a $250\,\mu m/0.8\,\mu m$ a-IGZO TFT. Reprinted, with permission, from [37] © 2020, IEEE.

2.3.2 Improvement in f_T

The first TFT designs were large. The channel dimensions were in the range of $500\,\mu m/5\,\mu m$ and $500\,\mu m/3\,\mu m$. Moreover, there were thin ground lines surrounding the TFTs for wafer probing. The structures have also been used in doubler design, as mentioned in chapter 4. An improvement was necessary for the TFT structures for RF application. Hence we removed the thin lines surrounding the TFTs and the electrodes were made short with fewer squares. The resultant decrease in R_D and R_S can cause a slight improvement in the f_T [44].

The major improvement in the transistor speed came from the reduction in transistor length L and the gate-source and gate drain overlap length L_{ov}. The reduced channel length reduced the intrinsic oxide capacitance, while at the same time increasing g_m. As a result, an improvement in f_T can been achieved, as shown in Fig. 2.3a. This improvement is more significant for TFTs with reduced overlap length L_{ov} as shown in the figure. The reduced overlap length doesn't impact the intrinsic g_m, but reduces the gate overlap capacitances. From 2017 to 2020, a 25 times improvement in the f_T has been achieved by the fabrication team. The highest reported f_T of 1.1 GHz for Cr-gate TFT was presented in [37], as shown in Fig. 2.3b.



(a) **(b)**

Figure 2.3: Evolution of (a) f_T variation over channel length L and (b) best-reported f_T of ≈ 1 GHz for a Cr-gate TFT. Reprinted, with permission, from [37], © 2020, IEEE.

2.3.3 Improvement in f_{max}

The improvement in f_T can cause a major increase in the TFT's f_{max}, according to eq. (2.20). However, more than this value is needed to generate power at GHz range. One must increase f_{max} up-to around 500 MHz as an input to a frequency up-converter circuit. For a transistor, we can achieve higher f_{max} by reducing the gate electrode resistance R_G of the TFT. The gate resistance of an electrode over a channel width W, length $L$and a overlap length L_{ov} is given by,

$$R_G = R_{sh}\frac{\frac{W}{3} + x_{tr}}{L + 2L_{ov}}, \tag{2.24}$$

where R_{sh} is the sheet resistance of the electrode material and x_{tr} is the additional distance to the channel from the measurement point [37].

The reduction in R_G can be made by:

- the reduction in the gate number of squares W/L,
- the reduction in the sheet resistance R_{sh} of the electrode material.

Fig. 2.4a shows the impact of gate width on f_{max}[37]. As channel width or electrode width decreases, so does the number of squares in the gate electrode. Hence f_{max} improves. However, this reduces the intrinsic gain of the transistor as both the transconductance and output conductance decrease. Hence power gain of the TFT would also reduce.

The second method is even more effective in reducing f_{max} without affecting the gain of the TFT. The first batches of TFTs were composed of chromium electrodes. A chromium sheet resistance of around $10\,\Omega/\square$ for a $100\,\mathrm{nm}$ thick gate electrode was reported in [37]. The titanium-gold-Titanium (Ti/Au/Ti) composite electrode has a 25-fold lower sheet resistance for the same thickness of the gate electrode [37]. It has also been reported in [53] that the resistivity in sputtered chromium films can increase due to the reduction of mean free path caused by the surface roughness of the oxide layer.

Applying Ti/Au/Ti, a three times improvement in f_{max} was achieved. Fig. 2.4b shows the difference in f_{max}. This record results were published in [37]. Mehlman et. al mentioned a similar improvement in [36]. They achieved an f_T of around $867\,\mathrm{MHz}$ and f_{max} of around $2\,\mathrm{GHz}$ using an Al/Cr/Al composite electrode.

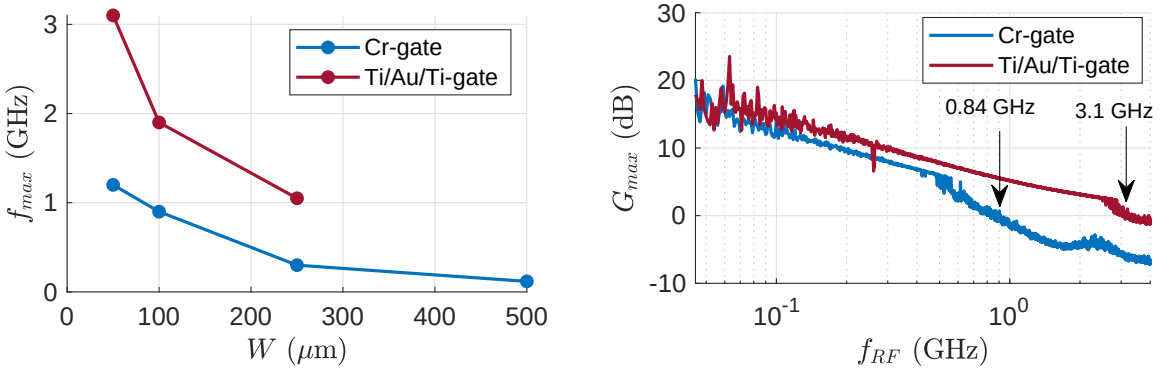


Figure 2.4: Evolution of (a) f_{max} over channel width W for $L = 0.8\,\mu\mathrm{m}$ and (b) best-reported f_{max} for a $50\,\mu\mathrm{m}/0.8\,\mu\mathrm{m}$ for a Cr-gate and Ti/Au/Ti-gate TFT. Reprinted, with permission, from [37], © 2020, IEEE.

2.3.4 Maximum available gain and stability

The maximum available gain is identical at below $600\,\mathrm{MHz}$ for different channel widths of the Ti/Au/Ti gate electrode as shown in Fig. 2.5a. However, the knee point frequency of the $50\,\mu\mathrm{m}/0.8\,\mu\mathrm{m}$ TFT almost coincide with its f_{max}. The same measurement setup has been used for the $100\,\mu\mathrm{m}$ wide and the $50\,\mu\mathrm{m}$ wide TFTs.

The stability factor K_f in Fig. 2.5b is negative at lower frequency (a few tens of MHz), owing to high reflection coefficient of field effect transistors at low frequency. However, as frequency increases S_{11} reduces and stability enhances. At the knee frequency of G_{max}, the K_f equals 1. This is the case for all the TFTs of different widths. However, the K_f of $50\,\mu m/0.8\,\mu m$ TFT doesn't stay stable even beyond this frequency. This indicate a presence of standing wave which causes $K_f \leq 1$.

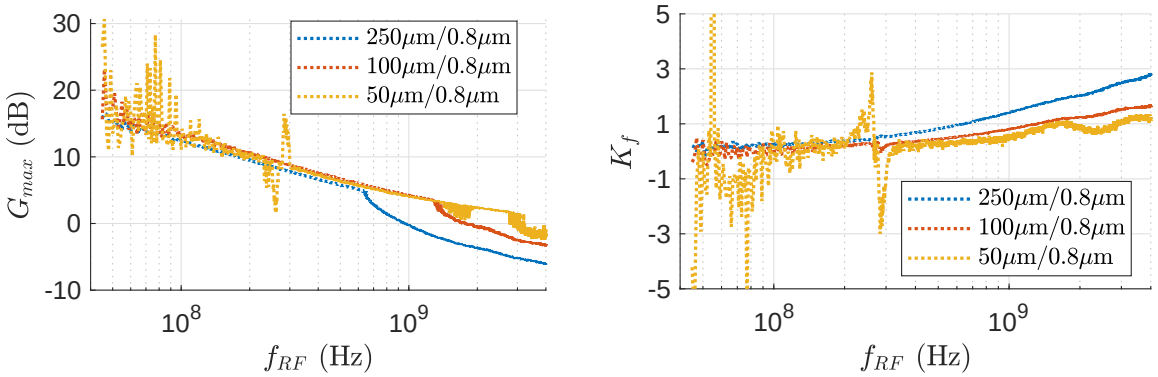


Figure 2.5: (a) G_{max} and (b) K_f over frequency for Ti/Au/Ti gate TFTs of different channel width.

Although with proper impedance matching, the K_f can be increased beyond 1, the fluctuation in K_f make the $50\,\mu m/0.8\,\mu m$ TFTs inherently unstable. To avoid unwanted oscillations, the $100\,\mu m/0.8\,\mu m$ TFTs with Ti/Au/Ti gate electrodes are the better suited for RF design.

2.3.5 Device breakdown

The TFT breakdown depends on the power dissipation in the channel, which in turn depends on the drain source voltage and current.

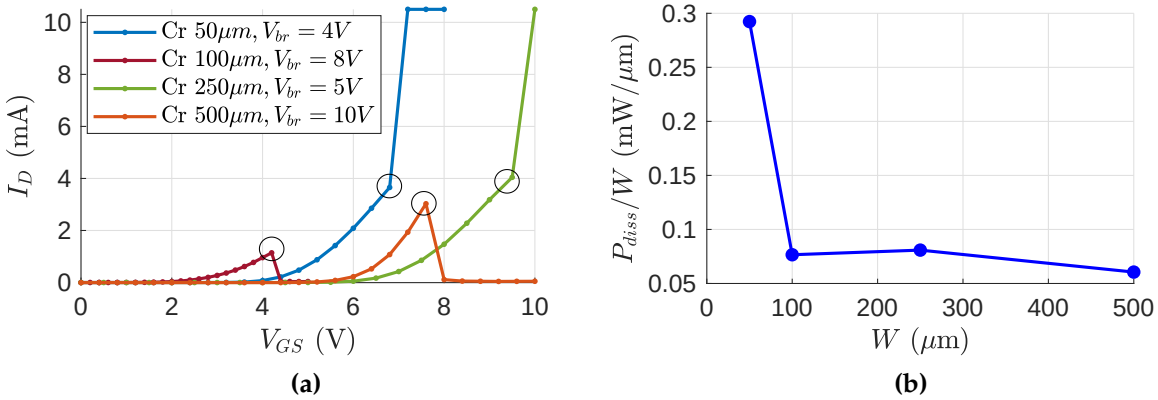


Figure 2.6: (a) Breakdown drain-source voltage V_{br} and current I_{br} measured for Cr-gate TFTs of channel length $0.8\,\mu m$, (b) a rough estimate of the breakdown power over width calculated from V_{br} and I_{br}.

During DC measurements, breakdown phenomenon could be observed in the $0.8\,\mu m$ channel length TFTs, as shown in Fig. 2.6a. The breakdown occurs at different drain-source breakdown

voltage V_{br} and drain current I_{br}. In some the $50\,\mu\mathrm{m}$ and $250\,\mu\mathrm{m}$ TFTs, the current increases after breakdown, indicating a short between the drain and source. The other two TFTs show breakdown, where the drain current stops flowing. Our assumption is that this is due to oxide breakdown, thereby creating a leakage current to the gate. These are only assumptions. To provide a definite answer about the breakdown mechanisms, more data points are required. This could not be done, due to the lack of available devices.

Based on the limited breakdown data, a rough estimate of the power dissipation $P_{diss} = I_{br}V_{br}$ per unit channel width W for breakdown is performed and shown in Fig. 2.6b. It is observed that, for the 100–$500\,\mu\mathrm{m}$ TFTs, breakdown happens at P_{diss}/W in the range of 60–$80\,\mathrm{mW\mu m^{-1}}$.It has been shown in [54] for a-Si:H TFTs that the breakdown voltage is independent of the channel width. However, the $50\,\mu\mathrm{m}$ TFT breaks down at a higher $P_{diss}/W = 292\,\mathrm{mW\mu m^{-1}}$. This contradictory result could be an outlier. More investigation is required for the proper characterization of the breakdown behavior of the in-house TFTs.

A photo of the top view of a TFT after the breakdown is shown in Fig. 2.7. As shown here, a part of the channel along the width shows the visible breakdown effect. This is a hard breakdown

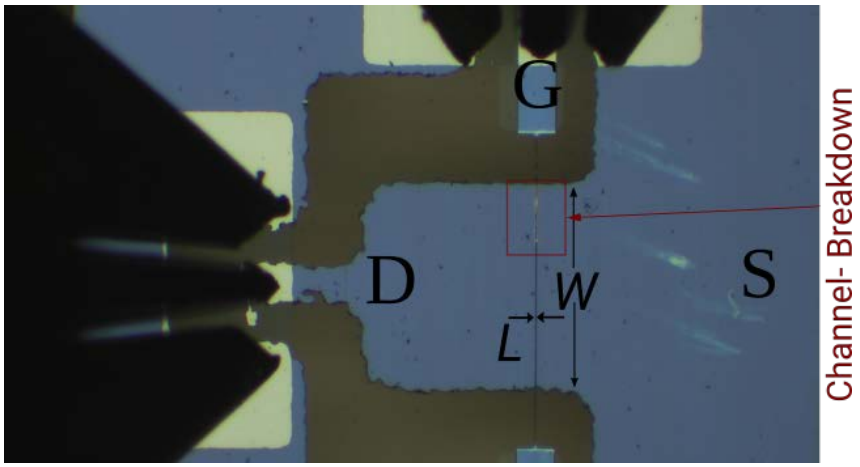


Figure 2.7: Photo of a TFT ($250\,\mu\mathrm{m}/0.8\,\mu\mathrm{m}$) top view after the breakdown.

as defined in section 2.2. The breakdown effect is irreversible and appears to result in a short between the drain and the source metal. More investigation in this field is needed to find the critical power density in a-IGZO.

2.4 Conclusion

We described the critical figure of merits for RF transistors in this chapter. For RF transistors, the fundamental bottlenecks are the transit frequency f_T and unity power gain frequency f_{max}. We showed how the in-house a-IGZO TFTs had made record results of $f_T = 1\,\mathrm{GHz}$ for Cr-gate TFTs and $f_{max} = 3.2\,\mathrm{GHz}$ for Ti/Au/Ti TFTs.

We have shown that the record $50\,\mu\mathrm{m}/800\,\mathrm{nm}$ TFTs, although fast, suffer from inherent instability. The next smallest TFTs of dimension $100\,\mu\mathrm{m}/800\,\mathrm{nm}$ offer more stability and hence can be adopted for RF circuit design.

However, other FoMs, like the mean time of failure and breakdown voltage, are also crucial for circuit reliability. For calculation of mean time of failure, an extensive statistical study of failure rate per hour for a large sample size is necessary. Hence, this FoM is beyond the scope of this time-limited thesis.

The breakdown voltage defines the power handling capability of transistors. Due to a lack of standardized process technology and environment, we cannot determine the accurate inherent power dissipation capability. However, the breakdown criteria showed a minimum power dissipation capability of at least $60\,\mathrm{mW}/\mu\mathrm{m}$ or $17.8\,\mathrm{dBm}/\mu\mathrm{m}$.

Due to the results mentioned above, the $100\,\mu\mathrm{m}/800\,\mathrm{nm}$ TFTs are chosen for the circuits designed and presented in the next chapter.

Chapter 3

Parameter Extraction and Modeling

As established in the last chapter, large-area electronics have much scope for improvement for GHz circuit design. Many design challenges appear in the endeavour to push the f_T and f_{max} barriers. The scaling of channel dimension can improve the speed but at the cost of output power capability. This trade-off is the equivalent of the gain-bandwidth product of a low-pass filter. To generate power in the GHz frequency range, one must simultaneously reduce the resistance of the electrodes, keeping the materials the same, and optimize the channel size for optimum g_m and C_{ox}.

The extrinsic parameters, such as gate resistance and the overlap capacitance and intrinsic parameters, like transconductance and output impedance, attribute the device speed and power output capability. Hence, the correct extraction of the transistor parameters is necessary for device modeling and simulation of power output, frequency mixing and impedance matching.

3.1 Requirement of DC and small-signal model

An a-IGZO TFT is a voltage-controlled device where the gate-source voltage induces a channel of charge carriers, and drain-source voltage is used to conduct these induced carriers.

Many RF circuits explore the inherent non-linearity of the transistors for harmonics generation. In most FETs, the current is a product of the powers of the gate-source and the gate-drain voltages V_{gs} and V_{ds}, respectively. This relationship is explored to design mixers and frequency multipliers in FET-based RF circuits. Therefore, it is crucial to know the relationship between the current and voltages in the TFT.

Many RF circuits also utilize the linear approximation of the transistors, which are inherently non-linear devices. The transistors usually are linearized with the small-signal approximation. In this case, the channel conductance, resistances, and capacitances are considered constant over a slight change in bias. A linear transistor provides the lowest distortion and does not create

parasitic signals. Calculating the linear parameters also depends on the bias and the current-bias relationships.

A square-law model is typically used to describe the current-voltage relationship. However, for a-IGZO TFTs, the square relationship is not always true. This fact is more pronounced as the channel dimension reduces. Hence, a correct relationship between the current and voltages must be derived. The DC/non-linear model and the extraction procedure are presented in section 3.2.

Many of the intrinsic properties of the channel change over frequency. For example, the intrinsic gain of a field-effect transistor reduces over frequency. Hence, the behavior of these small-signal parameters over frequency is also necessary for RF circuits.

The extraction and incorporation of the RF power into a transistor depend on the extrinsic elements of the transistors. RF circuit designers implement impedance matching to transfer the maximum power between different components. If the device parasitics are unknown, it is impossible to implement correct impedance matching. Hence, the knowledge of the extrinsic and intrinsic parameters is essential for RF circuit design. The extraction and modeling procedures for the intrinsic and extrinsic elements are described in section 3.3.

3.2 DC modeling of the transistor

For the DC modeling of a crystalline transistor, a basic SPICE level 3 model is usually enough. It is an empirical model, which gives the current equation as

$$\begin{aligned} Ids &= 0,\ V_G < V_{th} \\ &= \mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} (V_{GS} - V_{th} - \frac{1+fb}{2} V_{DS}) V_{DS},\ V_G > V_{th}, \end{aligned} \tag{3.1}$$

which is a simple square law equation. The level 3 model also assumes that the transistor goes into saturation region at higher V_{DS} and acts as a current source. The parameter fb accounts for the narrow width and short channel effect. Here μ_{eff} is the effective mobility of the carriers is expressed as [55]

$$\mu_{eff} = \frac{\mu_0}{[1+\theta(V_{GS}-V_{th})]\left[1+\frac{\mu_s V_{DS}}{v_{sat} L}\right]}, \tag{3.2}$$

where θ is a fitting parameter, V_D/L is the average longitudinal electric field, v_{sat} is the saturation velocity, and μ_s is a fitting parameter. The model assumes that the transistor turns on entirely as soon as the gate voltage exceeds the threshold voltage, i.e., $V_{th} = V_{ON}$. Moreover, the effective mobility is inverse relationship to the transverse field, described by the overdrive voltage $V_{GS} - V_{th}$ [44]. For a linear time-domain simulation of c-Si TFTs, these conditions are sufficient, and the model can be applied. For harmonic balance simulation, the discontinuities in the model functions and derivative can lead to a convergence problem [56].

For power amplifier design, the accuracy of $I-V$ characteristics is of utmost importance. SPICE level 3, following the square law assumes that the current reaches saturation at certain bias

conditions. However, for our a-IGZO TFTs, the current never reaches saturation, even at higher V_{DS}. The transition between triode and saturation is not as sharp as for c-Si FETs. As such, the level 3 model designed for a switching FET ($V_{th} \approx V_{ON}$) is less accurate. During a power amplifier simulation, this could lead to overestimating the output power.

From the device perspective, the bandgap in an a-IGZO TFT has a continuous distribution of trap states, resulting in the following effects [57] .

- At V_{th}, carriers are induced but still trapped in the aforementioned states, causing $V_{th} \neq V_{ON}$, unlike in c-Si FETs.
- The effective mobility is not always equal to the band mobility as the density of free carriers in the channel varies with biasing.
- The gate capacitance changes continuously over the bias as more and more carriers are released from the trapped state.

A continuous charge sheet-based model derived particularly for amorphous semiconductor devices is better suited to address these issues [58]. Cadence already supports a TFT model created by the Rensselaer Polytechnic Institute for amorphous (RPI-a) silicon TFT devices.

3.2.1 Current equation in RPI-a TFT model

The final current equation in the RPI-a model above threshold is given by

$$I_D = \frac{W}{L} C_g \mu_{FE} (V_{GS} - V_{th}) \frac{V_{ds}(1 + \lambda V_{ds})}{[1 + \frac{V_{ds}}{1+\alpha_{sat}^{M}(V_{gs}-V_{th})^{M}}]^{1/M}}, \tag{3.3}$$

where μ_{FE} is field effect mobility and depends on the band mobility μ_0 and the gate overdrive voltage with the relation

$$\mu_{FE} = \mu_0 \left(\frac{V_{GS} - V_{th}}{V_{AA}} \right)^{\gamma}. \tag{3.4}$$

where V_{AA} is the characteristic voltage of field effect mobility and γ is the power law mobility parameter [57]. The parameter α_{sat} in (3.3) represents the variation of depletion charge across the channel [57]. The saturation voltage in an amorphous TFT is given by

$$V_{DS,sat} = \alpha_{sat}(V_{GS} - V_{th}). \tag{3.5}$$

The parameter M defines the sharpness of the knee region in $I_D - V_{DS}$ characteristic. λ is the linearized channel length modulation parameter.

For a thin semiconductor layer, high I_D causes Joule heating, which lowers the V_{th} and enhances the mobility μ_{FE} [59]. An intermediate self-heating parameter r that deembeds the heating effect from the measured I_D was presented in [60] as

$$I_{D0} = \frac{I_D}{1 + r I_D V_{DS}}. \tag{3.6}$$

Considering the effect of channel length modulation factor λ to be nonlinear, the I_{D0} is given as [60]

$$I_{D0} = \frac{\frac{W}{L'} C_g \mu_{FE} \left(V_{GS} - V_{th}\right) V_{DS}}{\left[1 + R_{SD} \frac{W}{L'} C_g \mu_{FE} \left(V_{GS} - V_{th}\right)\right] \left[1 + \alpha_{sat}^{M} (V_{gs} - V_{th})^{M}]^{1/M}\right]}, \tag{3.7}$$

where the effective channel length L' is

$$L' = \begin{cases} L, & \text{triode region} \\ L - \lambda L(V_{DS} - (V_{GS} - V_{th})), & \text{saturation.} \end{cases} \tag{3.8}$$

3.2.2 Extraction procedure

The step-by-step procedure for the triode and saturation region parameter extraction of a-Si:H TFT has already been provided in [60]. Their model describes the non-saturating drain current accurately with the help of channel length modulation for short-channel TFTs. Another feature of the method was considering the self-heating effect that led to mobility enhancement at higher gate voltages.

Applying the method from [60], the level 61 parameters for a-IGZO TFT are extracted. During DC measurements, the TFT carries current instantaneously. However, the TFTs are proposed for RF circuits, where an RF signal would be superimposed over constant DC bias. Hence, it is necessary to model the self-heating effect for the TFTs.

A slight modification to the procedure is incorporated because the mobility enhancement in the saturation region due to the fudge factor is not considered. Our results show that the simulated $I_D - V_{DS}$ characteristics fit better when ignored. Three out of twelve single-finger TFTs from the same sample were functional, i.e., showing transistor $I_D - V_{DS}$ characteristics. The transistor with the median γ is chosen as the nominal transistor, and its extracted DC parameters with values precise to three decimal points are presented in Table 3.1. Further analysis and representation are done with the nominal TFT parameters.

The mean values of the three TFTs and the standard deviation are also presented. However, due to the low sample size of only three transistors, the data is not used for modeling. It is observable that the average power law mobility parameter γ is also around 1, which shows an approximately linear dependence of effective mobility of the TFTs on the gate overdrive voltage $V_{GS} - V_{th}$.

Table 3.1: Extracted RPI-a parameters values (precise to three decimal points) for a chosen single-finger TFT, mean values of 3 TFTs and the standard deviation. Reprinted, with permission, from [61], open access under creative common license CCBY-NC-ND.

Parameter	Unit	Description	Chosen TFT	Mean	Standard Deviation
W	µm	Channel width	100	100	0
L	µm	Channel length	0.8	0.8	0
α_{sat}	-	Saturation modulation parameter	0.906	1.007	0.090
ϵ_i	-	Relative permittivity of the insulator	8.5	8.5	0
γ	-	Power law mobility parameter	1.014	1.115	0.187
λ	1/V	Output conductance parameter	0.101	0.0601	0.040
m	-	Knee shape parameter	1.370	1.306	0.093
μ_0	m^2/Vs	Conduction band mobility	0.001	0.001	0
R_d	m	Drain contact resistance	160.077	161.771	16.902
R_s	m	Source contact resistance	160.077	161.771	16.902
T_{nom}	°C	Nominal temperature	24	24	0
t_{ox}	m	Oxide (Al_2O_3) thickness	5e-8	5e-8	0
V_{AA}	V	Characteristic voltages for field effect mobility	1.902	1.820	0.079
V_{th}	V	Zero bias threshold voltage	-0.948	-1.145	0.217

3.2.3 Result of DC modeling

The DC model of the latest generation of TFTs is implemented using the parameters listed in Table 3.1. The model is implemented in Verilog-A. Only the triode and saturation region of the TFTs are included in this model. All of our RF circuits operate at these two regions of operations, and hence, the subthreshold region is ignored.

The simulated versus measured output characteristics are shown in Fig. 3.1a.

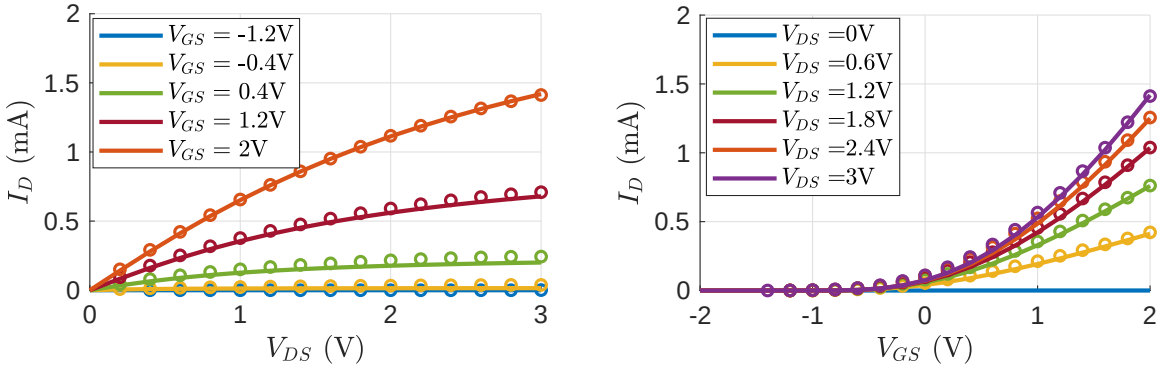


Figure 3.1: A TFT's simulated versus measured (a) output and (b) transconductance characteristics (solid lines - simulation and circular markers - measurement). Reprinted, with permission, from [61], open access under creative CCBY-NC-ND.

The root mean square error (RMSE) between the measured and simulated output characteristics for different V_{GS} is shown in Table 3.2. Dividing the RMSE by the difference between the

maximum and minimum I_D, the normalized root mean square error (NRMSE) for the output characteristics is obtained. NRMSE is high when V_{GS} is low and decreases gradually as V_{GS} increases.

Table 3.2: Normalized root mean square error in the DC output characteristics simulation. Reprinted, with permission, from [61], open access under creative common license CCBY-NC-ND.

V_{GS} (V)	-1.2	-0.4	0.4	1.2	2
RMSE	0.003	0.056	0.118	0.096	0.015
$I_{D,max} - I_{D,min}$ (mA)	0.002	0.039	0.244	0.710	1.41
NRMSE	0.125	1.438	0.484	0.136	0.011

The root mean square error (RMSE) between the measured and simulated transfer characteristics for different V_{DS} is shown in Table 3.3. Dividing the RMSE by the difference between the maximum and minimum I_D, the normalized root mean square error (NRMSE) for the output characteristics is obtained. NRMSE is less than 10% for $V_{DS} \geq 1.2\,\mathrm{V}$.

Table 3.3: Normalized root mean square error in the DC transfer characteristics simulation.

V_{DS} (V)	0	0.6	1.2	1.8	2.4	3
RMSE	0.005	0.046	0.058	0.075	0.092	0.083
$I_{D,max} - I_{D,min}$ (mA)	0	0.423	0.73	1.039	1.257	1.413
NRMSE	N/A	0.108	0.075	0.072	0.072	0.059

The model parameter extraction is a complicated process, and the modeling algorithm adopted incorporates least-square curve fitting to extract many of the parameters [60]. The accuracy of least square curve fitting depends highly on the number of data points and initial estimate input. Hence, achieving a higher accuracy of the model could be time-consuming. More investigation is required to reduce the measurement errors. The model must be applied against an ensemble of nominally identical devices in one batch and between different batches to analyze the process variation, especially the threshold voltage and the mobility variation.

3.3 RF parameters extraction techniques

The parasitic elements affect the performance of the TFT, particularly at high frequency. In order to extract the parasitic elements, one must apply deembedding algorithms. For RF transistors, the deembedding can be done in one of two ways - using calibration standards or applying the null-bias method.

3.3.1 Calibration standard based deembedding

This technique moves the calibration plane from the ground signal ground (GSG) probe tips to the intrinsic device under test. The method requires known calibration standards without changing the extrinsic interconnect geometry.

Based on the geometry of the structure and the frequency of operation, there can be different deembedding procedures - namely open short (OS), short-open-load (SOL), and short-open-load-thru (SOLT). There are also other transmission line-based methods, namely thru-reflect-load (TRL) and load-reflect-match (LRM). However, the required line standards are too long (a few meters) for the MHz to GHz frequency region to be implemented on a few centimeter-long glass substrate.

In the initial phase of this work, the eight-term error model [62] based deembedding procedure extracted from the SOL standards was adopted. The following results were presented as a poster presentation in the special session of FFlexCom in EuMW 2018.

The eight-term deembedding algorithm uses three measured standards at each port. It models the DUT and the ports as shown in Fig. 3.2. As seen here, the input port and the output ports

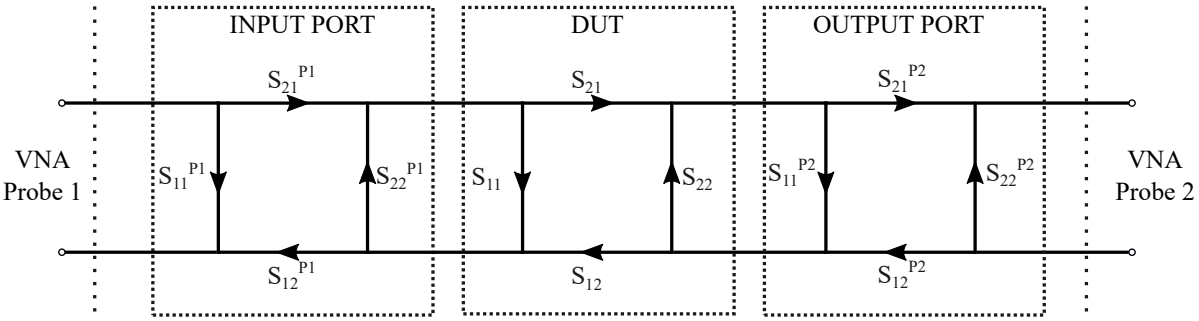


Figure 3.2: Eight-term error model for extrinsic interconnects.

constitute the error network. They transform the actual scattering parameters of the DUT (S^A_{xy}) with the measured one (S^A_{xy}), as shown in the following equation,

$$\begin{aligned} S^{P1}_{11} + S^M_{11} S^A_{11} S^{P1}_{11} - S^A_{11}\Delta(S^{P1}) = S^A_{11} \\ S^{P2}_{11} + S^M_{22} S^A_{22} S^{P1}_{22} - S^A_{22}\Delta(S^{P1}) = S^A_{22}, \end{aligned} \tag{3.9}$$

where $\Delta(S^P)$ represents the determinant of the port S parameters, i.e. $\Delta(S^P) = S^P_{11}S^P_{22} - S^P_{12}S^P_{21}$.

If we have the measured S-parameters of three different but known standards, such as short, open and load, then considering the reciprocity of the passive networks ($S^{P1}_{11} = S^{P2}_{11}$), three sets of equations for three unknowns at each of the input and output ports are obtained. This results in unique solutions to S^{P1} and S^{P2}. One can extract the extrinsic parasitic elements by converting the S-parameters to Y and Z-parameters.

Moreover, one can also estimate the intrinsic channel S-parameters from this method. For that, the S^{P1} and S^{P2}, as well as the measured S-parameter S^M_{DUT} are converted to their corresponding T-matrices. The actual T-parameters of the DUT T^A_{DUT} can be derived from the T^M_{DUT} using the equation

$$T^M_{DUT} = T^{P1} T^A_{DUT} T^{P2}, \tag{3.10}$$

in which case, T^A_{DUT} can be converted back to obtain the intrinsic S-parameters.

3.3.1.1 Application of Calibration Standard based Deembedding

The first batch of the TFTs was deembedded using this procedure. The device layout is shown in Fig. 3.3a. This TFT does not have the optimum layout for the RF application. Owing to large parasitic components and channel dimensions $\frac{500\,\mu\mathrm{m}}{3\,\mu\mathrm{m}}$, the devices exhibited large parasitic capacitances, thereby low f_T.

The measurement setup for S-parameters is shown in Fig. 3.3b. An Agilent E8363A vector network analyzer (VNA) measures the two-port S-parameters of the fabricated standards and the TFT. Before the measurement, the reference planes on both ports of the VNA were moved to the ground-signal-ground (GSG) probe tips with the help of a Picoprobe CS-5 100 calibration substrate. The data is averaged in the VNA with a factor of 20 samples in order to reduce the effect of noise on the measurements. A source meter unit (SMU) and power supply provide DC voltages to the drain and gates, respectively.

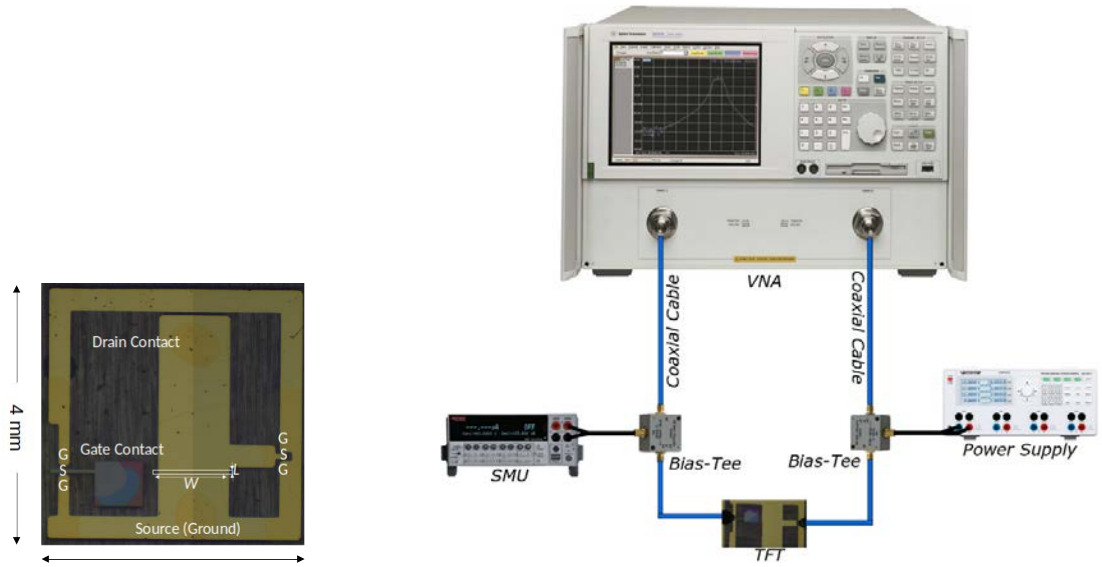


Figure 3.3: (a) Photo of the top-view of the TFT and (b) measurement setup for the S-parameter measurement.

The calibration standards are fabricated with geometry identical to the TFT devices but without the IGZO layer. The dielectric on top of the gate electrodes was omitted for the short standard in the channel region. Source and drain electrodes were then patterned using standard photolithography to obtain shorts between each source, drain, and gate. Open and load standards were fabricated using the same self-aligned photolithography process. For the open standard, the channel region of the gate electrode was separated from its probe contact area by wet etching. Additional metal structures of Cr (load) were patterned on the electrodes to create the load standard. Fig. 3.4 shows a schematic overview of each standard.

The setup in Fig. 3.3b is then used to measure the short, open and load standards and the TFT. Fig. 3.5a and 3.5b show the measured S_{11} and S_{22} of these three standards, respectively.

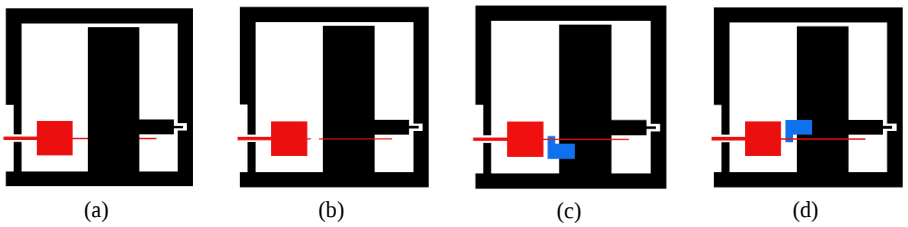


Figure 3.4: Schematic cross-section of the (a) short, (b) open, (c) source-drain load and (d) gate-source load.

The input port is highly reflective for the short standards due to the very narrow and long metallization of the gate contact, which creates a high resistance. Due to the wide area of the drain metal, the output port is less resistive and behaves like a transmission line.

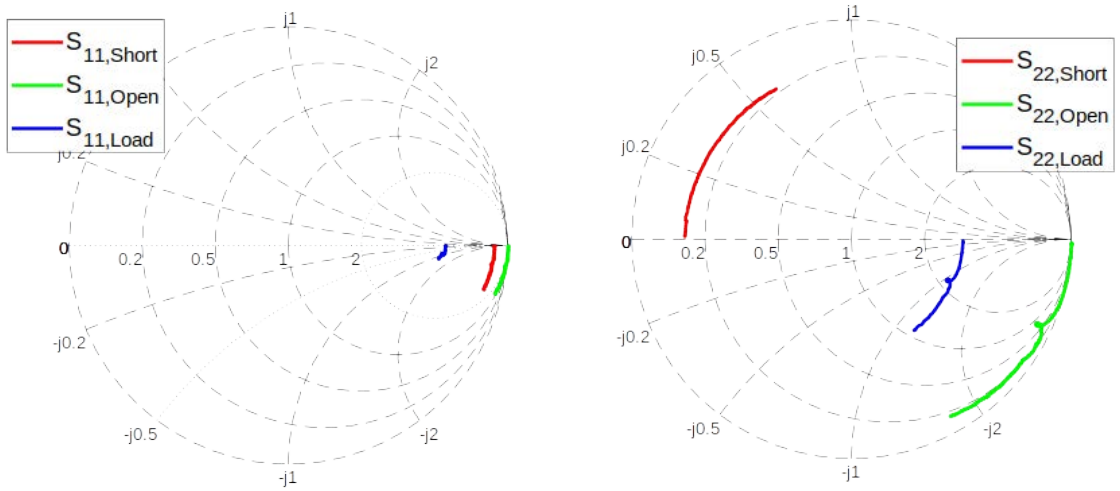


Figure 3.5: (a) S_{11} and (b) S_{22} of the in-house fabricated standards (2018).

A MATLAB code, based on the equations (3.9), is then used to deembed the input and the output ports from the TFT and measure the f_T of the channel. As described in section 3.3.1, the ideal impedances of the standards must be known to determine the error boxes of the ports. In large-area electronics, we cannot achieve the accurate placement of the standards with respect to one another. Furthermore, the gate metallization creates a distributive source-gate resistance for the short and load standards, making it difficult to measure their exact values. Therefore, we extracted the values for the ideal short and load resistances from the measured standard S-parameters at 45 MHz (the lower limit of the network analyzer). For the short standard, the ideal source-gate resistance is around $1.595\,\mathrm{k\Omega}$, while the same is $302\,\Omega$ for the load standard according to hand calculation, as seen in Fig. 3.6. The ideal source-drain resistances are $1.44\,\mathrm{m\Omega}$ and $121.8\,\Omega$ for the short and load standards, respectively. As a result, the algorithm skips the extrinsic resistances and deembeds only the extrinsic capacitances at the input port.

Fig. 3.6 shows the embedded and deembedded H_{21}. The extracted f_T value is identical to that obtained from the low-frequency H_{21} measurement.

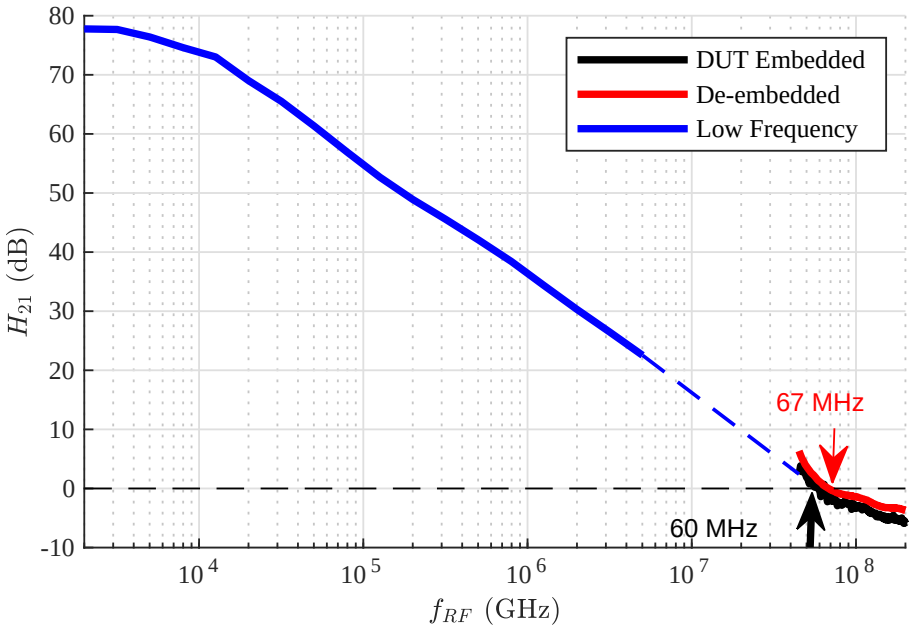


Figure 3.6: Deembedded H_{21} from the calibration standard-based method.

3.3.1.2 Limitations of Calibration Standard based Deembedding

The problem with the above procedure is the assumption of ideal broadband load calibration standards. If they are not accurate, the deembedding can also be not accurate. During the fabrication of the standards, an ideal broadband load material was unavailable in the process technology. However, it is now possible to use a metal alloy to produce the ideal load, and the resistance can also be controlled with proper dimensioning and electromagnetic field simulations. Nonetheless, a problem exists regarding the accurate placement of the load standards. Unlike the short and open structures, the load lines cannot simply be placed above the channel area. The additional contact is from the gate, and the drain electrodes would also be embedded into the final result.

Another critical issue with this procedure is the additional lead time. The fabrication and measurement time of such standards can delay the overall deembedding process each time a device structure changes.

Therefore, it is essential to incorporate a fast method that can give us the extrinsic and intrinsic parameters directly from the TFT itself without using any additional standards.

3.4 Deembedding without standards

A field effect transistor is assumed to consist of intrinsic and extrinsic lumped elements that follow simple Kirchhoff current and voltage laws. The impedance and admittance parameters can be formulated using these lumped elements based on nodal and mesh analyses. The interrelations between scattering, admittance and impedance parameters can then be exploited for step-by-step extraction of the parasitics. This method was used by Dambrine et al. for the

extraction of small MOS signal parameters for MOS transistors [63]. For polysilicon TFTs, Chen et al. used the same process in [64]. For a-IGZO TFTs, attention to high-frequency modeling and extraction has been lacking until recently.

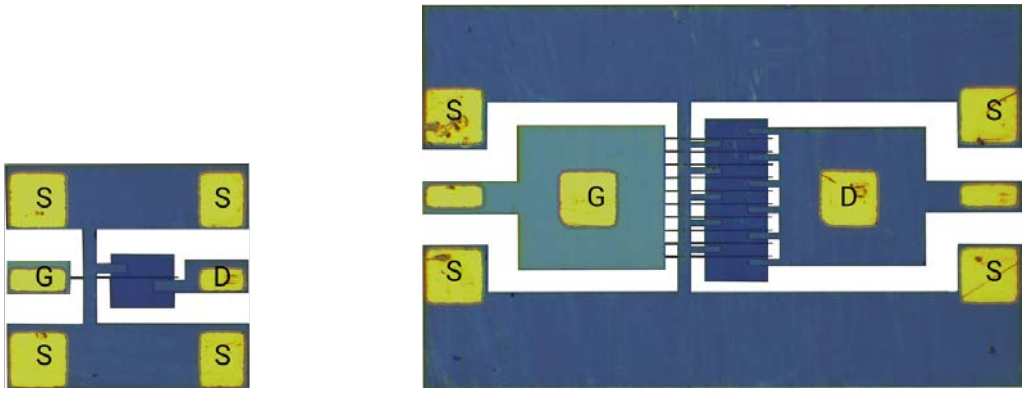
In the following sections, we present the step-by-step deembedding of the extrinsic and intrinsic components of our in-house a-IGZO TFTs.

3.4.1 Geometry of a TFT

The geometry of the TFTs can affect its performance in an RF circuit. Since we want to design a multi-finger architecture for higher output capability, the chosen geometry must generate the lowest possible parasitics.

A one-finger TFT is fabricated, as shown in Fig. 3.7a. Compared to the TFT presented in Fig. 2.7, the modeling of the new geometry is complicated in the GHz range since the gate is divided into two resistive regions and an overlap capacitance. However, this model corresponds to the best multi-finger architecture possible with two layers. A ten-finger TFT is fabricated, as shown in Fig. 3.7b. Here, the drain and source are arranged in an interdigitated configuration. Each of the gate-source and drain-source terminals are configured in a ground-signal-ground (GSG) configuration for wafer probing. The thin strip of source terminals connecting the two sides does overlap with the gate electrodes. However, in the case of high-frequency operation, an increase in the gate-drain capacitance is more detrimental to the unilateral gain of the TFT [45]. Since this geometry does not add gate-drain capacitance, it is the best architecture for high-frequency circuit design with only two metal layers.

We have observed that the one-lump model of the gate is valid only up to a few hundred MHz. Moreover, a higher sheet resistance of the gate electrode exacerbates the dispersion of capacitances during the extraction procedure. One must adopt a "two-lumped gate" model for the new TFT geometry. To confirm the scalability of the model, a multi-finger TFT is also fabricated, as shown in Fig. 3.7b.



(a) **(b)**

Figure 3.7: Photo of the top view of (a) a single and (b) a ten-finger TFT. Reprinted, with permission, from [61], open access under creative license CCBY-NC-ND.

3.4.2 Two-Lumped gate model

The two-lumped gate model is shown in Fig. 3.8. In that case, the gate resistance is divided into two parts: R_{G1} before the gate-source overlap region and $R_{G2} = r_G R_{G1}$ after the gate-source overlap region, where r_G is the ratio between the gate resistances. As mentioned earlier, the boundary conditions for the high-frequency gate current are not distinct. Hence, we must adopt a semi-analytic approach for the parameter extraction of the same. C_{PG} and C_{PD} are the pad capacitances at the gate and source terminals, respectively. R_{DS} is the combined drain-source metalization resistance. C_{OV} is the gate-source and gate-drain overlap capacitance, which is assumed to be identical to the TFT. C_{gs} and C_{gd} represent the gate-source and gate-drain capacitances of the intrinsic TFT.

Beyond a certain frequency limit of the input signal, the charge carriers cannot respond to the input instantaneously. This phenomenon is also called the non-quasi-static (NQS) effect. The simplest way to approximate the NQS effect in TFT is to consider distributed resistances r_{gs} and r_{gd} between the gate and source and gate and drain capacitances, respectively [65]. Another impact of this NQS phenomenon is the reduction of transconductance and output conductance at high frequencies. Hence, these frequency-dependent conductances are modeled as $g_{m,nqs}$ and $g_{ds,nqs}$, respectively [66].

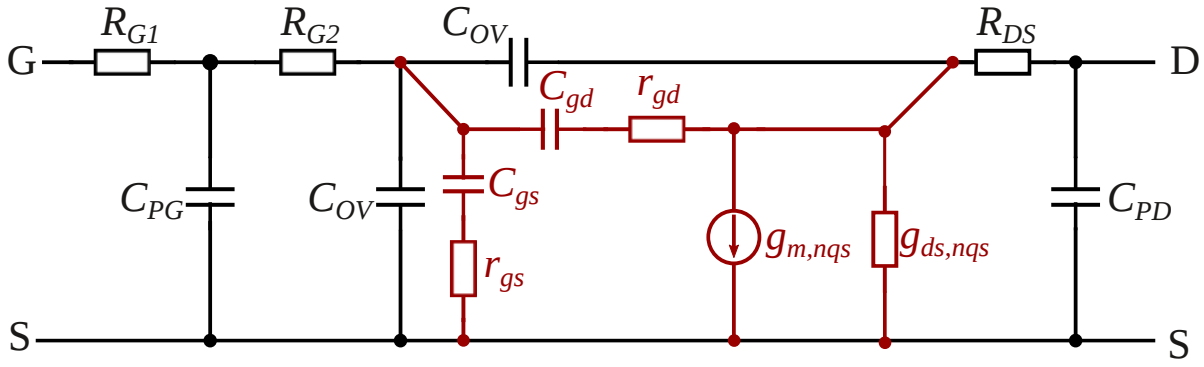


Figure 3.8: Two-lumped gate embedded model. Reprinted, with permission, from [61], open access under creative common license CCBY-NC-ND.

3.5 Extrinsic model and parameter extraction

For extraction of the parameters, as usual, we need to separate the extrinsic from the intrinsic parasitic. The extrinsic model at $V_{DS} = 0\,\mathrm{V}$ and $V_{GS} = -2\,\mathrm{V}$ is shown in Fig. 3.9. The drain-source resistance R_{DS} accounts for the sum of contact resistance between the drain/source and the channel. For the GHz frequency range, the positions of the R_{DS} and the drain pad capacitance C_{PD} against each other do not matter.

C_{PG}, $C_{OV} + C_{OX}/2$ and C_{PD} extracted from the measured zero biased Y-parameters, without applying resistance deembedding first, show large frequency dispersion. The dispersive

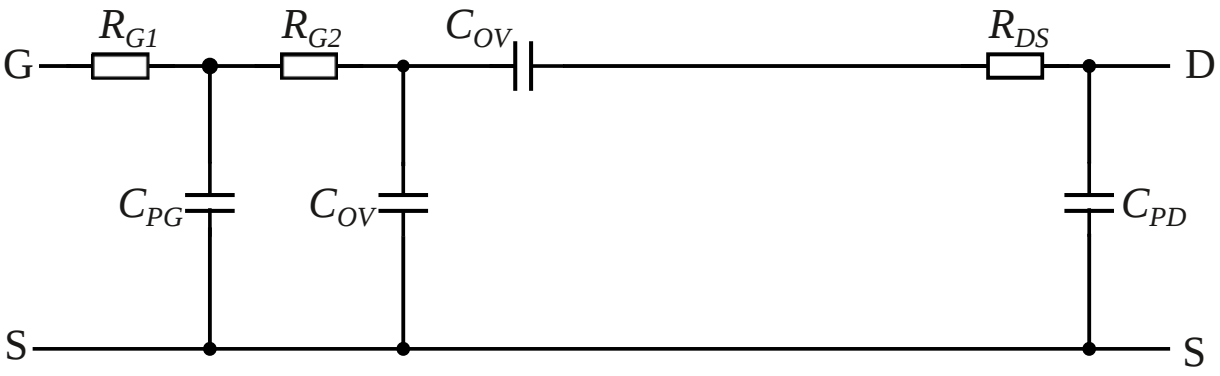


Figure 3.9: Two-lumped gate extrinsic model.

behavior also depends on the gate electrode sheet resistance. The extracted parasitic capacitances are shown in Fig. 3.10 for the measured chromium gate TFT.

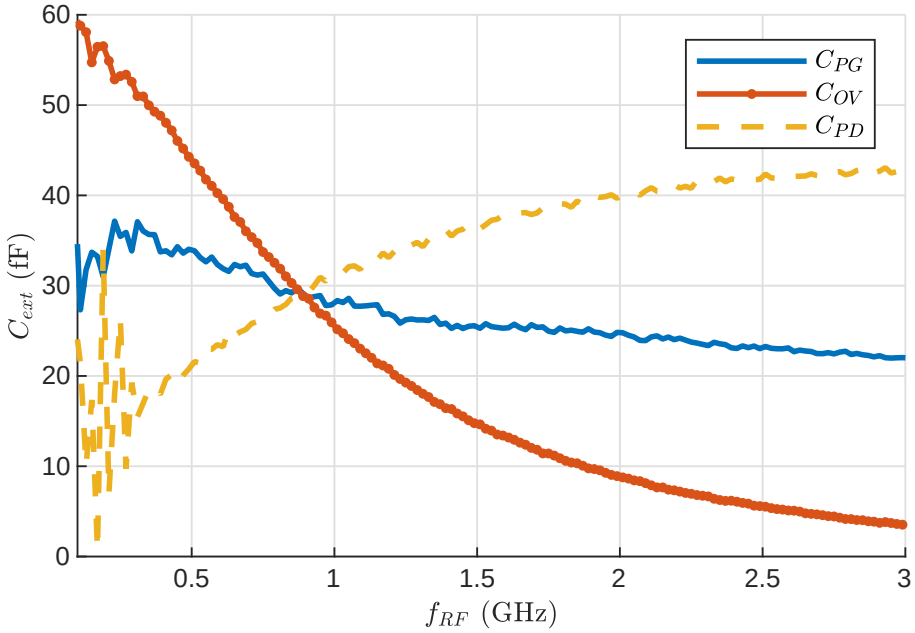


Figure 3.10: Extracted extrinsic capacitance without resistance deembedding showing dispersion.

The data is noisy at frequencies below $400\,\mathrm{MHz}$ due to the very high impedance of the FET gate and the network analyzer not being able to discern the high resistance values correctly. Therefore, to eliminate the dispersive behavior and the low-frequency noise, it is crucial to deembed the resistive parasitic in proper sequence. The issue is that the values of R_{G1} and R_{G2} are not easily deductible even with a simple RC ladder model, as the gate electrode will behave differently on either side of C_{PG}. As such, the initial boundary conditions are yet to be discovered. So, we apply fitting in order to calculate the value of R_{G1}.

3.5.0.1 Extraction of gate ratio and deembedding of R_{G1}

An initial calculation of the ratio r_G of R_{G2} and R_{G1} is done first. The resistance beyond the pad capacitance C_{PG} will follow the RC ladder rule, i.e., the total resistance will be divided by 3. So

r_G can be calculated as

$$r_G = \frac{\#squares\,beyond\,C_{PG}}{3\#squares\,before\,C_{PG}} = \frac{110/0.8 + 20/1.1}{3(2 + 20/1.1)} = 2.57. \tag{3.11}$$

However, the immediate region beyond C_{PG} and the electrode region beyond the channel are not covered on both sides (see Fig. 3.7a). Hence, the factor 3 in the denominator of (3.11) is not exact. The derivation for this factor is done in section A.1.3 in Appendix A. So fitting is needed to determine the ratio r_G.

With the help of fitting with Spectre and MATLAB, the r_G value is determined to be 2.8 (initially 3). The value of R_{G1} is calculated to be $385\,\Omega$ (ideally $403\,\Omega$).

3.5.0.2 Extraction of gate pad capacitance

The elimination of the gate resistance R_{G1} would result in the flattening of the overlap capacitance C_{OV}, while the gate pad capacitance increases with frequency, as seen in Fig. 3.11. This increase is due to parasitic resistances at the higher frequency. Hence, the capacitance values must be taken from the stable low-frequency data points.

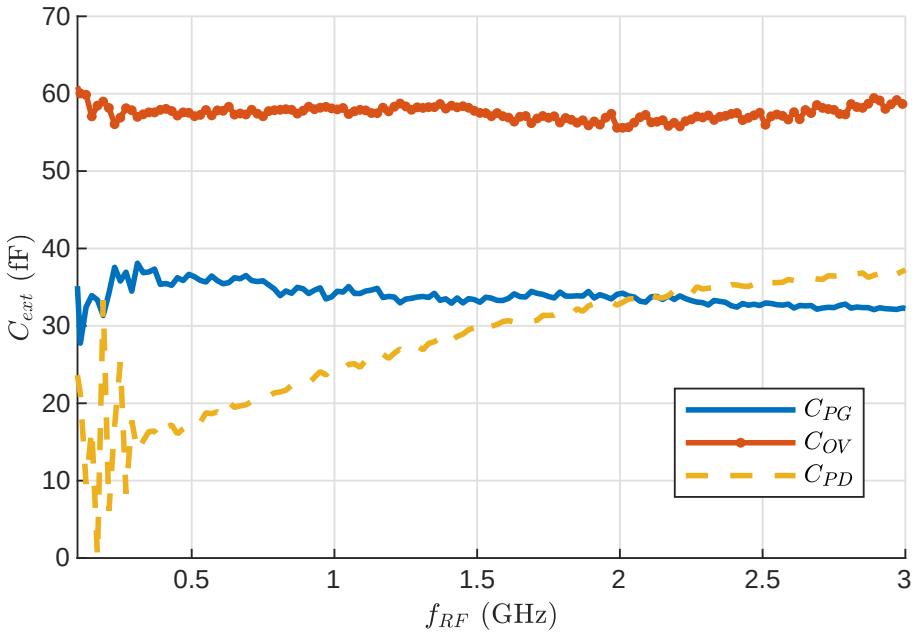


Figure 3.11: Extracted extrinsic capacitances after deembedding of R_{G1}, reducing the effect of frequency dispersion. Reprinted, with permission, from [61], open access under creative common license CCBY-NC-ND.

As shown in Fig. 3.11, the values of the capacitances are $C_{PG} = 36.7\,\text{fF}, C_{OV} = 57\,\text{fF}$ and $C_{PD} = 17\,\text{fF}$.

The extracted value of C_{PG} fits closely to the hand calculation. The capacitance from the thin source metal over a gate of area $20\,\mu\text{m} \times 1.1\,\mu\text{m}$ across an Al_2O_3 thickness of $50\,\text{nm}$ is $33\,\text{fF}$.

3.5.0.3 Extraction of second gate resistance and drain and source resistances

After eliminating the C_{PG} and C_{PD} from the Y-parameters, they can be further converted to Z-parameters and then the R_{G2} and R_{DS} can be evaluated. Fig. 3.12 shows the extracted resistances. For resistance calculation, ideally, the values at higher frequencies are taken [63]. The

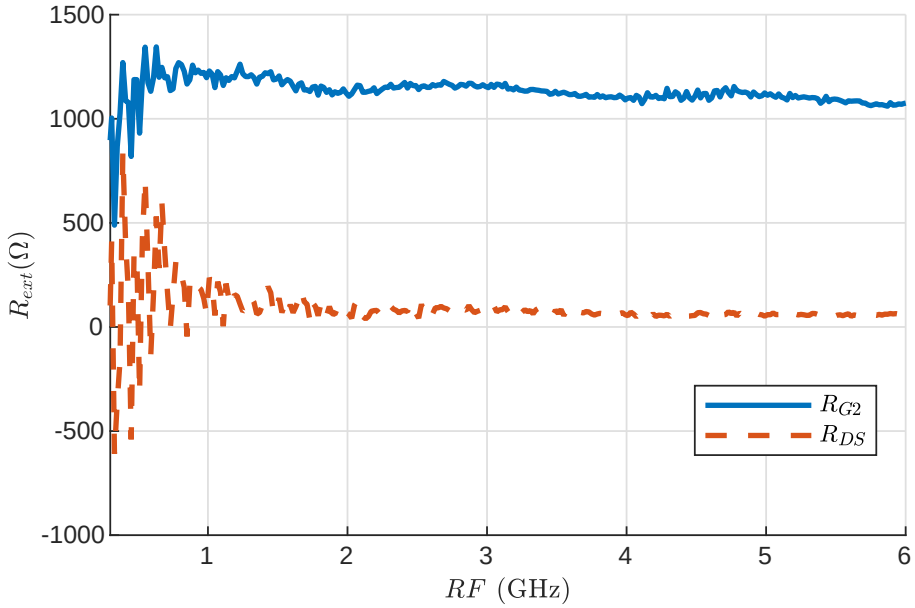


Figure 3.12: Extracted R_{G2} and R_{DS} over frequency. Reprinted, with permission, from [61], open access under creative common license CCBY-NC-ND.

high-frequency value with fitting in Cadence shows that for the in-house TFTs, $R_{G2} = 1078\,\Omega$ and $R_{DS} = 10\,\Omega$.

Here, R_{DS} corresponds to the additional metalization resistance of the source and drain electrode. They are made of molybdenum, which has very low sheet resistance. The occurrence of high values of R_{G1} and R_{G2} is due to the presence of chromium in the gate electrode. In the case of Ti/Au/Ti electrodes, an R_{G1} of around $7.7\,\Omega$ and an R_{G2} of around $21.6\,\Omega$ could be expected.

3.6 Intrinsic model and parameter extraction

The intrinsic model for a quasi-static operation was introduced in Fig. 2.1. Quasi-static operation means that the applied terminal voltages vary so slowly that charge per unit area at any instant at any position is the same as charge at that position if identical DC voltages were applied at the same terminals [66]. If the applied terminal voltages change rapidly, the charge distribution cannot follow without inertial. In this case, the channel behavior is called non-quasi-static (NQS).

If the applied frequency exceeds $1/3$ of the transit frequency of the transistor, the NQS effects have to be considered [67]. The intrinsic model for NQS extraction has been adopted from [65] as shown in Fig. 3.9. Here, r_{gs} and r_{gd} represent the distributed channel resistance corresponding

to capacitances C_{gs} and C_{gd}, respectively. NQS signifies the inertia of the channel with respect to a change in gate-source voltage. This phenomenon occurs at a higher frequency. The NQS has been represented by a transit delay τ, which is the same for both the transconductance and channel conductance. The first-order representation of the $g_{m,nqs}$ and $g_{ds,nqs}$ are given by [66]

$$g_{m,nqs} = \frac{g_m}{1 + j\omega\tau}, \tag{3.12}$$

$$g_{ds,nqs} = \frac{g_{ds}}{1 + j\omega\tau}. \tag{3.13}$$

3.6.1 Intrinsic Y-parameters

The intrinsic Y-parameters in the strong inversion can be given by the following equations [65].

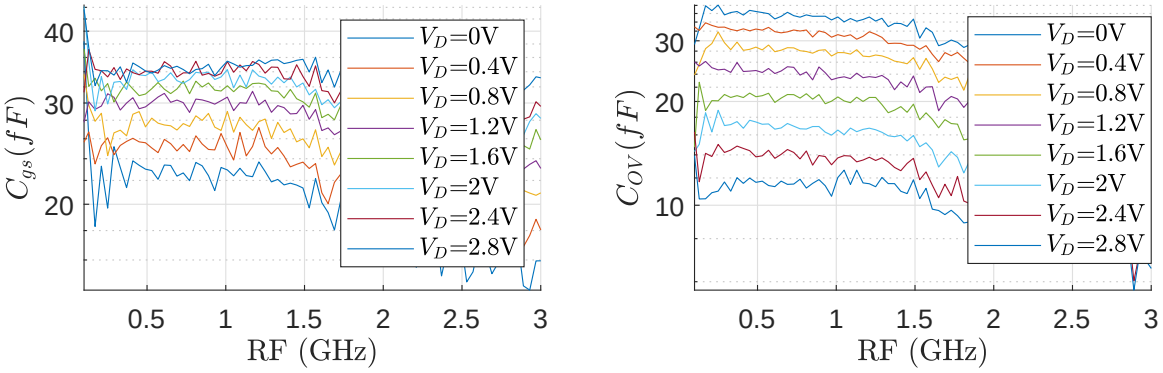
$$Y_{11,i} = \omega^2(r_{gd}C_{gd}^2 + r_{gs}C_{gs}^2) + j\omega(C_{gd} + C_{gs}), \tag{3.14}$$
$$Y_{12,i} = -\omega^2 r_{gd}C_{gd}^2 - j\omega C_{gd}, \tag{3.15}$$
$$Y_{21,i} = g_m - \omega^2 r_{gd}C_{gd}^2 - j\omega(C_{gd} + g_m\tau), \tag{3.16}$$
$$Y_{22,i} = g_{ds} + \omega^2 r_{gd}C_{gd}^2 + j\omega(C_{gd} + g_{ds}\tau). \tag{3.17}$$

As mentioned in [63], [64], [65], the effect of frequency dispersion on the extraction must be neglected. In that case, the following conditions must be assumed that $\omega^2 C_{gs}^2 r_{gs}^2 << 1$, $\omega^2 C_{gd}^2 r_{gd}^2 << 1$ and $\omega^2\tau^2 << 1$. Hence, the intrinsic elements are extracted from the (3.14) - (3.17) at low frequency.

3.6.2 Extraction of intrinsic capacitances

The extraction of intrinsic capacitances can be done after deembedding the extrinsic components and extracting the intrinsic Y-parameters. The imaginary parts of $Y_{12,i}$ and $Y_{11,i}$ provide the capacitances at strong inversion. It is observed that the total intrinsic gate capacitance at strong inversion $V_D = 1\,\mathrm{V}$ and $V_G = 2\,\mathrm{V}$ is around $60\,\mathrm{fF}$, while according to hand calculation, it should be $120\,\mathrm{fF}$. As mentioned in the last section, the presence of trap and contamination is assumed to be the reason for this underestimation of capacitance. The presence of traps can reduce the measured intrinsic capacitance by adding time constants, which causes the frequency dispersion of the gate capacitance. The reduction of gate capacitance at a frequency as low as $1\,\mathrm{MHz}$ has been reported for both a-Si and polysilicon TFTs in [68] and [69], respectively.

At different values for strong inversion, i.e., $V_G = 2\,\mathrm{V}$, the extracted values of C_{gs} and C_{gd} are plotted in Fig. 3.13a and Fig. 3.13b, respectively.



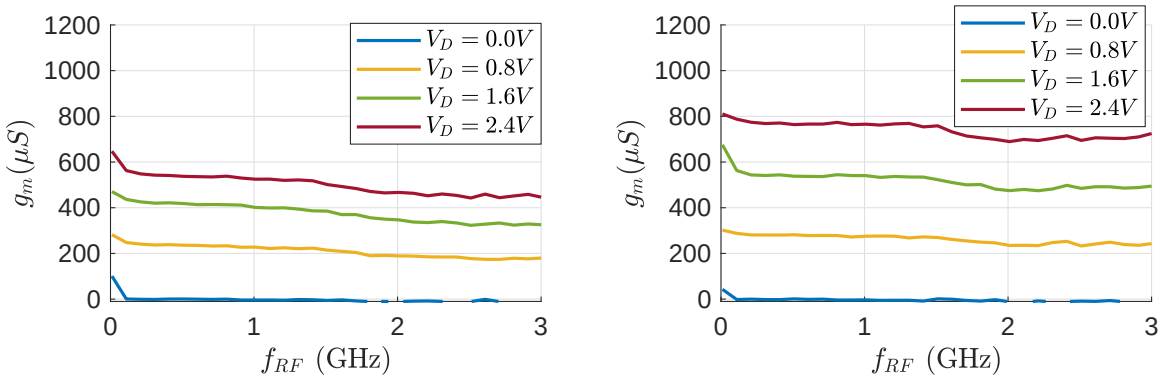
(a) C_{gs} **(b)** C_{gd}

Figure 3.13: C_{gs} and C_{gd} over V_D in strong inversion.

3.6.3 Extraction of transconductance and channel resistance

The transconductance and channel conductance can be extracted using the equations (3.14).

The extracted values of g_m over RF for different V_{DS} at $V_G = 1\,\mathrm{V}$ is plotted in Fig. 3.14a. The similar data for $V_G = 2\,\mathrm{V}$ are plotted in Fig. 3.14b.



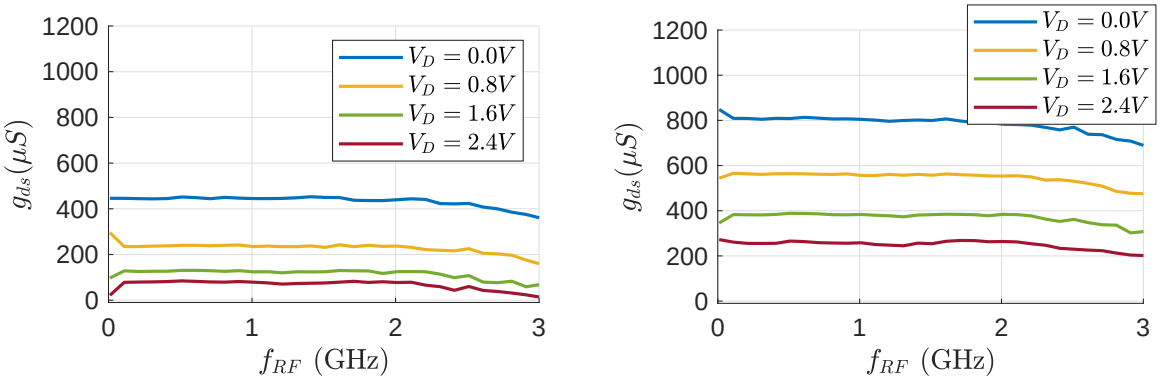
(a) $V_G = 1\,\mathrm{V}$ **(b)** $V_G = 2\,\mathrm{V}$

Figure 3.14: RF extracted g_m for (a) $V_G = 1\,\mathrm{V}$, and (b) $V_G = 2\,\mathrm{V}$.

The extracted values of g_{ds} over RF for different V_{DS} at $V_G = 1\,\mathrm{V}$ are plotted in Fig. 3.15a. The similar data for $V_G = 2\,\mathrm{V}$ is plotted in Fig. 3.15b.

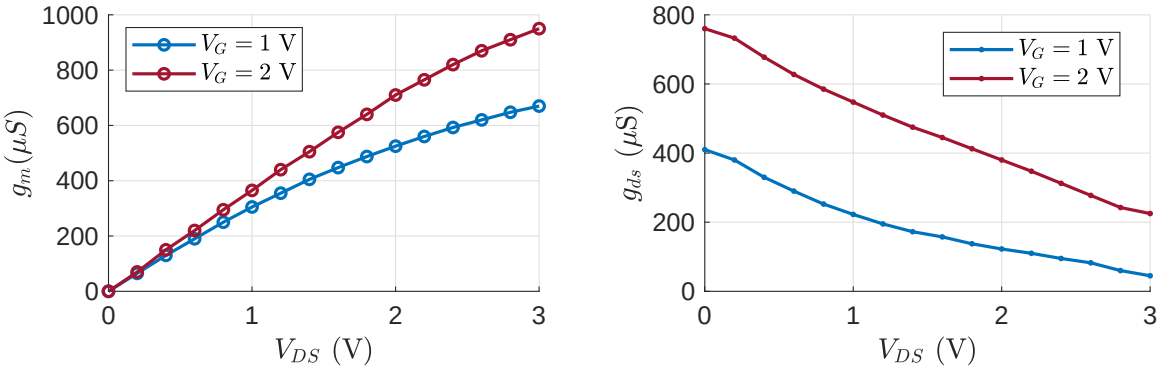
3.6.4 Relation between RF Model and DC Model

The conductance g_m and g_{ds} can also be extracted from the DC I-V characteristics if the V_G is swept with minute intervals during DC measurement. For our measured interval of $0.2\,\mathrm{V}$, we have calculated the g_m and g_{ds} for both $V_G = 1\,\mathrm{V}$ and $V_G = 2\,\mathrm{V}$. As seen from Fig. 3.16a and 3.16b, respectively. This agreement between DC and RF extraction lays the validity of our combined model, where we allow the RPI-a model to decide the channel conductance.



(a) $V_G = 1\,\mathrm{V}$ **(b)** $V_G = 2\,\mathrm{V}$

Figure 3.15: RF extracted g_{ds} for (a) $V_G = 1\,\mathrm{V}$, and (b) $V_G = 2\,\mathrm{V}$.



(a) $V_G = 1\,\mathrm{V}$ **(b)** $V_G = 2\,\mathrm{V}$

Figure 3.16: DC extracted (a) g_m and (b) g_{ds} for $V_G = 1\,\mathrm{V}$ and $V_G = 2\,\mathrm{V}$.

3.6.5 Extraction of channel delay and delay inductance

As described in [65], the channel delay can be extracted from (3.16) as

$$\tau = \frac{1}{g_m}\left(-\frac{im[Y_{21,i}]}{\omega} - C_{gd}\right). \tag{3.18}$$

As seen in Fig. 3.17, the channel delay is low for high V_{DS}. As drain-source voltage increases, the longitudinal electric field increases the carrier velocity. In terms of small signal parameters, it is evident from (3.18) that as g_m increases with an increase in V_{DS} (also shown in Fig. 3.16a), τ reduces. So, it can be concluded that the electric field is more dominant than velocity saturation in the measured range of drain voltage $V_{DS} \leq 3\,\mathrm{V}$.

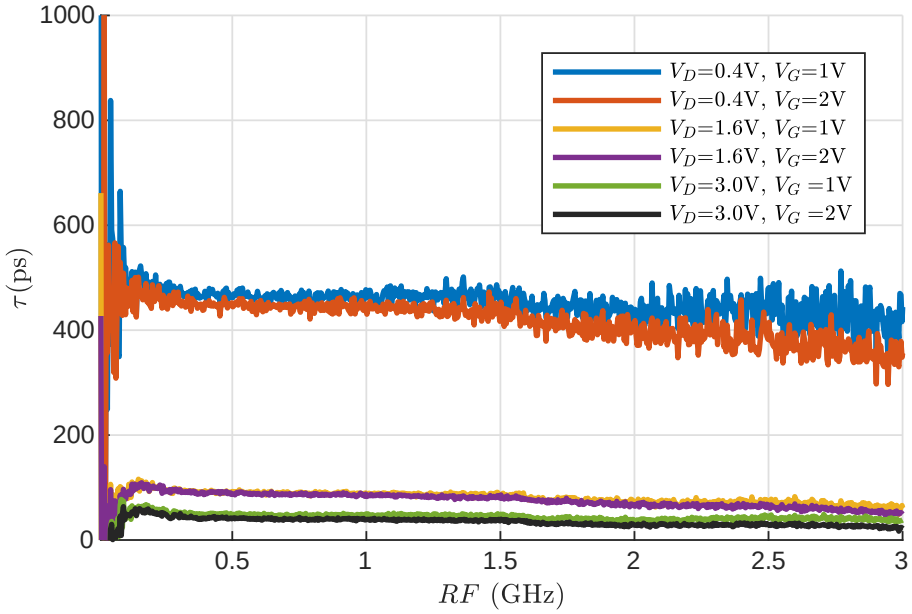


Figure 3.17: τ at different biases.

3.7 Implementation of the model

In Cadence, the extracted model parameters can be implemented as either a model library file or as Verilog-A code, implementing the equations derived from the above data.

3.7.1 Implementation of intrinsic capacitance

The Meyer model has been demonstrated to be valid for intrinsic capacitance in previous research papers for a-IGZO devices [70][71]. The Verilog-A model of the TFT includes the extrinsic components as constants. The voltage dependence of the gate-drain capacitance and the gate-source capacitance is implemented using the Meyer capacitance distribution, with a total oxide capacitance of $120\,\mathrm{fF}$. This value is calculated from the parallel plate formula using the TFT channel dimensions, oxide thickness of $50\,\mathrm{nm}$ and relative permittivity of 8.5 for Al_2O_3.

3.7.2 Implementation of NQS effect

The derived DC RPI-a model parameters control the value of g_m and g_{ds}.

The impact of τ on g_m, known as the NQS effect, is incorporated into the charge calculation using the "laplace_nd" function in Verilog-A. In contrast, the RPI-a model does not explicitly contain an equation for g_m. Instead, τ is included in the channel charge concentration (n_s) of the RPI-a model as

$$n_s = \frac{\epsilon_i \epsilon_0}{q t_{ox} V_{AA}^{\gamma}} \frac{(V_{gs} - V_{th})^{\gamma+1}}{1 + \omega\tau}. \tag{3.19}$$

The same function is used for g_{ds}, which can be given by

$$g_{ds} = \frac{g_{chi}}{1 + g_{chi}\frac{(R_D+R_S)}{F}} \frac{1}{1+\omega\tau}, \tag{3.20}$$

where g_{chi} is the intrinsic channel conductance of the RPI-a model and F is the number of fingers [57]. After repeated fitting, a constant value of the channel delay $\tau = 150\,\mathrm{ps}$ is taken for our modeling purpose.

The extracted RF model parameters for a single-finer TFT (fabricated in 2022) are presented in Table 3.4.

Table 3.4: Extracted RPI-a parameters and RF element values for a single-finger TFT. Reprinted, with permission, from [61], open access under creative common license CCBY-NC-ND.

Parameter	Unit	Description	Extracted Value
R_{G1}	Ω	First part of gate electrode resistance	385
R_{G2}	Ω	Second part of gate electrode resistance	1078
R_{DSE}	Ω	Drain-source electrode resistance	10
C_{PG}	fF	Gate pad capacitance	36.5
C_{PD}	fF	Drain pad capacitance	17
C_{OV}	fF	Gate-drain or gate-source overlap capacitance	57
r_{gd}	Ω	Distributed gate-drain channel resistance	0
r_{gs}	Ω	Distributed gate-source channel resistance	650
τ	ps	Channel transit delay	150

3.8 Model verification and scalability

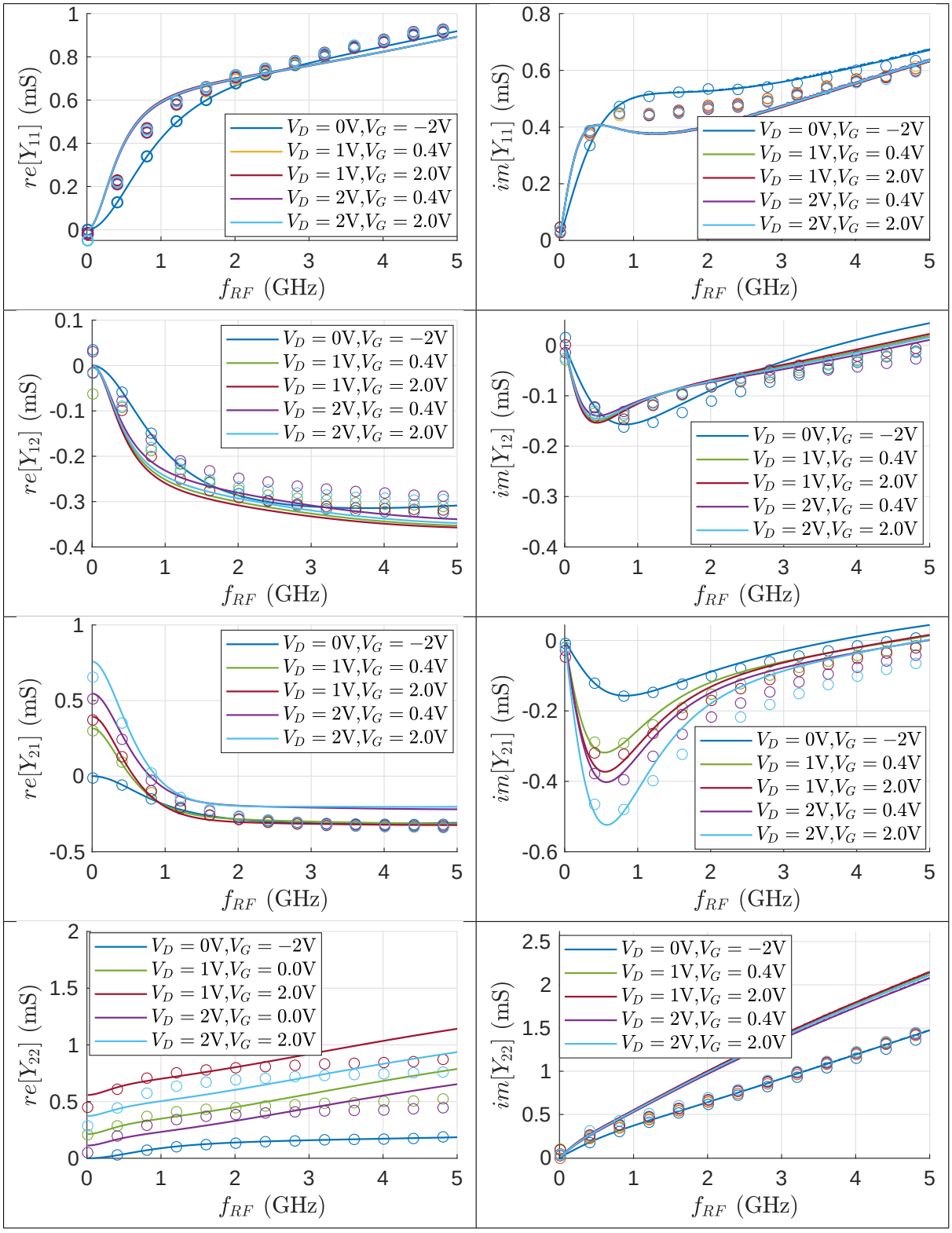
The DC measured versus simulated I-V characteristics have already been presented in Fig.s 3.1a and 3.1b. In this section, we verify the RF model and its scalability in terms of the Y-parameters. For verification purposes, four bias points are chosen, varying both V_{GS} and V_{DS}. The chosen bias points represent the triode and saturation regions.

3.8.1 Single-finger TFT

For a single-finger TFT, the simulated Y-parameters are in perfect agreement with the measured Y-parameter in the null bias condition, as seen in Table 3.5. As the transconductance and the channel conductance are derived from the DC model, the simulation errors in $re[Y_{21}]$ and $re[Y_{22}]$ increase as frequency increases. However, up to $1\,\mathrm{GHz}$, the simulated $re[Y_{21}]$ agrees with the measured data for the presented bias points.

This simulation error is prominent in the imaginary part of the output admittance $im[Y_{22}]$. The higher simulated Y_{22} represents an overestimation in the C_{PD} and C_{GD}. This overestimation could stem from traps in the oxide that could reduce the capacitance in the actual device during measurement.

Table 3.5: Measured (circular markers) versus simulated (solid lines) real and imaginary Y-parameters for a single-finger TFT.



3.8.2 Multi-finger TFT

For verification of the scalability of the derived model, the capacitances and conductances are multiplied by ten and the resistances are divided by 10 in Cadence and simulated for DC and S-parameters. It has been observed from measurements that the V_{th} decreases as the number of fingers increases. For the measured transfer characteristics of the multi-finger device at $V_{DS} = 0.4\,\mathrm{V}$ the threshold voltage $V_{th} = -1.38\,\mathrm{V}$ has been extracted using the integration method mentioned above.

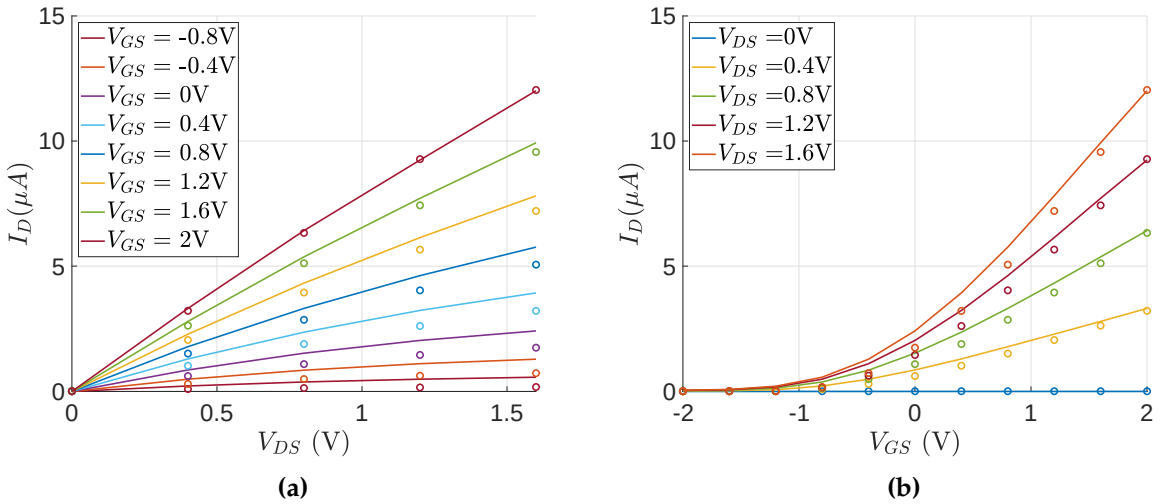


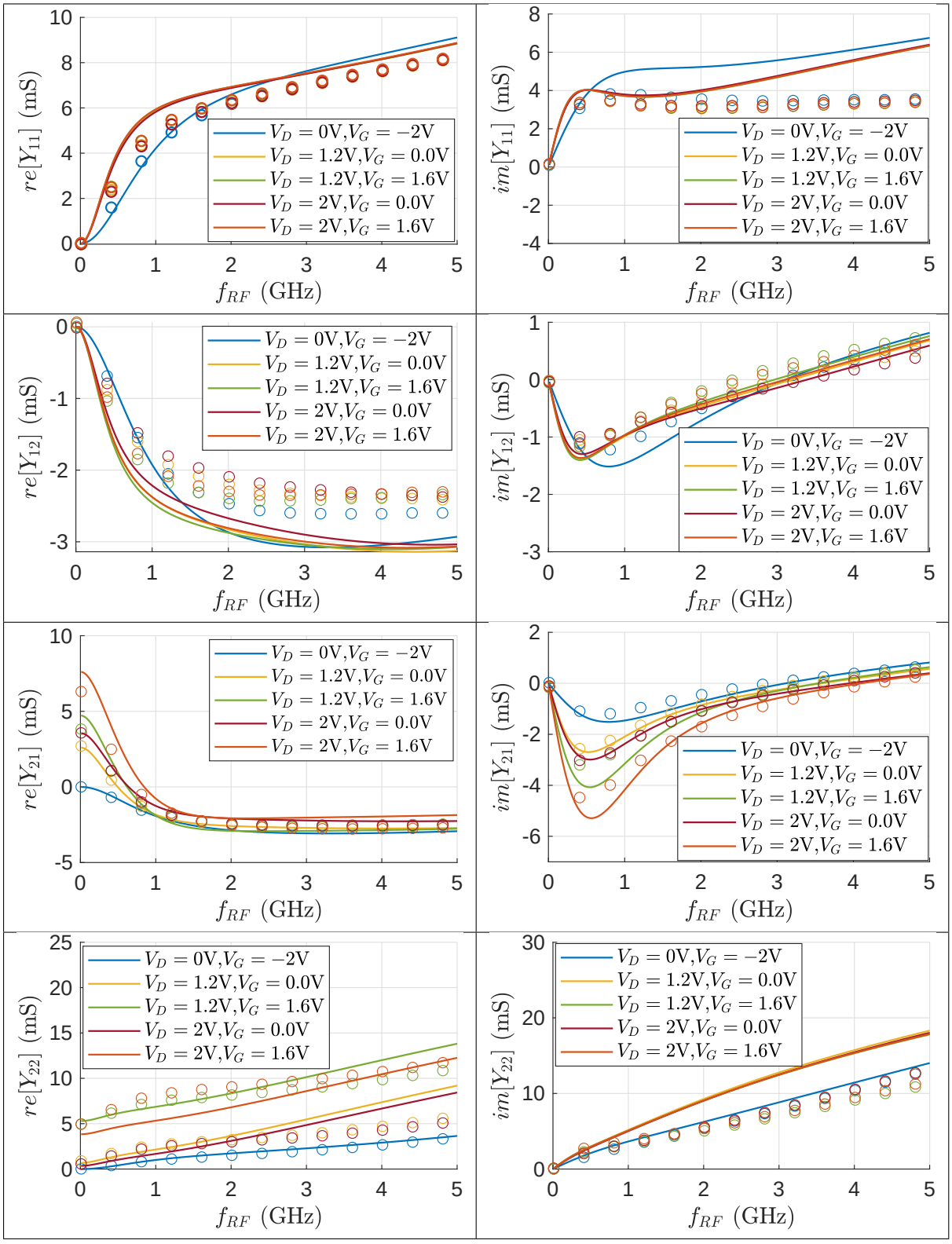
Figure 3.18: Multi-finger simulated versus measured (a) output and (b) transconductance characteristics (solid lines - simulation and circular markers - measurement).

The simulated versus measured output and transconductances characteristics are plotted in Fig. 3.18a and 3.18b, respectively. As seen in Fig. 3.18a, the simulated current (solid lines) matches the measurements (circular markers) better at high V_{GS}. In contrast, in Fig. 3.18b, the simulated transconductance curve matches the measurement better at low V_{DS}. This is one drawback of the modeling since we did not account for mobility variation. Moreover, the threshold voltage V_{th} is only the average mobility of ten fingers. In reality, each finger may have a different charge carrier and impurities, thus having different channel parameters. In any case, this is the best model that could be obtained for a ten-finger transistor for the first time.

The RF model of the ten-finger is verified by considering the identical gate-source overdrive voltage and the drain voltages as the drain voltage as the single-finger TFT presented in Table 3.5. This ensures the same mobility for the single and multi-finger TFTs. On increment of the number of fingers, most of the parasitic elements of the TFT scale with the number of fingers.

Only the extrinsic resistance R_{DE} is not scaled and is kept at $10\,\Omega$. The measured versus simulated RF Y-parameters for the ten-fingers are presented in Table 3.6.

Table 3.6: Measured (circular markers) versus simulated (solid lines) real and imaginary Y-parameters for a ten-finger TFT.



As seen in Table 3.6, the simulated Y-parameters do not deviate significantly from the measured results. The value of $re[Y_{22}]$ and $im[Y_{22}]$ are underestimated for the multi-finger TFTs. We assume that the process variation and parasitic capacitances between different fingers are reasons for this poor fitting. More investigation is needed in order to determine the actual cause.

3.8.3 Transit and maximum oscillation frequency

The RF modeling error can be simplified by observing the f_T and f_{max} of the TFTs. For single-finger TFT, the measured versus simulated f_T is shown for four different bias points in Fig. 3.19a. The comparison for the ten-finger TFT is presented in Fig. 3.19b.

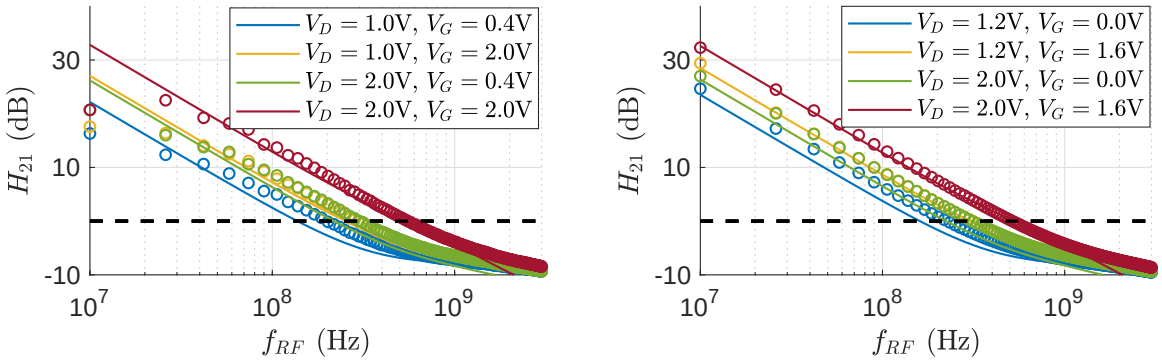


Figure 3.19: Measured (circular markers) versus simulated (solid lines) H_{21} showing f_Ts for (a) a single-finger and (b) a ten-finger TFT.

Here, $V_{GS,ov} = V_{GS} - V_{th}$. Since the value of V_{th} is -0.95 V for the single-finger and -1.38 V for the ten-finger TFT, the chosen bias points correspond to an approximately equal overdrive voltage in the single-finger and multi-finger transistors.

Table 3.7: Calculation of percentage error between simulated transit frequency $f_{T,sim}$ and measured transit frequency $f_{T,meas}$ for the single (one) and the ten-finger transistors.

		$V_{DS} = 1$ V		$V_{DS} = 1$ V	
Finger		$V_{GS,ov} \approx 1.35$ V	$V_{GS,ov} \approx 2.95$ V	$V_{GS,ov} \approx 1.35$ V	$V_{GS,ov} \approx 2.95$ V
One	$f_{T,sim}$	138	258	218	546
	$f_{T,meas}$	198	286	298	540
	% error	30	10	27	1
Ten	$f_{T,sim}$	162	310	226	538
	$f_{T,meas}$	222	314	306	530
	% error	27	1	26	1

A comparison between the simulated and measured values of the f_T is summarized in Table 3.7. The percentage error in simulation is as high as 30% for $V_{GS,ov} = 1.35$ V for both the single-finger and the multi-finger TFTs. At a higher $V_{GS,ov} \approx 2.95$ V, the simulation error reduces to 1%. We assume that the adopted Meyer capacitance model is not precisely accurate. More investigation is needed to derive a better model for the capacitor.

The measured versus simulated G_{max} for the single-finger and multi-finger TFTs are presented in Fig. 3.20a and 3.20b, respectively. It can be seen that the measured and simulated f_{max} are slightly in better agreement, as compared to f_T.

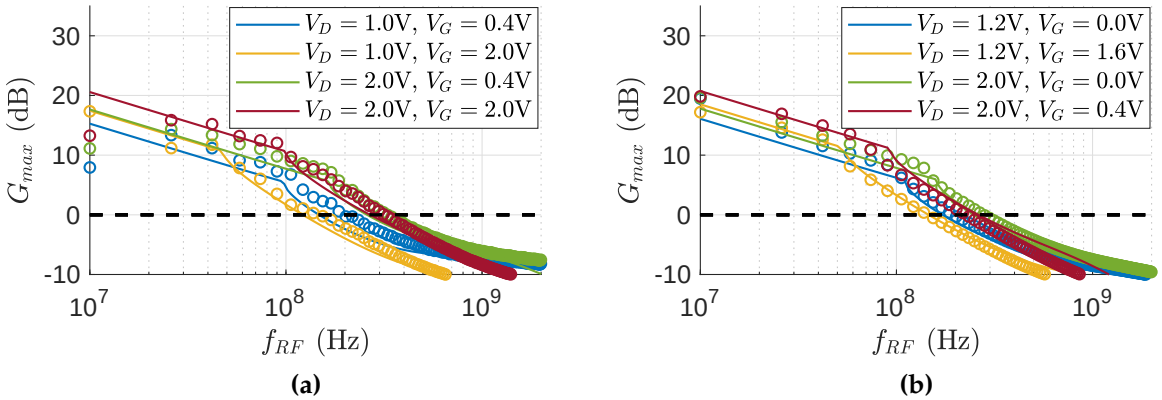


Figure 3.20: Measured (circular markers) versus simulated (solid lines) G_{max} showing f_{max}s for (a) a single-finger and (b) a ten-finger TFT.

A numerical comparison for f_{mmax} is presented in Table 3.8. For the single-finger TFT, the error is below 25%. However, for the ten-finger TFT, the error drops below 20%. It can be inferred that the modeling of the gate has higher accuracy.

Table 3.8: Calculation of percentage error between simulated transit frequency $f_{max,sim}$ and measured transit frequency $f_{max,meas}$ for the single (one) and the ten-finger transistors.

		$V_{DS} = 1$ V		$V_{DS} = 1$ V	
Finger		$V_{GS,ov} \approx 1.35$ V	$V_{GS,ov} \approx 2.95$ V	$V_{GS,ov} \approx 1.35$ V	$V_{GS,ov} \approx 2.95$ V
One	$f_{max,sim}$	150	122	258	266
	$f_{max,meas}$	198	150	326	318
	% error	24	19	21	16
Ten	$f_{max,sim}$	170	146	258	262
	$f_{max,meas}$	194	146	278	226
	% error	12	0	7	16

3.9 Conclusion of TFT modeling

In this chapter, the model for a-IGZO TFTs based on the RPI-a model is derived. The model provides a reasonable estimate for the DC current for both a single-finger and a ten-finger TFT.

We have also presented the high-frequency model for our transistor. Since the extrinsic components of the TFT are geometry and process-dependent, modification of the null-bias procedure is necessary. The gate resistance is divided into parts R_{G1} and R_{G2} separated by C_{PG}, unlike other architectures in the literature.

Based on hand-calculation and fitting, the values of R_{G1}, R_{G2}, gate pad capacitance C_{PG}, drain pad capacitance C_{PD}, overlap capacitance C_{OV}, and drain-source metalization resistance R_{DSE} are obtained and listed in Table 3.4. The model provides good agreement for both the single and ten-finger extrinsic Y-parameters.

The intrinsic transconductance and conductance values are obtained from the RPI-a model itself. The validity of the data is proven for different bias points. However, at high frequency, the simulated conductance deviates from the measured results. The reason is that at high frequency, the channel does not behave as a quasi-static channel. There is a significant deviation between the measured and simulated real and imaginary output conductances at frequencies above $500\,\mathrm{MHz}$. More investigations are needed in this regard.

The decrease in transconductance and conductances at higher frequencies is simulated with the channel transit delay τ. We have implemented a fixed transit delay in the model for simplicity. However, the extraction of τ also shows the behavior of the carriers at different drain voltages. If the drain voltage increases, the resulting electric field across the channel reduces the transit delay.

The combined DC and RF model shows less than 30% error between the simulated and measured transit frequency. For the maximum oscillation frequency, the error is less than 25%. The transit frequency is dependent on the transconductance and gate capacitance. It has been shown in Tables 3.5 and 3.6 that the model provides a good approximation of the transconductance based on the real part of admittance Y_{21}. Thus, the error in f_T is assumed to be from the Meyer capacitance formula incorporated into the TFT model.

Accurately extracting a bias-dependent model for amorphous transistors is a challenging endeavor, especially for submicron channel length. This is our first attempt at modeling an a-IGZO TFT for GHz application. More investigation must be done on the charge carrier dynamics at the GHz frequency range to improve the modeling accuracy.

Chapter 4

Harmonic Generation beyond f_T

For a-IGZO devices where the carrier mobility is low and parasitic capacitances are high, the ability of the TFT to generate high frequency decreases. The output power of a signal source decreases as the frequency of operation increases. In that case, we can use a frequency doubler to double the signal's frequency.

The doublers in this thesis work on the principle of resistive self-mixing [42]. Other complex techniques, both active and passive, are available in the literature for frequency multiplication. The advantage of an active multiplier such as Gilbert cell is that it can provide gain; however, it would also require a complex power distribution and matching network between the switching quad and the transconductance pair. Moreover, the power needed to switch these TFTs would be very high. So, an active mixer would be large, complex and inefficient.

On the other hand, one can use a passive multiplier, such as a traveling wave frequency doubler. This architecture would also cause complexity in the power distribution network between the common-gate and common-source transistors. Hence, a more straightforward passive multiplier is preferable. Although a single TFT can be used to implement frequency multiplication, the spectral purity of the output signal is not high due to odd harmonic contents [42]. Hence, a differential self-mixing circuit is chosen over a single-ended transistor.

The differential frequency multiplier can be implemented in a common-source or common-gate configuration, as shown in Fig. 4.1a and 4.1b, respectively. The latter is a better choice since it helps avoid the Miller capacitance, which could reduce the bandwidth.

4.1 Harmonics beyond f_T

When the active devices have low speed, we can use a doubler to generate a higher harmonic as an output signal. Since the frequency doubling is a non-linear phenomenon, the operating frequency of a doubler is not directly limited by the f_T and f_{max} of the transistors, which are derived considering a linear approximation, i.e., a constant g_m. Hence, although the efficiency

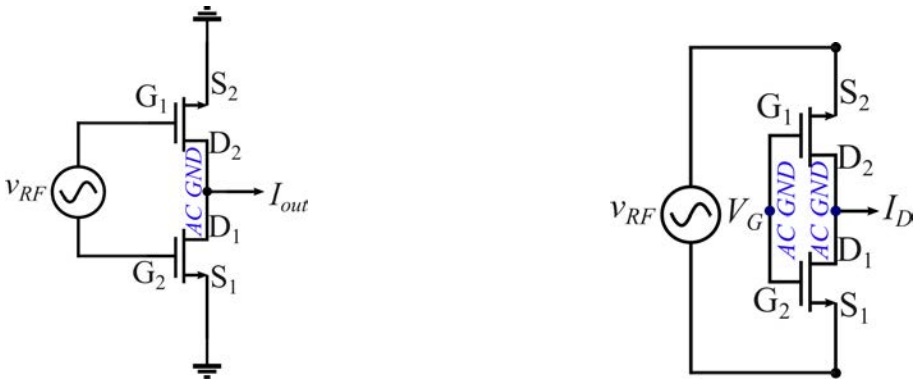


Figure 4.1: Schematic of (a) common-source and (b) common-gate frequency doublers. Reprinted, with permission, from [42], © 2019, IEEE.

of the doubler would reduce beyond the transit frequency due to channel inertia, an FET can still produce a non-linear second harmonic. Any undesired harmonics can be filtered out at the output of the doubler. Enhancement of transconductance by employing multi-finger TFT can improve the second-order transconductance, which in turn can improve the second harmonic output of the TFT.

This chapter shows the overall measurement procedure of the doublers designed during this thesis work. In the beginning, two doublers with single fingers were characterized. One worked on the idea of resistive self-mixing with the help of a capacitance. The other was a differential doubler with the in-built AC ground. The result of the differential doubler was published in [42]. Further improvement and better theoretical and experimental understanding allowed the fabrication of a recently created multi-finger architecture for the differential frequency doubler. It showed a record conversion gain of $-32\,\mathrm{dB}$.

4.2 Theory of frequency doubling

The concept of the square law doubler can be derived from the power law detector proposed in the resistive self-mixing topology presented in [72]. For frequencies below f_T, a single transistor with an external capacitor C_{ext} can be used, as shown in Fig. 4.2a.

The capacitor couples the radiation between the gate and the drain of the transistor. For a device operating in a triode region, the small signal drain current is

$$i_{ds} = v_{ds}(t) g_{ds}(t). \tag{4.1}$$

Here, $g_{ds}(t)$ is the time-varying channel-conductance and for strong inversion, it can be approximated by the square law model as

$$g_{ds}(t) = \frac{W}{L} \mu C_{ox} (v_{RF}(t)/2 + V_G - V_{th}), \tag{4.2}$$

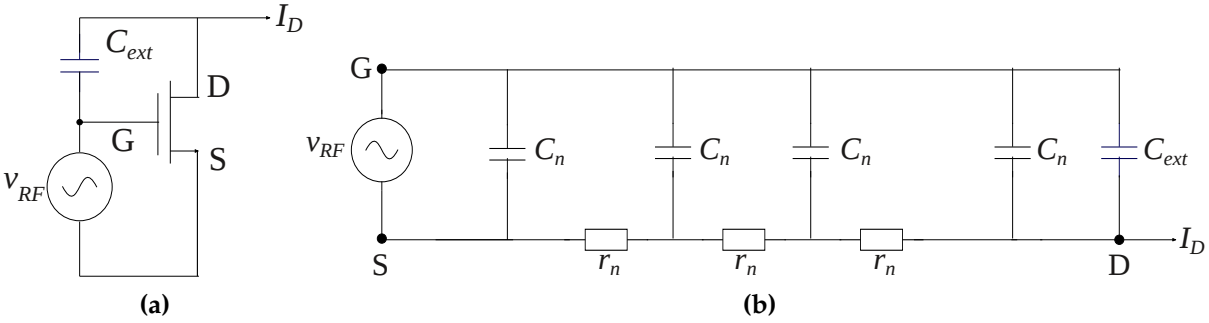


Figure 4.2: (a) Schematic of a single FET doubler with external capacitance, and (b) distributed resistance and capacitance model for a FET channel. Reprinted, with permission, from [42], © 2019, IEEE.

where μ is the carrier mobility, C_{ox} is the oxide capacitance and V_{th} is the threshold voltage of the transistor. From (4.1), and (4.2), the square law relation for the total current can be obtained as

$$i_{ds}(t) = \frac{W}{L}\mu C_{ox}(v_{RF}(t)^2/2 + v_{RF}(t))(V_G - V_{th}). \tag{4.3}$$

Considering v_{RF} to be a time-harmonic AC-signal $v_{RF} = V_{RF}cos(\omega t)$, the peak second harmonic current can be calculated from (4.3) as

$$I_{2f} = \mu C_{ox}\frac{W}{4L}{V_{RF}}^2(V_G - V_{th}). \tag{4.4}$$

The external capacitance can be removed using two differential TFTs, as shown in Fig. 4.1. In this case, the two transistors would create a virtually shared AC ground with a symmetrical structure. As a result, the RF signal between the gate and source also gets coupled to the drain, thereby achieving the square law mixing as shown in (4.4). From this I_{DS} and the DC conductance G_{DS} of the transistors, we can read out the DC voltage V_{out} of the circuit [72], given by $V_{out} = I_D/G_{DS}$.

For frequencies above the f_T of the transistors, the relatively high C_{ext} does not provide the coupling between the gate and drain. However, at such high frequencies, the transistor channel acts as an RC-ladder [72], which can be modeled, as shown in Fig. 4.2b. In this case, the channel is divided into n segments, each equipped with a variable capacitance C_n and a variable resistance r_n.

The gate-to-channel voltage depends on both time t and distance of the channel x from the source v_{RF} and is denoted by $v(x,t)$. For strong inversion of the channel, in the linear region of the transistor, C_n and r_n are related as $1/r_n = \mu C_n(v(x,t) - V_{th})$. This relation leads to a partial differential equation for time and space derivatives as

$$\frac{\partial v(x,t)}{\partial t} = \frac{\partial}{\partial x}[\mu(v(x,t) - V_{th})\frac{\partial v(x,t)}{\partial x}]. \tag{4.5}$$

A numerical approach to solve the above equation and obtain the distributive resistive mixing has been presented in [72]. This principle also enables the differential architectures to function

as a broadband detector.

4.3 Measurement setup

The measurement setup for the detector is shown in Fig. 4.3. A $-10\,\mathrm{dBm}$ RF input signal chopped at 28 kHz, which is above the flicker noise corner of the TFT, is provided by a Keysight E8257D synthesizer at nine different radio frequencies ranging from 50 MHz to 2 GHz. A bias tee and a power splitter are used to combine the signal to DC ground and to create two differential signals, respectively. An R&S HMP4040, a programmable power supply unit, provides a variable gate bias voltage V_G. The supply voltage V_{DD} is delivered by a Keithley 2400 source meter unit through a high $680\,\mathrm{k\Omega}$ resistance to prevent the loading of the detector output V_{OUT} by the source meter unit. The detector output is coupled to an amplifier FEMTO HVA-10M-60-F with a voltage amplification of 40 dB, an input impedance of 1 MΩ and an output impedance of 50 Ω. The amplified output voltage is read through an Agilent E4440A spectrum analyzer for different values of V_{DD} and V_G.

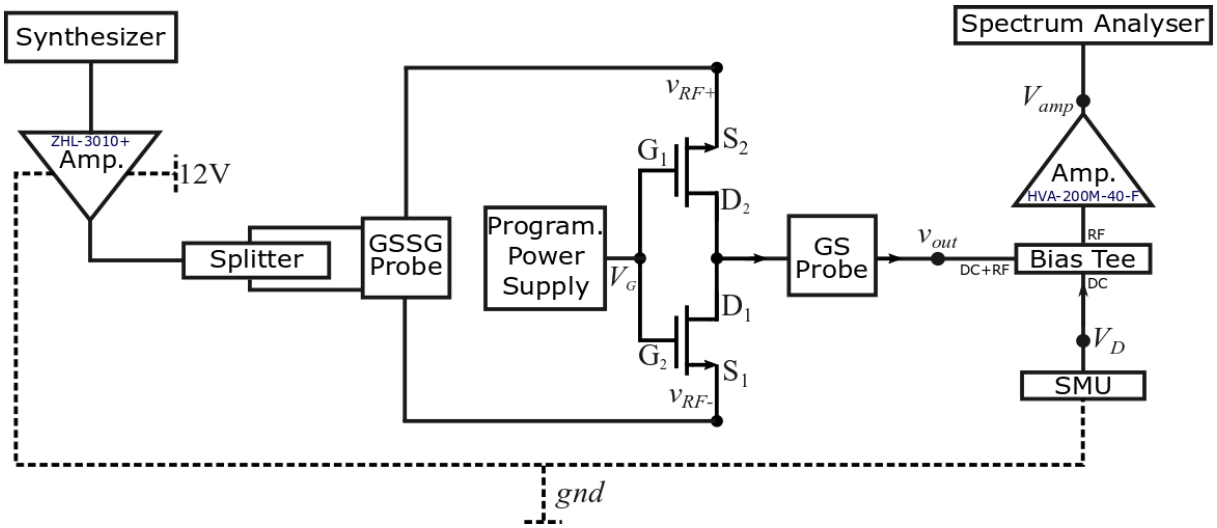


Figure 4.3: Measurement setup for the doubler.

The CG architecture helps avoid Miller capacitance, which can be seen in the case of a CS doubler. The differential architecture provides AC ground at the gate and the drain terminals when the doubler is symmetric[42]. If the two TFTs are symmetric, it helps eliminate the common-mode signal from the output.

4.4 Initial proof of concept

The frequency doubling beyond f_T for a-IGZO TFT was first published in [42] by us. As shown in Fig.4.5a, the doubler consisted of two single-finger TFTs of dimensions $500\,\mathrm{m}/3\,\mathrm{m}$ [42]. A pair of $100\,\mathrm{MHz}$ differential signals of varying amplitude are delivered into the source terminals. The output signal at the drain terminal is measured using a ground signal (GS) probe through a

FEMTO HVA-200M-40-F voltage amplifier and the spectrum analyzer at the bias point V_D= 4 V, V_G= 2.5 V. The gain of the amplifier has been deembedded from the final results.

As shown in Fig. 4.4a, the output spectrum depicts a fundamental leakage and a second harmonic component at the output. The doubler reaches compression at around 3 dBV of input voltage, as depicted in Fig. 4.4b. At this point, an output voltage of 36 dBV is observed. It must be noted that the absolute amplitude of the second harmonic component is not relevant, because there are no conjugate impedance matches provided at the input and the output of the TFT, as they are beyond the scope of this paper. The purpose of this letter is merely to show the beyond-f_T operation of the TFT-based circuit and its future potential for RF applications.

The parasitic output signal at the fundamental frequency is caused by asymmetries in the threshold voltages and the transconductances of the two devices.

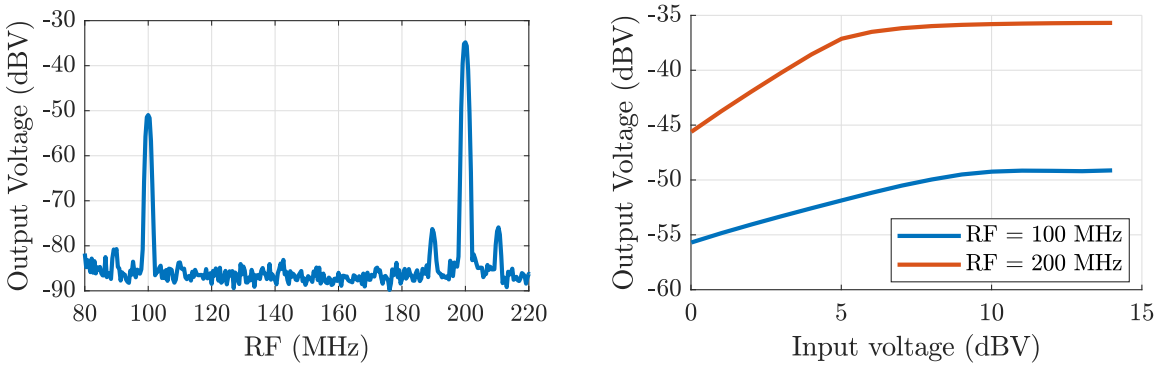


Figure 4.4: (a) Output spectrum at compression and (b) input vs. output RF voltage characteristic of the differential frequency doubler for the fundamental and second harmonic outputs. Reprinted, with permission, from [42], © 2019, IEEE.

4.5 Multi-finger frequency doubler for GHz frequency

Multi-finger frequency doublers can benefit from enhanced non-linearity. The results presented in [42] were for a single-finger TFT-based differential doubler (top view shown in Fig. 4.5a). For GHz frequency doubling, a new multi-finger doubler is fabricated with improved process technology of 100 µm/0.8 µm single channel dimension. As shown in Fig. 4.5b, the new doubler is more compact. In this case, each transistor has four fingers. Although initially designed for Ti/Au/Ti gate electrodes, due to process technology limitations, only Cr-gates could be implemented. Moreover, the fabrication was not ideal since the doubler showed degeneration and high drift over a short period. However, the doubler showed a conversion gain of -32 dB without impedance matching.

The analysis of the doubler is done with the model derived in Chapter 3. This was justified since the TFTs and the doubler belonged to the same batch of the fabricated sample.

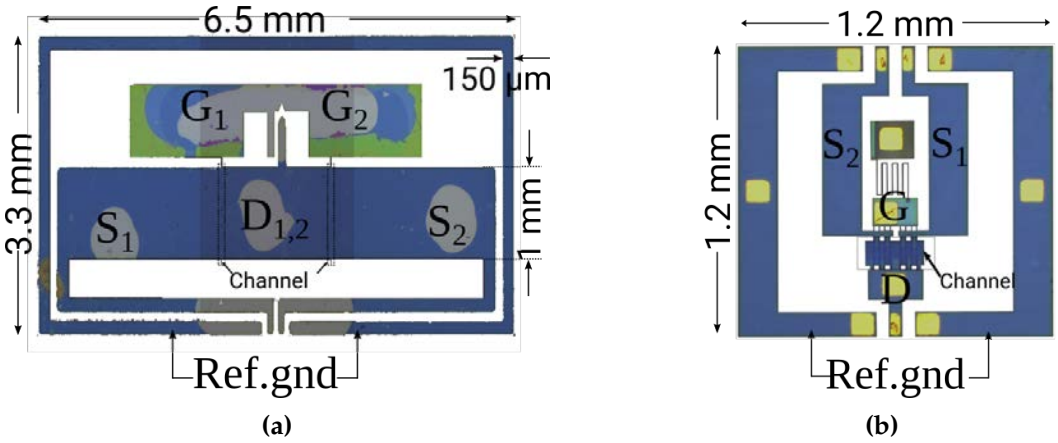


Figure 4.5: Photos of the top-view of CG differential doublers (a) based on two single-finger TFTs [42], (b) based on two four-finger TFTs. Reprinted from [61], open access under creative common license CCBY-NC-ND.

The transistor-level schematic for the simulation of the doubler is shown in Fig. 4.6. Here, the attenuation in the common ground path is considered to improve the precision of the simulation. This attenuation is modeled as an additional resistance $R_{S,add}$ at the source terminal of each TFT. The resistance is hand-calculated from the resistivity of $90\,\mathrm{nm}$ molybdenum, which is equal to around $5.6 \times 10^{-6}\,\Omega\mathrm{cm}$. This results in an $R_{S,add}$ of around $15\,\Omega$ [61].

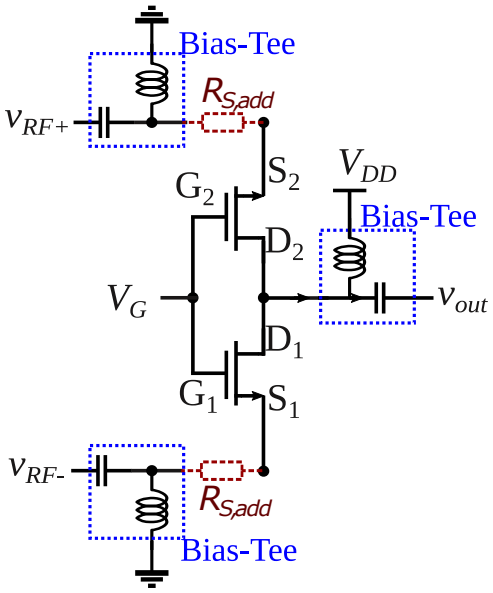


Figure 4.6: Schematic of the common-gate frequency doubler used in the simulation. Reprinted from [61], open access under creative common license CCBY-NC-ND.

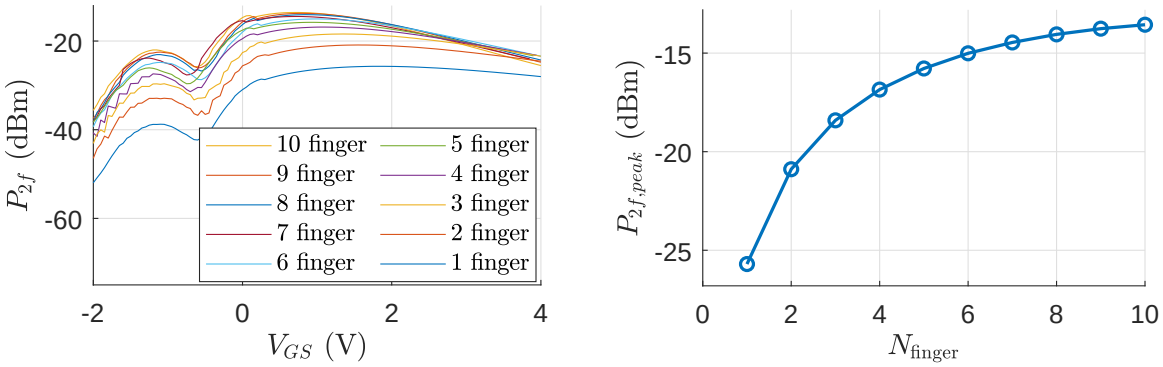
Consequently, the deembedding of the measurement setup has also been performed to calculate the actual input power. The chain of the power amplifier and a $20\,\mathrm{dB}$ attenuator are used to provide a $16\,\mathrm{dB}$ gain to the signal generated by the synthesizer. The splitter loss is taken to be $1.1\,\mathrm{dB}$ based on the datasheet [73]. Similarly, based on the data from Picoprobe [74], a GSSG probe loss of $1.6\,\mathrm{dB}$ is considered. The connector and cable losses are measured to be around

$0.5\,\mathrm{dB}$. The output power of the synthesizer is kept at $1\,\mathrm{dBm}$ [61].

4.5.1 Number of fingers versus output

Increasing the number of fingers enhances the power-handling capability of the transistor. Moreover, it increases the second-order transconductance g_{m2}, which is a measure of the second-order non-linearity [75].

So, the conversion gain of the doubler can be increased by increasing the number of transistors. This is verified in Fig. 4.7a. Here, the model extracted in Chapter 3 is used to simulate output power and conversion gain. The nominal V_{th} of the TFT is $-0.95\,\mathrm{V}$, as presented in Table 3.1. A drain voltage of $V_{DS} = 2\,\mathrm{V}$ and an input power P_{in} of $10\,\mathrm{dBm}$ is used for this simulation. The simulated P_{2f} is over V_{GS}, showing that as the number of fingers is increased, the output power increases. The relation between peak P_{2f} over N_{finger} is shown in Fig. 4.7b. As the N_{finger} increases, the peak P_{2f} also increases. However, the increment becomes smaller with more fingers. This is due to the increasing device capacitances, thus resulting in lower power coupling to the doubler input.



(a) **(b)**

Figure 4.7: Simulated (a) P_{2f} over V_{GS} for different fingers, and (b) peak achievable P_{2f} over number of fingers, given $V_{DS} = 2\,\mathrm{V}$, $V_{th} = -0.95\,\mathrm{V}$ and $P_{in} = 12.3\,\mathrm{dBm}$. Reprinted from [61], open access under creative common license CCBY-NC-ND.

Thus, ten fingers in each TFT would result in higher second harmonic output power. However, the fabrication yield scales inversely with the number of gate fingers. Moreover, higher N_{fingers} also increase the process mismatch since the alignment between the fingers could be erroneous. Hence, for our following experiment, we chose a doubler with four fingers in each TFT [61].

4.6 Results of multi-finger doubler

The fabricated multi-finger doubler is compact compared to the previous doubler, as shown in Fig. 4.5b. Moreover, the TFT speed is also higher, presenting a f_T of around $560\,\mathrm{MHz}$, as shown in Fig. 3.19a. However, the operating point of the doubler may not correspond to the peak f_T

bias points of the individual TFTs. The f_T in the doubler configuration cannot be measured due to the lack of an adequate calibration substrate.

4.6.1 DC simulation

In subsection 3.8.2, a deviation of the ten-finger TFT's V_{th} from that of the single-finger TFT was reported.

Since the doubler comprises of eight fingers, it should ideally show a current eight times the I_D for a single TFT. The initial DC characteristic of the doubler is shown in Fig. 4.8a and 4.8b with the circles. The V_{th} had to be adjusted in the model to fit the measured data. The best fit was achieved by just setting the V_{th} to $-1.475\,\mathrm{V}$. From the transfer characteristic in Fig. 4.8b; the simulation is in agreement with the measured data.

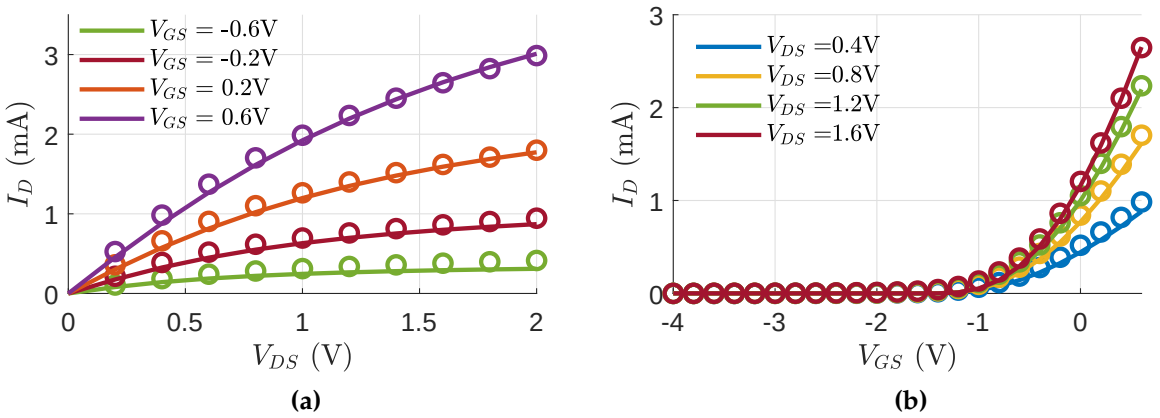


Figure 4.8: Initially measured (a) output and (b) transfer I-V characteristics of the doubler. Reprinted from [61], open access under creative common license CCBY-NC-ND.

4.6.2 Gate voltage versus output power

The breakdown voltage of the TFTs at high frequency is unknown. So, as a precaution, a very low supply voltage $V_{DD} = 500\,\mathrm{mV}$ is taken first for characterization. An input power of $12.3\,\mathrm{dBm}$ is provided, and the gate voltage is swept from $-4\,\mathrm{V}$ to $0.25\,\mathrm{V}$. The first harmonic output power P_f remains almost constant, as depicted in Fig. 4.9a. The second harmonic output power P_{2f} increases with increasing V_{GS}, as shown in Fig. 4.9b. The maximum is obtained at around $V_{GS} = -0.725\,\mathrm{V}$, then the fundamental and second harmonic output powers decrease.

The measurement setup is also simulated in Cadence to verify the model. The simulated output power does not match the doubler in terms of V_G location and the value of the peak power. The simulated peak P_{2f} is located at $V_{GS} = 1\,\mathrm{V}$, i.e., at a value of $2\,\mathrm{V}$ higher than the measured data. Moreover, for $12.3\,\mathrm{dBm}$ of input power, the peak simulated P_{2f} is $-16\,\mathrm{dBm}$, while the peak measured P_{2f} is around $-20\,\mathrm{dBm}$. Hence, it can be inferred that there is some unexpected non-linear behavior of the TFT during the measurement.

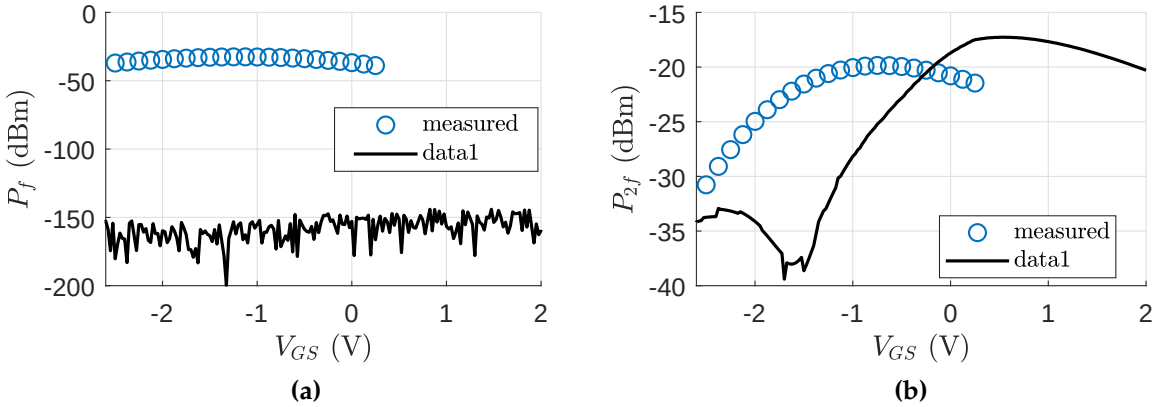


Figure 4.9: Measured versus simulated (a) P_f for and (b) P_{2f} for $V_{th} = -1.24\,\mathrm{V}$ and $\Delta V_{th} = 0\,\mathrm{V}$. Reprinted from [61], open access under creative common license CCBY-NC-ND.

4.6.3 First harmonic rejection

Compared to the simulation, the measured P_f is very high. Typically, a high first harmonic output arises from a mismatch between the two TFTs. The source voltage of one of the TFTs is swept to verify the V_{th} mismatch. The $V_{GS} = -725\,\mathrm{mV}$ and $V_{DS} = 0.5\,\mathrm{V}$ are kept constant. The lowest P_f is observed at $V_{S1} \approx -125\,\mathrm{mV}$, as seen in Fig. 4.10a). It can also be seen that P_{2f} is not affected by the source voltage sweep, thereby confirming the independence of the second harmonic output on the process mismatch.

4.6.4 Bias stress

The applied bias and high RF input cause a negative V_{th} shift. This shift is confirmed by fitting the model to the transfer curve measured simultaneously with the frequency doubling measurement. Fig. 4.10b shows the measured I_D in circles. As shown in Fig. 4.8, by keeping the V_{th} at $-1.475\,\mathrm{V}$, the same transfer curve cannot be obtained in the simulation. Hence, the V_{th} and the fitting parameter V_{AA} are swept in Spectre to arrive at the same current. The best fitting is observed for $V_{th1} = -3.525\,\mathrm{V}, V_{th2} = -3.65\,\mathrm{V}$ and $V_{AA} = 4.0$. This new fitting confirms the negative shift of V_{th} under the influence of RF. An adjustment in V_{AA} indicates a change in mobility as well (from (3.4)).

The negative shift in V_{th} is assumed to be caused by the long exposure of the TFT to bias and heat generated by the RF input, as suggested by [51]. Moreover, the presence of water molecules and hydrogen atoms in the oxide can also cause negative ΔV_{th}, which is only partially recoverable [51],[76].

The RF output is also simulated with the final chosen values $\gamma = 1.014$,$V_{th1} = -3.5\,\mathrm{V}$, $V_{th2} = -3.375\,\mathrm{V}$ and $V_{AA} = 4.6$. As shown in Fig. 4.11a, the difference between peak-to-peak fundamental output power is reduced to around $3\,\mathrm{dBm}$. However, the measurement error between The second harmonic output P_{2f} is in good agreement with the measured result, as shown in Fig. 4.11b. It must be noted that an accurate result is impossible to obtain as there are

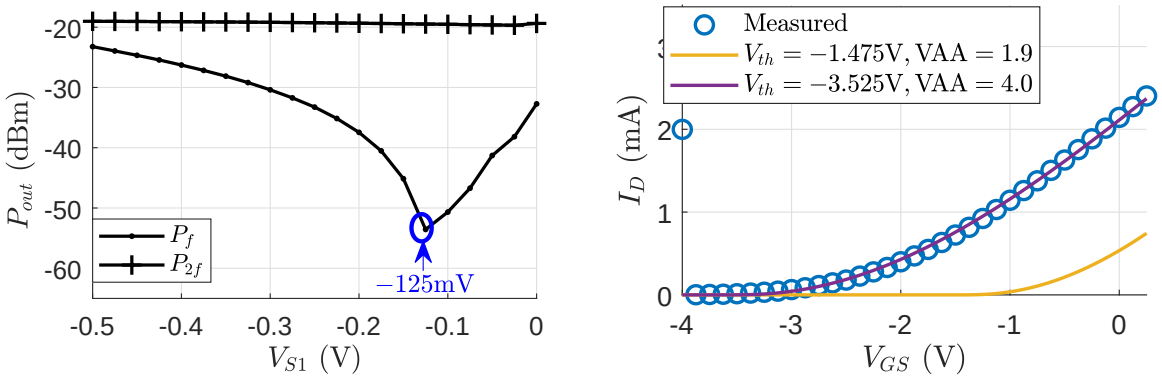


Figure 4.10: (a) Measured P_f and P_{2f} over V_{S1} and (b) measured versus simulated I_D during RF measurement, reprinted from [61], open access under creative common license CCBY-NC-ND.

four fingers in each transistor, and there may be mismatches in the process parameters among all the fingers. However, the peak simulated P_{2f} has the same value as the measured peak.

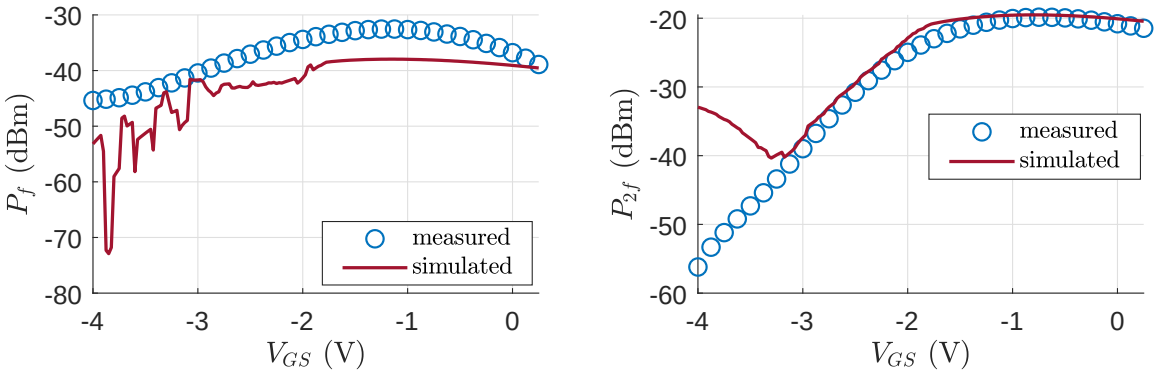


Figure 4.11: Measured (circle) versus simulated (solid lines) (a) P_f and (b) P_{2f} for $\gamma = 1.014$, $V_{th1} = -3.525\,\mathrm{V}$, $V_{th2} = -3.65\,\mathrm{V}$ and $V_{AA} = 4.0$ at $P_{in} = 10\,\mathrm{dBm}$. Reprinted from [61], open access under creative common license CCBY-NC-ND.

4.6.5 RF versus breakdown

A frequency doubler shows compressed second harmonic output power as the input fundamental power increases. The P_{2f} can typically be increased by increasing V_{DS}. This can be confirmed by observing the variation of g_{m2} over V_{DS} [75].

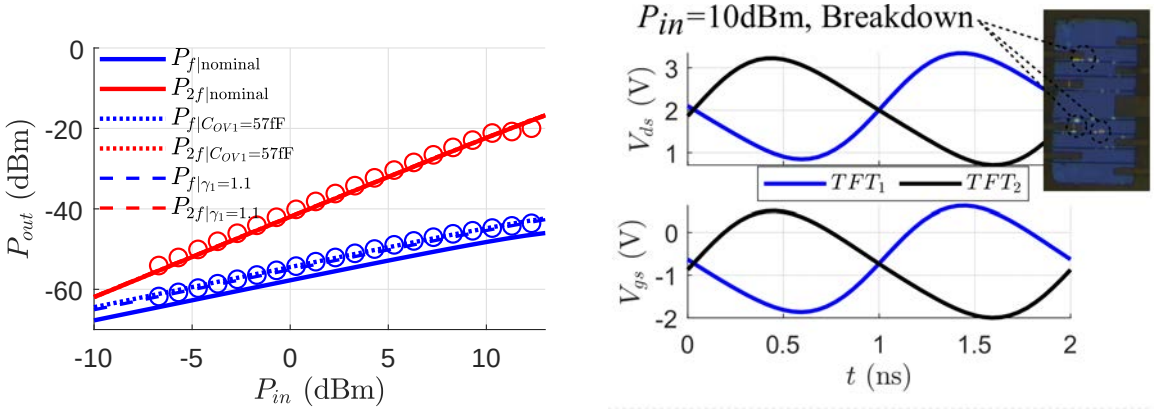
Hence, a higher $V_{DS} = 2\,\mathrm{V}$ is taken, and the input power is swept. The biasing point is at $V_{GS} = -0.775\,\mathrm{V}$ and $V_{S1} = -125\,\mathrm{mV}$ to compensate for a $V_{th1} - V_{th2} = 125\,\mathrm{mV}$. It must be noted that a simple difference in the source voltages cannot compensate for all the asymmetries. The measured data is compared against simulated power performed at the same bias condition. As shown in Fig. 4.12a, the simulated nominal P_{2f} and P_f increase linearly with the input power P_{in} for both simulation and measurements. The simulated $P_{2f|nominal}$ is around $1\,\mathrm{dB}$ lower than the measured data. The simulated $P_{f|nominal}$ is around $3\,\mathrm{dB}$ lower than the measured value.

As established in section 4.6.4, mismatches between the TFTs can result in higher fundamental output power. Here, two example cases are shown. It is seen in Fig. 4.12a that if the overlap capacitance of the first TFT with lower V_{th} is reduced by around $3\,\mathrm{fF}$, an almost perfect fit of the simulated fundamental output $P_{f|C_{OV1}=54fF}$ can be achieved. An identical effect can be observed when γ of the same TFT is increased from the nominal value of 1.0144 to 1.1. This behavior can only be obtained in the simulation. The measured data is not extensive enough to pinpoint the exact reason for the mismatch [61]. The capacitance or mobility mismatch does not affect the second harmonic output power.

The P_{2f} appears to compress at $P_{in} = 10\,\mathrm{dBm}$. However, beyond this input power, the doubler breaks down. Fig. 4.12b shows the simulated V_{ds} and V_{gs} over time of the two TFTs at the input power of $P_{in} = 10\,\mathrm{dBm}$. The $47\,\mathrm{nm}$ thick Al_2O_3 dielectric should sustain the root-mean-square V_{ds} of $0.84\,\mathrm{V}$ and drain current of $1.35\,\mathrm{mA}$ without breaking down [61].

The breakdown is assumed to be caused by the heat accumulation in the channel that has caused a dielectric breakdown. A photo of the top view of the doubler after the breakdown is shown in Fig. 4.13. The is not uniform across the fingers, resulting in a non-uniform breakdown across different fingers.

The quality of oxide also highly dictates the breakdown phenomenon. It has been reported in [77] that high-energy electrons can lead to oxide damage in the presence of traps. More investigations are required in this regard. The presence of traps can be confirmed by generation recombination noise [78]. Such noise behavior for a TFT measured in the same batch as the doubler is presented in section B.2.3 in Appendix B.



(a) **(b)**

Figure 4.12: (a) Measured (circle) versus simulated (solid lines) P_{out} over P_{in} with the breakdown (b) simulated V_{ds} and V_{gs} for $\gamma = 1.014$, $V_{th1} = -3.525\,\mathrm{V}$, $V_{th2} = -3.65\,\mathrm{V}$ and $V_{AA} = 4.0$ at $P_{in} = 10\,\mathrm{dBm}$. Reprinted, with permission, from [61], open access under creative common license CCBY-NC-ND.

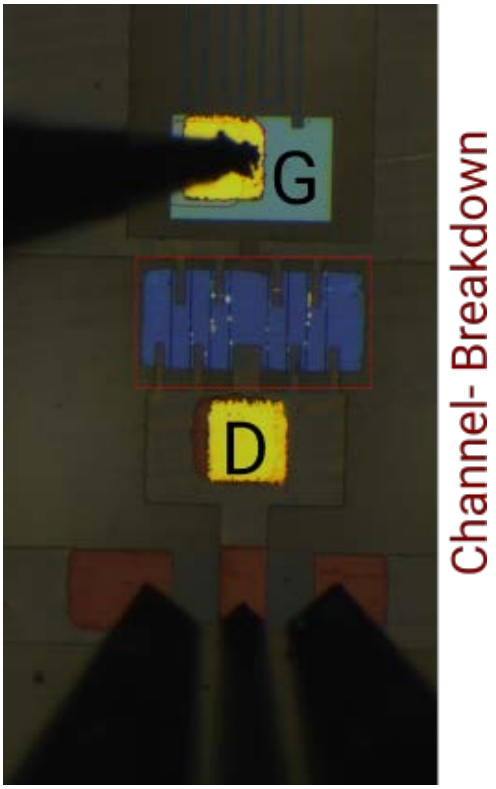


Figure 4.13: Breakdown viewed under microscope at $P_{in} = 10\,\mathrm{dBm}$ and $V_{DS} = 2\,\mathrm{V}$.

4.7 Conclusion of the doubler measurement

A four-finger TFT-based doubler shows a conversion gain of $-32\,\mathrm{dBm}$ for an input signal of $500\,\mathrm{MHz}$ without impedance matching. This is the first doubler with a GHz output frequency in literature till now. Due to the explored non-linear relation between V_{GS} and I_d, the frequency doubling can be achieved beyond transistor f_T and f_{max}. This is the record in terms of the conversion gain of a-IGZO doubler. The application of impedance matching can further improve the conversion gain in future designs.

Applying the RF input power, a significant V_{th} shift is observed. This shift is hypothesized to be due to hydrogen or water molecule presence in the dielectric. Since the TFT is handled in a laboratory atmosphere, the dielectric-semiconductor and the semiconductor-encapsulation interfaces contain water molecules that reduce the lifetime of the transistor.

The model replicated the effects of the threshold voltage shift into the second harmonic output of the doubler.

4.8 Application of the model for higher output power

The main motive behind the extraction and modeling of the intrinsic and extrinsic elements is the application of impedance-matching in GHz TFT circuits. Due to the low yield of the TFTs, the impedance matching could not be characterized. Even the TFTs used in this thesis' doubler measurements could not be used as they deteriorated over time. The cause of deterioration is discussed in the last chapter of this work.

However, it is intuitive and fundamental that the model can be effectively used for RF circuit design, covering the aspects of impedance matching and power generation. The impedance matching is simulated for the doubler with simple LC matching networks at input and output.

As shown in Fig. 4.14, the doubler differential input port is matched to a $100\,\Omega$ and the output port to a $50\,\Omega$ resistance. The input power is taken at $10\,\mathrm{dBm}$. The matching is performed for both high and low carrier mobility, i.e., for $V_{AA} = 2$ and $V_{AA} = 4$. The resultant matching element values are shown in Table 4.1.

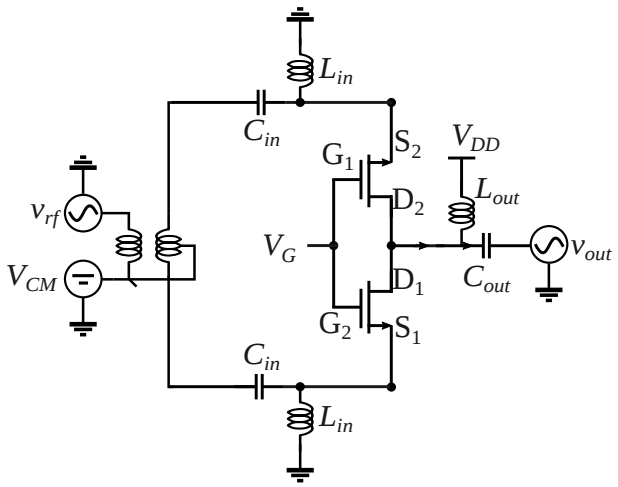


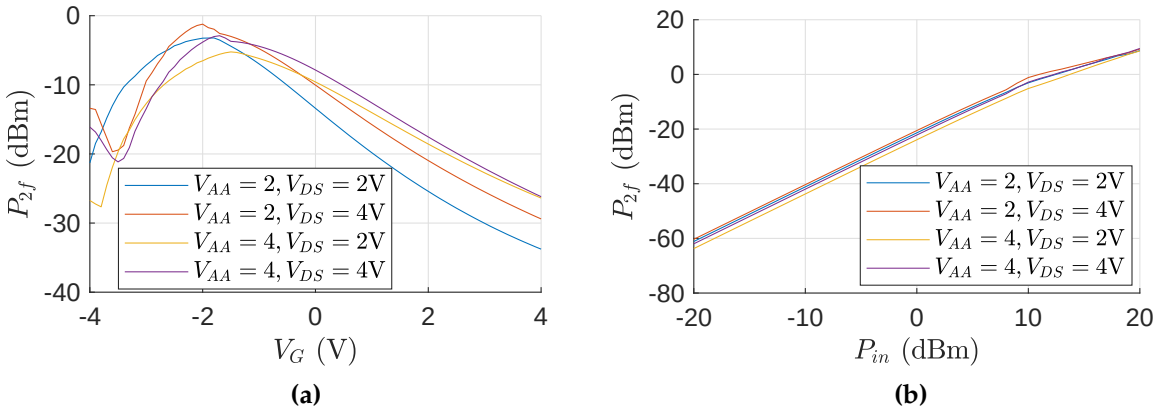
Figure 4.14: Impedance matching of frequency doubler for low and high mobility.

Table 4.1: Simulated values of the matching elements for high and low mobility of the doubler.

Elements	$V_{AA} = 2$		$V_{AA} = 4$	
V_{DS} (V)	2	4	2	4
C_{in} (pF)	2.5	2.5	2.56	2.77
L_{in} (nH)	43	39	42	42
C_{out} (pF)	1.07	1.18	1.33	1.05
L_{out} (nH)	16	15.5	15	16
P_{2f} (dBm)	-3.25	-1.22	-5.28	-2.90

Applying these matching elements improves the peak achievable conversion gain, as shown in Fig. 4.15a. The best possible conversion gain as high as $-11.22\,\mathrm{dB}$ for this generation of devices can achieved with $V_{AA} = 2$ and $V_{DS} = 4\,\mathrm{V}$. As seen in equation (B.3), V_{AA} is the gate overdrive voltage at which the effective mobility is equal to the band mobility. Thus, for maximizing the

second harmonic output of a doubler beyond f_T or f_{max}, the supply voltage should be high, and the V_{AA} or the characteristic voltage for mobility must be low.



(a) **(b)**

Figure 4.15: Simulated second harmonic output power under impedance matching for the above doubler over (a) gate voltage and (b) input power.

However, the effect of V_{AA} on P_{2f} is less dominant than the drain-source voltage, as seen in Table 4.1.

V_{AA} and V_{DS} also affect the compression behavior of a doubler, as seen in Fig. 4.15b. A higher drain-source voltage V_{DS} results in a sharper compression. Inversely, a higher V_{AA} leads to a softer compression as mobility changes slowly over the gate voltage.

4.9 Conclusion

This chapter proves that the second harmonic signal at GHz frequency can be generated from TFTs with lower f_T and f_{max}. Since the frequency doubler is a non-linear circuit, the mobility and the power handling capability are more important than the small signal FoMs such as f_T and f_{max}.

The power output capability of a-IGZO TFTs is severely dependent on the breakdown voltage, thermal property and environmental conditions. Although a-IGZO can handle large voltages, the presence of water or hydrogen molecules can degrade their performance [79]. The presence of traps or impurities in the oxide and the semiconductor-oxide interface strictly dictates the RF performance of the TFTs. Moreover, applying high input power for a longer time can also destroy the a-IGZO devices due to the accumulation of heating [80]. More investigation is required into the thermal performance of the in-house a-IGZO TFTs. The presence of traps can also manifest itself as generation-recombination noise in low frequency. The noise behavior of a TFT is presented in Appendix B, section B.2.3 can confirm the presence of traps.

Chapter 5

Incoherent Detection beyond f_T

As described in Chapter 1, an incoherent receiver directly demodulates the received signal and converts it to the baseband. Such a detector rectifies the input signal and does not preserve the phase information of the input signal. In an OOK communication system, only the amplitude of the carrier signal is modulated. Hence, envelope-detection of the received signal leads to the extraction of the baseband data.

Envelop detection can be achieved by applying resistive self-mixing using a square-law detector. A square-law detector exploits the non-linearity of the TFT, similar to the doubler and detects the baseband signal from a modulated carrier. If the input signal of the TFT is above the transit frequency (f_T), the distributed channel resistive self-mixing ensures detection of the baseband signal [42], [72].

In the following sections, two different generations of square-law detectors are presented.

5.1 Principle of square-law detection

The transfer characteristics of a generic square law detector are given by [81]

$$v_{out}(t) = a_1 v_{in}(t) + a_2 v_{in}^2(t), \tag{5.1}$$

where $v_{out}(t)$ and $v_{in}(t)$ are output and input voltages at time t, a_1 and a_2 are the coefficients of amplification.

The received OOK modulated signal can be ideally represented as

$$v_{in}(t) = \begin{cases} V_P cos(\omega_c t) & \text{if } T_b < t < 2T_b \\ 0 & \text{if } < 0 < t < T_b, \end{cases} \tag{5.2}$$

where V_P is the peak amplitude of the carrier when the transmitted bit is "1", T_b is bit duration, and ω_c is the carrier frequency.

Substituting the $v_{in}(t)$ from (5.2) in (5.1), we get

$$v_{out}(t) = \begin{cases} a_1 V_P cos(\omega_c t) + \frac{a_2}{2} V_P^2 \left(1 + cos(2\omega_c t)\right) & \text{if } T_b < t < 2T_b \\ 0 & \text{if } 0 < t < T_b, \end{cases} \tag{5.3}$$

The DC term in the above equation, i.e., $V_{DET} = \frac{a_2 V_P^2}{2}$ is the detected signal when the transmitted bit is "1".

Since a_2 is the non-linear coefficient of the transistor, the square-law detector is a non-linear detector. By applying a differential architecture, the first harmonic term in (5.3) can be eliminated. Hence, differential detectors are used as broadband detectors [72], [42],[82].

The term a_2 is also called the voltage (or current) responsivity R_V (or R_I). Responsivity is the ratio of the detected voltage (or current) over the input power. Another more critical FoM of a detector is noise equivalent power NEP. NEP is the noise power per square root of bandwidth. It sets the sensitivity or the minimum detectable signal by a detector. The NEP is calculated from $NEP = V_N/R_V$, where V_N is the detected noise voltage.

It is easier to formulate R_V for small-signal input (a few millivolts). In that case, it is approximately the product of second-order transconductance g_{m2} and load resistance R_L. However, if the input signal is large and the device is highly non-linear, the extraction of R_V becomes difficult.

5.2 Generation 1 detector: 2018

The first generation of the detector consisted of two differential TFTs, each of channel dimension $500\,\mu\text{m}/3.2\,\mu\text{m}$. The doubler architecture is presented in Fig. 4.5a. The TFTs had an $f_T = 40\,\text{MHz}$. The responsivity measurement setup is shown in Fig. 5.1. For the linear operation of the detector, a small-signal RF signal of $-10\,\text{dBm}$ was applied from the Keysight E8257D synthesizer. The RF signal was chopped at $80\,\text{kHz}$ to nullify the effect of 1/f noise of the TFT. A bias-tee and a power splitter Mini-Circuits $ZFSCJ-2-232-S+$ were used to combine the signal with DC ground and generate two differential signals. An R&S HMP4040 programmable source provided the gate voltage, while a Keithley 2400 source meter unit provided the drain voltage through a resistance of $680\,\text{k}\Omega$. The output was read with a DC needle connected to a FEMTO HVA-10M-60-F voltage amplifier with amplification of $40\,\text{dB}$, input impedance of $1\,\text{M}\Omega$ and output impedance of $50\,\Omega$. The spectrum analyzer at the output of the FEMTO amplifier reads the detected voltage.

The gate voltage was swept inside a loop for nine equidistant points (in logarithmic scale), as shown in Fig. 5.2a. The noise voltage was measured after turning the RF output from the synthesizer off and dividing the measured voltage by the measured responsivity. The NEP over V_G for different frequencies is shown in Fig. 5.2b. It can be observed that the peak R_V and

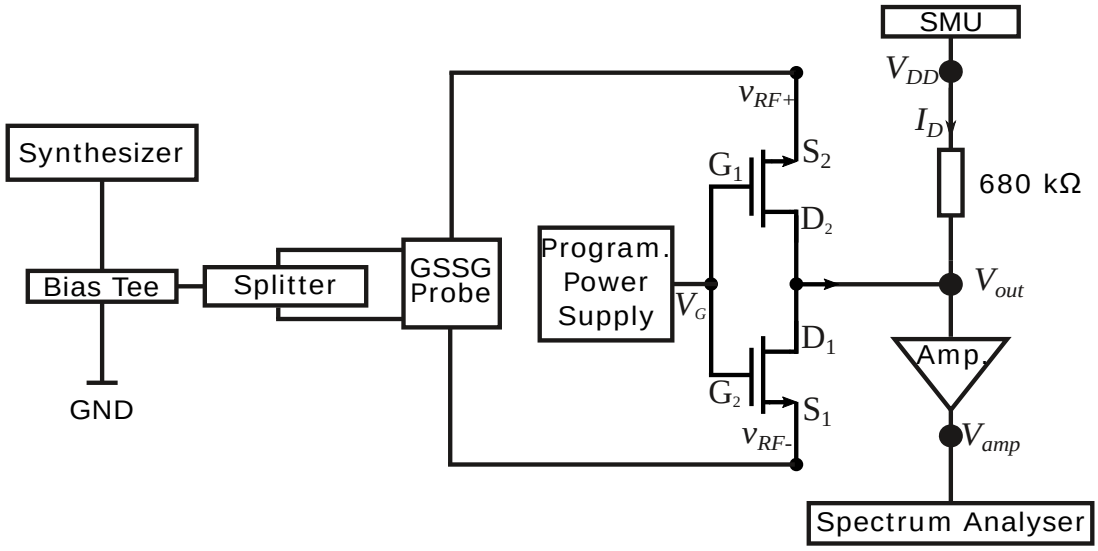
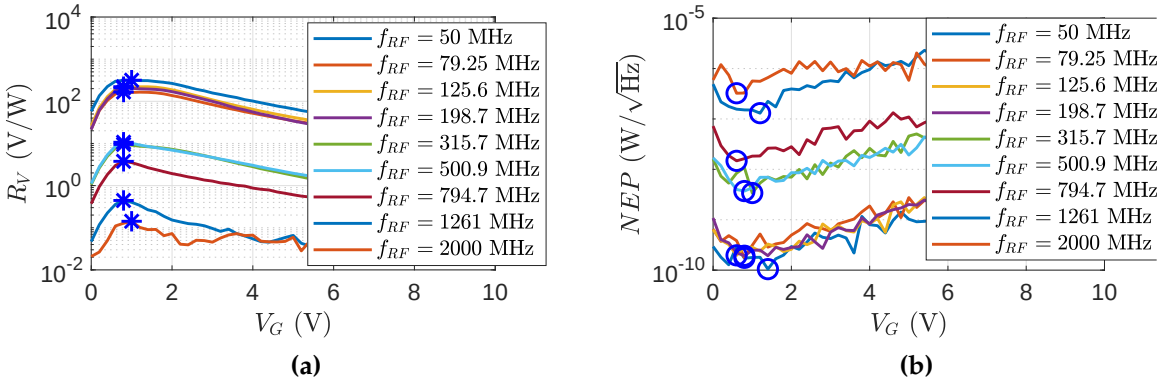


Figure 5.1: Measurement setup for the detector, Reprinted, with permission, from [42], © 2019 IEEE.

minimum NEP occur at very similar gate bias voltage. The non-linearity reaches a maximum at this point.



(a) **(b)**

Figure 5.2: (a) Measured responsivity and (b) NEP over gate voltage for different frequencies for the generation 1 detector.

5.3 Generation 2 detector: 2022

The second-generation detector is also measured in the same way. In this case, the input power is $P_{in} = -20\,\text{dBm}$, lower than the one used in the previous measurement. The lower input power is adopted due to the unpredictable breakdown behavior of the new batch of TFTs of this generation. Moreover, a $550\,\Omega$ resistance in combination with a bias tee is taken to supply the bias current to the detector. The new architecture allows (shown in Fig. 4.5b) the use of resistance and bias tee combination due to the presence of the GSG port at the drain. The calculated responsivities for different frequencies are shown in Fig. 5.3a. The NEPs are shown in Fig. 5.3b.

In order to find the actual power input to the detector, a one-port S-parameter measurement

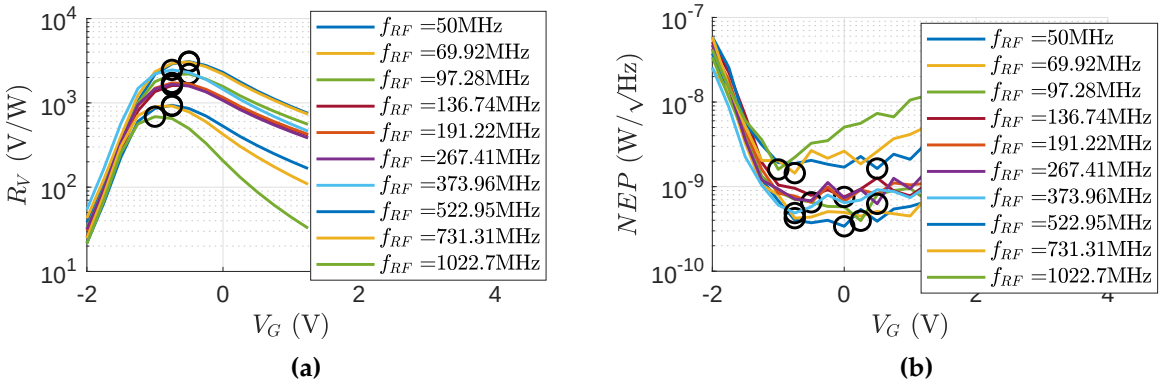


Figure 5.3: (a) Measured responsivity and (b) NEP over gate voltage for different frequencies for the multi-finger detector. The reflection coefficient is not deembedded.

with a VNA is done. In this case, the VNA replaces the frequency synthesizer. The power at the VNA is kept at $-20\,\text{dBm}$, i.e., the same as the input power during responsivity measurement. The S_{11} is thus measured at the input source terminals. The actual input power to available power ratio is given by $1-|S_{11}|^2$. Fig. 5.4 shows the $1-|S_{11}|^2$ for the bias points corresponding to the peak responsivity. The supply voltage is kept at $V_{DS}=1\,\text{V}$. It is important to note that the splitter used in this measurement setup limits the available frequency range to $1\,\text{GHz}$ only. So, there might be an error in the S_{11} de-embedding at $1\,\text{GHz}$.

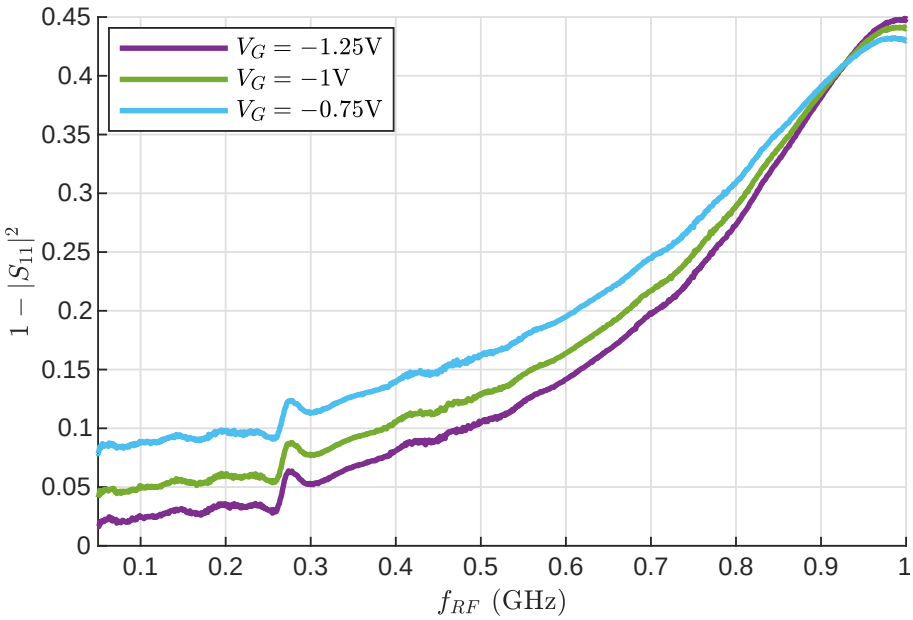
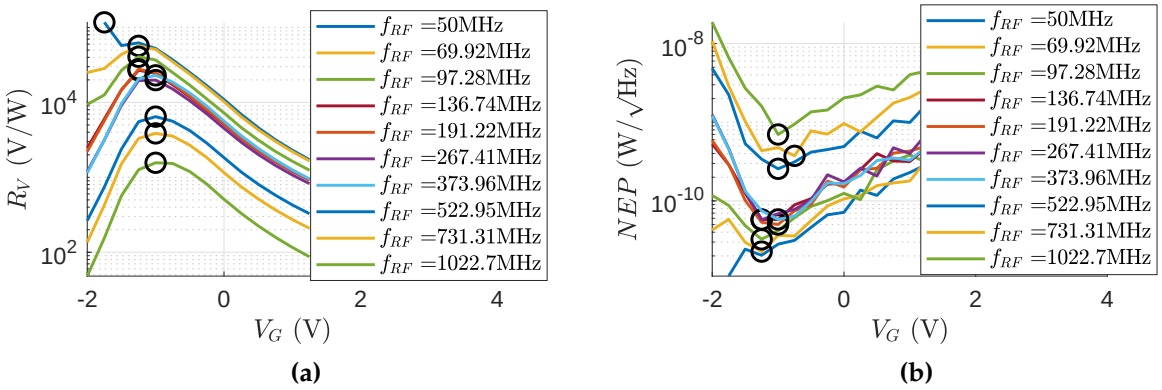


Figure 5.4: Ratio of actual input power to the detector to the available power from the synthesizer.

If the reflected power is thus de-embedded, the responsivity and NEP increases further as shown in Fig. 5.5a and 5.5b.



(a) **(b)**

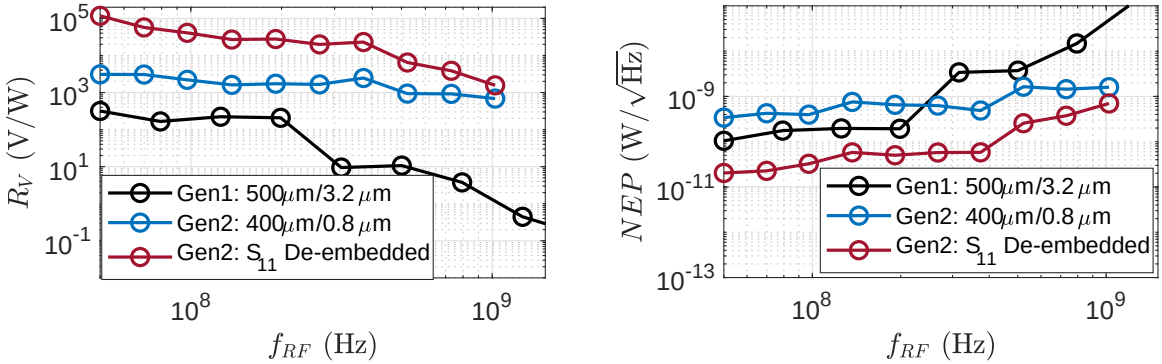
Figure 5.5: (a) Measured responsivity and (b) NEP over gate voltage for different frequencies for the multi-finger detector. The reflection coefficient is deembedded.

5.4 Improvement in responsivity and NEP

The improvement in responsivity is increased by technology improvement and gate resistance reduction. Compared to a single-finger TFT, a multi-finger TFT presents a significant improvement in the second-order transconductance g_{m2}.

Another factor affecting the responsivity is the gate spreading resistance reduction due to the multi-finger architecture. This results in a low attenuation of the signal throughout the width of the gate [83]. Hence, the responsivity of the transistor is high.

A comparison between the peak responsivities $R_{V,max}$ of generation 1 and generation 2 detectors is shown in Fig. 5.6a. Compared to generation 1, the generation 2 detector shows an eight times improvement. Moreover, owing to the high speed and low gate resistance, the responsivity is higher than $1.5\,\text{kV/W}$ frequency up to $373\,\text{MHz}$. The responsivity further improves if the reflected power (S_{11}) is deembedded. In that case, the $R_{V,max} > 20\,\text{kV/W}$ for frequency up to $373\,\text{MHz}$. However, they start converging as frequency increases above $373\,\text{MHz}$.



(a) **(b)**

Figure 5.6: Measured (a) peak responsivity and (b) minimum NEP over radio frequency.

The minimum noise equivalent power NEP_{min} are compared in Fig. 5.6b. For the generation 1 detector, the minimum NEP at $1\,\text{GHz}$ is around $30\,\text{nW}/\sqrt{\text{Hz}}$. For the generation 2 detector, this

reduces drastically to $1.6\,\mathrm{nW}/\sqrt{\mathrm{Hz}}$, without S_{11} deembedding. Removing the reflected power improves it only by half at $1\,\mathrm{GHz}$. However, at lower frequencies, i.e., below $373\,\mathrm{MHz}$, the NEP is almost ten times lower. This is due to the high responsivity of the deembedded measurement.

5.5 Conclusion of detector measurement

The second generation detector shows an $NEP \approx 1.6\,\mathrm{nW}/\sqrt{\mathrm{Hz}}$ without deembedding the reflection coefficient. NEP signifies the noise at the input that produces a signal-to-noise ratio 1 in a 1 Hz output bandwidth. This value reduces if the reflected power is subtracted. However, in real applications, a complete TFT with all the parasitics has to be used. Hence, the total responsivity without de-embedding can give us a better idea about the utility of the TFT for the envisioned transceiver.

For an unipolar OOK modulated signal of bit-rate $R_B = 256\,\mathrm{kbps}$, the bandwidth needed is $BW = 2R_B$. In this case, the minimum detectable power is $N_0 = NEP\sqrt{BW} = 715\,\mathrm{nW} \approx -29.5\,\mathrm{dBm}$ [84].

As described in section 1.1, for a unipolar OOK modulation of a bit error rate of 0.001, the required signal-to-noise ratio for detection is around $7\,\mathrm{dB}$. Thus, for adequate detection of OOK signals, the received signal power must be around $-22.5\,\mathrm{dBm}$. This puts a very high demand on the output power of any a-IGZO-based transmitter. A $1\,\mathrm{GHz}$ signal in a line-of-sight communication undergoes a path loss of $32.44\,\mathrm{dB}$ over a $1\,\mathrm{m}$ distance. Hence, the required transmitter power is around $10\,\mathrm{dBm}$ at $1\,\mathrm{GHz}$. This power requirement could be relaxed using two patch antennas of gain $3\,\mathrm{dBi}$ each. Recently, a differential antenna on a low-cost glass substrate at around $960\,\mathrm{MHz}$ has also been reported in the literature [85]. It provides a gain of around $4\,\mathrm{dBi}$ at $1\,\mathrm{GHz}$.

Table 5.1: Receiver and transmitter powers required for NEP of $1.6\,\mathrm{nW}/\sqrt{\mathrm{Hz}}$ assuming $6\,\mathrm{dBi}$ antenna gain.

RF (GHz)	Range (m)	Path-loss (dB)	NEP_{min} (nW/$\sqrt{\mathrm{Hz}}$)	Data Rate (kbps)	RF BW (kHz) (dBm)	Min. Rx Power (dBm)	Min. Tx Power (dBm)
1.0	1.0	-32.44	1.6	256	512	-22.4	4.03
1.0	0.5	-26.42	1.6	256	512	-22.4	-1.99
0.5	1.0	-32.44	1.6	256	512	-22.4	-1.99
0.5	0.5	-20.44	1.6	256	512	-22.4	-8.01

Table 5.1 shows the transmitter power required for a detector NEP of $1.6\,\mathrm{nW}/\sqrt{\mathrm{Hz}}$ without considering antenna gain. As seen here, the multi-finger TFT still creates a high demand for transmitter power. This could be mitigated by applying an antenna gain of $6\,\mathrm{dBi}$ in the path loss. However, there will be attenuation in the interconnects that could still reduce the power. Moreover, the SNR of $7\,\mathrm{dB}$ in OOK is valid only in the presence of white noise in the channel.

Chapter 6

A Coherent System: Design, Simulation and Layout

The circuits presented in chapters 4 and 5 provide only the concept of harmonic upconversion and incoherent detection, respectively. To design a high-power transmitter ($P_{out} > -10\,\mathrm{dBm}$), signal generation and power amplification are crucial. In this case, the maximum oscillation frequency f_{max} sets the upper limit. It has been reported in [86] that for practical applications considering all the losses, the operating frequency of a power amplifier must be kept at $f_{max}/3$. So, the Cr-gate TFTs presented in Chapter 3 with f_{max} in the range of a few hundred MHz are unsuitable for the GHz transceiver. The high-speed TFTs reported in [37] are a better choice.

This chapter explores the simulation of the GHz transmitter architecture for OOK communication designed with high-speed TFTs. The high power requirement is addressed in the transmitter design. Moreover, a heterodyne receiver is also designed and simulated. The noise figure of the receiver is simulated using a simple thermal noise and shot noise model of the TFT. The feasibility of an a-IGZO-based coherent OOK communication system is addressed based on the resultant transmitter power and receiver sensitivity.

6.0.1 High-speed TFT

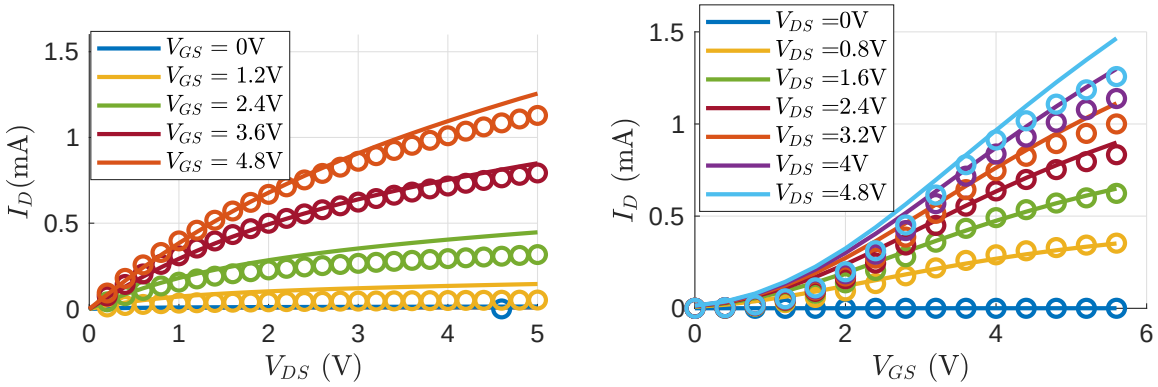
The TFTs presented in [37] had the highest f_T and f_{max} till now in the literature. We had two different channel widths available, namely $50\,\mu\mathrm{m}$ and $100\,\mu\mathrm{m}$. The photos of the top-views of the TFTs are shown in Fig. 6.1a and 6.1b, respectively.

(a) **(b)**

Figure 6.1: Top-view of a single (a) $50\,\mu\text{m}/0.8\,\mu\text{m}$ and (b) $100\,\mu\text{m}/0.8\,\mu\text{m}$ TFT.

6.1 Model extraction of the high-speed TFT

The modeling of the TFTs is done considering the dimensions of $W = 100\,\mu\text{m}$ and $L = 0.6\,\mu\text{m}$. Although the average channel length is $0.8\,\mu\text{m}$, the chosen L gives a better fit, as seen in the output and transfer characteristics in Fig. 6.2a and 6.2b, respectively. The DC extraction algorithm works on least-square fitting and susceptible to error. However, the error is observed only for the higher V_{DS}. That is why the model overestimates the g_m for certain biases.



(a) **(b)**

Figure 6.2: Extracted (a) output and (b) transfer characteristics of high speed $100\,\mu\text{m}/0.8\,\mu\text{m}$ TFTs; circular marker shows measured data and solid lines show modeled current.

6.1.1 Threshold drift in the high-speed TFT

The TFTs with the highest f_{max} are also susceptible to process variation. The change in the threshold voltage V_{th} can be observed between the DC currents measured independently and the DC current measured during the S-parameter measurements. Fig. 6.3a shows the change in the output current during S-parameter measurement (in solid lines). A drift in V_{th} of around 1.5–$2\,\text{V}$ can be better observed in Fig. 6.3b. The same setup as Fig. 3.3b is used with $-17\,\text{dBm}$ output power from the VNA. This low input power cannot change the V_{th}. The reason for the drift is unknown. We must compensate for the drift with proper design techniques.

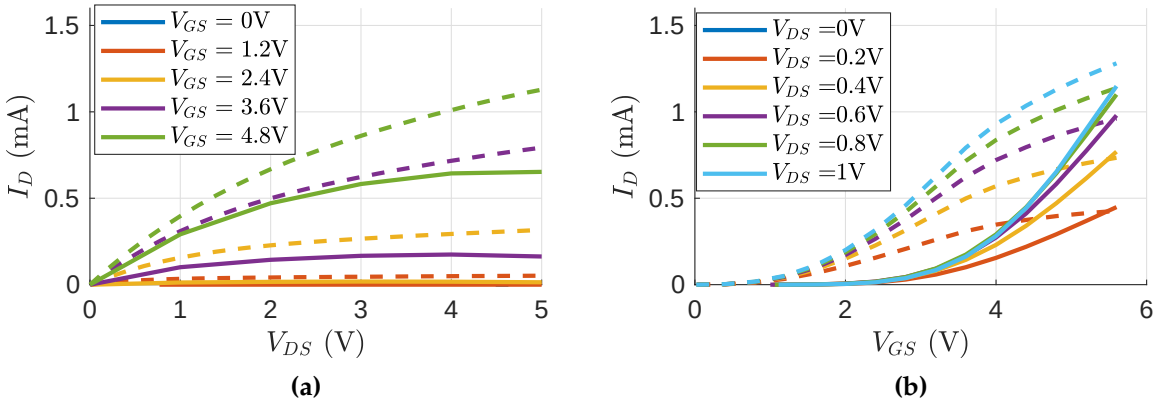


Figure 6.3: Drift in V_{th} showing difference in the measured (a) output and (b) transfer characteristics before (dashed line) and during (solid lines) S-parameter measurement.

6.1.2 Extraction of extrinsic elements

The null-bias method is applied for parasitic extraction. In these TFTs, the gate resistance was not divided into two parts like the one in Chapter 3. The R_{GE}, R_{DE} and R_{SE} are the extrinsic gate, drain and source resistances, respectively. C_{PG} and C_{PD} are the gate and drain pad capacitances respectively. C_{OV} is the overlap capacitance. As seen in Fig. 6.4a, R_{GE} is very high

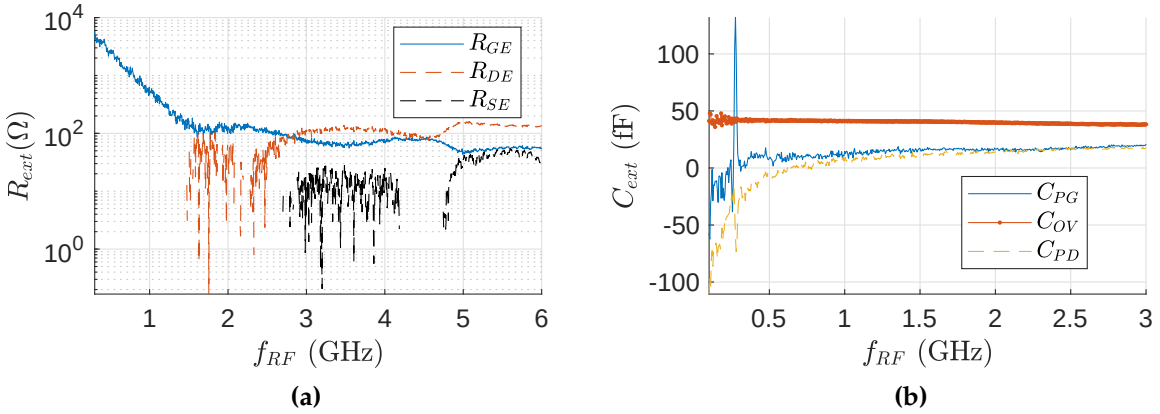


Figure 6.4: Extracted extrinsic (a) R_{GE}, R_{DE} and R_{SE} and (b) C_{PG}, C_{OV} and C_{PD} for the high-speed TFT at null-bias condition.

at low frequency. As mentioned in [63], the resistance values at high frequency give accurate results. The null-bias-extracted gate resistance also matches the formulated gate resistance from the equation presented in [37]. According to [37], $R_{GE} = R_{sh}\frac{W/3+xtr}{L+2L_{ov}}$, where R_{sh} is the sheet resistance for Ti/Au/Ti electrode (around $0.04\,\Omega/\square$), xtr is the extra length of gate electrode leading to the channel area and L_{ov} is the overlap area. This results in an $R_{GE} = 77\,\Omega$. The extracted $R_{DE} = 125\,\Omega$. Fig. 6.4b shows the extracted extrinsic capacitance. Although the total overlap length $2L_{ov}$ was found to be $300\,\text{nm}$, the overlap capacitance C_{OV} is around $40\,\text{fF}$. This value of overlap capacitance corresponds to a total overlap length of around $531\,\text{nm}$. The pad capacitances are negative at low frequencies, which implies that they can be considered zero.

6.1.3 Model verification

As mentioned above, there was a drift in V_{th} during the S-parameter measurement. However, the DC model is extracted from the measured DC before the S-parameter measurements. Hence, we must compare the RF characteristics at the same current level.

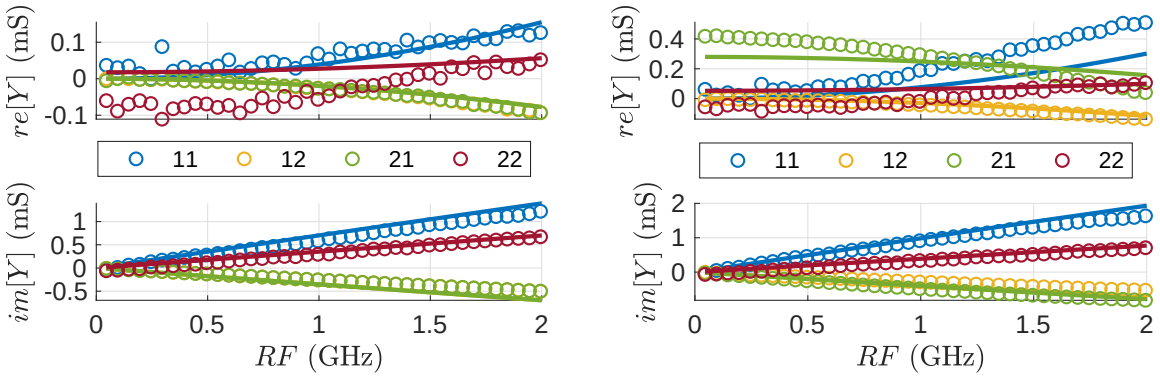


Figure 6.5: Measured (circular markers) versus simulated (solid lines) Y-parameters for (a) null bias and (b) $V_{DS} = 4\,\text{V}$, $V_{GS,sim} = 2.5\,\text{V}$, $V_{GS,meas} = 4.4\,\text{V}$, $I_{D,sim} \approx I_{D,meas} \approx 444\,\mu\text{A}$.

This model has been implemented as a model library file with HSPICE Level N=61 in Cadence Spectre. This is a replica of the RPI-a model. The model library file is shared in Appendix D, section D.2. A significant limitation of this approach is that the NQS effects, namely the distributed gate resistances, transconductance and conductance, cannot be implemented. However, since they are high-speed TFTs with the highest reported f_{max} of around $1.8\,\text{GHz}$, we can design our circuits with the quasi-static approach.

The resultant model versus simulated Y-parameters are plotted in Fig. 6.5a. The measured $re[Y_{22}]$ in circular markers are noisy and negative. The negative $re[Y_{22}]$ can be caused by a large capacitance in the input or output or due to fluctuations in the conductance due to temperature or bias instability. The rest of the parameters are in agreement with the measurement.

The parameters are also compared for the approximately equal simulated and measured current of $444\,\mu\text{A}$ and drain voltage $V_{DS} = 4\,\text{V}$, considering the drift in V_{th} mentioned above. The result is shown in Fig. 6.5b. The imaginary part is in good agreement, but the real parts of simulated Y parameters are slightly offset from the measured data.

These noisy conductances could be either because of device parasitics' frequency dependence or device properties' fluctuations due to temperature and bias fluctuations. Further investigations are needed in this regard.

6.2 Architecture of the OOK transmitter

The power amplifier (PA) decides the condition for a functional transmitter architecture. The gain of a power amplifier, in turn, depends on the active devices' power gain and maximum oscillation frequency. For our a-IGZO devices, as seen in section 2.3.4, the maximum available gain is less than $15\,\mathrm{dB}$, while the peak f_{max} is only around $2\,\mathrm{GHz}$. As frequency approaches f_{max}, the gain also decreases. Hence, we must determine the operating frequency of the PA beforehand to decide the operating frequency of Tx. First, the optimum width must be selected among $50\,\mu\mathrm{m}$, $100\,\mu\mathrm{m}$, $250\,\mu\mathrm{m}$ and $500\,\mu\mathrm{m}$. These are the available masks for the TFT fabrication. The output power P_{out} is calculated from measured IV characteristics using the formula $P_{out} = (V_{BR} - V_{DD})I_{MAX}/(2\sqrt{2})$, where V_{BR} is the breakdown voltage, V_{DD} is the supply voltage with an inductive load, and I_{MAX} is the DC current at V_{GS}, where the transconductance saturates. A simultaneous calculation of optimum output resistance $R_{opt} = (V_{BR} - V_{DD})/I_{MAX}$ is also performed.

A breakdown voltage V_{BR} between $5\,\mathrm{V}$ and $6\,\mathrm{V}$ is considered and P_{out} vs V_{DD} is plotted in Fig. 6.6. It shows that the $100\,\mu\mathrm{m}$ wide TFTs are optimal for designing a higher output power PA. Moreover, as the width increases, the f_{max} of the channel also decreases.

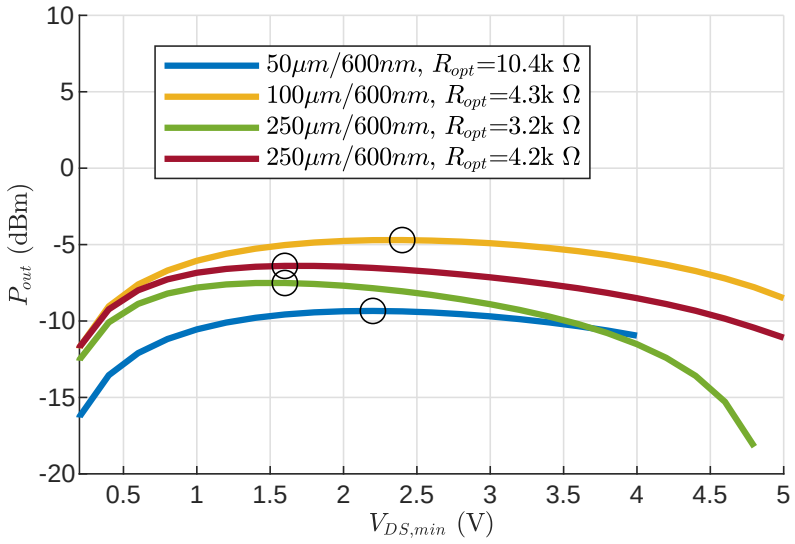


Figure 6.6: Output power over drain-source voltage for an 800nm long TFT with a different channel width.

However, as seen in Fig. 6.6, a single $100\,\mu\mathrm{m}$ wide TFT can ideally generate a maximum output power of $-4.7\,\mathrm{dBm}$ only under perfect load matching. To create a transceiver that can work over at least $1\,\mathrm{m}$ distance at $1\,\mathrm{GHz}$, we need around $-10\,\mathrm{dBm}$ of output power from the TX itself after considering the loss from a passive frequency multiplier and internal attenuation in the circuit. Therefore, it is imperative to increase the amplifier's output power. One must increase the output power by increasing the transconductance, which changes proportionally to width. However, as increasing width causes the f_{max} to drop, we have to adopt the multi-finger TFTs,

which do not affect the f_{max} to a large extent. The choice of the number of fingers depends on many factors, including the load resistance required at the output and the ease of fabrication. A simulation of the output power over drain voltage was carried out for the $100\,\mu\text{m}$ channel width TFTs for different numbers of fingers, as shown in Fig. 6.7. As seen here, output power increases with the number of fingers while the optimum load resistance decreases. A 10-finger TFT can generate around four dBm output power with a load resistance of $310\,\Omega$. Next comes

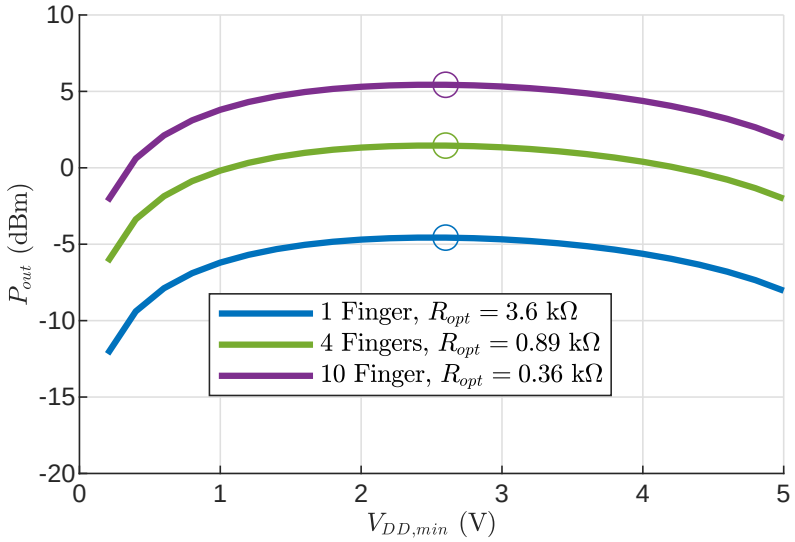


Figure 6.7: Simulated output power over drain-source voltages for an $800\,\text{nm}$ long TFT with different number of fingers.

the choice of the operating frequency of the amplifier. The load line analysis is done based on the DC output current of the TFT. As we go higher in frequency, the output power decreases. However, as we go lower in the operating frequency of the PA, the multiplication factor must be increased in the transmitter chain. This lowering of PA operating frequency would, in turn, result in higher conversion loss for the subsequent doublers. One could mitigate this by designing an active frequency multiplier. The design of such a circuit is more complex in a technology with high process variation. Hence, we limit the frequency multiplication factor to only 2. The final architecture of the transmitter is shown in Fig. 6.8. The frequency doubler, in this case, follows the PA operated at 500 MHz. The PA is fed from a local oscillator (LO) through a baseband modulator. The LO signal is at 500MHz to avoid any doubler preceding the PA, thereby incurring more conversion loss.

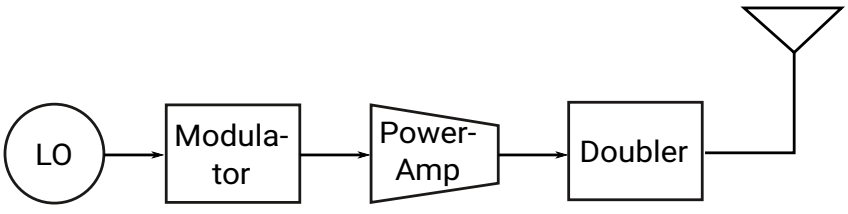


Figure 6.8: Block diagram of the proposed a-IGZO transmitter.

6.2.1 Local oscillator

The oscillators are two types - non-linear or relaxation and linear or harmonic. The simplest example is the ring oscillator (RO), where an odd number of inverter stages are used to create an oscillating waveform. Relaxation oscillators produce non-sinusoidal waves like square, sawtooth or triangle waves. If we use an RO for carrier generation, we must deal with a square wave carrier at 250 MHz. A square wave carrier system is ideal for closed-channel applications like fiber optic and optical line-of-sight communication. The receiver can absorb almost all the transmitted energy.

However, the non-linear carrier can produce a lot of harmonic content for in-air communication. The harmonics cause spectral impurity. An obvious issue is also interference with other channels. A large interferer can cause desensitization of the receiver, also known as jamming [41].

Other possible effects of non-linear carriers in the following PA stage could be:

- Harmonic Distortion: It is an odd harmonic for the square wave carrier. Moreover, that would be amplified by the differential PA. If the modulation is done in the PA, the distortion will create inter-symbol interference.
- Gain Compression: The third harmonic would compress the gain of the amplifier [41].
- Thermal Effect: High-frequency current can heat a power amplifier since the transistors must charge up faster.

To resolve the above issues, one can filter out the odd harmonics from the square wave with pulse width modulation, like a class-D amplitude-modulated transmitter. However, designing such a band pass filter is complicated in flexible electronics. Moreover, the filter has to be active in order to avoid attenuation of the signal. It is almost impossible to design a filter with such a high Q-factor of $1\,\mathrm{GHz}/1\,\mathrm{MHz}$.

Hence, one must use a harmonic or linear oscillator, which ideally has no harmonics and occupies zero bandwidth. There are two types of linear oscillators, namely

- Feedback Oscillator: Electronic noise in the circuit creates the oscillation by getting amplified over the feedback loop. (a) RC Oscillator: Used for low-frequency generation (one could generate baseband), e.g. Phase Shift Oscillator and Wien Bridge Oscillator (b) LC Oscillator: A tuned circuit is used at radio frequencies, e.g. Hartley, Colpitts and Clapp. (c) Crystal: A quartz crystal connected to a-IGZO modulator.
- Negative Resistance Oscillator: Although classically built using one port devices with negative resistance, it could also be built with FETs. The idea is to apply a specific load to the FET that would make the other port unstable and oscillate due to internal feedback. The most popular of these types of oscillators is the cross-coupled oscillator.

The oscillator is chosen to be of the cross-coupled architecture, as it lowers the requirement on the device's transconductance compared to Colpitt or Hartley architecture [87]. A ring oscillator

is not chosen as it is unsuitable for high-frequency design. The frequency of oscillation for the cross-coupled oscillator is determined by the inductor L_{OUT} and the capacitor C_{OUT}. The frequency of oscillation is given by [41]

$$\omega_{osc} = \frac{1}{\sqrt{L_{out} * (C_{GS2} + 4C_{GD} + C_1)}}, \tag{6.1}$$

where C_1 represents the C_{out} and the capacitance of the subsequent buffer stage C_{Buff}. From the simulation, $C_{Buff} = 246.6\,\text{fF}$.

The criterion for oscillation is set by the loop gain of the device as [41]

$$(g_m * R_p)^2 \geq 1, \tag{6.2}$$

or

$$(g_m)^2 \geq \frac{1}{(L_{out} * \omega * Q))^2} = (636\mu S)^2. \tag{6.3}$$

The transconductance of the device determines the output power. For that purpose, the number of fingers should be high. However, incrementing the number of fingers can also increase the parasitic capacitance and non-linearity. Choosing the transistors' number of fingers is a tradeoff between linear transconductance and desired power, parasitic capacitances, non-linearity and ease of fabrication.

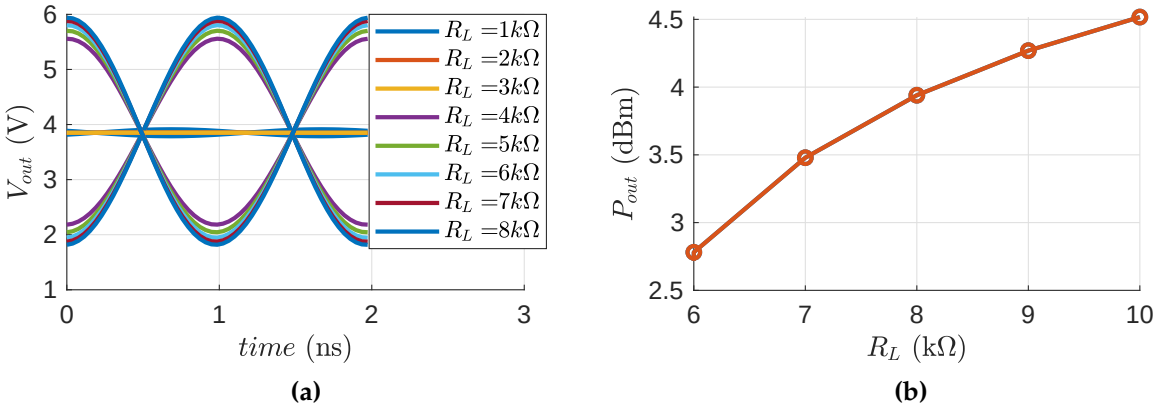
A ten-finger TFT-based cross-coupled oscillator output voltage waveform is shown in Fig. 6.9a with different load resistances, i.e., ignoring the capacitance of the subsequent buffer stage. The amplitude of the output voltage is given by

$$V_{out} = I_D R_P. \tag{6.4}$$

Hence, the higher the load resistance, the lower the loading on the oscillator output and, hence, the higher the power, as shown in Fig. 6.9b.

Here, I_D is controlled by the transconductance or, in turn, the width of the TFTs. However, the TFTs' average V_{GS} also equals V_{DD}. The next stage has a higher supply voltage to prevent clipping of the oscillator output voltage.

In an OOK transmitter, since the LO signal is not being used to switch any transistor, the requirement of a square wave can be relaxed. As seen here, the output of the LO is a differential sinusoidal wave with a swing of around $4\,\text{V}$. This voltage swing from Fig. 3.1 is enough to turn the subsequent buffer stages on and off. These large LO voltage swings are transmitted through the buffer and reach the PA through the modulator, a simple pass transistor.



(a) **(b)**

Figure 6.9: Simulated (a) output voltage swing and (b) output power versus load resistance of the oscillator.

Phase noise is an essential figure of merit for an oscillator as it affects the tuning range and power dissipation due to the broadening of its frequency. For an LC oscillator, the phase noise is inversely proportional to the Q of the LC tank. Since this Q factor is dominated mainly by the inductor, a high-quality external inductor prevents phase noise to a large extent.

6.2.2 Buffer and modulator

The buffer and modulator are designed together, as shown in Fig. 6.10. The buffer stage consists of common-drain differential TFTs. The oscillator's output is coupled to the gate of the buffer TFTs via a capacitor. A bias resistance $R_B = 4\,\mathrm{kW}$ provides the gate bias voltage. The gate voltage is kept at the oscillator's output voltage at $4\,\mathrm{V}$. The RC stage also acts like a high pass filter that allows only the oscillator output to be coupled to the buffer stage. The V_{DD} of the buffer is kept at $8\,\mathrm{V}$ to prevent clipping of the oscillator output. The output of the buffer TFTs is connected to the drains of the modulator, which are pass transistors controlled by an external baseband pulse. Stacking the two stages also reduces the overhead on the drain, thereby preventing breakdown.

When the pulse is on, the RF signal moves from the oscillator to the LC-matching network. An inverse baseband pulse switches the two parallel branches of pass transistors. When the baseband signal is OFF, the RF signal goes to the ground through these transistors. The parallel branches use two $540\,\Omega$ resistors. These resistance values are decided based on the ON-branch impedance at $500\,\mathrm{MHz}$. The ON branch is matched to the power amplifier input port. The matching is done with an L-matching network. The matching network connects the modulator output to the PA input at $600\,\Omega$. Since the amplifier is FET-based, it is better to drive them with voltage instead of current. Hence, as we go higher in matching impedance, it is better. However, the simulation shows that going higher than $600\,\Omega$ prevents us from using an L-matching network with an inductor for setting the DC point. Hence, our maximum limit of matching impedance is kept at $600\,\Omega$.

The buffer's small signal S_{21} is simulated with the input high pass RC filter and the output

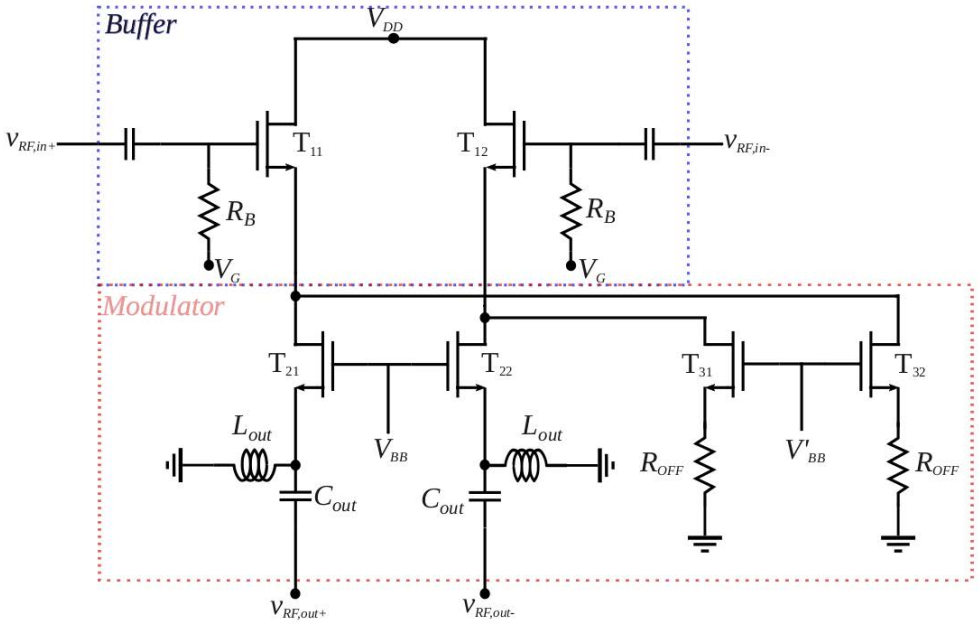
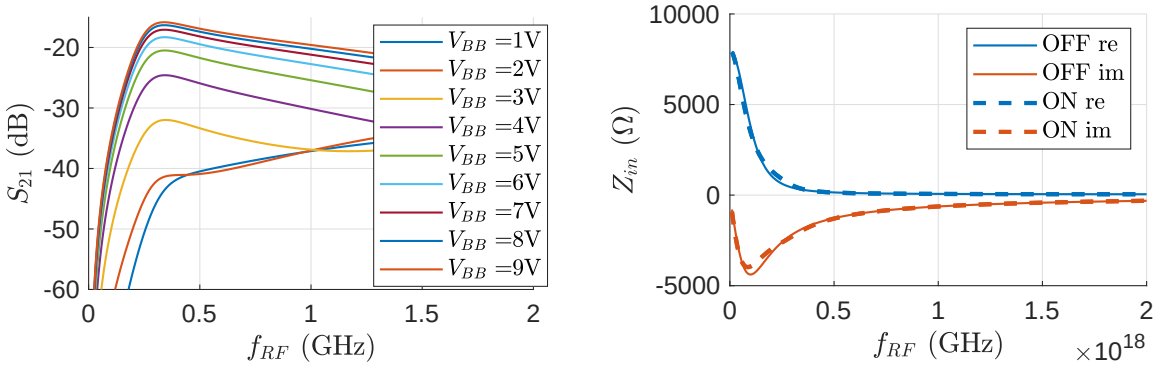


Figure 6.10: Schematic of the modulator and buffer.



(a) **(b)**

Figure 6.11: (a) S_{21} versus frequency for different baseband voltage V_{BB} at the modulator and (b) comparison of the ON-state and OFF-state input impedance to the buffer seen by the oscillator.

matching network at $600\,\Omega$. Here, the chosen L_{out} and C_{out} are set at $135\,\text{nH}$ (LQW2BANR13G00 in [88]) and $1.58\,\text{pF}$, respectively, to make the node impedance $600\,\Omega$. Fig. 6.11a shows the buffer modulator's various S_{21}s for different baseband voltages. The modulating TFTs $T_{21,22}$ act as pass transistors in the triode region and as baseband voltage at the gate increases, the channel conductivity also increases. So, with the rise in V_{BB}, we see an increase in the device's S_{21}. However, beyond a specific value of V_{BB} (5V in this case), the S_{21} does not show a significant change in its maximum value. This behavior could be explained by the typical transconductance curve of a FET where the current, i.e., the channel resistance, becomes independent of the gate voltage beyond a specific value.

The OFF branches form the ground path to the RF signal. The impedance seen by the buffer outputs for both ON and OFF cases is shown in Fig. 6.11b. The impedance's real and imaginary

parts are almost identical over frequency, as seen by the buffer output for both the ON and OFF modulations. The only mismatch here could be caused by process variation among the ON and OFF TFTs.

The output power of the oscillator-buffer-modulator chain is simulated with harmonic balance. As seen in Fig. 6.12, a $-12.5\,\mathrm{dBm}$ output power at $494\,\mathrm{GHz}$ is obtained at the output of the buffer, considering a $600\,\Omega$ load.

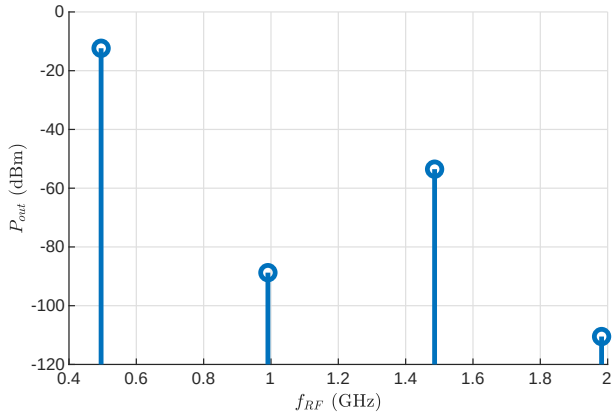


Figure 6.12: Output power of the oscillator buffer modulator chain at a load impedance of $600\,\Omega$.

6.2.3 Power amplifier

The signal obtained from the buffer stage is input into a power amplifier operating at $500\,\mathrm{MHz}$.

The power amplifier is designed in two stages to get a higher gain. It is a basic class-A amplifier as it can operate closer to f_{max}. As such, the efficiency of the device is the lowest. Ten fingers are taken for the PA, as mentioned in section above. Moreover, the PA is also made differential so that its output can be fed directly to a differential doubler with a lower conversion loss than a single-ended transistor. It also eliminates the need for a power divider (or balun) from the differential modulator. The design methodology of the PA is similar to the one mentioned in [45]. First, the cross-coupled capacitor C_{cross} is swept across the two differential ten-finger devices, as shown in Fig. 6.13 and the small signal Rollet stability factor K_f is observed. The K_f peaks at $C_{cross}{\approx}600fF$. It is important to note that K_f each of the stages of the PA peaks at this same value of $C_{cross} = 600fF$. At this point, the maximum available gain has a local minimum of 8.5 dB in the stability region. Although we could boost gain at the ends of the stability region (i.e., $K_f = 1$) up to 10.5 and 11 dB, this is not explored as the fabrication process could lead to variations, and the PA could become unstable. Hence, the design that provides the maximum neutralization of the PA is the main focus.

The presence of $re[Y_{12}]$ prevents the full unilateralization of the TFT by external equivalent capacitance [45]. Capacitive neutralization works at $f \leq f_{max}/2$. In that case $U \leq G_{max} \leq (2U-1) + 2\sqrt{U(U-1)}$. When $f \geq f_{max}/2$, the parasitics in the layout are absorbed in the transistor RF model and can degrade performance. They can even create a negative G_{max}.

Degradation of U due to $C_{GD,ext}$ is twice due to $C_{GS,ext}$. Normally, the advantage of multi-finger is a lower R_G. However, the disadvantage of having a multi-finger on one side is that the drain is stretched and causes higher $C_{GD,ext}$, which lowers the unilateral gain. The advantages of differential architecture are the shorter physical interconnection of source terminals and insensitivity to modeling inaccuracies of the decoupling capacitors. Also, a lower G_{max} of PA causes poor power-added efficiency. More stages need a more cascaded architecture, which reduces the bandwidth.

It should be noted that the total G_{max} observed in Fig. 6.13 is achievable only when both ports of the PA are matched to $100\,\Omega$. In reality, if load matching is done at the amplifier stage's output, the actual transducer gain becomes lower than G_{max}. Hence, a two-stage power amplifier topology has to be adopted to enhance the gain. When the matching is done only between two stages, it is possible to adjust them during measurements since some of the matching elements can be externally implemented. Increasing the number of stages to above two would cause the inter-stage matching to be more complicated. Therefore, with ten-fingers TFTs, the two-stage

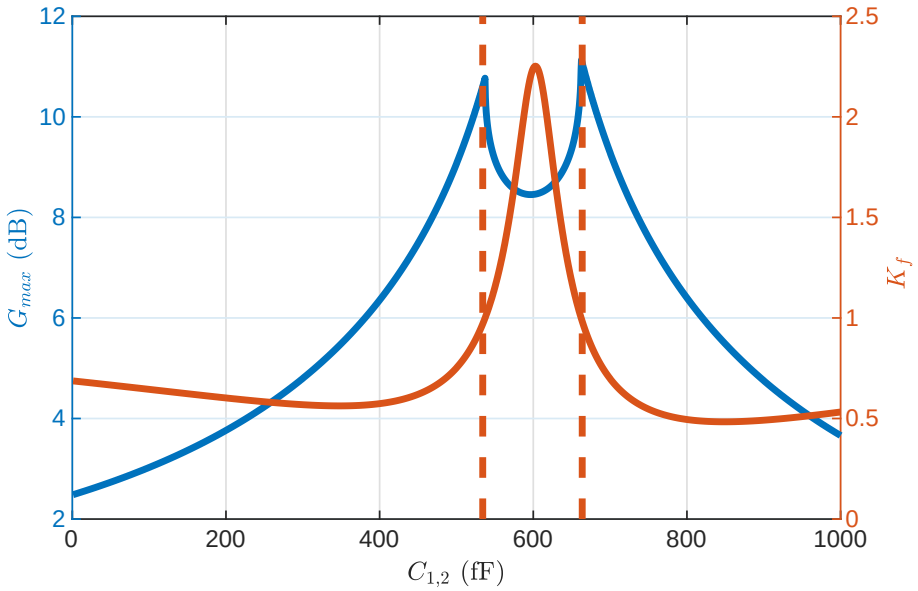


Figure 6.13: Differential pair (10 fingers) gain and stability over cross-coupled capacitance.

differential power amplifier is designed as shown in Fig. 6.14. First, the output of the second stage is load-matched to 600 Ω. For the biasing purpose, the inputs are provided with $V_G = 2.5V$ via ideal large inductors. The first stage's output and the second stage's input are connected using an inductive-capacitive-inductive π-matching network. The elements are kept at large values at this point. Next, the output of the first stage is matched to $600\,\Omega$ as well, with the π-matching network connected to the input of the second stage. This matching topology helps in simultaneous load matching of the first stage, AC-coupling between the stages and biasing of the second stage. At last, the input of the first stage is matched to a differential $100\,\Omega$ impedance at 500 MHz with an L-matching network.

The resultant S_{21} is shown in Fig. 6.15a. As seen here, the resonant frequency of the PA is

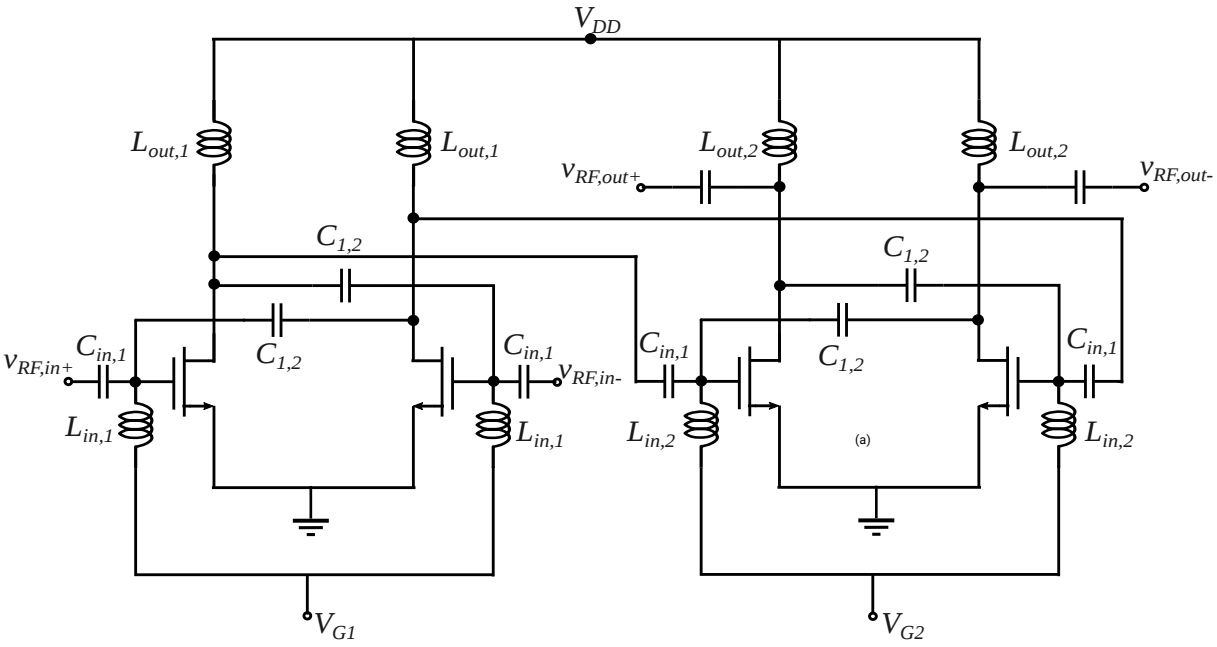


Figure 6.14: Schematic of the power amplifier.

precisely 500 MHz. The 3 dB small signal bandwidth of the device is around 20 MHz. The peak S_{21} is around $10.5\,\mathrm{dB}$ under impedance matching. The stability factors K_f of the matched power amplifier are shown in Fig. 6.15b. The differential mode is inherently unconditionally stable, as highlighted by the dashed curve since $K_f > 1$. The common mode is inherently unstable. We could improve the common-mode stability by implementing a $50\,\Omega$ resistance at the common-mode gate terminals.

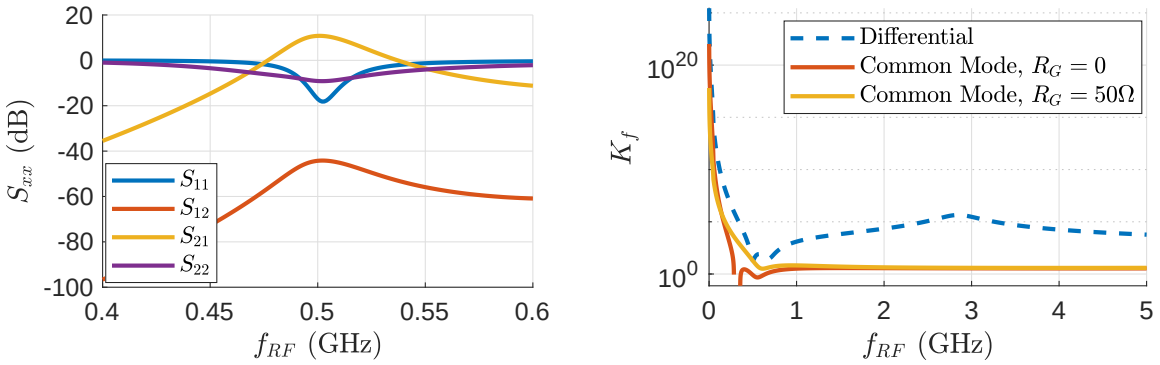


Figure 6.15: (a) Small signal $S-$ parameter of the two-stage PA after matching, (b) differential and common-mode stability factors of the PA.

Based on this, the power amplifier is now simulated with harmonic balance simulation sweeping the input power. The resultant output is shown in Fig. 6.16a. As seen here, the saturated output power is $10\,\mathrm{dBm}$. The high number of fingers helps achieve early compression, which is necessary to amplify the attenuated output power of the oscillator by the modulator and the buffer. The maximum transducer gain of the device is around $10.8\,\mathrm{dB}$. The gain curve follows

Table 6.1: Matching elements' values for the power amplifier designed with the high-speed TFT model.

Stage	Parameter	Value	muRata [88]
1st	$C_{in,1}$	405 fF	
1st	$L_{in,1}$	34 nH	LQW2BAN33NG000
1st	$L_{out,1}$	28 nH	LQW2BAN30NG00
Coupling	$C_{1,2}$	760 fF	
2nd	$L_{in,2}$	27 nH	LQW2BAN27NJ00
2nd	$L_{out,2}$	30 nH	LQW2BAN30NG00
2nd	$C_{out,2}$	2.35 pF	

typical class-A behavior. The input 1-dB compression point is at $-5\,\mathrm{dBm}$.

The output power over frequency for different input powers is plotted in Fig. 6.16b. The 3-dB bandwidth at linear range ($P_{in} = -18\,\mathrm{dBm}$) is around $25\,\mathrm{MHz}$. The bandwidth increases as the PA operation goes towards compression. At $P_{in} = 0\,\mathrm{dBm}$, the bandwidth increases to $29\,\mathrm{GHz}$. At full compression $P_{in} = 7\,\mathrm{dBm}$, the bandwidth increases to around $45\,\mathrm{GHz}$.

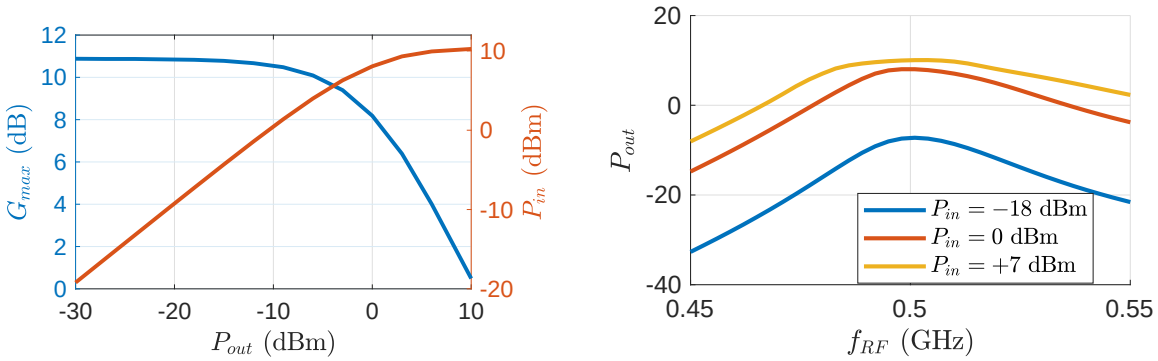


Figure 6.16: Harmonic balance simulation showing (a) transducer gain and output power of the PA over input power, (b) bandwidth of the PA at different input power.

The simulated values of the matching devices are mentioned in Table 6.1. The values are further verified using the S-parameter of high-Q SMD inductors (LQBAN- series) from Murata Manufacturing Co. Ltd. [88]. Due to unavailability, a few inductors' values had to be changed. The new inductor values are provided in column 4 of the Table 6.1.

At an input power of $-12\,\mathrm{dBm}$, the PA outputs around $-2\,\mathrm{dBm}$ power.

6.2.4 Doubler

The 500 MHz signals from the power amplifier's output are converted to $1\,\mathrm{GHz}$ using a common-gate doubler. The doubler works on the principle of resistive self-mixing [42]. The performance of a doubler of the same architecture has already been demonstrated in Chapter 4. In 4.8, it was shown with simulation that applying impedance matching at the doubler can provide a conversion gain as high as $-11\,\mathrm{dB}$. Fig. 6.17 shows the doubler configuration and the

Table 6.2: Matching elements' values for the doubler with high-speed TFT model.

Stage	Element	Value	muRata [88]
Input	C_{in}	800 fF	895 fF
Input	L_{in}	85 nH	LQW2BAN82NJ00
Output	C_{out}	540 fF	520 fF
Output	L_{out}	31 nH	LQW2BAN30NG00

input and output matching network. The high-speed TFTs presented in this chapter can exceed the previous doubler's efficiency.

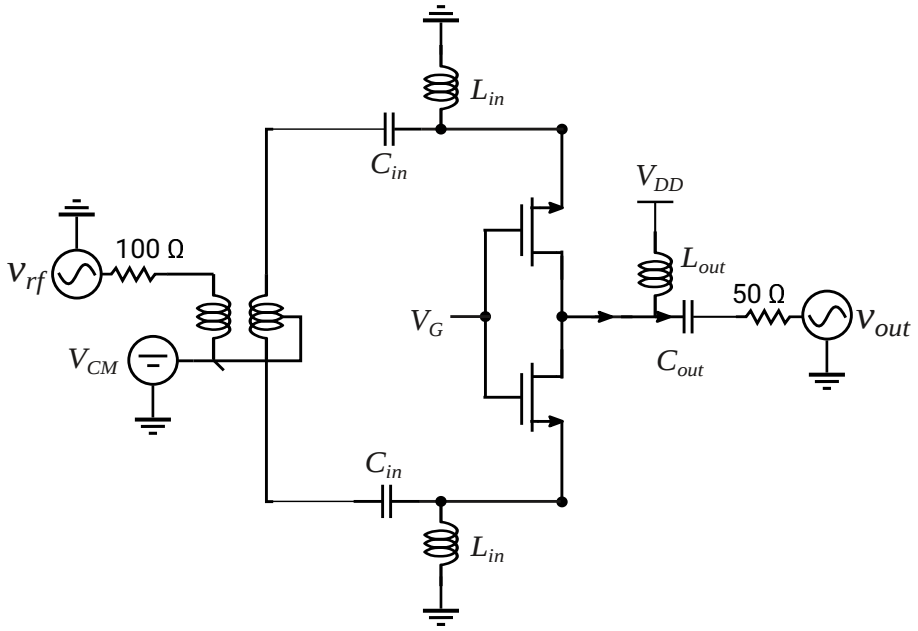


Figure 6.17: Schematic of the common-gate frequency doubler.

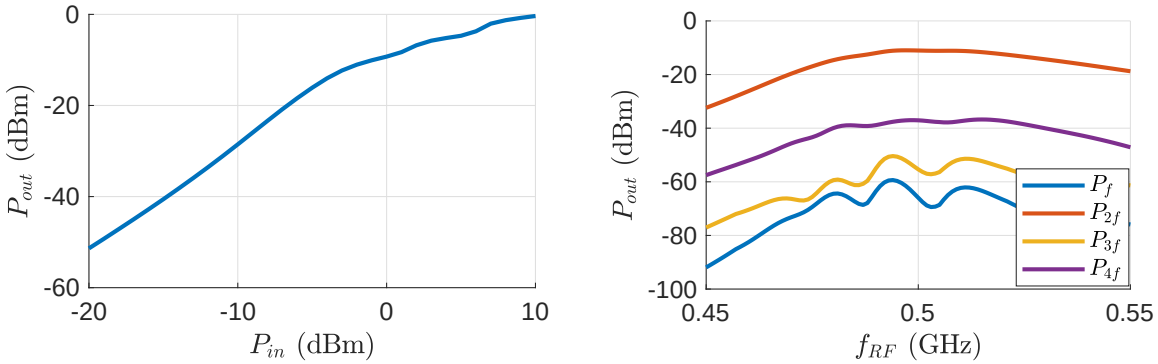
A large signal harmonic-balance-s-parameter (HBSP) simulation is carried out in Spectre for the doubler impedance simulation and matching. The input power from the PA is kept at $-2\,\mathrm{dBm}$.

The input port of the doubler is matched to $100\,\Omega$ by applying L_{in} and C_{in} as described in Table. 6.2.

The output of the doubler is load-matched to a $50\,\Omega$ port. It is observed that the higher the load resistance, the higher will be the output power. The load is matched to a $300\,\Omega$.

The second harmonic output power versus the input power is shown in Fig. 6.18a. The doubler achieves compression at around $-2\,\mathrm{dBm}$ input first harmonic power. The compression is soft due to the amorphous nature of the TFTs. The output power at this point is around $-11\,\mathrm{dBm}$, implying a conversion gain of around $-9\,\mathrm{dB}$.

At $-2\,\mathrm{dBm}$ input power, the frequency at the input is swept in HB analysis. As seen in Fig. 6.18b, the 3-dB bandwidth is around $48\,\mathrm{MHz}$ from 481–$529\,\mathrm{MHz}$. The isolation between the second and fourth harmonic is around $26\,\mathrm{dB}$. Moreover, the first harmonic output power is



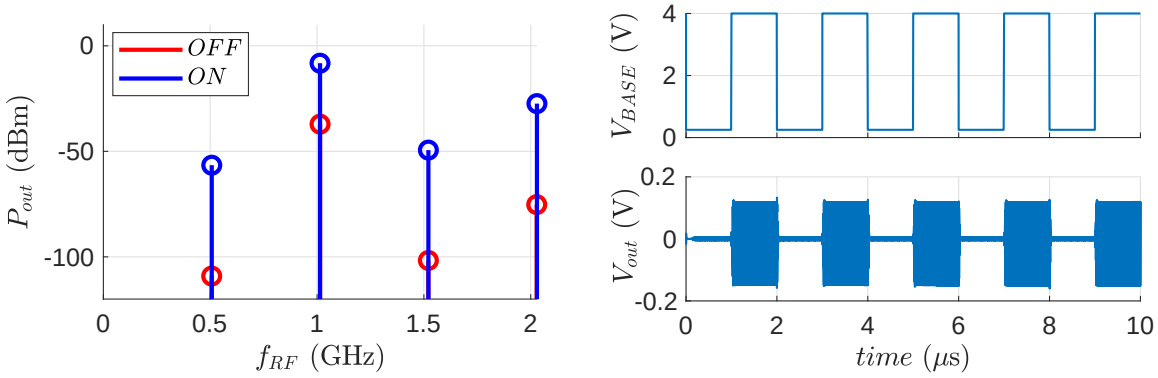
(a) **(b)**

Figure 6.18: HB analysis results of doubler showing (a) output power vs. input power and (b) output harmonic power over frequency.

around $-60\,\mathrm{dBm}$. The first harmonic power matches the output described in Chapter 4 under no threshold voltage mismatch.

6.2.5 Simulation of transmission power

An HB simulation of the completer transmitter is shown in Fig. 6.19a. When the baseband signal is ”1”, the output power is around $-9\,\mathrm{dBm}$. When the baseband signal is ”0”, the transmitter emits a $-43\,\mathrm{dBm}$ output power. A transient simulation is also done by switching the baseband signal between $4\,\mathrm{V}$ for ”1” and $0.25\,\mathrm{V}$ for ”0”. This results in a peak ON voltage of $119\,\mathrm{mV}$ and a peak off voltage of $5\,\mathrm{mV}$.



(a) **(b)**

Figure 6.19: Baseband voltage and transmitter output voltage.

6.3 Architecture of the OOK receiver

The receiver chosen here is of heterodyne architecture. The noise behavior of the TFTs limits the condition of the receiver. As mentioned in [42], the NEP of a square-law detector is 30nW/$\sqrt{Hz}$. According to the link budget calculation, a transceiver operating at 1 GHz over a distance of 1m needs 100pW/$\sqrt{Hz}$ when the transmitted power is -12 dBm. Hence, a simple detector with a matching network will not be able to communicate with the specified range and frequency. The receiver architecture is shown in Fig. 6.20. The LO-generated signal at 1 GHz is mixed with the RF signal from the antenna. The mixer generates the baseband signal, which is then filtered by the baseband buffer (BB Buffer). The buffered signal is then amplified before being delivered to an amplifier. The amplified baseband signal is observed in an oscilloscope.

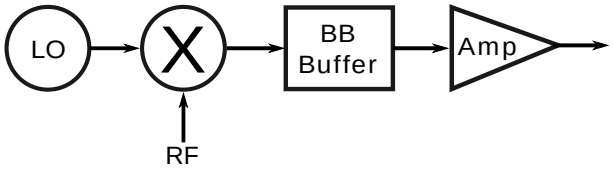


Figure 6.20: Architecture of the heterodyne receiver.

6.3.1 Local oscillator

Same as described in the section 6.2.1.

6.3.2 Mixer

The mixer consists of a single TFT (T_1) used in the saturation region, which is the most straightforward architecture. It mixes the LO and RF signals from the antenna to generate the baseband signal. The LO signal switches the mixer at the gate on and off. The RF signal is fed from the source terminal of the TFT. The mixer topology and the test bench are used, as shown in Fig. 6.21. The gate and sources are matched to the ports with the help of the two LC matching networks (L_{LO}, C_{LO}) and (L_{RF}, C_{RF}), respectively. Both the LO and RF ports have internal series resistances of $50\,\Omega$ to simulate the LO and antenna input. The gate and source voltages mix to create an intermediate frequency (IF) current that flows through the channel. This current is converted to voltage using a simple resistor R_{BB}. The resistor is chosen instead of a trans-impedance amplifier. As the open loop gain of the TFTs is not large enough, an op-amp based on a-IGZO cannot provide a high gain for a feedback amplifier.

HBSP analysis is done to simulate the RF to IF forward path loss $S_{\mathrm{IF/RF}}$ and isolation between LO and RF $S_{\mathrm{LO/RF}}$, as shown in Fig. 6.22. The mixer shows a conversion loss of $-15\,\mathrm{dB}$ for an R_{BB} of $100\,\mathrm{k}\Omega$. The isolation between LO and RF is small, almost $6\,\mathrm{dB}$. This LO to RF feedthrough is expected from a single-ended mixer. The forward gain from LO to IF, $S_{\mathrm{IF/LO}}$, is $6\,\mathrm{dB}$ lower than $S_{\mathrm{IF/RF}}$. However, as LO is at the GHz range and the IF is only in the MHz range, we can easily filter out the unwanted signal with a low order low pass filter.

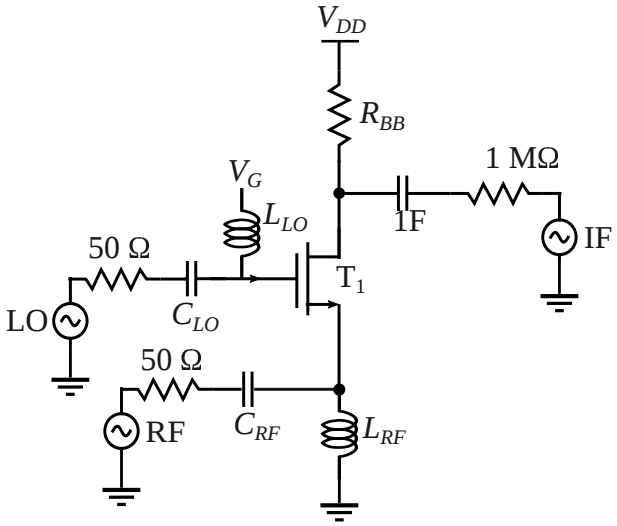


Figure 6.21: Schematic of a single-ended single-switch mixer.

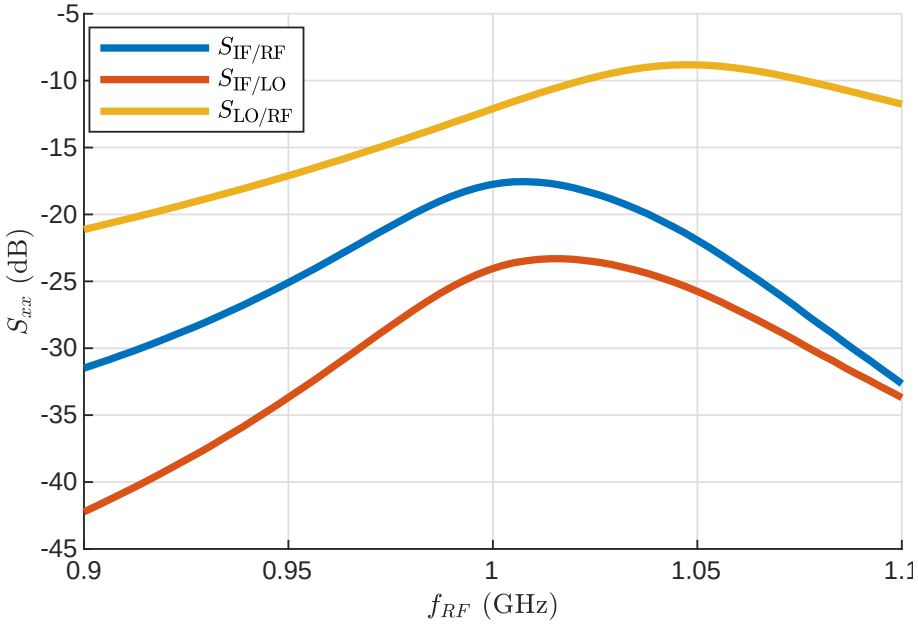


Figure 6.22: Conversion gains between IF, RF and LO of the mixer.

6.3.3 Load resistance and noise figure

The load resistance R_{BB} controls the mixer conversion gain and the noise figure. The value of the resistance defines the bias point of the TFT for the minimum noise figure.

For NF simulation, the shot noise and thermal noise of the TFTs are implemented as parallel current sources around the TFT. The total noise current PSD is given by

$$i_n^2 = 2qI_D + 4kTg_m, \tag{6.5}$$

where the first term on the right-hand side corresponds to shot noise, and the second term

corresponds to thermal noise.

A Verilog-A noise current source connected to the TFT model can extract the g_m and I_D to implement the noise current.

A parametric sweep in the HB simulation and the HBSP simulation reveals the NF dependency on the R_{BB}. As seen in Fig. 6.23, the minimum NF is seen at an R_{BB} of $100\,\mathrm{k\Omega}$.

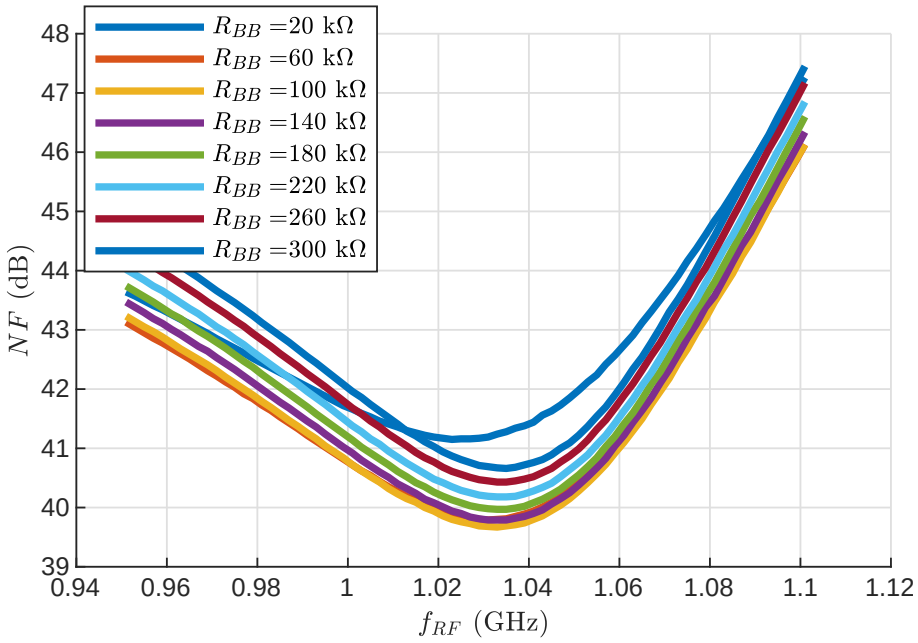


Figure 6.23: NF of the single FET mixer over radio frequency for different load resistance values.

6.3.4 Baseband amplification

The generated BB output voltage v_{IF} is then put through a buffer stage. The buffer consists of a source follower TFT (T_2), as depicted in Fig. 6.24. The input terminal of the buffer is biased by the mixer output itself, eliminating the need for a bias network. This strategy eliminates the need for capacitance at the output of the mixer. Hence, the IF bandwidth is not affected. A common-gate TFT (T_3) is connected to the source terminal to control the bias current through the follower. The length of (T_3) is chosen so that the output resistance of the channel is maximum. The biasing of T_3 is done using a V_{load} applied at the gate of the buffer load TFT T_3. Fig. 6.25a shows the DC output voltage V_{BB}, the gate-source voltage of T_2 $V_{GS,2}$ and the drain-gate voltage of T_3 $V_{DG,3}$ over V_{LOAD}. If V_{LOAD} goes above $1.4\,\mathrm{V}$, the load transistor T_3 comes out of the saturation region (considering $V_{th} = 0\,\mathrm{V}$), thereby not acting like a suitable current source. If V_{LOAD} is too low, then T_2 has low $V_{GS,2}$.

As seen in Fig. 6.25b, $A_V \approx -0.5\,\mathrm{dB}$ at lower V_{LOAD}. Nevertheless, for low V_{LOAD}, the TFT T_3 cannot be in deep saturation. Hence, an optimal V_{LOAD} of $1\,\mathrm{V}$ is chosen, where $V_{BB} = 1.7\mathrm{V}$ and $A_V = -2\,\mathrm{dB}$.

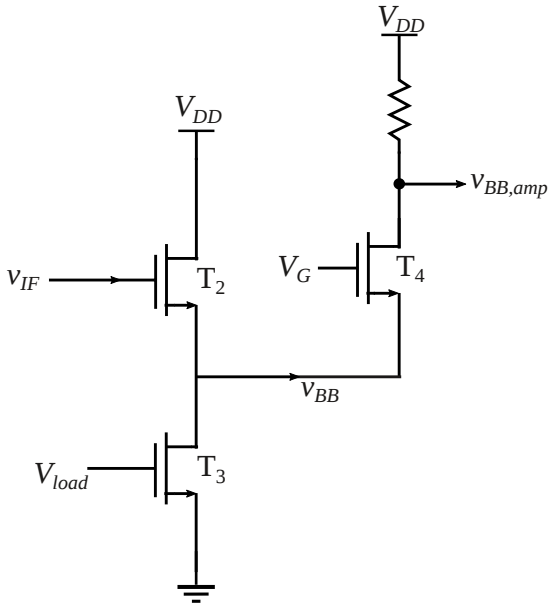


Figure 6.24: Schematic of the buffer and baseband amplifier.

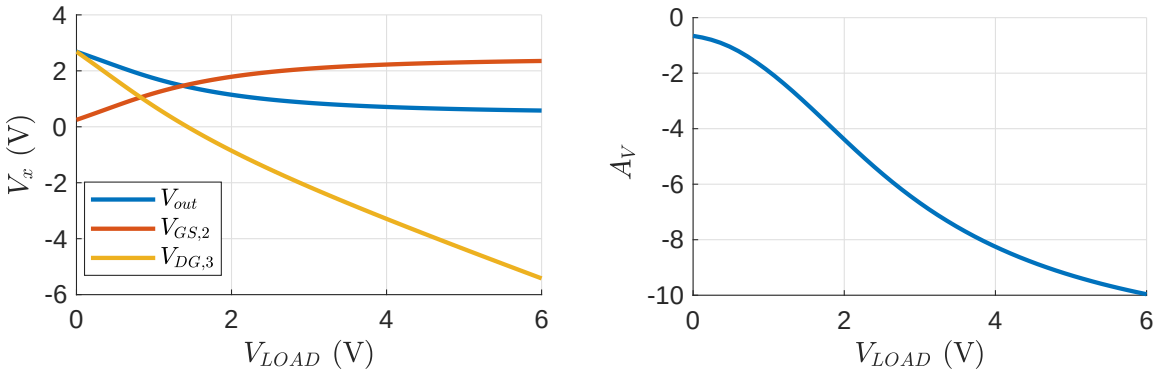


Figure 6.25: (a) DC node voltages versus the gate bias voltage of the load transistor, (b) AC simulation of buffer gain over the load transistor's gate bias voltage.

The BB amplifier is connected directly to the output of the buffer. The amplifier is a basic TFT T_4 with a resistive load. The BB signal from the buffer is fed through the source terminal, while the gate is biased with a controlled DC voltage. The absence of Miller capacitance in the chosen architecture provides high bandwidth for the amplifier. Moreover, by applying the biasing at the gate and the baseband signal at the source, we can keep the gate voltage above $0\,\mathrm{V}$. Simulation shows that the gate bias must be higher than the source bias by $400\,\mathrm{mV}$ for maximum gain.

The resistive load of the amplifier is chosen with AC simulation in Cadence Spectre. For a $100\,\mu\mathrm{m}$ wide TFT, the resistive load that gives the maximum gain is 100 kΩ. The open loop gain magnitude and the amplifier's phase are shown in Fig. 6.26. As seen, the amplifier delivers a maximum voltage gain of 11 dB. From the phase curve, the first pole appears at 41 MHz, way above the baseband frequency of $1\,\mathrm{MHz}$. From the open loop gain, we can conclude that the device would not be suitable for a closed loop system as the error signal would be very high,

which could impact the system's stability.

The overall gain of the buffer and the amplifier is shown in Fig. 6.26. Here, the circuit has a voltage gain of around 7.5 dB and a bandwidth of 10 MHz. The buffer stage limits both the gain and the bandwidth.

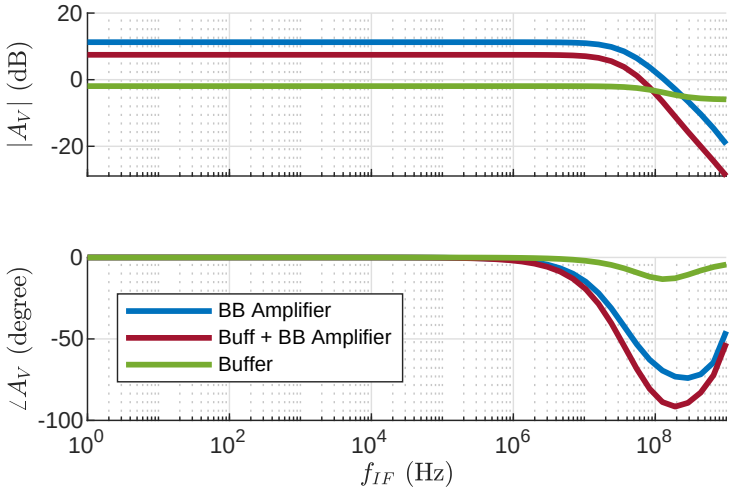


Figure 6.26: Bode plot of the buffer, amplifier and buffer and amplifier together.

6.3.5 Simulation of the receiver

A transient simulation of the device is done with a similar local oscillator as in input and RF input power of $-45\,\mathrm{dBm}$. The different transient voltage signals are shown in Fig. 6.27. As seen here, the peak-to-peak voltage at the output of the amplifier is $117\,\mathrm{mV}$. We can calculate the responsivity of the complete receiver from the simulation. The input RF power P_{in} equals $-45\,\mathrm{dBm}$ on a matched input impedance of $50\,\Omega$. The output RMS voltage is around $41\,\mathrm{mV}$, which leads to a responsivity of around $1.3\,\mathrm{MV/W}$.

A noise analysis of the heterodyne receiver is done. The noise over frequency at the output node of the receiver is shown in Fig. 6.28a. The noise voltage at $500\,\mathrm{kHz}$ is around $207\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. According to the simulation, the highest noise contribution is from the shot noise of the mixer TFT T_1, which contributes to 60% of the noise, while the shot noise of the BB amplifier TFT T_4 contributes to around 17% of the noise.

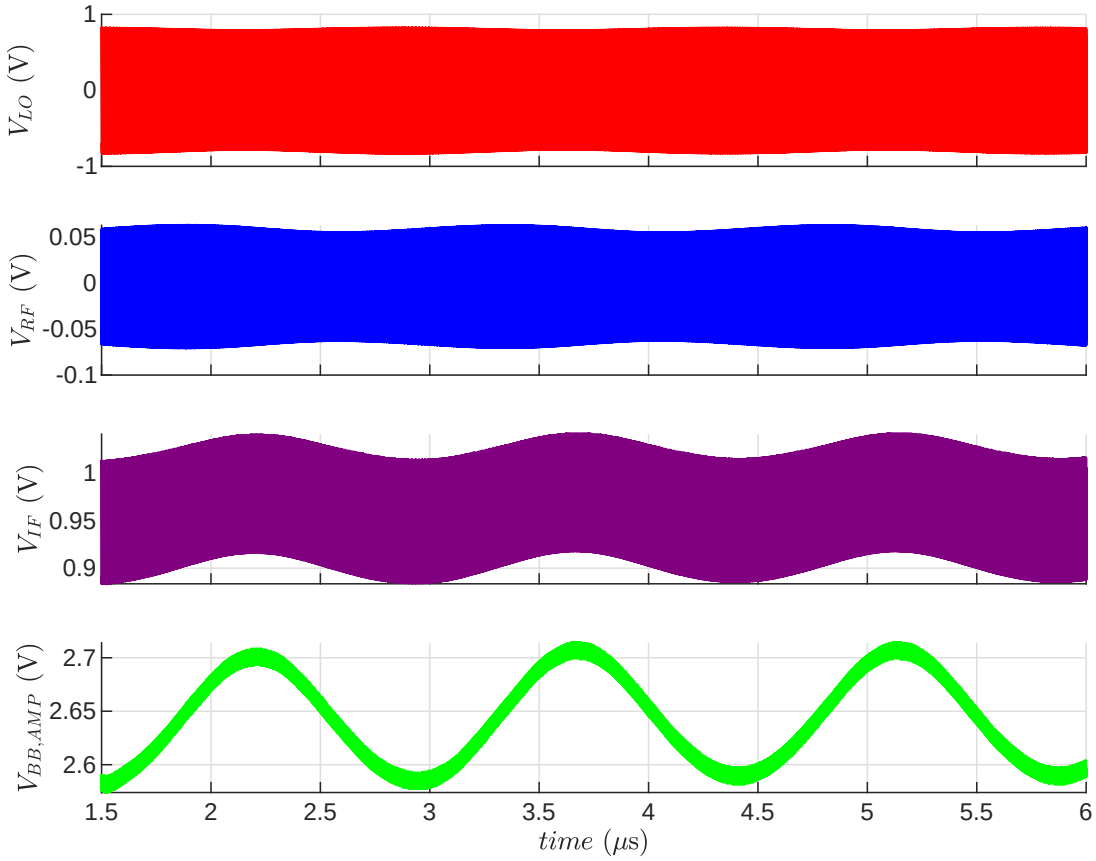


Figure 6.27: Voltage input and output of the heterodyne receiver.

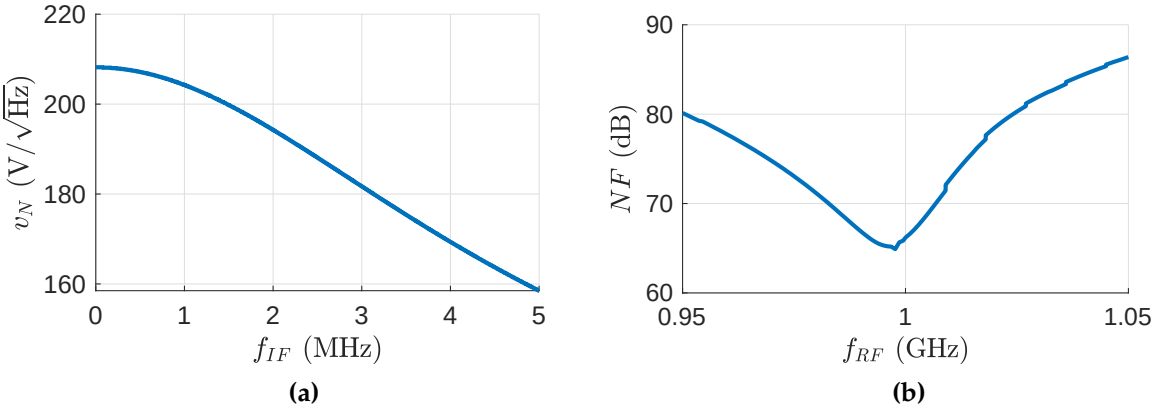


Figure 6.28: (a) Noise voltage over IF at the receiver output and (b) NF of the receiver over RF.

A noise voltage of $207\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ over a responsivity of $1.3\,\mathrm{MV/W}$ results in an NEP of around $0.160\,\mathrm{pW}/\sqrt{\mathrm{Hz}}$.

An HBSP simulation of the completer receiver, including the oscillator and the doubler, shows an NF of around $66\,\mathrm{dB}$, as depicted in Fig. 6.28b.

The sensitivity of the receiver S_{Rx} can be calculated from the NF of the receiver, according to [89]

$$S_{Rx} = (10 * log10(kTB) + 30) + NF + SNR_{OOK}, \tag{6.6}$$

where k is the Boltzmann Constant, T is the temperature, B is the channel bandwidth and SNR_{OOK} is the signal-to-noise ratio for the OOK receiver for a given bit error rate. Thus, for a $500\,\mathrm{kHz}$ channel bandwidth, and SNR_{OOK} of $7\,\mathrm{dB}$ (according to Fig. 6.28, the receiver sensitivity is calculated to be $-43.74\,\mathrm{dBm}$. Thus, a minimum received power of $-43.74\,\mathrm{dBm}$ can be detected for the NRZ-OOK modulation.

6.4 Layout of the transceiver

The layout has two metal layers, as shown in Fig. 6.28. The layout compensates for the process

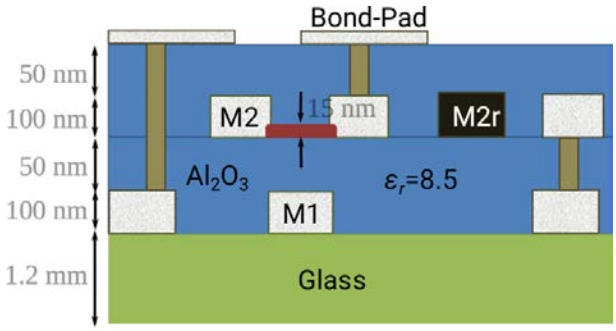


Figure 6.29: Layer Stack in the a-IGZO technology. M1 is metal layer 1, M2 means metal layer 2 and M2r is a metal layer with high sheet resistance. The dimensions are not matched to the scale.

variations and drifts in the TFTs and circuits. The salient features of the layout are as follows:

- . The inductors will be soldered on PCBs and connected to the chip with bond wires.
- There are bonding pad openings on the interconnects, and gold is deposited for wire bonding.
- Both branches of the differential circuits have separate bias sources. The separation of biases accounts for any mismatch between the two branches.
- A few resistors will be implemented externally to account for the modeling error.
- The matching capacitors are implemented as multi-finger for post-fabrication adjustment if required.

- For the power amplifier layout, the cross-coupled capacitances are implemented with two different metal layers and vias connected at TFT terminals.

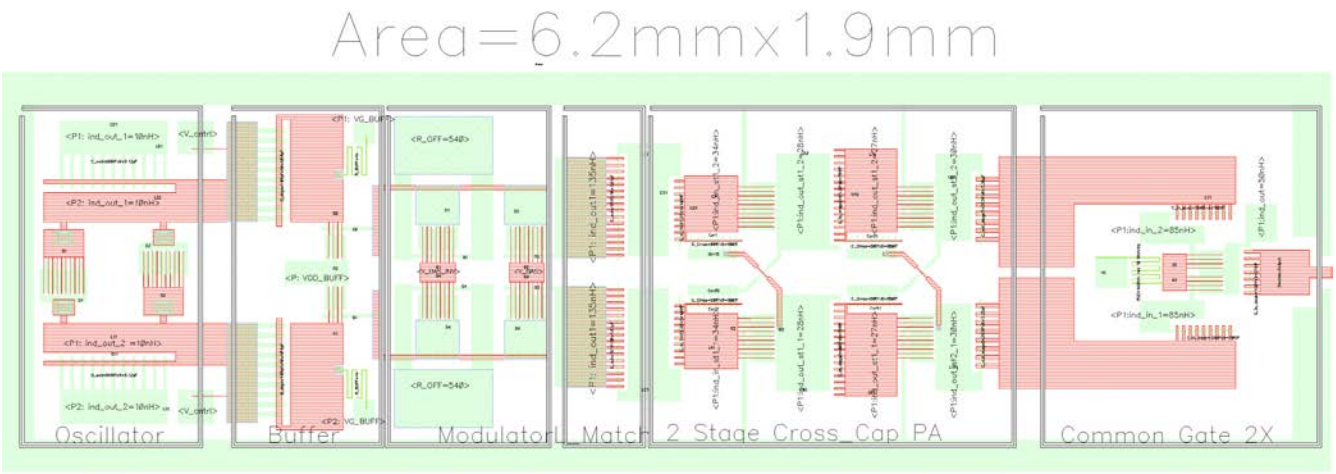


Figure 6.30: The transmitter layout consisting of oscillator, buffer, modulator, a matching network, power amplifier and a common-gate doubler.

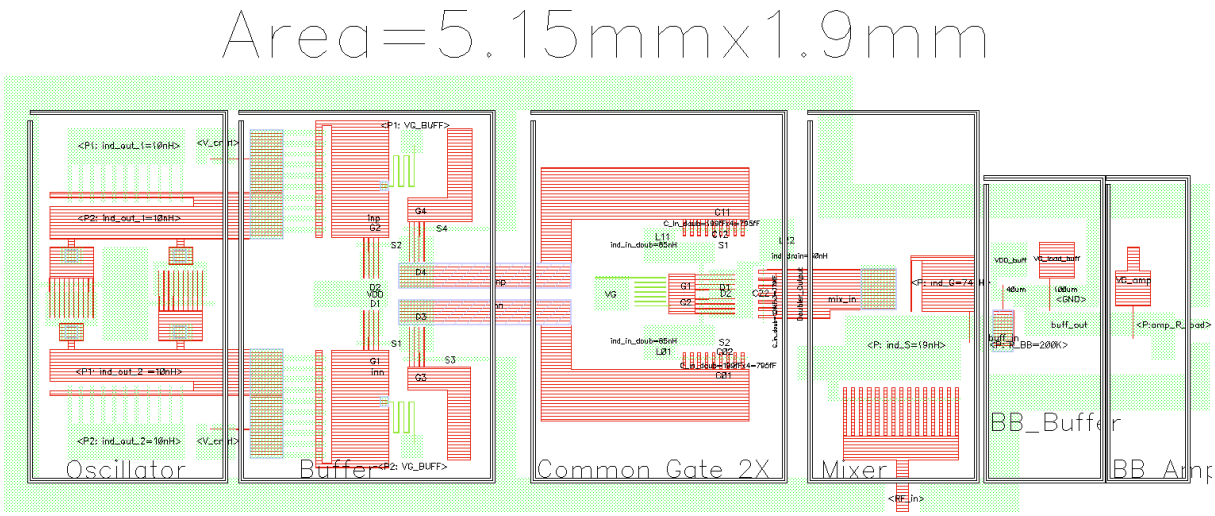


Figure 6.31: The receiver layout consisting of an oscillator, buffer, doubler, mixer, baseband buffer and baseband amplifier.

6.5 Fabrication yield problem

The complete GHz transceiver could not be successfully implemented owing to low fabrication yield. As mentioned at the beginning of this chapter, a Ti/Au/Ti composite material is needed for the gate electrodes of the transceiver for GHz systems. However, it has been observed post-fabrication that the complete circuit yield is zero. Fig. 6.32 shows the microscope photo of the fabricated transmitter with red circles showing its active area. None of the active devices were functional. The gate and channel definitions were not sharp. All the TFTs showed at least one broken finger.

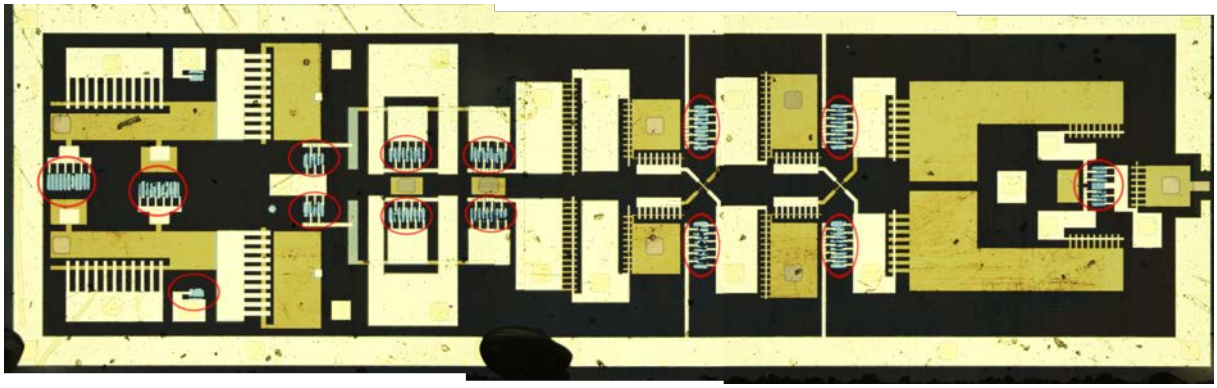


Figure 6.32: Photo of a fabricated GHz transmitter under microscope; the circular markers show the broken active area.

6.5.1 Dependency on gate material

The bottom gate material is deposited by sputtering. The positive photoresist is applied on the glass substrate. Then, a high-resolution mask is used to apply the UV light, and after the development of the resist, the Cr is sputtered on top. Finally, the lift-off process in acetone and N-Methylpyrrolidone (NMP) is performed to remove the remaining resist and the unwanted metal parts.

The gate electrode is then used as a mask for the lithographic lift-off structuring of the drain-source electrode [42]. It has been observed from repeated fabrication processes that the Cr-gate provides the sharpest edges for the lift-off procedure during UV exposure. As a result, the yield is higher when Cr is used as a gate electrode than the Ti/Au/Ti or Al/Cr, which also has a sheet resistance of $0.4\,\Omega/\square$, as reported in [36].

6.5.2 Dependency on architecture

As the number of fingers in a TFT increases, the possibility of shorted drain-source contact increases. For a differential device with multiple fingers at each transistor, this significantly increases the chance of device mismatch. The multi-finger, although necessary for power generation, exhibits a lower yield.

6.5.3 Dependency on dielectric

The high k-dielectric Al_2O_3 is grown using trimethylaluminum (TMA) as a precursor and ozone as an oxidizing agent [90]. The "layer" of TMA is deposited due to the self-limitation of the ALD process. After pulsing TMA into the reactor, the reactor is purged with dinitrogen (N_2) so that a monolayer of TMA remains on the surface. Then, the oxidant (ozone) is pulsed into the reactor to form Al_2O_3. Afterward, the reactor is purged again to remove the excess ozone and methane from the reaction with TMA. The process is repeated layer by layer until the desired Al_2O_3 thickness is achieved. A faulty valve can lead to the presence of water molecules in the dielectric. A source of water, such as residuals in tubes, leakage at the surface of the chamber, or impurities in the gases, can cause parasitic growth during the ALD process since water also reacts well with the TMA. This growth can lead to a negative threshold voltage offset in the TFT. Moreover, the presence of water reduces the adhesion among the dielectric layers. Applying a high voltage can cause the dielectric to burst, breaking the device down. This phenomenon has been observed in the new TFTs.

6.5.4 Dependency on encapsulation

A similar ALD procedure is also used to grow the Al_2O_3 encapsulation layer. A lack or faulty encapsulation usually causes a negative V_{th}. This has also been observed in the new TFTs. Water or hydrogen can interact with the surface of the IGZO which may cause the negative shift of V_{th}.

The multi-finger doublers presented in the last chapter suffered from this drift phenomenon. When the devices were measured after two months, the V_{th} went from around $-1\,\mathrm{V}$ to around $-10\,\mathrm{V}$. The TFTs stopped behaving as transistors and the frequency doubling could not be reproduced.

6.6 Conclusion of the system design

In this chapter, we have done the simulation and layout of a $1\,\mathrm{GHz}$ transceiver based on our highest speed TFTs with $f_{max} = 1.5\,\mathrm{GHz}$. These TFTs were published in [37].

We simulated the model and layout in Cadence with a SPICE level 61 model library file. The model is similar to the RPI-a model described in Chapter 3.

A transmitter consisting of a $500\,\mathrm{MHz}$ cross-coupled oscillator is designed to create an output power of around $4\,\mathrm{dBm}$ at a load of $8\,\mathrm{k\Omega}$. The oscillator, in conjunction with a buffer and an OOK modulator, generates an output power of around $-12.5\,\mathrm{dBm}$ when the baseband signal is "1". A two-stage differential power amplifier is designed to provide around $10\,\mathrm{dB}$ transducer gain at $500\,\mathrm{MHz}$ to the modulated signal. The frequency doubler follows the power amplifier to generate a $1\,\mathrm{GHz}$ output with an output power of around $-9\,\mathrm{dBm}$ when the baseband is "1". The transmitted power is $-43\,\mathrm{dBm}$ when the transmitted bit is "0". In terms of voltage, on a $50\,\Omega$ load, the ON voltage peaks at around $119\,\mathrm{mV}$. The OFF voltage peaks at around $5\,\mathrm{mV}$.

Thus, the transmitter can generate an OOK-modulated signal with an ON-OFF ratio of around 24 for a $500\,\mathrm{kHz}$ baseband signal at a carrier frequency of $1\,\mathrm{GHz}$.

A $1\,\mathrm{GHz}$ receiver has also been designed based on a single-ended mixer consisting of a single TFT. The source terminal of the TFT receives the RF signal from an antenna. The gate terminal is excited by the LO. The IF signal is extracted from the drain and fed to a source-follower buffer and a common-gate baseband amplifier. The mixer has a conversion loss of around $-17\,\mathrm{dB}$ from RF to IF. A single-ended mixer is always susceptible to poor isolation. An HBSP simulation shows an RF to LO isolation of only around $-8\,\mathrm{dB}$. There is also LO to IF feedthrough with a gain of $-22\,\mathrm{dB}$. The baseband buffer at the IF output has a bandwidth of $18\,\mathrm{MHz}$. The baseband amplifier is of a common-gate configuration, which provides a large bandwidth of $40\,\mathrm{MHz}$ and $11\,\mathrm{dB}$ open loop voltage gain. The combined open loop gain of the buffer and amplifier is around $7.5\,\mathrm{dB}$ with a gain of $25\,\mathrm{MHz}$. The complete receiver simulation shows a peak-to-peak voltage of $115\,\mathrm{mV}$ at $1\,\mathrm{M\Omega}$ load for a baseband frequency of $615\,\mathrm{kHz}$ (based on LO generation). The RF input power is $-45\,\mathrm{dBm}$. This results in a responsivity of around $1.3\,\mathrm{MV/W}$. The receiver's sensitivity is around $-43\,\mathrm{dBm}$.

Considering the $-32.44\,\mathrm{dB}$ path loss at $1\,\mathrm{GHz}$ for the $1\,\mathrm{m}$ range and a transmitter output power of $-9\,\mathrm{dBm}$, we have received a power of $-41\,\mathrm{dBm}$ without considering any antenna loss and bandpass filter. Thus, given accurate local oscillators, theoretically, a heterodyne receiver can communicate with a transmitter based on Ti/Au/Ti gate electrode-based a-IGZO TFTs.

The successful realization of the communication system was hindered by a defective active area, which was observed in Figure 6.32 after fabrication. Therefore, it is imperative to enhance the device yield to ensure the operational effectiveness of the communication system.

Chapter 7

Conclusion and Outlook

In this thesis, we aimed to develop the world's first a-IGZO-based transceiver frontend that can operate in the GHz frequency range. The prerequisites were feasibility analysis, speed, power generation capability improvement, and knowledge of the breakdown voltages.

The a-IGZO TFTs are the basic building blocks for all GHz circuits. Hence, we have first improved the TFT technology itself. We require power amplifiers for power conversion from DC to RF, which can operate typically at $1/3$ of the maximum oscillation frequency f_{max}. The f_{max} depends on the transit frequency and the gate electrode resistance. We have reduced the gate resistance by using low-resistive Ti/Au/Ti as electrode material and reducing the device width. A record f_{max} of $3.1\,\mathrm{GHz}$ was achieved for a $50\,\mu\mathrm{m}/0.8\,\mu\mathrm{m}$ TFT with Ti/Au/Ti gate electrode [37].

The high-speed TFTs are then modeled from their measured DC and RF characteristics. For DC analysis, the RPI-a TFT model is chosen. This model suits amorphous TFTs, where the transition between the triode and saturation region is not sharp [57]. We adopt the null-bias technique for RF modeling to extract the extrinsic resistances and capacitances [63]. The de-embedding of these extrinsic elements then helps us extract the intrinsic components.

The extracted values are used to model the TFTs in Cadence. This model can be implemented as a Verilog-A code or a model library file. The Verilog-A code gives us better control of the intrinsic and extrinsic parameters. Moreover, the non-quasi-static transit delay can also be implemented using Verilog-A.

Using the model above, we have designed and characterized a multi-finger doubler. A multi-finger geometry can increase the power handling capability of a TFT without affecting its f_{max} compared to a single-finger transistor.

The doubler was implemented with high-resistive Cr-gate TFTs due to fabrication limitations. Moreover, due to possible impurities in the material, the TFTs could not handle more than $8\,\mathrm{dBm}$ output power.

We could also verify the presence of impurities from the low-frequency noise behavior of two a-IGZO TFTs produced around the same time. The presence of impurities causes generation-recombination (g-r) noise at low frequencies. The g-r noise spectrum is inversely proportional to the frequency square [78]. The Cr-gate TFTs produced in 2022 showed this PSD-frequency relationship (please see section B.2.3).

Based on the behavior of the best f_{max} TFTs reported in [37], we have also simulated and fabricated a complete GHz transceiver. For that purpose, we have designed a process development kit for a-IGZO in Cadence, including a model, a library file for simulation, and a design rule file ("display.drf") for layout. We expected process variation, drift, and modeling error based on our experience. Hence, we did the layout with variable capacitors implemented as multi-fingers and external inductances to be implemented on external circuit boards. Moreover, to compensate for the asymmetry in any differential architecture, we have also implemented individual biases for each differential circuit.

However, we could not account for the yield issue. The low yield prevented us from fabricating the transceiver and many breakout circuits that employed Ti/Au/Ti-based multi-finger architecture.

7.0.1 Summary of results

As published in [37], we achieved a record maximum oscillation frequency of $3.1\,\mathrm{GHz}$ by scaling the TFTs and fabricating the gate with a low resistive Ti/Au/Ti electrode. We have also designed a $500\,\mathrm{MHz}$ to $1\,\mathrm{GHz}$ multi-finger doubler with a conversion gain of $-32\,\mathrm{dB}$. The doublers were based on TFTs with f_{max} of only $240\,\mathrm{MHz}$. It is the first doubler showing a frequency upconversion up to $1\,\mathrm{GHz}$. Our previous work in this field showed only a $-44\,\mathrm{dBV/dBV}$ conversion gain for doubling from $100\,\mathrm{MHz}$ to $200\,\mathrm{MHz}$, as shown in Table 7.1. We have improved both the conversion gain and the frequency of operation using the multi-finger technique and speed improvement. The doubler could receive up to $10\,\mathrm{dBm}$ input power before breaking down. The RF output power $-22\,\mathrm{dBm}$ is much less than the breakdown limit observed in Fig. 2.6b for previous Cr-gate TFTs. The presence of impurities is assumed to be the reason.

Table 7.1: Comparison of doubler with the state of the art. Reprinted, with permission, from [61], open access under creative common license CCBY-NC-ND.

Year	Circuit	TFT W/L (µm/µm)	f_T (MHz)	Frequency (MHz)	Conversion Gain	Ref
2018	Doubler	500/3	$60\,\mathrm{MHz}$	100×2	$-44\,\mathrm{dBV/dBV}$	[42]*
2022	Doubler	4× 100/0.8	$500\,\mathrm{MHz}$	500×2	$-32\,\mathrm{dB}$	This work

* is also part of this thesis

The performance of the doubler circuit as a detector is also presented. Compared to our previous detector published in [42], the new multi-finger provides a more than tenfold reduction in the noise equivalent power. This reduction in noise power is attributed to the increment in the W/L.

The increment in W/L reduces the channel resistance of the TFTs. Moreover, owing to lower gate spread resistance. The multi-finger structure detector shows a 1500-fold improvement in responsivity. A comparison of the multi-finger detector and the detector from [42] is presented in Table 7.2.

Table 7.2: Comparison of receiver with the state of the art

Year	Circuit	TFT W/L (µm/µm)	f_T (MHz)	Op. Freq. (MHz)	Responsivity (V/W)	NEP ($\mathrm{nW}/\sqrt{\mathrm{Hz}}$)	Ref
2015	AM receiver (active)	40/5 - 40/25	N.A.	20	15 dBV*		[32]
2018	Square-law detector	500/3	60	1000	2	30	[42]**
2022	Square-law detector	400/0.8	500	1000	685	1.6	This work

* is reported conversion gain,
** is also part of this thesis.

A complete $1\,\mathrm{GHz}$ OOK transceiver with all the building blocks is also designed and simulated. We did a simulation and layout of a ten-finger cross-coupled oscillator as a $500\,\mathrm{MHz}$ signal source. Compared to state-of-the-art, our simulation shows a peak-to-peak voltage swing of around $4\,\mathrm{V}$. However, the device could not be fabricated owing to low transistor yield.

Table 7.3: Comparison of simulated oscillator with the state of the art

Year	Technology	TFT W/L	f_{max} (GHz)	Frequency (GHz)	V_{p2p} (V)	Ref
2018	ZnO	4× 100/0.9	2.7	1.25	2.8	[36]
2022	a-IGZO	4× 100/0.8	1.8	0.5	≈ 4	Simulated

The transmitter simulation showed a $-9\,\mathrm{dBm}$ output power at $1\,\mathrm{GHz}$ for the ON signal in a unipolar NRZ OOK system. The ON/OFF ratio of the transmitted signal was $119\,\mathrm{mV}/5\,\mathrm{mV}$.

Two receiver architectures were studied. The direct detection using a square-law detector was studied using an eight-finger detector with four-finger in each TFT. The direct detection of an unmatched detector put a high output power demand (around $4\,\mathrm{dBm}$ for $1\,\mathrm{GHz}$ signal across a $1\,\mathrm{m}$ distance with $6\,\mathrm{dBi}$ antenna gain assumption) on the transmitted signal. This power margin could be improved by increasing the number of fingers, thereby increasing the second-order non-linearity. Also, impedance matching should be taken into account. A heterodyne architecture was also studied with the derived model for high-speed TFTs. The heterodyne architecture requires a sensitivity of $-43.7\,\mathrm{dBm}$ for a $512\,\mathrm{kHz}$ bandwidth signal. In this case, the basic thermal noise and shot noise model of the TFTs are assumed. The receiver sensitivity lies in the link-budget boundary, thus promising a $1\,\mathrm{m}$ OOK communication link at $1\,\mathrm{GHz}$ with the simulated transmitter.

7.0.2 Significance of the work

Large-area electronics for radio frequency design is a relatively new field. A-IGZO was invented in 2004; since then, this semiconductor technology has revolutionized display devices.

This thesis strives to improve the a-IGZO TFTs for radio frequency circuit design. We have addressed this issue by demonstrating frequency up-conversion (doubling) in the field of a-IGZO. We have demonstrated the advantages of multi-finger architecture and shown the capability of a-IGZO in the generation and detection of a $1\,\mathrm{GHz}$ radio signal.

The literature has yet to show the efficacy of multi-finger architecture in this technology. We designed our own a-IGZO TFT geometry with the lowest additional parasitics. The low parasitics have helped achieve different record results regarding device speed and circuit performance. The extensive modeling of the TFTs' DC and RF behavior for single and multi-finger architecture is also done for circuit designing. The scalable model helps us answer impedance matching and power gain questions.

We have also closely observed device breakdown behavior and the effect of impurities on breakdown and noise. Power dissipation is one of the most critical factors in power amplifier design. Although power dissipation is susceptible to drift, we have observed that our original a-IGZO TFTs have a critical DC power dissipation above $50\,\mathrm{mW/\mu m}$ based on a rough estimate of observed breakdown voltage and current during DC measurements.

7.0.3 Potentials for improvement

The following points need to be researched further in the future.

1. Power handling capability

   The power handling capability and power dissipation issue severely limited our research. In Fig. 2.6b, we have shown a coarse estimate of critical power per unit width. However, this estimate is only from DC observations and at different biasing conditions. Any research in terms of RF power dissipation still needs to be done. When a transistor is excited beyond its f_{max}, the internal channel capacitances charge and discharge rapidly. Hence, the transistor needs to handle a large amount of charge quickly beyond its transfer capacity, which causes higher power dissipation than at low frequencies. This could reduce the breakdown voltage. A more rigorous thermal analysis is required to see the effect of frequency on breakdown.

2. Modeling Error Reduction

   The model derived presented around 30% error in the simulated transit and maximum oscillation frequencies. The reason is assumed to be the failure of the adopted Meyer capacitance model. A more rigorous analysis must be done in order to increase the accuracy of the intrinsic capacitance modeling.

3. Threshold voltage dependency on supply

   The RPI-a model that we have extracted has a fixed threshold voltage. It does not consider the dependency of the threshold voltages on the drain-source voltage. At high drain-source voltage, the threshold voltage decreases. This dependency must also be considered to improve the simulation's accuracy.

4. Process variation among fingers

   In large-area multi-finger TFTs, there will be process variation among the fingers. Hence, all the channels will behave differently. We have modeled the multi-finger only by simple linear multiplication of conductances and capacitances of a single transistor. For higher frequency design, we must also develop a model of the coupling among the channels. Electromagnetic simulators like Ansys HFSS or Sonnet can be used for this purpose.

5. Bias stress

   We observed drifts in the threshold voltage of the TFT between two consecutive measurements. Further study on this drift and stress induced by high-frequency input, bias, temperature, or light must be done. Moreover, the stability of the semiconductor also needs to be further addressed. Jeon et al. have reported that one can improve the stability of the a-IGZO TFTs with the help of two-step thermal annealing [91]. The dependency of stability on fabrication steps must be addressed to achieve better design reliability.

6. Improvement in Yield

   A higher device yield is imperative for a functional communication system incorporating multi-finger transistors. More investigation into new composite materials with low resistivity that offers well-defined interface, good adhesion and mechanical strength can be beneficial.

7.0.4 Outlook

The next step in this thesis is to verify models in terms of impedance matching. We have shown in Chapter 4 that impedance matching can provide a conversion gain of around $-11\,\mathrm{dB}$ for the multi-finger Cr-gate doubler.

Another near-future application would be off-chip antenna integration into the detector and doubler circuits. The integration would demonstrate the true capability of the TFTs in communication technology. A real-time LoRA receiver operating at $902\text{–}928\,\mathrm{MHz}$ could easily be implemented with an a-IGZO detector, external antenna and bandpass filter.

The work presented in this thesis is one of the first attempts in the scientific community to enable a low-cost, room temperature-fabricated communication system operating at $1\,\mathrm{GHz}$. By improving the device yield, this technology could soon be used for radio frequency communication systems.

Appendix A

Distributed Model of Gate Electrode

A.1 RC ladder Gate electrode model

The bottom gate under the electrode overlaps the drain and source metals. The overlap capacitance in this case causes a dispersion effect on the input RF signal. A resistance-capacitance ladder network, as shown in Fig. A.1, presents the more accurate gate impedance model as presented in [92].

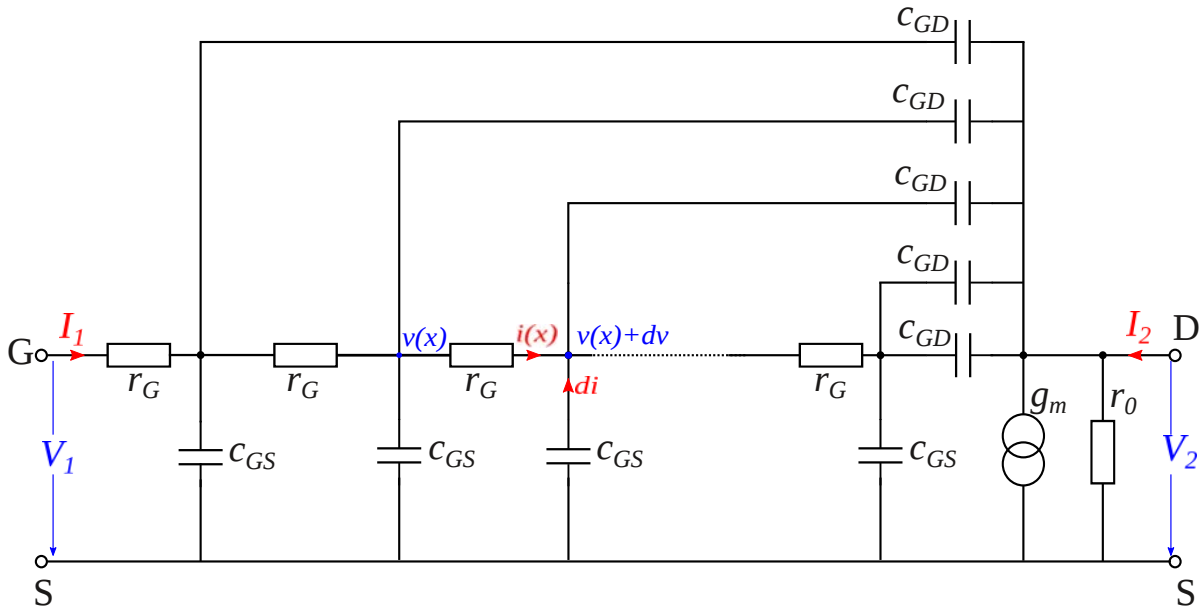


Figure A.1: Distributed gate resistance model [92]. Reprinted, with permission, from [92] © 1997, IEEE.

The voltage and current are given by [92] [© 1997, IEEE]

$$\begin{aligned} dv(x) &= -i(x)R_G\frac{dx}{W}, \\ di(x) &= -sC_{GS}\frac{dx}{W}(v+dv) - sC_{GD}\frac{dx}{W}\left((v+dv)-v_2\right). \end{aligned} \tag{A.1}$$

From this, we get

$$\begin{aligned}\frac{d^2i(x)}{dx^2} &= s\frac{R_GC_G}{W^2}i(x),\\ \frac{d^2v(x)}{dx^2} &= s\frac{R_GC_G}{W^2}v(x) - \frac{R_GC_G}{W^2}v_2.\end{aligned} \tag{A.2}$$

The general solutions for current and voltages are

$$\begin{aligned}i(x) &= I_Ae^{-\gamma x} + I_Be^{\gamma x},\\ v(x) &= V_Ae^{-\gamma x} + V_Be^{\gamma x} + \frac{C_{GD}}{C_{GG}}V_2,\end{aligned} \tag{A.3}$$

where the gate propagation constant $\gamma = \frac{\sqrt{j\omega C_GR_G}}{W}$ defines the change in magnitude and phase per unit change in width as the signal traverses from the input terminal.

Applying the boundary conditions $v(x=0) = v_1$ and $i(x=W) = 0$, the $v(x)$ and $i(x)$ equations are given by [92] [© 1997, IEEE]

$$\begin{aligned}v(x) &= \left(v_1 - \frac{C_{GD}}{C_G}\right)\frac{cosh(\gamma(W-x))}{cosh(\gamma W)} + \frac{C_{GD}}{C_G}v_2,\\ i(x) &= \left(v_1 - \frac{C_{GD}}{C_G}\right)\frac{sC_G}{\gamma W}\frac{sinh(\gamma(W-x))}{cosh(\gamma W)}.\end{aligned} \tag{A.4}$$

The average gate voltage is given by [92] [© 1997, IEEE]

$$\overline{v} = \frac{tanh(\gamma(W-x))}{\gamma W}v_1 + \frac{C_{GD}}{C_G}\left[1 - \frac{tanh(\gamma(W-x))}{\gamma W}\right]v_2. \tag{A.5}$$

A.1.1 Y-Parameters in distributed RC gate model

The Y-parameters changes from the lumped model under the influence of the ladder network. The new equations for Y-parameters are given as [92][© 1997, IEEE]

$$\begin{aligned}y_{11} &= sC_G\frac{tanh(\gamma(W-x))}{\gamma W},\\ y_{12} &= sC_{GD}\frac{tanh(\gamma(W-x))}{\gamma W},\\ y_{21} &= (g_m - sC_{GD})\frac{tanh(\gamma(W-x))}{\gamma W},\\ y_{22} &= g_{DS} + sC_{GD} + (g_m - sC_{GD})\left(\frac{C_{GD}}{C_G}\right)\left(1 - \frac{tanh(\gamma(W))}{\gamma W}\right).\end{aligned} \tag{A.6}$$

A.1.2 Z-Parameters in distributed RC gate model

For formulation of Z-parameter, the null bias condition is taken where $g_m \to 0$ and $r_{DS} \to \inf$. In this case, we can derive the input impedance as given below

$$z_{11} = \frac{\gamma W}{sC_G tanh(\gamma(W))} + \frac{C_{GD}}{sC_G C_{GS}}. \tag{A.7}$$

A.1.3 Effect of propagation constant

With the increase in the gate electrode sheet resistance or capacitance, the value of $\gamma = \sqrt{jw\frac{R_G}{W}\frac{C_G}{W}}$ increases as well. For both the perceived terminal capacitance and resistance, the propagation constant appears in the form of $tanh(\gamma W)$. The hyperbolic tangent can be expressed in terms of Taylor series as

$$tanh(\gamma W) = \gamma W - \frac{(\gamma W)^3}{3} + \frac{2(\gamma W)^5}{15} - \frac{17(\gamma W)^7}{315} + \frac{62(\gamma W)^9}{2835} - ..... \tag{A.8}$$

Depending on the value of γW, the formulation of $tanh(\gamma W)/(\gamma W)$ can be simplified as shown in Fig. Thus for the range $\gamma W < 0.5$, we can take the 3rd order approximation of the hyperbolic tangent. In that case, one can derive from (A.7) as ,

$$re(z_{11}) = \frac{r_G W}{3\left(1 + \left(\frac{\omega r_G W C_G}{3}\right)^2\right)}. \tag{A.9}$$

For small r_G, the TFTs with same dimensions would produce a constant terminal resistance of $r_G W/3$ that can be extracted from S-parameter measurements applying the above formulation.

Appendix B

Low Frequency Noise of in-house a-IGZO TFTs

B.1 Types of low frequency noise

The noise in field effect devices can be attributed to 4 different sources listed below.

- flicker of 1/f Noise: It is the most dominant noise at low frequency in a field effect transistor. The noise power is inversely proportional to frequency. It can be caused by fluctuations in mobility or in charge carrier numbers [93].
- Thermal Noise: This noise is caused by the random fluctuations of electron in the channel. The noise spectral density is independent of frequency in this case.
- Shot Noise: The shot occurs due random arrival of charge carriers at the output terminal of the TFT.
- Generation-Recombination Noise: The presence of traps (impurities) in the interface can absorb charge carriers and cause generation and recombination with free carriers. This causes a low frequency noise which is inversely proportional to the square of frequency [78].

B.1.1 Origin of 1/f noise

Normally, current-noise measurement techniques are applied for low-frequency noise characterization of FETs. At low frequency for a field effect transistor, the 1/f or flicker noise is dominant. The source of flicker noise can be either of the two following ways [94]

- Carrier number fluctuation: charge trapping and de-trapping by the gate oxide leading to a random change in a number of channel charges
- mobility fluctuation: phonon number fluctuations causing a random change in mobility of the charge

In case of the carrier number fluctuation, the charge in the insulator region also changes causing a change in the flat-band voltage of the FET. This causes a change in the drain current. If the effective mobility of the carrier is independent of the number of charges [95], then the current fluctuation is given just by the change in the flat-band voltage of the FET. In actual devices, however, the carrier number fluctuation would also affect the scattering of the carriers, thereby causing a fluctuation in effective mobility. So the current fluctuation combines both flat-band voltage fluctuation and other mobility fluctuation. The drain current fluctuation δI_d is given by [95],

$$\delta I_d = \delta V_{fb} \frac{\partial I_d}{\partial V_{fb}}|_{\mu_{eff}=const} + \delta\mu_{eff} \frac{\partial I_d}{\partial \mu_{eff}}|_{V_{fb}=const}, \tag{B.1}$$

where $\delta V_{fb} = -\delta Q_i/(WLC_{ox})$ is the change in flat-band voltage and μV_{eff} is the change in mobility of the inversion layer. For drift current, i.e. in the ohmic region of FET, the current per unit area is given by

$$\frac{I_d}{WL} = Q_i \mu_{eff}(-\frac{V_d}{L}), \tag{B.2}$$

where μ_{eff} is the effective mobility of the carriers. This effective mobility, on the other hand, is dependent on the inversion charge via the relation [96]

$$\frac{1}{\mu_{eff}} = \alpha Q_i + \frac{1}{\mu_0}, \tag{B.3}$$

where μ_0 is an empirical mobility parameter and α is an empirical parameter dependent on the doping concentration level. The first differential in the right hand side of equation (B.1) is $\frac{\partial I_d}{\partial V_{fb}} = g_m$, the transconductance of the FET. The second term can be derived from (B.2) and (B.3). So finally (B.1) can be expressed as

$$\delta I_d = -g_m \delta V_{fb} - \alpha I_d \mu_{eff} \delta Q_i = -g_m \delta V_{fb} - \alpha I_d \mu_{eff} \delta V_{fb} WLC_{ox}. \tag{B.4}$$

The noise spectral density of any parameter x can be expressed as the square of the fluctuation i.e. $S_x = \delta x^2$. So the normalized noise spectral density for the carrier number fluctuation can be given in terms of the transconductance of the device as

$$\frac{S_{Id}}{I_d^2} = \left(1 \pm \alpha \mu_{eff} WLC_{ox} \frac{I_d}{g_m}\right)^2 \left[\frac{g_m}{I_d}\right]^2 S_{Vfb}, \tag{B.5}$$

where the $+\mu_{eff}$ represents donor-like traps and $-\mu_{eff}$ represents acceptor-like traps. The parameter α, which represents the sensitivity of the effective mobility, determines whether the normalized noise power spectral density is strongly or weakly dependent on g_m/I_d. The flat band voltage spectral density, on the other hand, takes the form [97]

$$S_{Vfb} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f}, \tag{B.6}$$

where N_t is the volume oxide trap density. This equation shows the inverse relation of the noise

to the frequency. The second model presented by Hooge [98] states that mobility fluctuates due to lattice scattering, i.e. scattering of the vibrational energy of the charge carriers [99]. This, in turn, causes a change in the normalized drain current spectral density, which is inversely proportional to the number of charge carriers in the inversion layer Q_i [100]

$$\frac{S_{Id}}{I_d^2} = \frac{\alpha_H}{fWL^2} \int_0^L \frac{dx}{Q_i(x)/q}, \tag{B.7}$$

where α_H is the Hooge parameter, $Q_i(x)$ is the absolute inversion charge per unit area along the channel and q is the absolute electron charge.

In triode region, $Q_i(x) = Q_i$ uniform, i.e.,

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{fWLQ_i}. \tag{B.8}$$

The inverted charge Q_i could be expressed in terms of gate voltage and oxide capacitance as $Q_i = C_{ox}(V_G - V_{th})$, which transforms (B.8) to [101]

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{fWLC_{ox}|V_G - V_{th}|}. \tag{B.9}$$

In the non-linear region, the charge distribution is not uniform but rather would depend on the Fermi level shift (ϕ) between the source and the drain, according to gradual-channel approximation [100]. In this case, current along the length x of the channel is

$$\frac{S_{Id}}{I_d^2} = W\mu_{eff}Q_i(x)\frac{d\phi_c}{dx}. \tag{B.10}$$

So from ((B.7)), one obtains the general equation for mobility fluctuation as

$$\frac{S_{Id}}{I_d^2} = \frac{q\mu_{eff}\alpha_H}{fL^2}\frac{V_d}{I_d}. \tag{B.11}$$

The proper choice of either of the two models depends on how the normalized noise current spectral density behaves with respect to the gate voltage or the transconductance. If S_{ID}/I_d^2 changes proportional to the square root of $(g_m/I_D)^2$, then according to (B.5), the charge number fluctuation is to be adopted. On the other hand, if the normalized noise current density shows the $-10\mathrm{dB/dec}$ slope with respect to the gate overdrive voltage, then the validity of the mobility fluctuation theory would be firmly established, excluding the number fluctuation model.

B.2 Noise measurement setup

The noise measurement is done in an RF lab isolated from external interference. All the cables used in the setup are shielded. The device under test (DUT) is probed at two locations for gate and drain with two power-power-ground (PPG) probes. The center pin P connects to the terminal being measured. Both probes' G and other P pins connect to the source terminal. The cable corresponding to these P pins is shorted using an SMA (SubMiniature A) short. The drain is connected to a $545\,\Omega$ thin film resistor, which acts as a load in a shielded box. The other end is connected to a bias tee that allows only DC signals to pass. The drain terminal is simultaneously connected to a FEMTO HVA-10M-60-F voltage amplifier with its output at a Keysight EXA N9010B signal analyzer.

The drain and gate terminal must be biased variably to see the operating point's effect on noise. A Keysight B2962B low noise power supply with an additional Keysight N1298B low noise filter is used for V_{DD}. The supply also measures the drain current. However, we observed that even with the presence of the filter, the power supply adds considerable noise to the measurement setup. Hence the supply is used only at the drain terminal. The gate bias is provided with a $200\,\mathrm{mAh}$ Nickel-Metal-Hybrid rechargeable CONRAD battery. A resistance chain is created on a PCB and connected to an SMA female port with a jumper cable to vary the biasing.

The noise spectrum and the DC measurement of the TFTs are done simultaneously with the setup to calculate the deembedded S_{ID} and the I_D. The V_{DD} is swept using the supply source with a step size of $1\,\mathrm{V}$ each. The V_G is applied through the battery powered resistive divider.

The noise measured at the spectrum analyzer is divided by gain of the FEMTO amplifier and the load resistance value to calculate the noise current i_n. The square of the noise current gives the noise current power spectral density (PSD) of the TFT.

B.2.0.1 Noise floor of the setup

The FEMTO amplifier has an input noise voltage of $4.7\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ [102]. It measures the noise voltage at the input, based on the input resistance.

The addition of the power supplies for biasing deteriorates the noise performance of the setup only in terms of additional spikes at the harmonics of $50\,\mathrm{Hz}$, which is the standard AC power supply frequency in Germany. However, the thermal noise floor is not raised compared to the floating FEMTO noise floor.

Fig. B.1 shows the difference between the noise PSDs of different loads at the FEMTO input. The noise floor is lowest when the FEMTO input is shorted or loaded with a SMA $50\,\Omega$ resistance. Turning on the drain supply through the load resistance of $550\,\Omega$ increases the noise floor slightly. A TFT with a floating drain and shorted gate shows a slightly higher noise. In this case, an inversion layer is formed in the semiconductor, but the noise is not high enough, since the electrons are not mobile.

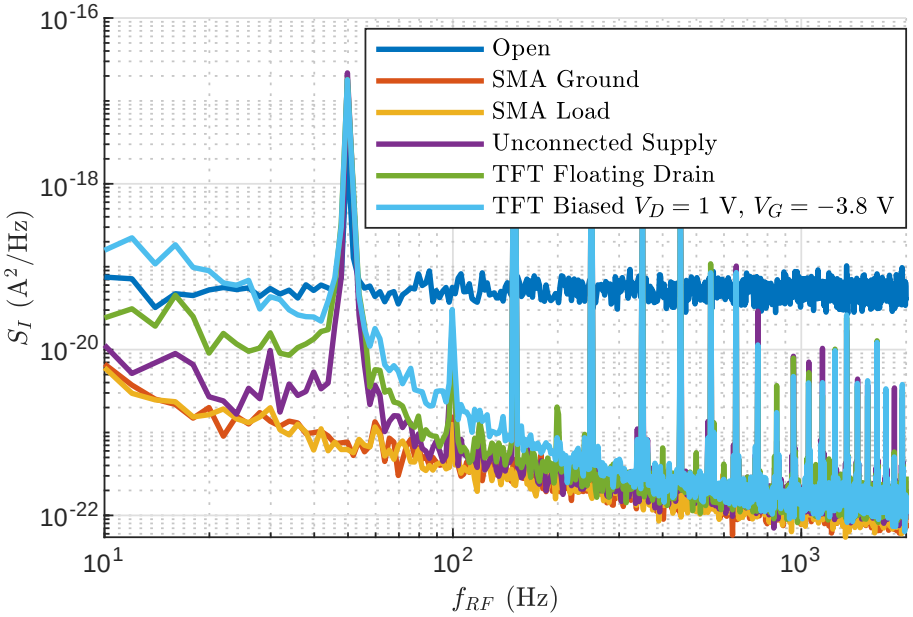


Figure B.1: Noise PSD of the setup showing open, TFT, and a $50\,\Omega$ resistance at the FEMTO input.

The open input of the FEMTO shows a flat PSD over frequency. At open, the resistance at the input is maximum at $1\,\mathrm{M}\Omega$. Hence, the S_I is also higher than the floating drain.

If a bias is applied to the TFT, the noise floor increases and exceeds the S_I for open. This is the low frequency noise of the TFT. Hence it can be concluded that the TFT low frequency noise can be measured.

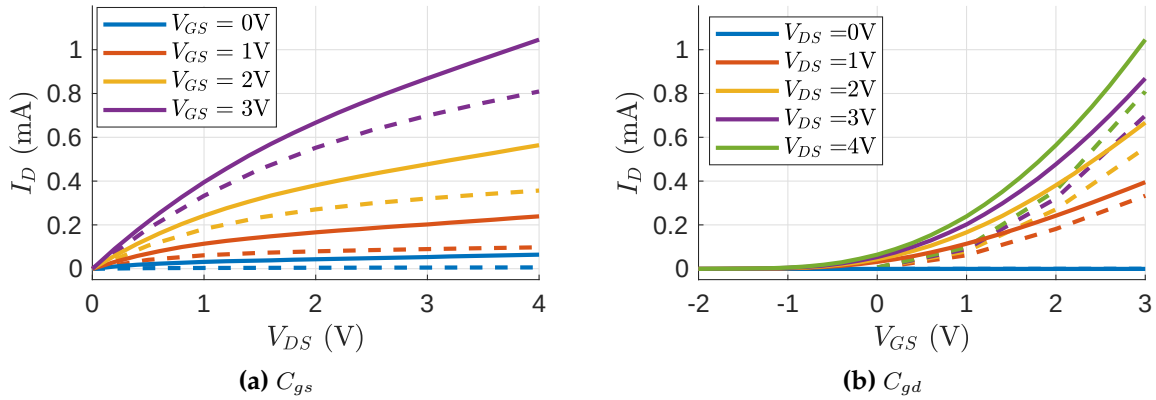
It must be noted that the spikes are due to the power supply still being coupled to the spectrum analyzer through the TFT channel. However, as frequency increases, their effect reduces.

B.2.1 TFT Noise measurement results

Fig. B.3 shows current power spectral density (PSD) S_I for a $250\,\mu\mathrm{m}/1\,\mu\mathrm{m}$ channel TFT. The TFT was fabricated in 2019. However, some of them showed comparable output characteristics, when measured 2 years apart, as shown in Fig. B.2a. TFT 1 (in dashed lines) was measured in 2019 and TFT 2 (in solid lines) was measured in 2021. Fig. B.2b shows the transfer characteristics, with the TFT 2 measurement of 2021 showing a lower threshold voltage. This negative shift in threshold voltage is assumed to be due to deterioration in encapsulation. Nevertheless, the TFT is still capable of achieving comparable current to the ones measured two years earlier.

The noise measurement was performed in 2021 and 2022. The S_I of a $250\,\mu\mathrm{m}/1\,\mu\mathrm{m}$ channel TFT is shown in B.3. S_I is very low for negative gate voltage and decreases inversely to the frequency square. For $V_G \geq 0\,\mathrm{V}$, the TFT follows 1/f noise with slope of $10\,\mathrm{dB/dec}$.

It can be seen that there is no difference in the noise PSD for different gate voltages. So, further investigation is done by normalizing the noise PSD as shown in Fig. B.4.



(a) C_{gs} **(b)** C_{gd}

Figure B.2: Comparison of measured (a) output and (b) transfer characteristics of two 250 µm/1 µm TFTs on the same glass substrate measured two years apart. Here, dashed lines show TFT 1 measured data in 2019, and solid lines show TFT 2 measured data in 2021.

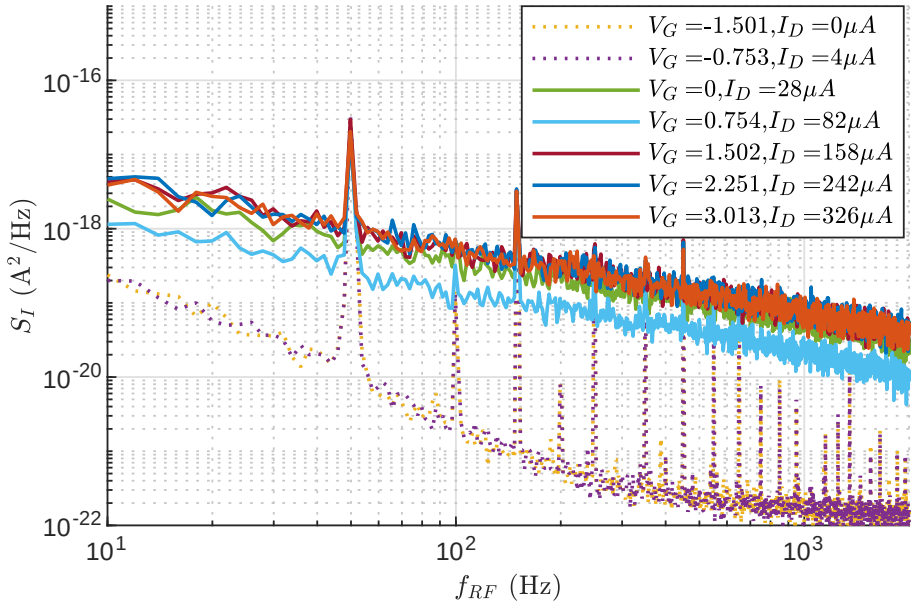


Figure B.3: Noise PSD for 250 µm/1 µm TFT fabricated in 2019, measured in 2022.

B.2.2 1/f Noise of in-house TFT

The origin of 1/f noise can be verified with the normalized PSD S_I/I_D^2. From (B.5), it can be seen that for carrier number fluctuation, S_I/I_D^2 scales proportionately with $(g_m/I_D)^2$. We plotted the S_I/I_D^2 versus $(g_m/I_D)^2$ as seen in Fig. B.5a and performed a linear fit. As we see, the measured data doesn't follow a straight line. The mobility fluctuation verification can be done by plotting S_I/I_D^2 against $1/I_D$, based on (B.11). As displayed in Fig. B.5b, the two parameters follow a linear relation, thereby proving the Hooge Model of mobility fluctuation generated 1/f noise.

The Hooge model has been verified for all our TFTs designed in 2019. Fig. B.6 shows the S_I/I_D^2 versus $1/I_D$ for different TFTs. From slope of the normalized PSD $\Delta S_I/\Delta I_D^2$, the Hooge parameter can be extracted applying (B.11).

The extracted Hooge parameters for different TFT channel width and length are shown in Table

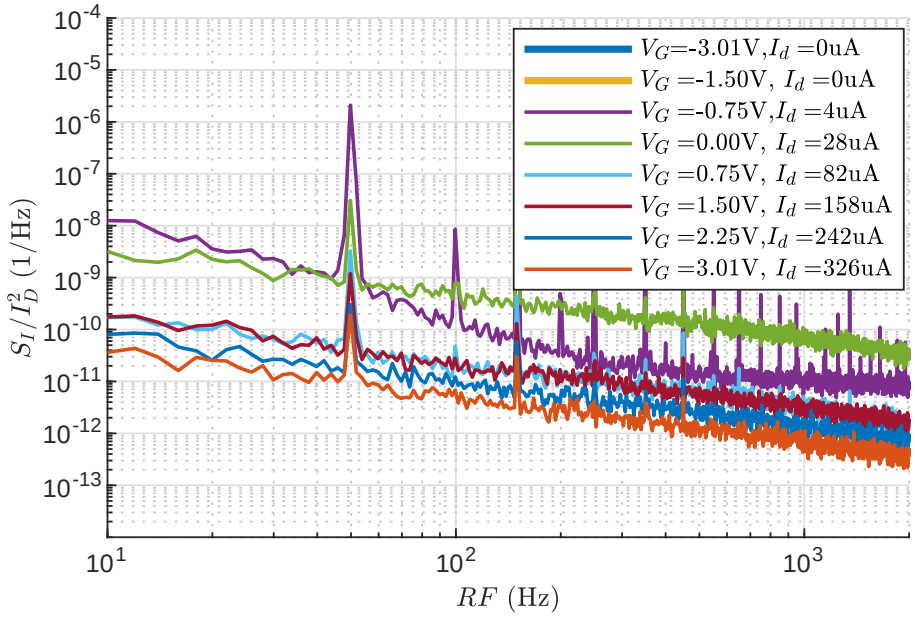
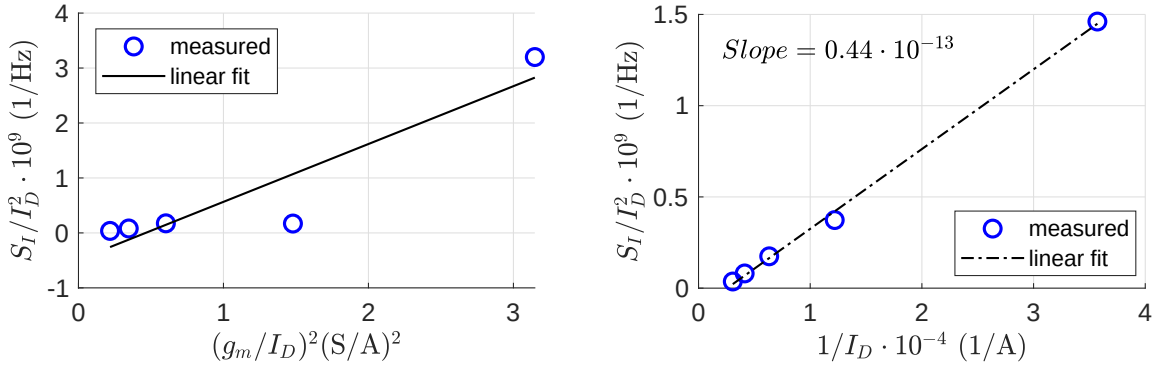


Figure B.4: Normalized noise PSD S_I/I_D^2 for $250\,\mu\text{m}/1\,\mu\text{m}$ TFT fabricated in 2019, measured in 2022.



(a) C_{gs} **(b)** C_{gd}

Figure B.5: S_I/I_D^2 versus $1/I_D$.

B.1. For majority of the TFTs, the extracted α_H is between $2 \cdot 10^{-3}$ and $4.5 \cdot 10^{-3}$. This result is comparable to the study done by Cho et. al in [93], which reported an $\alpha_H = 2 \cdot 10^{-3}$. One TFT of dimension $500\,\mu\text{m}/1\,\mu\text{m}$ shows a slightly higher α_H. This can be due to measurement error. Noise measurement is sensitive to the noise in the environment, especially at low frequencies, where the connectors also get coupled to external noise.

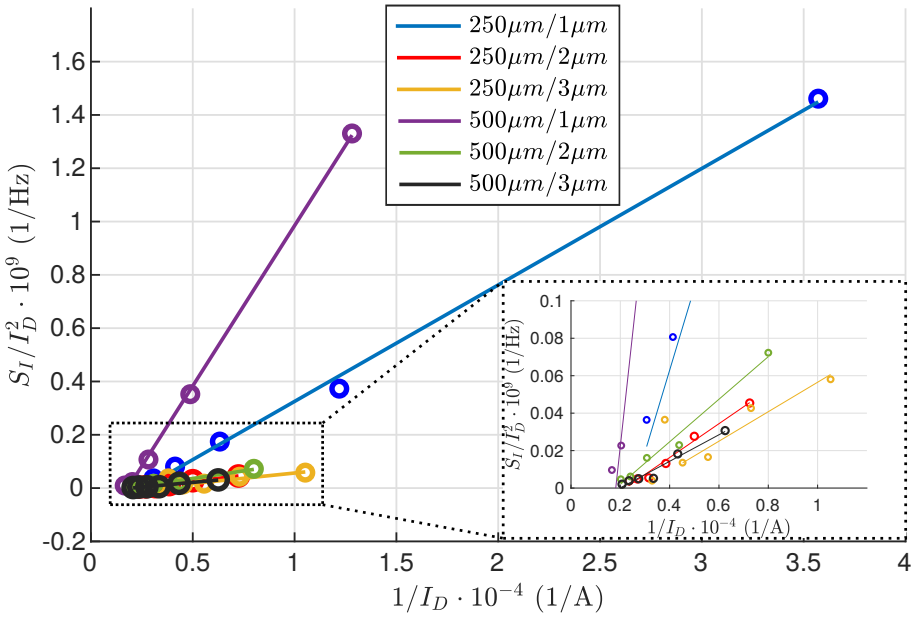


Figure B.6: Hooge verification for different TFTs of Cr gate, fabricated in 2019, measured in 2022.

W (µm)	L (µm)	$\frac{\Delta(S_I/I_D^2)}{\Delta(1/I_D)}$	μ_{eff} ($\mathrm{Vcm^{-2}s^{-1}}$)	α_H
250	1	$0.44 \cdot 10^{-13}$	10	$2.73 \cdot 10^{-3}$
250	2	$0.09 \cdot 10^{-13}$	10	$2.26 \cdot 10^{-3}$
250	3	$0.079 \cdot 10^{-13}$	10	$4.43 \cdot 10^{-3}$
500	1	$1.2 \cdot 10^{-13}$	10	$7.52 \cdot 10^{-3}$
500	2	$0.11 \cdot 10^{-13}$	10	$2.84 \cdot 10^{-3}$
500	3	$0.07 \cdot 10^{-13}$	10	$3.89 \cdot 10^{-3}$

Table B.1: Extracted Hooge parameter α_H for different TFTs.

B.2.3 Low Frequency noise of the 2022 TFTs

We hypothesized in chapter 4, that the doubler fabricated with multi-finger $100\,\mu\mathrm{m}$ TFTs broke down because of presence of impurities.

The low frequency noise measurement of the same batch of TFTs also shows the presence of impurities. As seen in Fig. B.7a and B.7b, the PSDs decrease with $-20\,\mathrm{dB/dec}$ slope for these both the single and multi-finger TFTs respectively.

As mentioned in [78], the $1/\mathrm{f}^2$ relation appears for generation-recombination noise caused by trapping of charge carriers.

Several experiments in the literature show the coexistence of both $1/\mathrm{f}$ and $1/\mathrm{f}^2$ noise. However, one must measure from $0\,\mathrm{Hz}$ to discern such an effect. This frequency range is beyond the lower limit of our spectrum analyzer.

In any case, the noise behavior of TFTs can also give a good idea about the presence of traps in the interface.

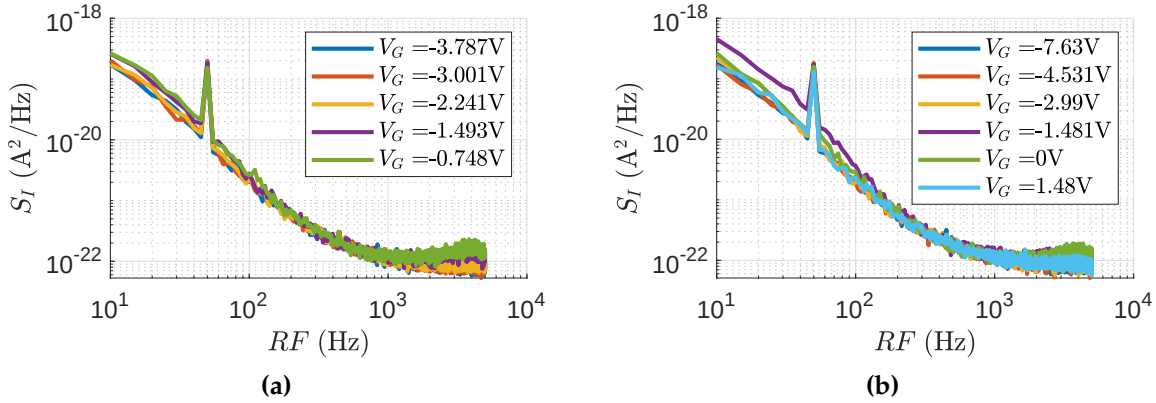


Figure B.7: Noise PSD for (a)a single and (b) a ten-finger TFTs, fabricated in 2022.

B.3 Summary of noise measurements

Here, we have shown how the distributed model of the gate electrode affects the input Y- and Z-parameters. The dispersion of extracted intrinsic and extrinsic capacitances reduces if the gate electrode material has a low propagation constant. The extraction of capacitances is easier in this case.

We have performed the noise characterization of different TFTs of different dimensions. Following Hooge's theory, the in-house TFTs intrinsically show mobility fluctuation and generate 1/f noise. However, if there are impurities in the fabrication process, the trap (or impurity) induced generation-recombination noise dominates the low-frequency noise behavior of the TFT. This type of noise manifests itself as a $1/f^2$ noise as low frequency. Thus the low frequency noise behavior can give us an idea about the presence of impurities in a-IGZO TFTs.

Appendix C

Inductor Design

C.1 Planar inductor on glass substrate

When designing an inductor, we must consider several important factors: inductance value, quality factor, self-resonant frequency and occupied area.

For hundreds of MHz to GHz frequency ranges, the value of inductors must lie in the range of $10\,\mathrm{nH}$ to $100\,\mathrm{nH}$. Most RF circuits and measurement equipment are calibrated to impedances of $50\,\Omega$. This is the value at which interstage impedance matching is done for a single-ended circuit. As we see in chapter 3, the TFT input capacitance is around few tens of fF. If, for example, a single TFT with a capacitance of C_{in} is used, a series inductance of $L = \frac{1}{(2\pi f_o)^2 C_{in}}$ would be required to compensate the C_{in} at frequency f_o. So at $f_o = 1\,\mathrm{GHz}$ and $C_{in} = 100\,\mathrm{fF}$, this required $L_{in} \approx 6.5\,\mathrm{nH}$.

For designing a spiral metal inductor in the 5–$10\,\mathrm{nH}$ range, the empirical formula is used [41]

$$L = 1.310^{-7} \frac{A_m^{5/3}}{A_{tot}^{1/6} W^{1.75} (W+S)^{0.025}}, \tag{C.1}$$

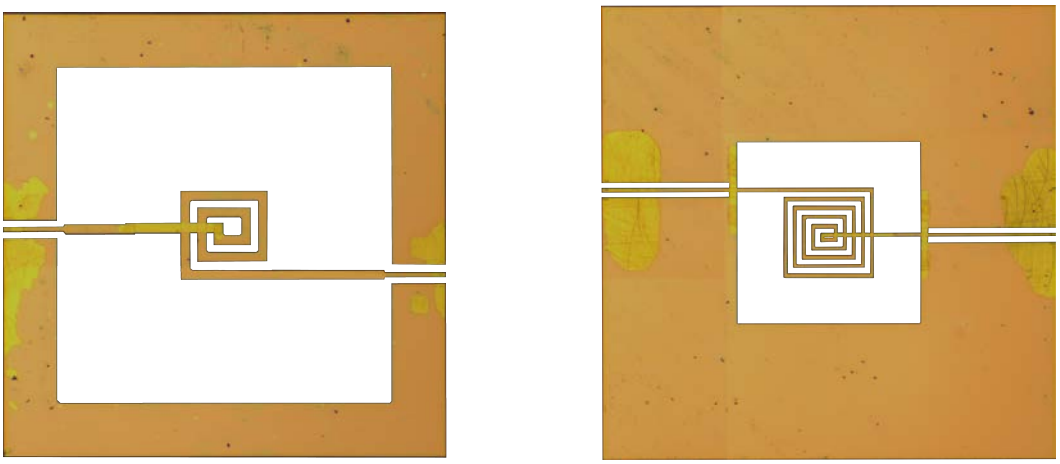
where A_m is the total area of the metal lines, A_{tot} is the total area of the inductor region, W is the width of the line and S is the separation between the lines. However, there are also other limitations imposed by parasitics. The following figure of merits describes the effect of the parasitics on inductors.

An inductor's quality factor (Q) is the ratio between the reactance and resistance. In terms of energy, it is the ratio between the energy stored as a magnetic (or electric) field to that dissipated as heat. In terms of frequency, it is the ratio of operating frequency over bandwidth. The higher the Q-factor, the sharper is the resonance, but with reduction in the bandwidth.

The self-resonance frequency is related indirectly to the area of the inductor. The size of the integrated circuit always imposes a constraint on the inductor. Moreover, one must shield the inductor's electromagnetic wave with a grounded ring. Hence large on-chip inductances

are folded and implemented in a spiral configuration. Parasitic capacitances exist between the conductors, and the conductor and the ground plane. Hence at a certain frequency $f_R = \frac{1}{2\pi\sqrt{LC_{par}}}$, the inductance shows resonance, beyond which the total parasitic capacitance C_{par} starts dominating. That is why, the value of f_R should be much higher than the operating frequency of the RF circuit involving the inductor.

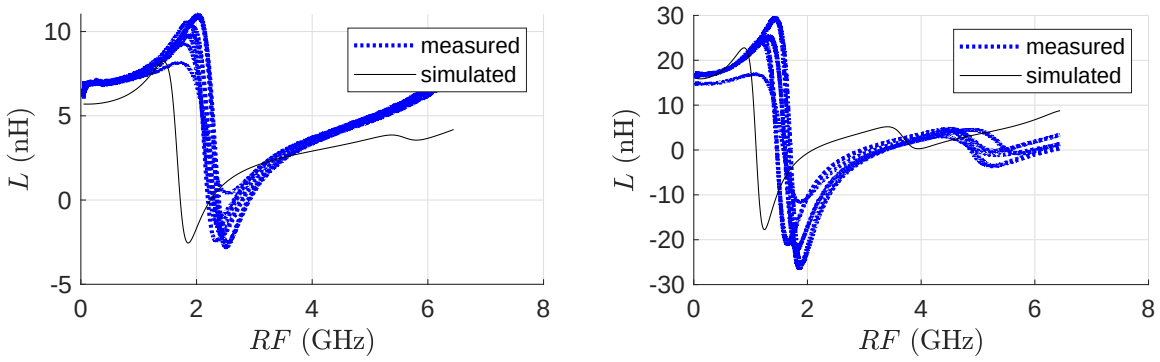
For design purposes, we designed and simulated two inductances of $5\,\mathrm{nH}$ and $12\,\mathrm{nH}$ in the Sonnet EM simulator. The fabrication was done on a glass substrate with a $220\,\mathrm{nm}$ copper electrode as an inductance material. Copper has excellent thermal and electrical conductivities, which are $390\,\mathrm{W/mK}$ and $59\,\mathrm{S/m}$ respectively [103],[104]. Hence, they are the elements of choice in many RF designs. Lately, IHP Technologies have also incorporated the copper back-end for their 'SG13G3Cu' devices [105].



(a) $5\,\mathrm{nH}$ **(b)** $12\,\mathrm{nH}$

Figure C.1: Fabricated (a) $5\,\mathrm{nH}$ and (b) $12\,\mathrm{nH}$ inductors.

The fabricated inductances were measured using an Agilent E3685A Vector Network Analyzer. The fabricated inductances are in good agreement with simulation. However the self-resonant frequency increases slightly above the simulated results.

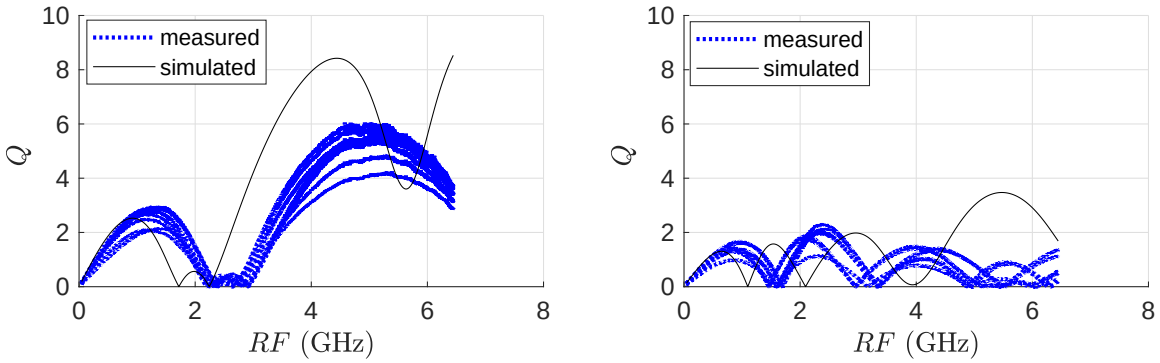


(a) $5\,\mathrm{nH}$ **(b)** $12\,\mathrm{nH}$

Figure C.2: Simulated versus measured (a)$5\,\mathrm{nH}$ and (b)$12\,\mathrm{nH}$ inductors.

The Q-factors were also extracted from the measured S-parameters. Due to the lower number of

turns, the simulated and measured Q-factor for both the $5\,\mathrm{nH}$ and $12\,\mathrm{nH}$ inductors were around 2 as seen in Fig. C.3a, which is very low.



(a) $5\,\mathrm{nH}$ **(b)** $12\,\mathrm{nH}$

Figure C.3: Simulated versus measured Q-factors for the (a)$5\,\mathrm{nH}$ and (b)$12\,\mathrm{nH}$ inductors.

We cannot compromise the value of Q in case the TFTs have poor transconductances. Hence, these inductances are not used for circuit design. Rather we planned to use external PCB inductances with extremely high-quality factors. Such inductances are produced by Murata Electronics [88].

C.2 Summary of inductor design

In this process, we have also designed and fabricated inductors on a glass substrate. Although the inductors fabricated showed a good fit between the measurement and simulation, their quality factors were low. Low-quality factors result in power dissipation in high frequencies. Hence off-chip inductors (PCB planar inductors or coils) for transmitters with high output power are usually required.

Appendix D

TFT Model Files

D.1 Verilog-A model for the Cr-gate TFT

```
// VerilogA for IGZOTFT20_basic, TFT_ver, veriloga

`include "constants.vams"
`include "disciplines.vams"

module TFT0p8(S,D,G);
 inout  S,D,G;
 electrical  S, D, G, G1, G2, D1, D1S, G1D1, G1S, G2D1, G2S,S2;
 branch (G,G1) resgext1;
 branch (G1,G2) resgext2;
 branch (G1,S) cappg;
 branch (G2,S) capgso;
 branch (G2,D1) capgdo;
 branch (D,D1) resde;
 branch (D1,S) cappd;
 branch (G2,G2S) capgsi;
 branch (G2,G2D1) capgdi;
 branch (G2D1, D1) resgdi;
 branch (G2S,S) resgsi;
 branch (D1,S) resdsi;
// branch (S2,S) inds;
////////////////////////////////////////////////////////
//////////////////////Noise PARAMETERS//////////////////////
integer mcd,count,retval;
real frq,val;
```

```
parameter string filename="vg_0_noise.dat";
parameter maxpoints=2004;
parameter debug=0;
real noisetab[0:maxpoints-1];
////////////////////////////////////////////////////////////
// Fitting Parameters for Compact Model
////////////////////////////////////////////////////////////
 localparam real W = 100E-6;
 localparam real L = 0.8E-6;
////////////////////////////////////////////////////////////
// PARAMETER FROM ALGO
////////////////////////////////////////////////////////////
  localparam real alphasat =0.90595;
  //localparam real GAMMA=1.0144;
  localparam real GAMMA=1.0144;
//  localparam real VAA=2.6565;
  parameter real VAA=1.9018;
  localparam real M=1.3698;
  localparam real EPSI=8.5;
  localparam real EPS=13.9;
  localparam real LAMBDA=0.10132;
  localparam real MUBAND=0.001;
  localparam real RD =160.0773;
  localparam real RS =160.0773;
  localparam real TNOM =24;
  localparam real TOX =4.7e-08;
  parameter real VTO =-0.94779;
  localparam real VFB =-4.9712;

  parameter real RG1=385;
  parameter real RG2=1078;
//  localparam real RDE=10.0;
  localparam real RDE=10;

  localparam real CPG=37E-15;
  localparam real CPD=17E-15;
  localparam real COV=57E-15; //

  localparam real taum=150E-12;
  localparam real rgdi=1;
  localparam real rgsi=650;
```

```
  parameter real NF=1;

  localparam real Nt=1E21*6.2415E24;
////////////////////////////////////////////////////////////;
// Declaring intermediate constants for calculations
////////////////////////////////////////////////////////////
  real VGS, VDS, VSD;
  real IOFF, I_B, ID_ON, Leakage,Vth0, Vth;

  analog function integer sign;
    input arg;
    real  arg;
    sign = (arg >= 0) ? +1 : -1;
  endfunction

 analog function integer onoff;
input arg1;
real arg1;
onoff = (arg1 > 0) ? +1 : 0;
 endfunction
////////////////////////////////////////////////////////////
// Calculations start
////////////////////////////////////////////////////////////
//(* ignore_hidden_state *)
 analog begin: FET
real Cf, CG, mufet, fR, denom, CGC, SS, eta, Vgt, Vgte,Vgfb
 Vgfbe, Vdse, CG1, IGD, IGS,  gmId, Svfb, Pn, Isub, Cds, IDS,
 tm, ISUB, Ve, Nc, nso, nsb, ID, nsa,ns, gchi,Vsate,gch,Qch,
 Ci,Vgtn,Rsd, SID, SGR;

    real gm;
real CGS;
real CGD;

// Set the values of VGS and VDS via the access functions
// Running routine for intercheangable drain/source regions
    VGS = V(G,S);
    VDS = V(D,S);
    VSD = V(S,D);

Vth=VTO;
```

```
Vgt=VGS-VTO; //
Vgte=VMIN/2*(1+Vgt/VMIN+sqrt(pow(DELTA,2)+pow(Vgt/VMIN-1,2)));
Vgte=Vgt;
Vgfb=VGS-VFB;
// Vgfbe=VMIN/2*(1+Vgfb/VMIN+sqrt(pow(DELTA,2)+pow(Vgfb/VMIN-1,2)));

//ABOVE THRESHOLD
nsa=EPSI*'P_EPS0/('P_Q*TOX*pow(VAA,GAMMA))
*laplace_nd(Vgte**(GAMMA+1),[1],[1,taum]);


//Total Current
ns=nsa;// ns=nsa*nsb/(nsa+nsb);
gchi = 'P_Q*ns*MUBAND*(NF*W)/L;
gch=gchi/(1+gchi*(RD+RS));
gch=laplace_nd(gchi/(1+gchi*1*(RD+RS)/NF),[1],[1,taum]);
Vsate = alphasat*Vgte;
Vdse = VDS/pow((1+pow((VDS/Vsate),M)),(1/M));

// Intrinsic Capacitance
CGC= (EPSI*8.854E-12*W*NF*L/TOX)*1/1*onoff(Vgt);
CGS=(1-((Vgte-Vdse)/(2*Vgte-Vdse))**2)*CGC*2/3;;
CGD=(1-((Vgte)/(2*Vgte-Vdse))**2)*CGC*2/3;;


//AC Current
I(resgext1)<+V(resgext1)/(RG1/NF);
I(resgext2)<+V(resgext2)/(RG2/NF);
I(cappg)<+ddt(V(cappg))*(CPG*NF);
I(capgdo)<+ddt(V(capgdo))*(COV*NF);
I(capgdi)<+ddt(V(capgdi))*(CGD);
I(capgso)<+ddt(V(capgso))*(COV*NF);
I(capgsi)<+ddt(V(capgsi))*(CGS);
I(resgsi) <+ V(resgsi)/(rgsi/NF);
I(resgdi) <+ V(resgdi)/(rgdi/NF);
I(resde)<+V(resde)/(RDE);
I(cappd)<+(CPD*NF)*ddt(V(cappd));

// Total Current

I(resdsi) <+ gch*Vdse*(1+LAMBDA*Vdse);
```

```
ID=I(resdsi);

// gm Extraction
Rsd=(RD+RS)/NF;
Ci=CGC/(W*L*NF);
gm=(pow(Vgte, GAMMA)*(2*Ci*L*MUBAND*(W*NF)*pow(VAA,
    GAMMA)*pow(VDS, 2) + Ci*L*MUBAND*VDS*(W*NF)*pow(VAA,
    GAMMA)*pow(Vsate, M) + Ci*GAMMA*L*MUBAND*(W*NF)*pow(VAA,
    GAMMA)*pow(VDS, 2) + 2*Ci*L*LAMBDA*MUBAND*(W*NF)
    *pow(VAA, GAMMA)*pow(VDS, 3) + Ci*GAMMA*L
    *MUBAND*VDS*(W*NF)*pow(VAA, GAMMA)*pow(Vsate, M) +
    Ci*L*LAMBDA*MUBAND*(W*NF)*pow(VAA, GAMMA)*pow(Vsate,
    M)*pow(VDS, 2) + Ci*GAMMA*L*LAMBDA*MUBAND*(W*NF)
    *pow(VAA, GAMMA)*pow(VDS, 3) + Ci*GAMMA*L*LAMBDA*MUBAND
    *(W*NF)*pow(VAA, GAMMA)*pow(Vsate, M)*pow(VDS, 2)) +
    Ci**2*MUBAND**2*Rsd*Vgte*(W*NF)**2*pow(Vgte,
    GAMMA)**2*pow(VDS, 2)  +  Ci**2*LAMBDA*
    MUBAND**2*Rsd*Vgte*(W*NF)**2*pow(Vgte, GAMMA)**2
    *pow(VDS, 3))/(pow(Vgte,GAMMA)*
    (2*Ci*L*MUBAND*Rsd*Vgte*(W*NF)*pow(VAA, GAMMA)
    *pow(Vsate, M)*((VDS + pow(Vsate, M))/pow(Vsate, M))**(1/M)
    + 2*Ci*L*MUBAND*Rsd*VDS*Vgte*(W*NF)*pow(VAA, GAMMA)*
    ((VDS + pow(Vsate, M))/pow(Vsate, M))**(1/M))
     + L**2*pow(VAA, GAMMA)**2*pow(Vsate, M)*((VDS +
     pow(Vsate, M))/pow(Vsate, M))**(1/M) + L**2*VDS
     *pow(VAA, GAMMA)**2*((VDS + pow(Vsate, M))
     /pow(Vsate, M))**(1/M) +Ci**2*MUBAND**2*Rsd**2
     *VDS*Vgte**2*(W*NF)**2*pow(Vgte, GAMMA)**2
     *((VDS + pow(Vsate, M))/pow(Vsate, M))**(1/M)
+ Ci**2*MUBAND**2*Rsd**2*Vgte**2*(W*NF)**2
*pow(Vgte, GAMMA)**2*pow(Vsate, M)*
((VDS + pow(Vsate, M))/pow(Vsate, M))**(1/M));

endmodule
```

D.2 Model library for high-speed TFT of Chapter 6

```
* DATE: 15-Apr-2020

* Utpal Kalita

* derived from IGZO TFT Ti/Au electrodes 100um/0.6um

* Temp= 27

.MODEL AIMSPICE15 NMOS LEVEL = 61

+ alphasat =0.61511 gamma =1.0644 cgdo =4e-10 cgso =7.3e-10
+ VAA =5.543 m =1.2857
+ epsi =8.5 eps =4.6
+ lambda =0.060844 muband =0.001
+ rd =772.2934 rs =772.2934
+ tnom =24 tox =5e-08
+ vto =-0.10423
+ VFB =0.43504
```

D.2.1 Additional white noise and shot noise current source

```
// VerilogA for BSIM_n_Spice, res_va_vccc, veriloga

`include "constants.vams"
`include "disciplines.vams"

module nois_curr( a, b);

  inout a, b;
  electrical a, b;

//  parameter real AF =  1.0    from (0.1:inf);
//  parameter real EF =   1.1    from (-inf:inf);
//  parameter real q=1.6E-19;
  parameter real lambda=0.1E-9;
  parameter real Nt=2E19*6.2415E24; //[Joule]=6.2415E24*[eV]
  parameter string inst_nam = "my_instance";
  analog function integer sign;
```

```
    input arg;
    real  arg;
    sign = arg >= 0 ? +1 : -1;
  endfunction

  analog begin : vaResistor
real Ir, Pn, gm_fet, gmId, Svfb, Cgs, Cgd, Ci, w, l, gm2;
string nam;
gm_fet = $simprobe(inst_nam, "gm", 0.0);
// $display("gm=%r",gm_fet);

//Take the data from the DC Analysis
w = $simprobe(inst_nam, "w", 500e-6);
l = $simprobe(inst_nam, "l", 3e-6);
// Cgs = $simprobe(inst_nam, "cgs", 0.0);
// Cgd = $simprobe(inst_nam, "cgd", 0.0);
// Ci = (Cgs+Cgd)/(w*l);
// $display("w=%r, l=%r, Cgs=%r, Cgd=%r, Ci=%r", w, l, Cgs, Cgd, Ci);

Ir= $simprobe(inst_nam, "id", 0.0);
gmId= gm_fet/Ir;

// Svfb = (pow(q,2)*`P_K*$temperature*lambda*Nt)/(w*l*pow(Ci,2));
// Pn = pow(gm_fet,2)*Svfb;

//
I(a,b) <+ white_noise(4.0*`P_K*$temperature*gm_fet*1/3, "thermal");
// I(a,b) <+ flicker_noise(sign(Ir)*(Pn), EF, "flicker");
//creates a noisy signal with power Pn at 1 Hz
I(a,b)  <+ white_noise(4.0* `P_K*$temperature*gm_fet,"th0");
I(a,b)  <+ white_noise(2* `P_Q*Ir,"shot");
  end

endmodule
```

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